Si3474 Data Sheet

Up to four 802.3bt or eight 802.3at Ethernet Port PoE PSE Controllers

The Si3474 is a fully programmable, 50 to 57 V power management controller for IEEE 802.3af, 802.3at, and 802.3bt compliant Power Sourcing Equipment (PSE). Designed for use in PSE endpoints (switches), the Si3474 integrates eight independent ports, each with the IEEE-required powered device (PD) detection and classification functionality. When used in 802.3af/802.3at (two-pair power) mode each PSE port supports one Ethernet connection, for a total of eight PoE Ethernet connections. 802.3bt operation (four-pair power) uses two PSE ports per Ethernet connection, for a total of four PoE Ethernet connections.

In addition, the Si3474 features a fully-programmable architecture that enables powered device (PD) disconnect using dc-sense algorithms, a robust multipoint detection algorithm, software configurable per-port current and voltage monitoring, and programmable current limits to support the IEEE 802.3af, 802.3at, and 802.3bt standards. Intelligent protection circuitry includes input undervoltage detection, output current limit, and short-circuit protection. The Si3474 operates autonomously or by host processor control through a two wire, I^2C compatible serial interface. An interrupt pin is used to alert the host processor of various status and fault conditions.

Applications

- IEEE 802.3af, 802.3at, and 802.3bt Power Sourcing Equipment (PSE)
- Power over Ethernet Switches
- IP Phone Systems
- Smartgrid Switches
- Ruggedized and Industrial Switches

KEY FEATURES

- Octal-Port Power Sourcing Equipment (PSE) controller
- IEEE 802.3af, 802.3at, and 802.3bt compliant
- Autonomous or I^2C host interface
- Emergency Shutdown support with port priority control
- Adds enhanced features for maximum design flexibility:
  - Per-port current and voltage monitoring
  - Multi-point detection
  - Programmable power MOSFET gate drive control
  - Configurable watchdog timer enables failsafe operation
- Maskable interrupt pin
- Comprehensive fault protection circuitry includes:
  - Power undervoltage lockout
  - Output current limit and short-circuit protection
  - Thermal overload detection
- Extended operating temp range: –40 to +85 °C
- 56-pin, 8 x 8 mm QFN package (RoHS-compliant)

1. Ordering Guide

Table 1.1. Si3474 Ordering Guide

Ordering Part Number[1]	Product Revision	Current Sense Resistor[2]	Package	Temperature Range (Ambient)
Si3474A-A01-IM	A01	255 mΩ	56-pin, 8 x 8 mm QFN RoHS-compliant	–40 to 85 °C
Si3474B-A01-IM	A01	200 mΩ	56-pin, 8 x 8 mm QFN RoHS-compliant	–40 to 85 °C

Note:

1. Add an “R” to the end of the part number for tape and reel option (e.g., Si3474A or Si3474A-A01-IMR).
2. Options include industry-standard 255 mΩ or more thermally efficient 200 mΩ sense resistor.

Table of Contents

2. Functional Description

2.1 Overview

Integrating a high-performance microcontroller with high-resolution A/D and D/A capabilities, along with eight independent, high-voltage PSE port interfaces, the Si3474 enables an extremely flexible solution for virtually any PoE switch application. The Si3474 integrates all PSE controller functions needed for an octal-port PoE design.

The Si3474 includes many additional features that can be individually enabled or disabled by programming the extended register set appropriately.

- Per-port current / voltage monitoring and measurement
- Multipoint detection algorithms
- Programmable gate drive for external MOSFETs
- Watchdog timer (WDT)

2.2 Functional Block Diagram

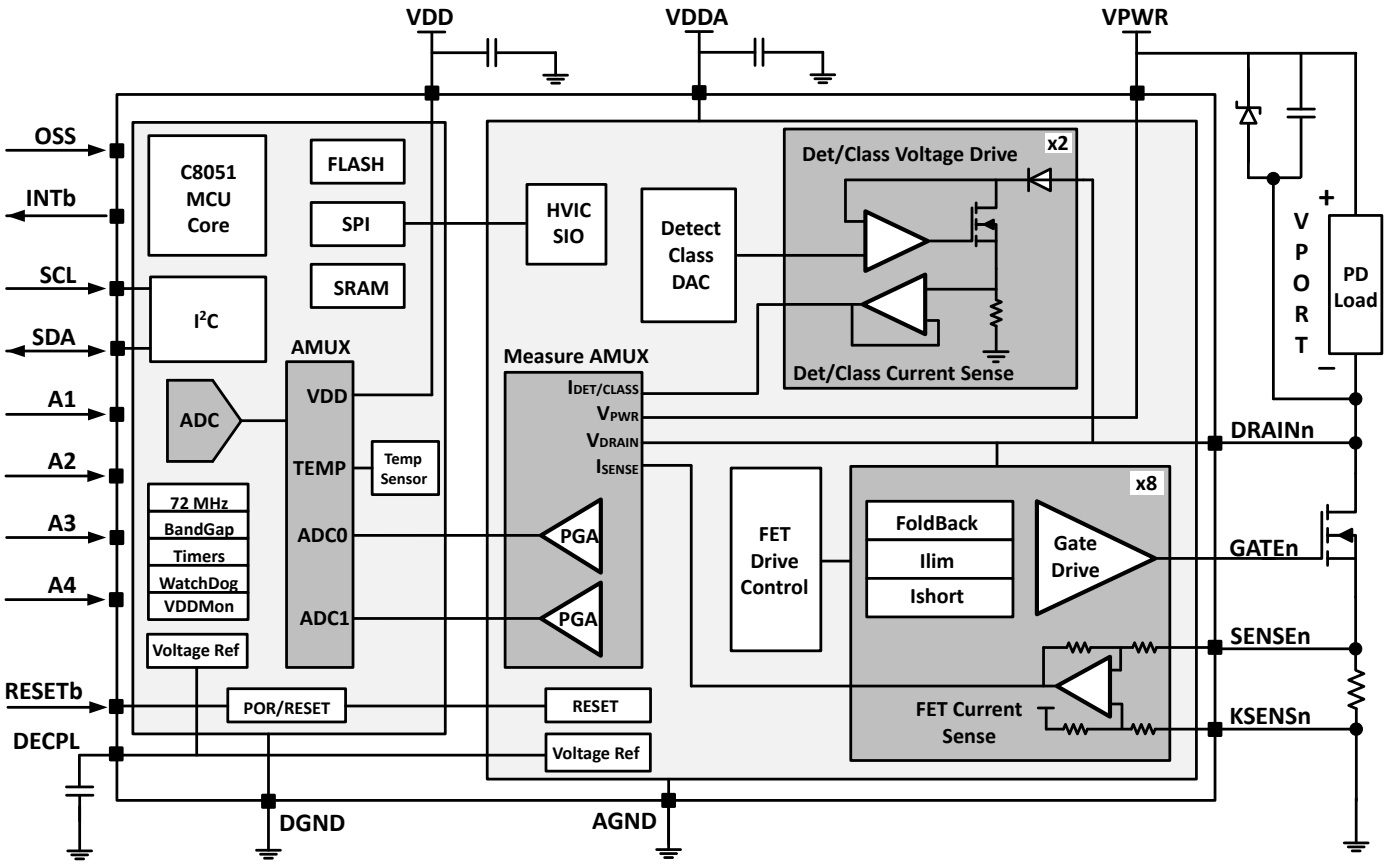


Figure 2.1. Si3474 Functional Block Diagram

2.3 Operational Modes

The Si3474 has three different operating modes: Autonomous, Semi-Autonomous, and Manual, plus one non-operating mode, Shut-down. The appropriate operating mode can be chosen depending on system requirements, such as whether the PSE system is power-constrained, whether the PSE system has a power manager host, or whether the PSE system must identify any power-non-conforming PD loads.

2.3.1 Autonomous Mode

Autonomous Mode should only be used in PSE systems where there is enough power to power all ports simultaneously to their total allocated power. In other words, Autonomous Mode can only be used in non-power constrained PSE systems. In Autonomous mode, the Si3474 will automatically detect, classify and power on ports that present a valid PD signature without any external host interaction.

There are two methods to place the Si3474 into Autonomous mode. One method is to configure the AUTO pin using an external voltage and power cycling the Si3474. The following types of systems are suitable for AUTO pin Autonomous Mode:

- Homogenous ports configuration. For each Si3474, all ports must be configured as either four-pair powered ports (4P) or all ports configured as two-pair powered ports (2P).
- Each port must have the same Power Allocation setting.
- PSE system must be able to supply sufficient VPWR current to all ports under maximum loading.

The second method is to an external host processor to configure and start the Autonomous Mode through the I^2C registers. For systems whose ports are not homogenous or if the ports are to have different power allocations, use I^2C Autonomous Mode instead of the AUTO pin. Whether Autonomous Mode is invoked by the AUTO pin or by the I^2C interface, the I^2C register interface remains active so an external host processor can poll the event registers, for example, to control indicator LEDs.

For more details on autonomous operation, refer to 2.10.1 AUTO Pin Autonomous Mode and 2.10.2 I^2C Autonomous Mode.

2.3.2 Semi-Autonomous Mode

In PSE systems with high port counts, rarely is there a PSE system power supply that is capable of powering all ports to their maximum load simultaneously. The Si3474 I^2C register interface is designed to accommodate a host processor to act as a power manager that can choose or deny PD power requests as new PD loads are attached. In these systems, the Si3474 controller performs low level PoE protocols with the PD loads and provides real-time fault monitoring and power consumption measurements required by the external host processor to perform power management. For these hosted, power-constrained systems, the Si3474 operates in Semi-Autonomous mode.

2.3.3 Manual Mode

Manual mode is special case of Semi-Autonomous mode where the external host processor forces a condition on the port(s) that bypasses the low-level PoE protocol. For example, forcing a port to power on a PD load immediately without exercising detection and classification protocol. As such, manual mode should be used for diagnostic or debug purposes only.

2.4 Host Interface

The Si3474 communicates with the host processor through an I2C interface using:

- Registers
- Events
- Pushbuttons

In this data sheet, register names, fields and bits are listed in all capitals. Some have prefixes such as PORTn_ or PORTnm_. The PORTn_ describes attributes that are associated with 2P ports. The prefix PORTnm_ applies to attributes associated with 4P ports. Some registers are global to the entire Si3474. Some registers are associated with one set of four 2P ports (quad). The Si3474 has two quads and the second set of four 2P ports are accessed in the same register but through the alternate I2C address. Refer to 4. Register Map for a complete listing of registers.

During operation, the Si3474 monitors global conditions such as temperature and supply voltage, and some conditions that are associated with the individual PoE ports. When an event occurs, the Si3474 will drive the INTb pin low. The host processer will then read the INTERRUPT register and decode what event has occurred. The Si3474 drives the INTb low until the appropriate Clear-on-Read (CoR) register is read by the host processor.

There are some events in which cause the Si3474 to take immediate action without instructions from the host, and there are some that are intended to be indicators to allow the host processor to take desired actions as its role being the PSE system power manager. Once the host receives notification of an event, it is expected to act upon that event. The details and mechanics of event handling is described in 2.9 Event Handling.

The host processor can instruct the Si3474 to take certain actions through a Pushbutton (PB) command. All write-only registers are Pushbutton registers. A register designated as Pushbutton will always return as zero when read. Some read-write registers can also act as pushbuttons depending on the context as described in .

Each Si3474 port can be in one of four operational modes, controlled by the PORT_MODE register. PORTn_PORT_MODE can be set to:

- SHUTDOWN
- MANUAL
- SEMI_AUTO
- AUTO

The AUTO mode is most applicable to a non-hosted PSE system. The MANUAL mode is used primarily for diagnostic and debug purposes. For hosted PSE systems, SHUTDOWN and SEMI_AUTO port modes are the most important. When PORTn_PORT_MODE is set to SHUTDOWN, that port is in an idle state, ready to be configured by the host.

A port enters SHUTDOWN by:

- A hard reset (power on reset or by deasserting RESETb pin)
- Setting RESET_QUAD in PB_RESET register sets all ports in that quad to SHUTDOWN
- Setting individual PORTn_RESET_PORT in PB_RESET register. Each port has a dedicated bit
- Any SUPPLY_EVENT sets all ports to SHUTDOWN
- An I2C WATCHDOG event is equivalent to a RESET_QUAD that sets all ports to SHUTDOWN

A port in SEMI_AUTO mode, when combined with PORTn_DETECT_CC_ENABLE and PORTn_CLASS_ENABLE, instructs the Si3474 to actively look for connected PDs on a port. In a power-managed, hosted PSE system, the figure below describes the key interactions and events between the power manager host and the PoE port conditions in the Si3474. The following sections describe the control flow of a Semi-Auto PSE.

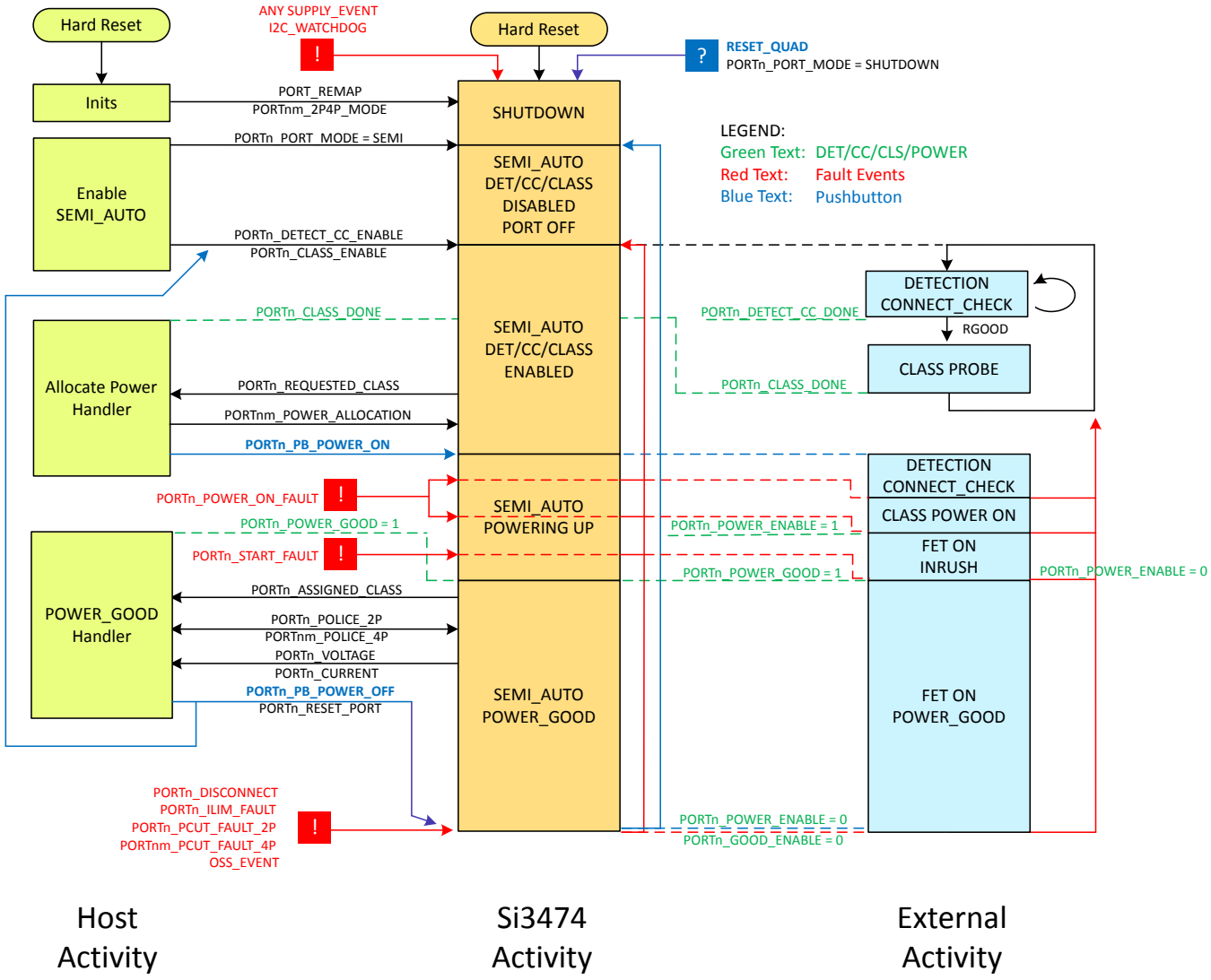


Figure 2.2. Semi-Auto System State Diagram

2.5 Reset and Initialization

Hard resets are invoked by either cycling power (Power on Reset or PoR) and/or deasserting RESETb input. After a hard reset, all registers are set to default values. A PoR will always set all registers to default values. Invoking a hard reset by deasserting the RESETb input will set all registers to default values except the upper nibble of SUPPLY_EVENT to default values. The upper nibble is sticky until the condition that is causing the global event is cleared. For specific information, refer to 4.8 SUPPLY_EVENT and SUPPLY_EVENT CoR (0x0A, 0x0B).

Immediately after a hard reset, the host must initialize at least two registers, the PORT_REMAP register and the PORTnm_2P4P_MODE field in POWER_ALLOCATION register. These registers must be set to match the hardware configuration, ex. how the ports are wired, of the PSE system. For specifics, refer 4.24 PORT_REMAP (0x26) and 4.26 POWER_ALLOCATION (0x29). These two registers once written to, are locked until a hard reset of the Si3474 to unlock them again.

During the initialization, the host can set other global registers as needed.

2.6 Semi-Auto Detection, Connection Check, and Class Probe

The host instructs the Si3474 to start detecting attached PDs by setting:

- PORTn_PORT_MODE = SEMI_AUTO
- PORTn_DETECT_CC_ENABLE and PORTn_CLASS_ENABLE in DETECT_CLASS_ENABLE

Prior to driving the detection waveform, the Si3474 performs a check that the port's external FET is properly off and is not damaged. The first test is a current measurement across the external sense resistor and the second test is a voltage measurement at the DRAINx pin. If excessive current detected or an unexpected drain voltage, PORTn_DETECTION_STATUS will indicate a MOSFET_FAULT and detection is aborted.

The Si3474 detects a PD by making a differential resistance measurement by driving 4 V to 8 V and back to 4 V on each enabled port through the DRAINx pin, while measuring current at each step. The results are used to calculate measured detection resistance, also known as the PD Signature Resistance, which is nominally 25 kΩ. The Si3474 reports the detection results in the PORTn_DETECTION_STATUS field of the PORTn_DETECT_CLASS_STATUS registers.

During detection the Si3474 monitors the voltage driven for evidence of a contention with another PSE driving the same line. If the measured voltage deviates significantly from the driven voltage, PORTn_DETECTION_STATUS will report a PSE to PSE fault. The Si3474 also uses the voltage/current measurements taken during the detection waveform to determine if the PD Signature Resistance measures too capacitive and reports in the PORTn_DETECTION_STATUS.

If the port is configured as a 2P port, a DETECT_CC_DONE event will be reported to the host after the detection sequence. If the detection result is RGOOD, the Si3474 begins a class probe to determine the PD's class signature. A class probe will always consist of three class fingers to determine the PD requested power followed by a class reset. The following figure shows the expected waveform for a 2-Pair powered PD.

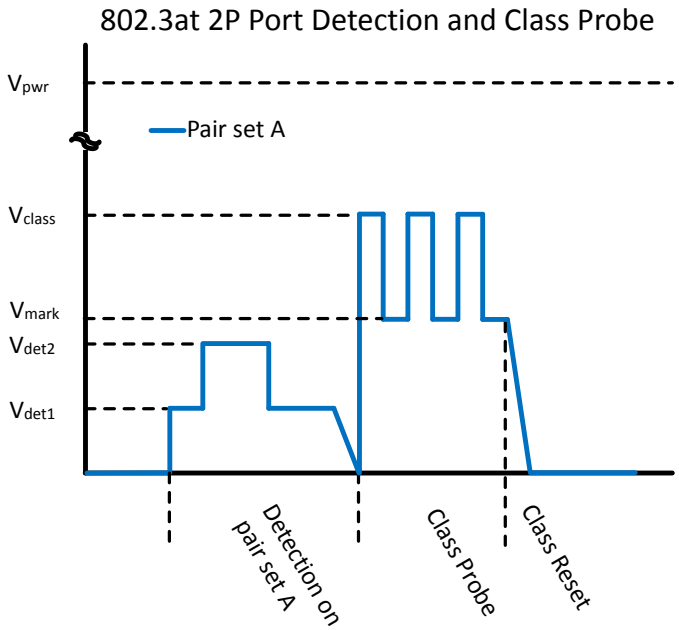


Figure 2.3. Semi-Auto DET/CLASS 2-Pair Waveform

The sequence changes if the port is configured to be a 4P port. After one of the two ports that comprise a 4P port detects a valid PD detection signature, a connection check (CC) is performed to determine if the attached PD is a single-signature PD or a dual signature PD. If the connection check indicates a single-signature PD, then Si3474 indicates a DETECT_CC_DONE and continues onto class probe on the primary pairset that detected the valid PD detection signature. The following figure shows the expected waveform for a 4-Pair powered single signature PD.

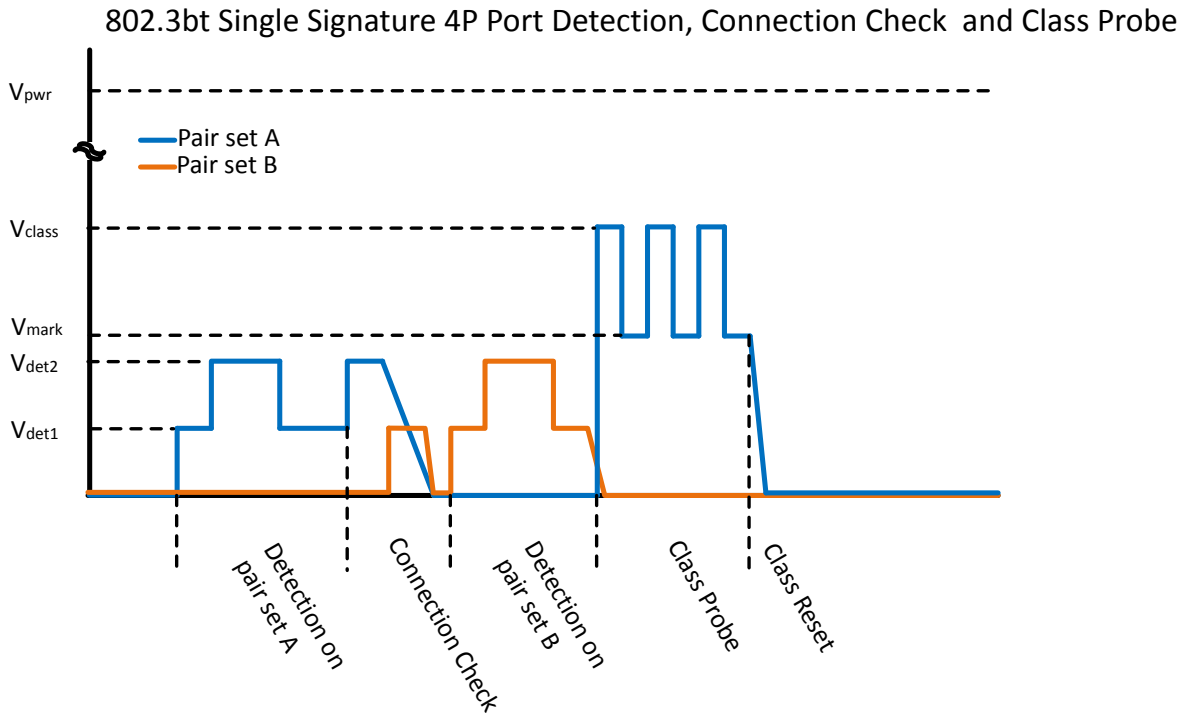


Figure 2.4. Semi-Auto DET/CC/CLASS 4-Pair Single-Signature Waveform

If the connection check indicates a dual-signature PD, the Si3474 detects and class probes on both the primary and secondary pairsets. The following figure shows the expected waveform for a 4-Pair powered dual-signature PD.

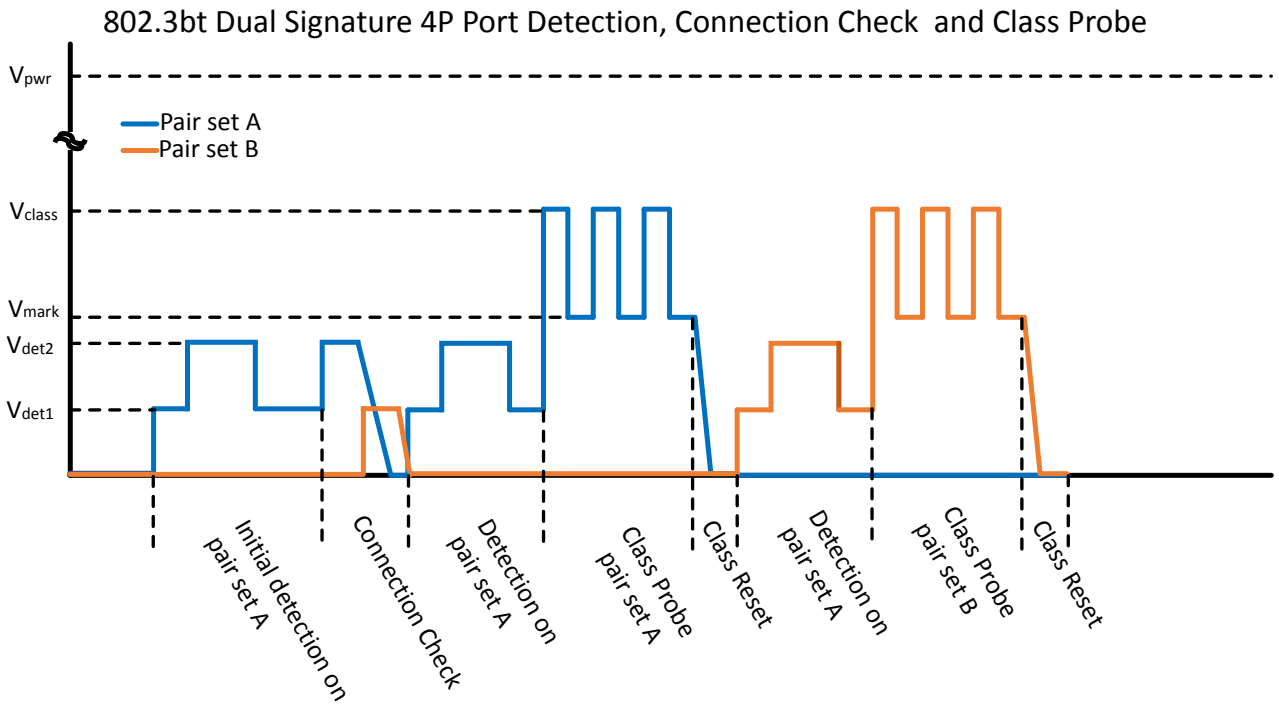


Figure 2.5. Semi-Auto DET/CC/CLASS 4-Pair Dual-Signature Waveform

Upon class probe completion, the Si3474 will report a PORTn_CLASS_DONE event and place the requested power in the PORTn_CLASS_STATUS field of the PORTn_DETECT_CLASS_STATUS register and in the PORTn_REQUESTED_CLASS field in the PORTn_CLASS_RESULTS register.

2.7 Powering Up

A port is ready to be powered on after the PORTn_CLASS_DONE event is reported. The host can examine the results of the PORTn_CLASS_STATUS to discover the PD's requested class. The host can then set or adjust the PORTnm_POWER_ALLOCATION as needed, followed by setting the PORTn_PB_POWER_ON for the port.
The Si3474 goes through the sequence of events described in the following subsections.

2.7.1 Power Demotion

Upon powering on a port, the host knows how much power the PD has requested by reading the PD's requested class. If the host determines that it has the requested power available, it will typically set PORTnm_POWER_ALLOCATION so that the PD receives the power it has requested. If the host knows it does not have the full power available, it can choose to set the PORTnm_POWER_ALLOCATION such that the assigned class will be less than the requested class; this is known as Power Demotion.

A power-demoted PD can request more power at any time through the Ethernet Link-Layer protocol (LLDP). Through LLDP, if the PD requests additional power (and if the PSE has more power to spare at that time), it can then grant the additional power. The host communicates the allowable additional power to the Si3474 by updating the PORTn_POLICE_2P or PORTnm_POLICE_4P registers without needing to put the port in SHUTDOWN and perform another PORTn_PB_POWER_ON sequence.

When putting a PD in Power Demotion, there are some considerations. There is a risk of encountering a PORTn_POWER_ON_FAULT "Insufficient Power Allocation" in a dual-signature 4P Port if one pair-set consumes all of the power in a way that prevents supplying additional power to the other pair-set. The other nuance is that, when a Class 4 to Class 8 PD is only provided Class 3 power, the PSE can only send one classification finger to the PD. In this case, the Si3474 will supply Class 3 power and communicate report "Class 4+ Type 1 Limited" in PORTn_CLASS_STATUS. PORTn_ASSIGNED_CLASS will show Class 3, and the PORTn_REQUESTED_CLASS shows the result of the Class Probe, which will show Class 4 to Class 8.

2.7.2 Final Detection, Connection Check, and Class Probe

When PORTn_PB_POWER_ON is received by the Si3474, it is likely that it is performing a DET/CC/CLASS PD discovery sequence that is unrelated to the port receiving the PB_POWER_ON pushbutton. The Si3474 allows those started sequences to complete before executing the Pushbutton command for the specified port. PB_POWER_ON consists of a final set of Detection, Connection Check (for 4P Ports), and Class Power On for the ports that the host wants to power on.

The PB_POWER_ON detection sequence is similar to that performed by Semi-Auto Detection, Connection Check and Class Probe, with some slight differences. If the detection results are anything other than RGOOD for the ports being powered up, the PORTn_POWER_ON_FAULT event is set to *Invalid Detection*. If the PB_POWER_ON is issued to a 4P Port, a connection check will be performed the same way. The Si3474 then performs another Class Probe to reconfirm the PD's requested class followed by a Class Reset.

2.7.3 Class Power On

Unlike Class Probe, Class Power On intends to power on the PD afterwards. The other important factor to consider is that, with Class Power On, the number of classification fingers is significant as the PD will count them so as to learn what power it has been allocated by the Si3474. For example, a Class 4 PD learns it has been power demoted and is allocated only 15.5 W of power if the PSE presents a single classification finger. But, a Class 4 PD learns it may draw the full 30 W if the PSE presents it with two fingers during the Class Power On.

If, during Class Power On, an overcurrent or an invalid classification occurs, the PORTn_POWER_ON_FAULT event is set to *Classification Error*. Another error that will trigger a PORTn_POWER_ON_FAULT event is *Insufficient power allocation*. This can occur when a one pair-set of a dual-signature PD consumes the remaining power allocation and, therefore, there is no power available for the other pair-set. *Insufficient power allocation* is also reported if the host issues a PB_POWER_ON to only one pair-set of a Single Signature port and the attached PD requested Class 5 or higher power.

Class Power On results are stored in PORTn_ASSIGNED_CLASS. However, PORTn_CLASS_STATUS can contain additional information. In the case of a Power Demotion where a Class 4 or higher PD is demoted to Class 3, PORTn_CLASS_STATUS will report *Class 4+ Type 1 Limited*, whereas the PORTn_ASSIGNED_CLASS will report Class 3. Refer to Table 4.2 Classification Event Timing on page 67 in 4.36 CLASS_RESULTS (0x4C – 0x4F) for a comprehensive list of class codes and when they are updated.

The Si3474 sends out a long class pulse on the first finger during Class Power On for two purposes. First, a long first classification finger communicates to the PD that the Si3474 supports Short Maintain Power Signature (MPS) to save more power when in standby. Second, with the initial long class pulse, it is possible to detect if the PD supports Autoclass. Refer to 2.8.4 Autoclass for details.

After Class Power On has completed, the FET is turned on, and the Inrush period begins. The following figure show the entire expected waveforms for a PORTn_PB_POWER_ON for 2P, 4P Single Signature, and 4P Dual Signature PDs.

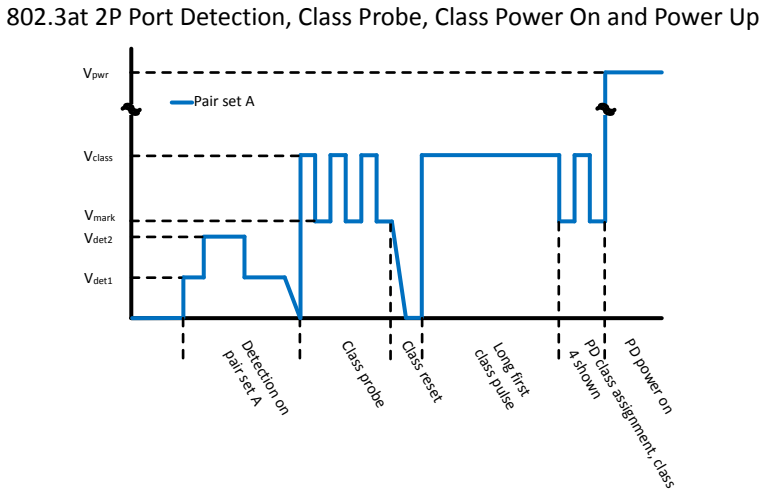


Figure 2.6. 2P Port Detection Waveform

802.3bt Single Signature 4P Port Detection, Connection Check, Class Probe, Class Power On and Power Up

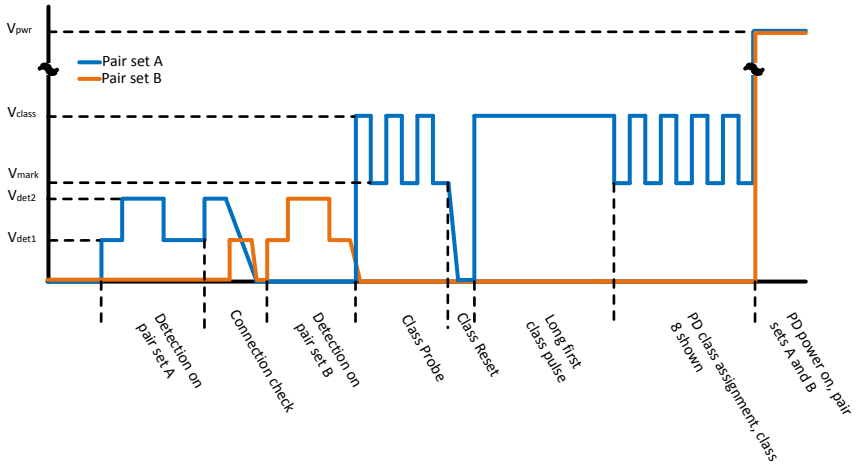


Figure 2.7. 4P Single-Signature Port Detection Waveform

802.3bt Dual Signature 4P Port Detection, Connection Check, Class Probe, Class Power On and Power Up

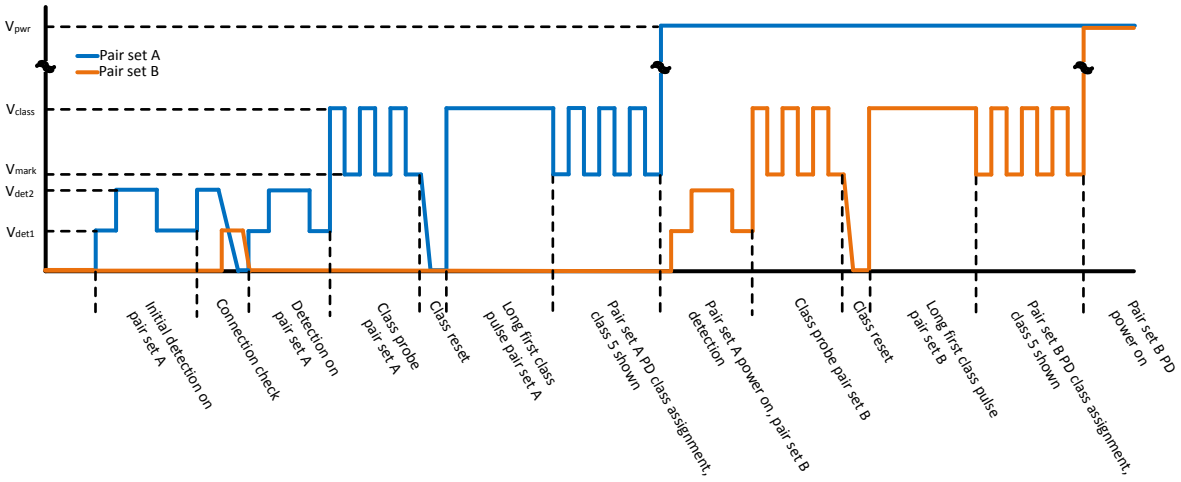


Figure 2.8. 4P Dual-Signature Port Detection Waveform

2.8 Powered States

There are two states for which the FET is ON:

1. Inrush Period
2. Power Good State

2.8.1 FET On Status

Each pair set has the PORTn_POWER_ENABLE and PORTn_POWER_GOOD status information suitable for tracking the general state of the Si3474 after a PORTn_PB_POWER_ON.

PORTn_POWER_ENABLE	PORTn_POWER_GOOD	FET State	After PORTn_PB_POWER_ON
0	0	OFF	Final Detection Connection Check Class Probe Class Power
1	0	ON	Inrush Period
1	1	ON	Power Good
0	1	—	Invalid

The corresponding events PORTn_POWER_ENABLE_CHANGE and PORT_POWER_GOOD_CHANGE events in the POWER_EVENT register track the changes in the POWER_ENABLE and the POWER_GOOD fields in the POWER_STATUS register.

Changes to PORTn_POWER_GOOD and PORTn_POWER_ENABLE affects the corresponding events PORTn_POWER_GOOD_CHANGE and PORTn_POWER_ENABLE_CHANGE. These events can be used by the host to check the POWER_STATUS register to check the most up-to-date port status.

PORTn_POWER_GOOD and PORTn_POWER_ENABLE elicit changes to the PORTn_POWER_GOOD_CHANGE and PORTn_POWER_ENABLE_CHANGE event bits. Once set, the PORTn_POWER_GOOD_CHANGE and PORTn_POWER_ENABLE_CHANGE bits are typically cleared by reading the POWER_CHANGE CoR register. In addition, PORTn_POWER_GOOD_CHANGE and PORTn_POWER_ENABLE_CHANGE events are cleared when PORTn_RESET_PORT is set, PORTn_PB_POWER_OFF is set, and when a port is turned off as a result of an OSS Event.

2.8.2 Inrush Period

Immediately after the FET is turned on, the Si3474 enters the Inrush Period. The Inrush Period is a fixed time period defined by t_{INRUSH}, During the Inrush Period, the Si3474 performs a voltage-foldback function for currents higher than 425 mA in order to limit the current drawn from the VPWR rail. The Si3474 also has a proprietary short-circuit FET protection circuit intended to protect the FET from damage.

The terms “start” and “inrush” are used interchangeably in this document. The Inrush Period is the initial part of a power-on in which the PSE is expected to supply current to the PD’s bulk capacitors. As is normal with any capacitor, if permitted, it will consume as much current as the PSE can supply. During the Inrush Period, a port implements a 425 mA current limit, with a 30 V Foldback, during a t_{START} or t_{INRUSH} time period.

After t_{INRUSH}, the port should no longer be in a current-limited state. If the port is still in a current-limited state, the port is powered off, and the PORTn_START_FAULT event is raised. Otherwise, the port reaches a POWER_GOOD state, and the Si3474 begins monitoring the port.

See 2.8.5 Current Limit and Voltage Foldback for an illustration of how current limiting and voltage foldback work.

2.8.3 Power Good State

When a port is in a POWER_GOOD state, three things are monitored:

1. Disconnection
2. ILIM / Current Limit
3. PCUT / Power Overload

Of these three things monitored, the Disconnection monitoring is to check if the PD is drawing too little current.

For the next two items, the Si3474 is monitoring for “too much current”. The difference between these two over-current monitors is the speed of the action taken.

For ILIM / Current Limit events are considered to be fast, high current events. As such, Si3474 circuits aim to limit the current by reducing port voltage. Under extremely high current conditions, the Si3474 shuts off the port completely to protect the FET from damage.

On the other hand, a PCUT does not involve FETs operating in current-limited state. But rather, the Si3474 is monitoring the port voltage and port current, then comparing them against the POLICE register limits.

2.8.3.1 Disconnection

While in the POWER_GOOD state, the Si3474 checks whether or not the PD is still connected to the port. A connected PD is obligated to draw a minimum amount of current. To keep the PSE from declaring a disconnection, the PD must meet a “Maintain Power Signature” for time duration of t_{MPDO}. If the PD does not meet these MPS requirements, the PSE may choose to power down the port.

When the Si3474 determines that the PD is no longer present, it sets the PORTn_DISCONNECTION event.

2.8.3.2 ILIM / Current Limit

Depending on the PD Class, the Si3474 chooses a current-limit template designed to allow normal PD currents to flow, while also setting a peak current threshold to begin a voltage foldback. Ostensibly, the Si3474 implements a number of current limit templates. The current limit template is a 2-dimensional function that defines a current limit against the drain voltage. At low drain voltages, the current limit is set at its maximum.

Whenever the measured port current exceeds these current limits, a feedback circuit then adjusts the gate voltage of the FET to fold-back the voltage. The speed at which the gate voltage is adjusted is a function of the difference between the current limit threshold at the drain voltage against the sensed port current.

The foldback mechanism is done automatically, while the drain voltage is monitored to check for evidence of a current-limited state. The device implements a counter that counts up by 1 whenever the FET is in an over-current state. For every subsequent non-overcurrent event is encountered, the counter is then decreased by 1/16. This allows current limited events to self-clear if it is a transient event. This prevents nuisance disconnections while also allowing disconnecting a port based on the severity of the event.

As a simple example, if the device continuously detects overcurrent for time t_{LIM} time periods, it will be considered an ILIM fault and remove power from the port.

In addition to the programmable current-limit foldback voltage templates, the Si3474 also implements a separate short circuit monitor so that if the difference between the measured current and the current limit is very large, the FET is turned off. In a certain sense, turning off a FET is a form of “extreme foldback”. This is implemented this way as it intends to protect the FET in the case of an unexpected short-circuit.

Current Limit faults are reported through the PORTn_ILIM_FAULT in the ILIM_START_FAULT register.

2.8.5 Current Limit and Voltage Foldback shows an illustration of how current limiting and voltage foldback works.

2.8.3.3 PCUT Faults

After the Class Power On, both the PSE and PD would have a mutual understanding of the power that the PSE is obligated to supply, as well as an understanding by the PD on how much power it is entitled to receive. Once the Port has reached a POWER_GOOD state, the Si3474 enforces this mutual power agreement through the various police registers.

The power values represented in the various police registers represents the power level consistent with what the PSE is obligated to supply, at the very minimum. Based on these values, the actual police limits internal to the Si3474 are slightly higher, to err on the side of supplying power to the PD.

There are generally two kinds of police registers PORTn_POLICE_2P and PORTnm_POLICE_4P.

The PORTn_POLICE_2P defines the power limits for each pair set, independently of each other. PORTnm_POLICE_4P is used also for 4P Ports. The PORTnm_POLICE_4P takes the total power of the two pair sets forming the 4P Port and compares against the power thresholds implied by the PORTnm_POLICE_4P.

At the completion of the Class Power On, the Assigned Class is determined based on the value of PORTnm_POWER_ALLOCATION, PORTnm_2P4P_MODE, PORTnm_CONNECTION_CHECK_RESULTS and the PORTn_REQUESTED_CLASS. For each pair set, the PORTn_ASSIGNED_CLASS is converted into a minimum power threshold and is stored in the applicable PORTn_POLICE_2P. For 4P Ports, there are two PORTn_POLICE_2P registers that are initialized, and in addition, the PORTnm_POLICE_4P.

For Single Signature 4P Ports, Autoclass can be enabled in the Si3474, and if the PD also supports Autoclass, then the PD will draw its expected maximum power during the first two to three seconds of being powered, allowing the Si3474 to know exactly how much power the PD would use. As such, the various police registers are initialized based on the Autoclass results, rather than using the Assigned Classification. Autoclass is discussed separately in 2.8.4 Autoclass.

In summary, the Si3474, upon reaching the POWER_GOOD state will have an initialized police register set. These police registers are the basis of checking for PCUT events. The Si3474 implements an algorithm that monitors compliance against the police registers.

After the initialization of the police registers, the host can make adjustments to the various police registers once it has more accurately determined the actual usage either through long term checking of the pertinent PORTn_VOLTAGE and PORTn_CURRENT, or through LLDP link-layer messaging.

PCUT faults are reported in PORTn_PCUT_FAULT_2P if the fault is associated with the PORTn_POLICE_2P. PORTnm_PCUT_FAULT_4P events are reported in the case where the PCUT faults are associated with PORTnm_POLICE_4P.

2.8.4 Autoclass

Autoclass is a protocol that only affects Single Signature 4P Ports. When automatic Autoclass is enabled, the Si3474 monitors the first long class finger of the Class Power On to detect if the PD is Autoclass-capable. If the Si3474 detects the PD acknowledgement, the PORTn_AUTOCLASS_DETECTED bit is set on that pair set. The Si3474 then takes voltage and current measurements when the pair sets reach POWER GOOD state. Both the two PORTn_POLICE_2P registers and the PORTnm_POLICE_4P registers will be initialized based on measured power plus margin. If PORTn_AUTO_AUTOCLASS is set, the corresponding PORTn_POLICE_2P and/or PORTnm_POLICE_4P are updated using the information in PORTn_AUTOCLASS_POWER information, plus some power margin.

The host may also initiate a Manual Autoclass by setting PORTn_MANUAL_AUTOCLASS (both pair sets must be set) in the AUTOCLASS_CONTROL register. The manual autoclass feature is typically used in conjunction with the LLDP-initiated autoclass procedure. As such, the host is expected to initiate a Manual Autoclass when the PD is drawing its maximum power. The Si3474 stores the computed Autoclass power results in the PORTn_AUTOCLASS_POWER (one for each pair set). Once the results are written into PORTn_AUTOCLASS_POWER fields, the Si3474 clears the PORTn_MANUAL_AUTOCLASS bits. When both PORTn_MANUAL_AUTOCLASS bits are cleared, the host can use this as an indication that the information is ready. The host may then overwrite the results of the police registers based on the power information supplied by the two PORTn_AUTOCLASS_POWER registers.

2.8.5 Current Limit and Voltage Foldback

The figure below illustrates how current limiting works. Consider an initial condition where the FET is ON, with the PD appearing like 167 Ω load. Let's say that suddenly, the load changes from 167 Ω to 62.5 Ω. The initial point condition is below the Green Line, which represents an ILIM Threshold vs VDRAIN template that the Si3474 is maintaining. Any difference between the actual current and this threshold results in whether or not current is flowing into the gate of the FET, or if it is flowing into the gate. The magnitude of the gate current is proportional to the difference between where the actual current through the sense resistor, relative to the set point.

When the load initially changes from 167 Ω to 62.5 Ω, the sensed current is higher than the ILIM Threshold at that VDRAIN voltage, and as such, the current is removed from the gate, leading to the FET shutting down slightly, leading to the VDRAIN increasing.

Eventually, the VDRAIN will increase high enough so that it meets the 62.5 Ω, where the gate drive becomes zero since the sensed current is at the green line. In this example, when the PD Load decreases from 167 Ω to 62.5 Ω, the port voltage folds back from 50 V down to around 22 V.

Note that the example does not show the intermediate steps, only the starting points and end points. This is a feedback circuit and this illustration cannot show the fact that the speed by which the VDRAIN increases is in proportion to the magnitude difference between the sensed current and the ILIM curve.

Some things to note include:

1. The FET power in the current limited state is 28 V * 350 mA = 9.8 W. To prevent damage, the Si3474 limits the time the FET spends in this condition.
2. The DRAIN Voltage is high. The Si3474 can measure this, and magnitude of the DRAIN Voltage, when taking the ILIM Template into account, is a good clue of the power level being experienced by the FET.

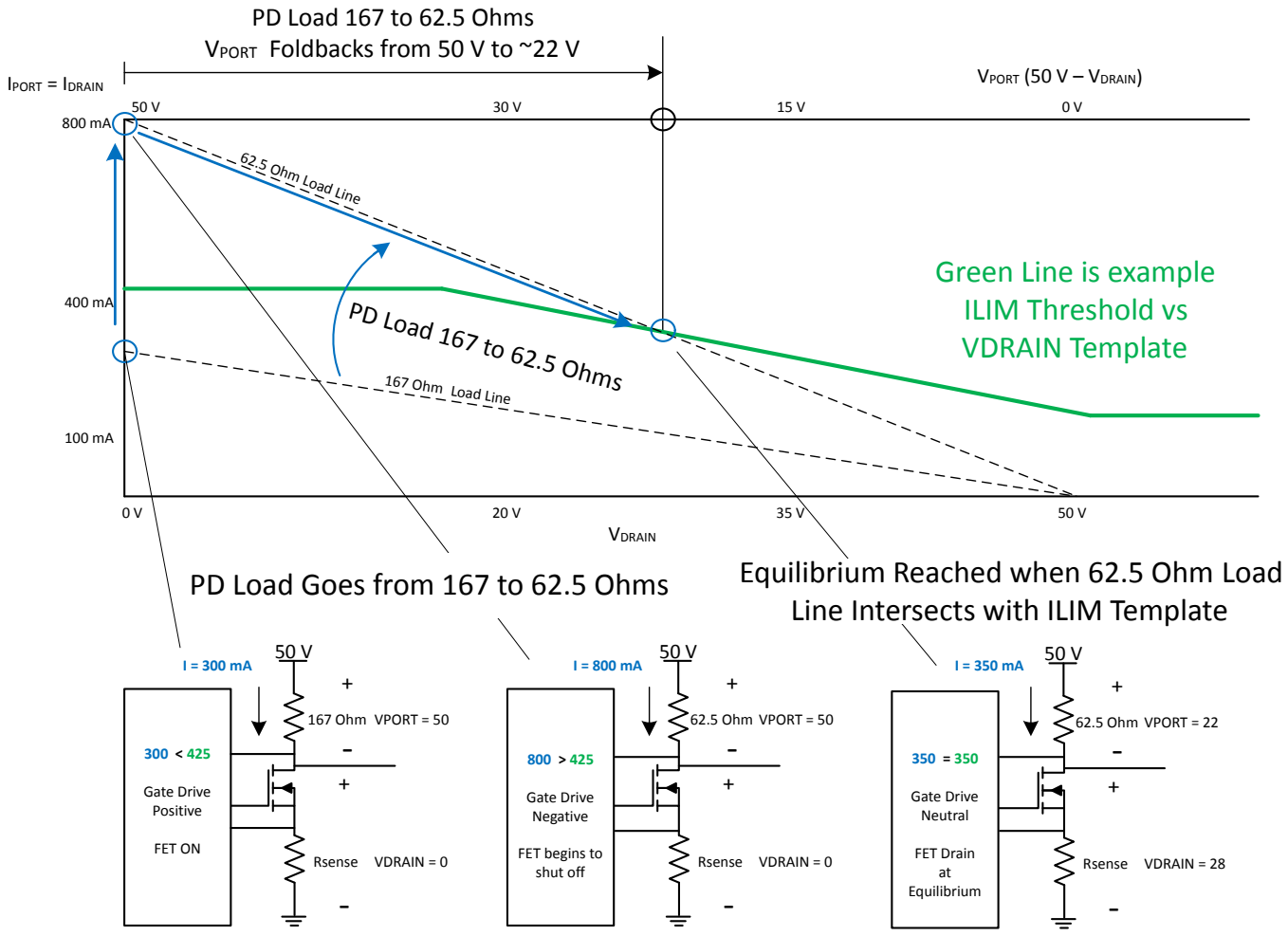


Figure 2.9. Current Limiting and Voltage Feedback

2.9 Event Handling

The host can communicate with the Si3474 at any time since the host is an I²C Master. For the Si3474 to communicate vital information to the host, it can only do so by asserting the INTb pin, and wait for the host to service the Si3474. However, it is not known when the host will service the Si3474. Therefore, there needs to be a way to have a way of communicating information without losing any of it if the host does not service the Si3474 immediately.

When the Si3474 wants attention from the host, it does so by setting an event in the event register map. The event bits map into a corresponding bit in the INTERRUPT register. If the corresponding INTERRUPT_MASK bit is also set, then this will cause INTb to assert.

Whenever the host receives an interrupt, the host should first read the INTERRUPT register from every I²C address. If there is a bit set, the host should then check the fields associated with that interrupt.

Refer to the figure below. The events are color-coded to have the same color as the associated bits in the INTERRUPT register. For example, when the host reads INTERRUPT, it sees the DISCONNECT_BIT set only. Note the color coding of DISCONNECT. The DISCONNECTION field and the OSS_EVENT fields are of the same color. In this case, the host would know to read DISCONNECT_PCUT_FAULT register SUPPLY_EVENT register as those are where the DISCONNECTION field and OSS_EVENT fields are located at.

Once the DISCONNECT_PCUT_FAULT_COR (0x07) and SUPPLY_EVENT_COR (0x0B) are read, the Si3474 will clear the DISCONNECT_BIT in the INTERRUPT register. If the DISCONNECT_BIT is the only bit that is set, then the INTb pin will negate.

It is important to note that each Si3474 contains two Quads. So, INTb will assert whenever there is an unserved interrupt in either Quad.

It is also important to note that if the host reads all the COR registers, it is not a guarantee that the INTb would negate. The reason being that a new event may have occurred after the COR register was read to clear the event. The host should take care to only service the events that it reads from the COR register as this is how the Si3474 knows that the host has picked up the event and had cleared it by reading the COR register.

It is important to note that PORTn_POWER_ON_FAULT is slightly different from the other event registers. When a PORTn_POWER_ON_FAULT event is reported, the corresponding PORTn_START_FAULT is also set. To service a PORTn_POWER_ON_FAULT, both the ILIM_START_FAULT CoR register and the POWER_ON_FAULT CoR register must be read to clear the START_EVENT_BIT in the INTERRUPT Register.

Address	Name	Access	7	6	5	4	3	2	1	0
INTERRUPT REGISTERS										
0x00	INTERRUPT	RO	SUPPLY_EVENT	START_EVENT	P_I_FAULT	CLASS_DONE	DETECT_CC_DONE	DISCONNECT	POWER_GOOD_CHANGE	POWER_ENABLE_CHANGE
0x01	INTERRUPT_MASK	R/W								
EVENT REGISTER BITS ASSOCIATED WITH INTERRUPT REGISTER										
0x02	POWER_EVENT	RO	POWER_GOOD_CHANGE				POWER_ENABLE_CHANGE			
0x03		CoR								
0x04	CLASS_DETECT_EVENT	RO	CLASS_DONE				DETECT_CC_DONE			
0x05		CoR								
0x06	DISCONNECT_PCUT_FAULT	RO	DISCONNECTION				PCUT_FAULT_2P			
0x07		CoR								
0x08	ILIM_START_FAULT	RO	ILIM_FAULT				START_FAULT			
0x09		CoR								
0x0A	SUPPLY_EVENT	RO	OVER_TEMP	VDD_UVLO_FAIL	VDD_UVLO_WARN	VPWR_UVLO	PORTnm_PCUT_FAULT_4P		OSS_EVENT	--
0x0B		CoR								
0x24	POWER_ON_FAULT	RO	PORT4_POWER_ON_FAULT		PORT3_POWER_ON_FAULT		PORT2_POWER_ON_FAULT		PORT1_POWER_ON_FAULT	
0x25		CoR								

2.10 Autonomous Operation

If it can be assumed that the total PD load can be supplied by the system VPWR, then it is suitable to use one of the two autonomous operations.

The two autonomous modes will be described as "virtual register settings", so as to leverage much of the prior discussion with typical use case when using Semi Auto and Pushbutton Power On.

2.10.1 AUTO Pin Autonomous Mode

A voltage divider is needed on the AUTO pin. A 15 kΩ resistor is needed from VDD to the AUTO pin, and the following resistors can be populated from the AUTO pin to GND.

Lower Resistor	2P / 4P Port	Class	Power	Equivalent Register Setting POWER_ALLOCATION
None	Hosted I2C Operation			
124 kΩ	2P	Class 3	15 W	0x00
61.9 kΩ	2P	Class 4	30 W	0x33
35.7 kΩ	4P	SS Class 4, DS Class 3 + Class 3	30 W	0xBB
22.6 kΩ	4P	SS Class 5, DS Class 4 + Class 3	45 W	0xCC
15.8 kΩ	4P	SS Class 6, DS Class 4 + Class 4	60 W	0xDD
11 kΩ	4P	SS Class 7, DS Class 5 + Class 4	75 W	0xEE
7.68 kΩ	4P	SS Class 8, DS Class 5 + Class 5	90 W	0xFF

The operation of AUTO Pin Autonomous Mode is identical to setting the following in both Quads:

1. PORT_REMAP = 0xE4 (no remapping)
2. POWER_ALLOCATION = AS_SHOWN_ABOVE
3. INTERRUPT_MASK = 0xE4 (faults enabled)
4. PORT_MODE = 0xFF (all ports in AUTO Mode)
5. PORT_DETECT_CLASS_ENABLE = 0xFF (all ports DETECT_CC_ENABLE = 1 and CLASS_ENABLE = 1)

2.10.2 I2C Autonomous Mode

When the PORTn_MODE is set to AUTO instead of SEMI_AUTO, as long as the PORTn_DETECT_CC_ENABLE and PORTn_CLASS_ENABLE is also set, then the operation is similar to SEMI_AUTO.

The main difference between SEMI_AUTO and AUTO is that when a PD successfully classifies, in SEMI_AUTO, the Si3474 keeps repeating Detection/Connection Check/Class Probe, whereas in AUTO Mode, the Si3474 acts as though it immediately received a PORTn_PB_POWER_ON, and proceeds with a Final Detection, Connection Check and Class Power On before powering up the port.

If a fault were to occur at any time, the Si3474 will go back into Continuous Detection / Connection Check / Class Probe and repeats the process over again. In summary, the Si3474 will simply “keep trying”.

Placing the Si3474 in I2C Autonomous Mode requires the following register settings to both Quads:

1. PORT_REMAP = 0xE4 (no remapping)
2. POWER_ALLOCATION = This depends on your system
3. INTERRUPT_MASK = 0xE4 (faults enabled)
4. PORT_MODE = 0xFF (all ports in AUTO Mode)
5. PORT_DETECT_CLASS_ENABLE = 0xFF (all ports DETECT_CC_ENABLE = 1 and CLASS_ENABLE = 1)

The setting of the POWER_ALLOCATION consists of setting the PORTnm_2P4P_MODE as well as the PORTnm_POWER_ALLOCATION registers. Refer to 4.26 POWER_ALLOCATION (0x29) for more details.

2.11 OSS Operation

2.11.1 Emergency Shutdown Feature

The Si3474 supports two kinds of Emergency Shutdown procedures, both of which are controlled by the host via the OSS pin (pin 36). If MULTIBIT_PRIORITY_ENABLE = 0 (in MISC register), then 2.11.1.1 1-Bit Shutdown Priority describes the Emergency Shutdown behavior. Otherwise, if MULTIBIT_PRIORITY_ENABLE = 1 (in MISC register), then 2.11.1.2 Multi-Bit Shutdown Priority describes the Emergency Shutdown behavior.

2.11.1.1 1-Bit Shutdown Priority

If MULTIBIT_PRIORITY_ENABLE = 0, then PORTn_PORT_POWER_PRIORITY bit in each port defines the port Shutdown priority. PORTn_PORT_POWER_PRIORITY bits are found in the POWER_PRIORITY_PCUT_DISABLE register. If PORTn_PORT_POWER_PRIORITY is set, then the associated port is tagged as a "Low Priority" ports. "High Priority" ports are unaffected by an OSS event.

A positive-going edge on pin 36 (OSS), will shut down powered lower priority ports. All powered lower priority ports will be shut down within 50 µs. Refer to the PORTn_PB_POWER_OFF description for all event and register bits that are cleared. Since PORTn_CLASS_ENABLE and PORTn_DETECT_CC_ENABLE are among one of the many bits that are cleared, no detection, connection check, or classification activity will occur until the PORTn_CLASS_ENABLE and PORTn_DETECT_CC_ENABLE are set again. As such, all events and associated measurement data are cleared. For as long as OSS is asserted high, low priority ports cannot be powered on.

2.11.1.2 Multi-Bit Shutdown Priority

If MULTIBIT_PRIORITY_ENABLE is set, then PORTn_MULTIBIT_PRIORITY defines the port priority and OSS action.

The figure below shows the operation and timing diagram of the OSS pin in multi-bit mode.

- The priority of each port is defined by a 3-bit value in PORTn_MULTIBIT_PRIORITY for each port.
- A port whose priority setting is "000" has the highest priority; priority setting of "111" has the lowest priority.
- When the host system wants certain priority ports to be shut down, it will transmit the “Shutdown code” over the OSS pin.
- Ports whose port priority settings are greater than or equal to the received Shutdown code will be turned off.
- For example, a received OSS Shutdown code of "101" will shut down ports whose port priority settings are "101", "110" or "111".

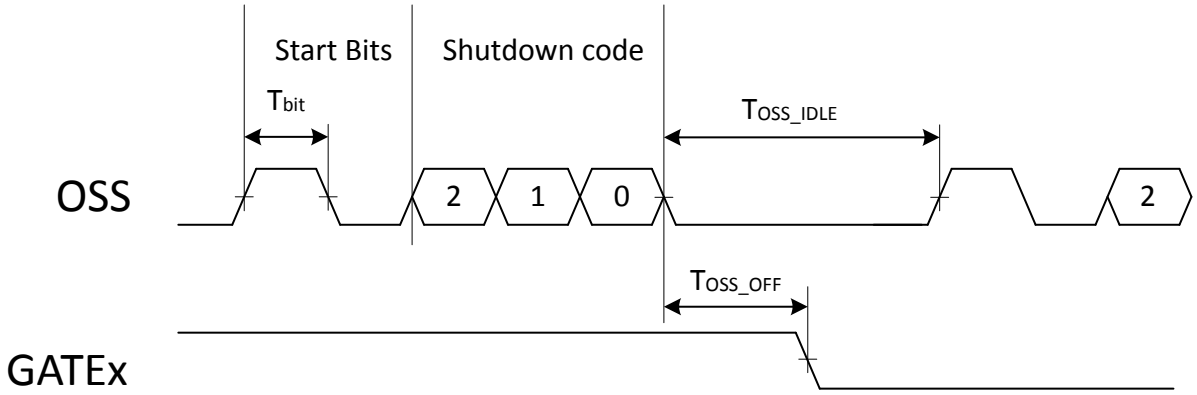


Figure 2.10. OSS Pin in Multi-Bit Mode

The following table describes the timing parameters associated with the OSS pin in multi-priority bit mode.

Table 2.1. Description of Timing Parameters Associated with the OSS Pin In Multi-Bit Mode

Parameter	Description	Min	Typ	Max	Units
T_{bit}	Bit Period	24	25	26	µs
T_{OSS_OFF}	Maximum time between receiving Shutdown code and shutting down of the ports	—	—	50	µs
T_{OSS_IDLE}	Idle time between consecutive Shutdown code transmission in multi-bit mode	125	—	—	µs

2.12 I²C Interface

2.12.1 I²C Protocol

Communicating with the Si3474 is accomplished through a 2-wire I²C compatible serial interface. An I²C transaction begins with a START condition and concludes with a STOP condition. Technically speaking, the interface to the Si3474 is better described as SMBus instead of I²C. SMBus transactions consist of I²C accesses in a manner that resembles a register map. The Si3474 registers are described in Table 4.1 Si3474 Registers[1] on page 27. Note that the Register Map describes the operation of a quad (four ports). Each Si3474 has two quads. As such the Si3474 responds to two I²C Addresses, one for each quad.

2.12.1.1 Slave Address

The I²C Slave Addresses, for which the Si3474 responds to, are dependent on the following:

- A1, A2, A3 and A4 pin strapping
- Quad

As mentioned previously, each Si3474 responds to two I²C Addresses since there are two quads in each Si3474.

The 7-bit Slave Address is effectively constructed as this bit pattern:

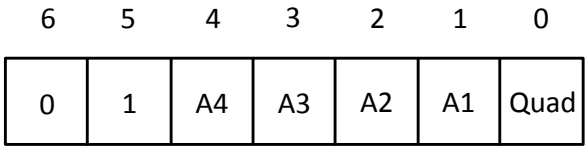


Figure 2.11. 7-bit I²C Address Bit Pattern

The following table outlines the I²C Addresses that the Si3474 will respond to, based on the A1, A2, A3 and A4 pin strapping as well as which quad the host intends to access:

Table 2.2. Si3474 I²C Slave Address

A4	A3	A2	A1	Quad 0 I²C Address	Quad 1 I²C Address
0	0	0	0	0x20	0x21
0	0	0	1	0x22	0x23
0	0	1	0	0x24	0x25
0	0	1	1	0x26	0x27
0	1	0	0	0x28	0x29
0	1	0	1	0x2A	0x2B
0	1	1	0	0x2C	0x2D
0	1	1	1	0x2E	0x2F
1	0	0	0	0x30	0x31
1	0	0	1	0x32	0x33
1	0	1	0	0x34	0x35
1	0	1	1	0x36	0x37
1	1	0	0	0x38	0x39
1	1	0	1	0x3A	0x3B
1	1	1	0	0x3C	0x3D
1	1	1	1	0x3E	0x3F

2.12.1.2 Available I²C Transfer Types

All Si3474 registers are accessible using 8-bit Writes and 8-bit Reads.

In addition, 16-bit Port Parametric Measurement Registers must be read using a 16-bit Read address in order to guarantee that the MSB and LSB of the Voltage or Current measurement belong to each other. The 16-bit Read Register Address should be pointing to the least significant byte so that the burst-read will end with the MSB.

Legend

S	Start Bit
Sr	Repeated Start Bit
P	Stop Bit
A1…A4	Si3474 A1, A2, A3, A4 pin strapping
Q	Si3474 Quad Selection (virtual ‘A0’)
R0…R7	Si3474 Register Address
D0…D7	Si3474 Register Data LSB
D8…D15	Si3474 Register Data MSB
Wr	Write Bit
Rd	Read Bit
A	ACK bit
N	No ACK bit

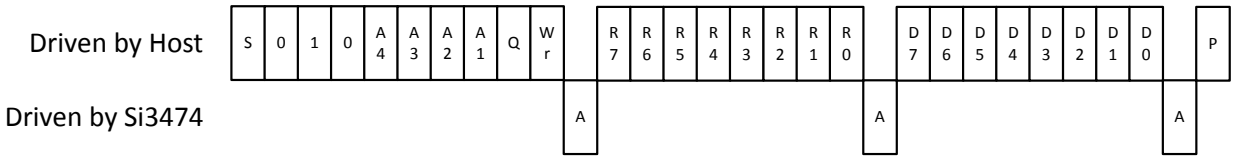


Figure 2.12. 8-Bit Write

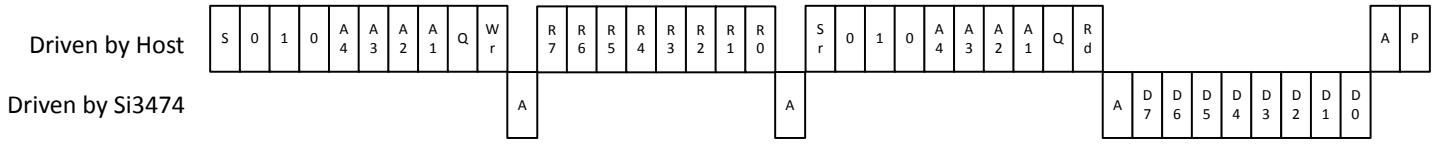


Figure 2.13. 8-Bit Read

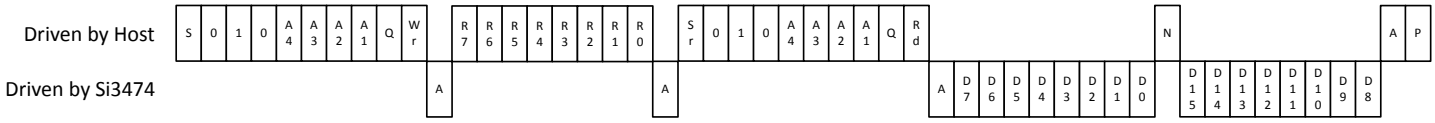


Figure 2.14. 16-Bit Read

2.13 Bootloader

2.13.1 Updating Si3474 Flash

The Si3474 Firmware can be updated through the I²C interface. The Si3474 firmware is roughly separated into the 'Application' firmware and a 'Bootloader' firmware. To ensure that the flash loading process never results in a non-communicating device, only the 'Application' part of the firmware is capable of being updated; the Bootloader cannot be updated.

The registers FLASH_CONTROL, FLASH_ERASE_KEY_FLASH_ADDRESS_LSB, FLASH_ADDRESS_MSB, FLASH_DATA work together to implement the flash update process. The figure above illustrates the flash loading sequence.

As a general rule, the flash update must always begin with checking the FIRMWARE_REVISION to see if a flash update is necessary or not. It is recommended to double-check that the Si3474 does not already have the latest firmware and that it does not need to be reflashed.

Once it has been determined that the device is to be updated, start the flash update procedure with a device reset.

Figure 2.15. Flash Loading Sequence

The chip reset is illustrated in Step 1. After a RESET, wait 30 ms before starting communication, as the device is booting. After the 30 ms wait period, the devices should be able to communicate through I²C, via the standard I²C Address based on the A1-A4 pin strapping.

In Step 3, Step 4 and Step 5, the host will individually command each device to enter its bootload state (FLASH_CONTROL=0xC1). Note that the host must access each device individually through its normal I²C address. It is also important to note that the host must access only the Quad 0. Quad 0 of each device has an even I²C Address. After each device receives its FLASCH_CONTROL=0xC1 command, each device will reset into a special state where the device will now respond to the Global Address 0x7F.

Once the host has send FLASH_CONTROL=0xC1 through each individual I²C Address it should delay an additional 30 ms in order to allow the last device to be ready. This 30 ms delay is illustrated in Step 6. After this final delay, the host can then proceed to Step 7, where the host would send another FLASH_CONTROL=0xC1 command. However, this time, the host will use the Global Address 0x7F. In addition, FLASH_ERASE_KEY=0xDB is sent prior to the FLASH_CONTROL=0xC1. This is illustrated on Step 7.

Upon receiving the FLASH_ERASE_KEY=0xDB and FLASH_CONTROL=0xC1 in Step 7, each device will begin to erase the Application FLASH area. This process takes 250 ms, and the host should not initiate communication during this time. This is illustrated on Step 8.

After the 250 ms delay, the host should then write 0x00 to both the FLASH_ADDRESS_LSB and FLASH_ADDRESS_MSB registers to indicate the starting address. This is illustrated in Steps 9 and 10.

The host then sends the contents of the new firmware by writing to the FLASH_DATA continuously. For accessing FLASH_DATA, in addition to the standard I^2C Register Byte Write method, the Si3474 also supports burst writes in order to increase the throughput of the flash update. The burst write is illustrated in the figure below:

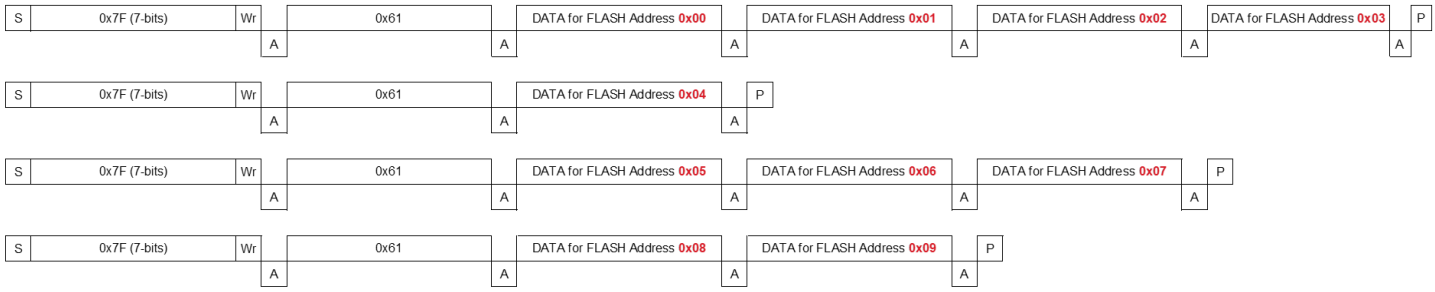


Figure 2.16. Burst Write

To complete the flash update, the host then writes FLASH_CONTROL=0x08 using the Global Address 0x7F. This is illustrated in Step 12. When each Si3474 device receives the FLASH_CONTROL=0x08 command, it completes the flash update process and computes the Flash CRC. Normally, the Si3474 reboots, and the FIRMWARE_REVISION Register can be checked using the normal non-global addresses to make sure that the firmware revision has been updated.

As previously mentioned, there is a separate Bootloader from the 'Application' firmware. As such, the Bootloader doesn't know what the FIRMWARE_REVISION is, that's why the check for the proper firmware revision needs to be done using the normal, non-global I^2C Addresses.

If in the event something goes wrong with the flash update, the host will receive a response of 0xFF response to a FIRMWARE_REVISION read. The host will receive 0xFF for all registers if the firmware update procedure fails. If this happens, the host should simply restart the entire process from the very beginning.

3. Typical Application Example

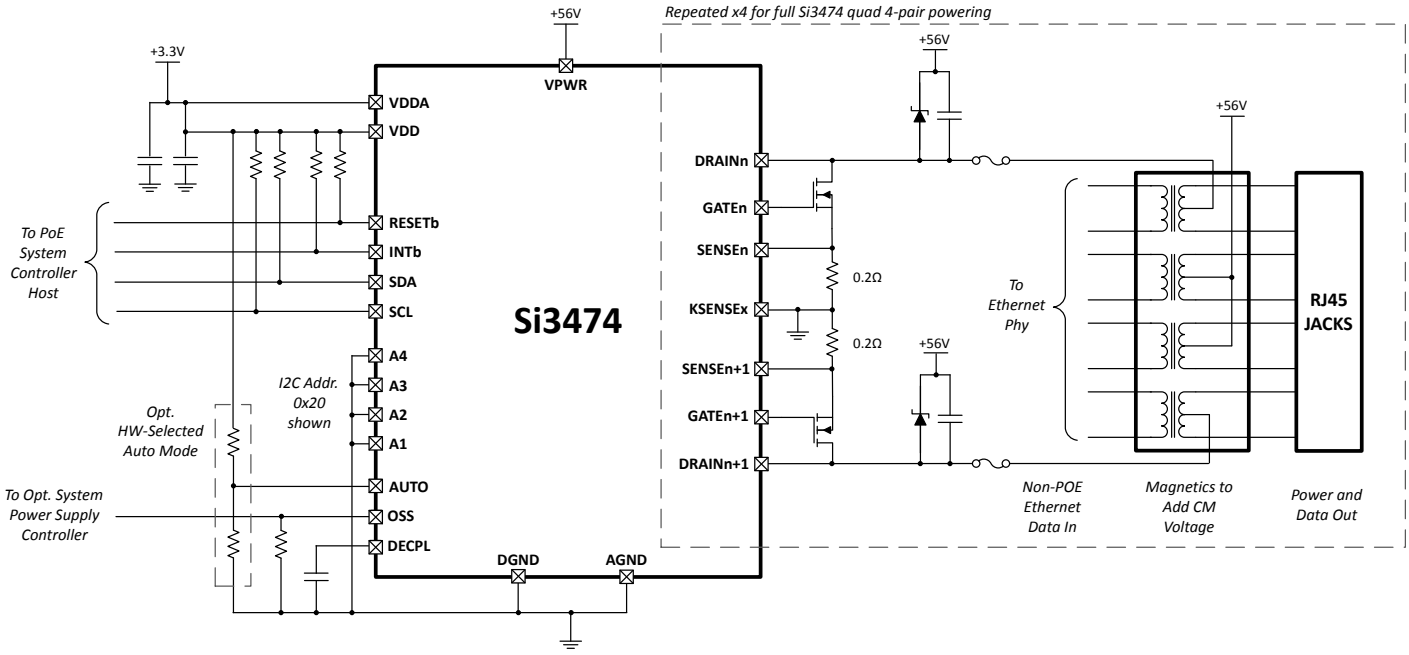


Figure 3.1. Si3474 Typical Application Circuit

4. Register Map

Table 4.1. Si3474 Registers[1]

Addr	Name	Access	Reset State	7	6	5	4	3	2	1	0
Interrupt Registers											
0x00	INTERRUPT	RO	1000 0000	SUPPLY_ EVENT	START_ EVENT	P_I_ FAULT	CLASS_ DONE	DETECT_ CC_ DONE	DISCON-NECT	POWER_ GOOD_ CHANGE	POWER_ ENABLE_ CHANGE
0x01	INTERRUPT_MASK	R/W	1000 0000								
Event Registers											
0x02	POWER_EVENT	RO	0000 0000	POWER_GOOD_CHANGE				POWER_ENABLE_CHANGE			
0x03		CoR									
0x04	CLASS_DETECT_EVENT	RO	0000 0000	CLASS_DONE				DETECT_CC_DONE			
0x05		CoR									
0x06	DISCONNECT_PCUT_FAULT	RO	0000 0000	DISCONNECTION				PCUT_FAULT_2P			
0x07		CoR									
0x08	ILIM_START_FAULT	RO	0000 0000	ILIM_FAULT				START_FAULT			
0x09		CoR									
0x0A	SUPPLY_EVENT	RO	0??? 0000	OVER_ TEMP	VDD_ UVLO_ FAIL	VDD_ UVLO_ WARN	VPWR_ UVLO	PORTnm_ PCUT_FAULT_4P		OSS_ EVENT	—
0x0B		CoR									
0x24	POWER_ON_FAULT	RO	0000 0000	PORT4_POWER_ ON_FAULT		PORT3_POWER_ ON_FAULT		PORT2_POWER_ ON_FAULT		PORT1_POWER_ ON_FAULT	
0x25		CoR	0000 0000								
Main Status Registers											
0x0C	PORT1_CLASS_ DETECT_STATUS	RO	0000 0000	PORT1_CLASS_STATUS				PORT1_DETECTION_STATUS			
0x0D	PORT2_CLASS_ DETECT_STATUS	RO	0000 0000	PORT2_CLASS_STATUS				PORT2_DETECTION_STATUS			
0x0E	PORT3_CLASS_ DETECT_STATUS	RO	0000 0000	PORT3_CLASS_STATUS				PORT3_DETECTION_STATUS			
0x0F	PORT4_CLASS_ DETECT_STATUS	RO	0000 0000	PORT4_CLASS_STATUS				PORT4_DETECTION_STATUS			

Addr	Name	Access	Reset State	7	6	5	4	3	2	1	0
0x10	POWER_STATUS	RO	0000 0000	POWER_GOOD				POWER_ENABLE			
0x11	PIN_STATUS	RO	0aaa aq00	—	PIN_A4	PIN_A3	PIN_A2	PIN_A1	QUAD	—	—
Main Configuration Registers											
0x12	PORT_MODE	R/W	0000 0000	PORT4_PORT_MODE		PORT3_PORT_MODE		PORT2_PORT_MODE		PORT1_PORT_MODE	
0x13	DISCONNECT_ENABLE	R/W	0000 1111	—				DISCONNECT_ENABLE			
0x14	DETECT_CLASS_ ENABLE	R/W	0000 0000	CLASS_ENABLE				DETECT_CC_ENABLE			
0x15	POWER_PRIORITY_ PCUT_DISABLE	R/W	0000 0000	PORT_POWER_PRIORITY				DISABLE_PCUT			
0x16	TIMING_CONFIG	R/W	0000 0000	TLIM		TSTART		TOVLD		TMPDO	
0x17	MISC	R/W	1000 0000	INT_PIN_ ENABLE	CAP_ MEAS_ ENABLE	—	MULTI-BIT_ PRIORI-TY_ ENA-BLE	CLASS_ CHANGE	DETECT_ CHANGE	—	—
Pushbuttons											
0x18	PB_DETECT_CLASS	WO	0000 0000	RESTART_CLASS				RESTART_DETECT			
0x19	PB_POWER_ENABLE	WO	0000 0000	PB_POWER_OFF				PB_POWER_ON			
0x1A	PB_RESET	WO	0000 0000	CLEAR_ ALL_INTS	CLEAR_ INT_PIN	—	RESET_ QUAD	RESET_PORT			

Addr	Name	Access	Reset State	7	6	5	4	3	2	1	0
Miscellaneous											
0x1B	VENDOR_ID	RO	0100 0101	MANUFACTURER_ID					IC_ID		
0x1C	AUTOCLASS_ CONNECTION_CHECK	RO	0000 0000	AUTOCLASS_DETECTED				CONNECTION_CHECK_RESULTS			
0x1D	Reserved	R/W	0000 0000	Reserved							
0x1E	PORT1_POLICE_2P	R/W	1111 1111	PORT1_POLICE_2P							
0x1F	PORT2_POLICE_2P	R/W	1111 1111	PORT2_POLICE_2P							
0x20	PORT3_POLICE_2P	R/W	1111 1111	PORT3_POLICE_2P							
0x21	PORT4_POLICE_2P	R/W	1111 1111	PORT4_POLICE_2P							
0x22-0x23	Reserved	R/W	0000 0000	—							
0x26	PORT_REMAP	R/W	1110 0100	PORT4_REMAP		PORT3_REMAP		PORT2_REMAP		PORT1_REMAP	
0x27	PORT1_PORT2_ MULTIBIT_PRIORITY	R/W	0000 0000	—	PORT2_MULTIBIT_PRIORITY			—	PORT1_MULTIBIT_PRIORITY		
0x28	PORT3_PORT_4_ MULTIBIT_PRIORITY	R/W	0000 0000	—	PORT4_MULTIBIT_PRIORITY			—	PORT3_MULTIBIT_PRIORITY		
0x29	POWER_ALLOCATION	R/W	0000 0000	—	PORT34_POWER_ALLOCATION			—	PORT12_POWER_ALLOCATION		
0x2A	PORT12_POLICE_4P	R/W	1111 1111	PORT12_POLICE_4P							
0x2B	PORT34_POLICE_4P	R/W	1111 1111	PORT34_POLICE_4P							
0x2C	TEMPERATURE	RO	???? ????	TEMPERATURE							
0x2D	ILIM_PCUT_ DISCONNECT_4P	R/W	0000 1100	ILIM_BEHAVIOR		PCUT_BEHAVIOR		PCUT_ENABLE		DISCON-NECT_THRESH	

Addr	Name	Access	Reset State	7	6	5	4	3	2	1	0
Must Use 16-BIT SMBUS Reads for Parametric Measurements											
0x2E	VPWR	RO	???? ????	LSB							
—		RO	00?? ????	—		MSB					
0x30	PORT1_CURRENT	RO	0000 0000	LSB							
—		RO	0000 0000	—		MSB					
0x32	PORT1_VOLTAGE	RO	0000 0000	LSB							
—		RO	0000 0000	—		MSB					
0x34	PORT2_CURRENT	RO	0000 0000	LSB							
—		RO	0000 0000	—		MSB					
0x36	PORT2_VOLTAGE	RO	0000 0000	LSB							
—		RO	0000 0000	—		MSB					
0x38	PORT3_CURRENT	RO	0000 0000	LSB							
—		RO	0000 0000	—		MSB					
0x3A	PORT3_VOLTAGE	RO	0000 0000	LSB							
—		RO	0000 0000	—		MSB					
0x3C	PORT4_CURRENT	RO	0000 0000	LSB							
—		RO	0000 0000	—		MSB					
0x3E	PORT4_VOLTAGE	RO	0000 0000	LSB							
—		RO	0000 0000	—		MSB					

Addr	Name	Access	Reset State	7	6	5	4	3	2	1	0
Firmware Revision And Chip Revision											
0x40	MAX_ILIM_MANUAL_POLICE	RW	0000 0000	MAX_ILIM				MANUAL_POLICE			
0x41	FIRMWARE_REVISION	RO	???? ????	MAJOR_REVISION				MINOR_REVISION			
0x42	I2C_WATCHDOG	RW	0001 0110	0	0	0	WATCHDOG_DISABLE				WATCH-DOG_STATUS
0x43	CHIP_REVISION	RO	???? ????	CHIP_REVISION							
Detection Resistance Results											
0x44	PORT1_DETECT_RESISTANCE	RO	0000 0000	PORT1_DETECT_RESISTANCE							
0x45	PORT2_DETECT_RESISTANCE	RO	0000 0000	PORT2_DETECT_RESISTANCE							
0x46	PORT3_DETECT_RESISTANCE	RO	0000 0000	PORT3_DETECT_RESISTANCE							
0x47	PORT4_DETECT_RESISTANCE	RO	0000 0000	PORT4_DETECT_RESISTANCE							
0x48	PORT1_DETECT_CAPACITANCE	RO	0000 0000	PORT1_DETECT_CAPACITANCE							
0x49	PORT2_DETECT_CAPACITANCE	RO	0000 0000	PORT2_DETECT_CAPACITANCE							
0x4A	PORT3_DETECT_CAPACITANCE	RO	0000 0000	PORT3_DETECT_CAPACITANCE							
0x4B	PORT4_DETECT_CAPACITANCE	RO	0000 0000	PORT4_DETECT_CAPACITANCE							

Addr	Name	Access	Reset State	7	6	5	4	3	2	1	0
Assigned Class and Requested Class											
0x4C	PORT1_CLASS_RESULTS	RO	0000 0000	PORT1_ASSIGNED_CLASS				PORT1_REQUESTED_CLASS			
0x4D	PORT2_CLASS_RESULTS	RO	0000 0000	PORT2_ASSIGNED_CLASS				PORT2_REQUESTED_CLASS			
0x4E	PORT3_CLASS_RESULTS	RO	0000 0000	PORT3_ASSIGNED_CLASS				PORT3_REQUESTED_CLASS			
0x4F	PORT4_CLASS_RESULTS	RO	0000 0000	PORT4_ASSIGNED_CLASS				PORT4_REQUESTED_CLASS			
Autoclass Configuration and Results											
0x50	AUTOCLASS_CONTROL	R/W	0000 0000	MANUAL_AUTOCLASS				AUTO_AUTOCLASS			
0x51	PORT1_AUTOCLASS_ RESULTS	R/W	0000 0000	0	PORT1_AUTOCLASS_POWER						
0x52	PORT2_AUTOCLASS_ RESULTS	R/W	0000 0000	0	PORT2_AUTOCLASS_POWER						
0x53	PORT3_AUTOCLASS_ RESULTS	R/W	0000 0000	0	PORT3_AUTOCLASS_POWER						
0x54	PORT4_AUTOCLASS_ RESULTS	R/W	0000 0000	0	PORT4_AUTOCLASS_POWER						
Miscellaneous											
0x55	ALTERNATIVE_FOLDBACK	R/W	0000 0000	PGOOD_FOLDBACK				INRUSH_850MA			
0x56 - 0x5E	Reserved	R/W	0000 0000	—							

Addr	Name	Access	Reset State	7	6	5	4	3	2	1	0
Flash Control											
0x5F	FLASH_ERASE_KEY	R/W	0000 0000	FLASH_ERASE_KEY							
0x60	FLASH_CONTROL	R/W	0000 0000	START_ FLASH-ING	RESET_ CPU	0	0	END_ FLASH-ING	0	0	CLEAR_ POINTER
0x61	FLASH_DATA	R/W	0000 0000	FLASH_DATA							
0x62	FLASH_ADDRESS_LSB	R/W	0000 0000	FLASH_ADDRESS_LSB							
0x63	FLASH_ADDRESS_MSB	R/W	0000 0000	FLASH_ADDRESS_MSB							
0x64-0xFF	Reserved	R/W	0000 0000	—							

Note:

1. A firmware FLASH update is required to use PORTn_DETECT_CAPACITANCE, TLIM, and PORTn_MAX_ILIM. Contact Skyworks for details.

4.1 INTERRUPT Register (Address 0x00)

INTERRUPT	Register Address: 0x00 Access Type: Read Only Reset: 1000 0000

7	6	5	4	3	2	1	0
SUP-PLY_EVENT_BIT	START_EVENT_BIT	P_I_FAULT_BIT	CLASS_DONE_BIT	DE-TECT_CC_DONE_BIT	DISCON-NECT_BIT	POW-ER_GOOD_CHANGE_BIT	POWER_ENA-BLE_CHANGE_BIT

Bit	Name	Description
7	SUPPLY_EVENT_BIT	VDD, VPWR or Temperature failed 0 = No Events 1 = At least one event in OVER_TEMP, VDD_UVLO_FAIL, VDD_UVLO_WARN, VPWR_UVLO in SUPPLY_EVENT
6	START_EVENT_BIT	Fault occurred after PORTn_PB_POWER_ON but before achieving PORTn_POW-ER_GOOD 0 = No Events 1 = At least one event bit in START_FAULT in ILIM_START_FAULT
5	P_I_FAULT_BIT	A port previously reached POWER_GOOD state is now unpowered due to a PCUT or ILIM event 0 = No Events 1 = At least one event bit in ILIM_FAULT in ILIM_START_FAULT, PCUT_FAULT_2P in DISCONNECT_PCUT_FAULT, PORTnm_PCUT_FAULT_4P in SUPPLY_EVENT
4	CLASS_DONE_BIT	Class Probe completed successfully 0 = No Events 1 = At least one event in CLASS_DONE in CLASS_DETECT_EVENT
3	DETECT_CC_DONE_BIT	Detection and Connection check completed 0 = No Events 1 = At least one event in DETECT_CC_DONE in CLASS_DETECT_EVENT
2	DISCONNECT_BIT	A port previously reached POWER_GOOD state is now unpowered because of PD disconnection or OSS_EVENT 0 = No Events 1 = At least one event bit in DISCONNECTION in DISCONNECT_PCUT_FAULT, OSS_EVENT in SUPPLY_EVENT
1	POWER_GOOD_CHANGE_BIT	POWER_GOOD in POWER_STATUS changed 0 = No Events 1 = At least one event in POWER_GOOD_CHANGE in POWER_EVENT
0	POWER_ENA-BLE_CHANGE_BIT	POWER_ENABLE in POWER_STATUS changed 0 = No Events 1 = At least one event in the POWER_ENABLE_CHANGE in POWER_EVENT

4.2 INTERRUPT_MASK Register (Address 0x01)

INTERRUPT_MASK	Register Address: 0x01 Access Type: Read / Write Reset: 1000 0000

7	6	5	4	3	2	1	0
SUP-PLY_EVENT_MASK_BIT	START_EVENT_MASK_BIT	P_I_FAULT_MASK_BIT	CLASS_DONE_MASK_BIT	DE-TECT_CC_DONE_MASK_BIT	DISCON-NECT_MASK_BIT	POW-ER_GOOD_CHANGE_MASK_BIT	POWER_ENA-BLE_CHANGE_MASK_BIT

Bit	Name	Description
7	SUPPLY_EVENT_MASK_BIT	Masks SUPPLY_EVENT_BIT in the INTERRUPT register 0 = SUPPLY_EVENT_BIT not can assert INTb 1 = SUPPLY_EVENT_BIT can assert INTb
6	START_EVENT_MASK_BIT	Masks START_EVENT_BIT in the INTERRUPT register 0 = START_EVENT_BIT cannot assert INTb 1 = START_EVENT_BIT can assert INTb
5	P_I_FAULT_MASK_BIT	Masks the P_I_FAULT_BIT in the INTERRUPT register 0 = P_I_FAULT_BIT cannot assert INTb 1 = P_I_FAULT_BIT can assert INTb
4	CLASS_DONE_MASK_BIT	Masks the CLASS_DONE_BIT in the INTERRUPT register 0 = CLASS_DONE_BIT cannot assert INTb 1 = CLASS_DONE_BIT can assert INTb
3	DE-TECT_CC_DONE_MASK_BIT	Masks the DETECT_CC_DONE_BIT in the INTERRUPT register 0 = DETECT_CC_DONE_BIT cannot assert INTb 1 = DETECT_CC_DONE_BIT can assert INTb
2	DISCONNECT_MASK_BIT	Masks DISCONNECT_BIT in the INTERRUPT register 0 = DISCONNECT_BIT cannot assert INTb 1 = DISCONNECT_BIT can assert INTb
1	POW-ER_GOOD_CHANGE_MASK_BIT	Masks POWER_GOOD_CHANGE_BIT in the INTERRUPT register 0 = POWER_GOOD_CHANGE_BIT cannot assert INTb 1 = POWER_GOOD_CHANGE_BIT can assert INTb
0	POWER_ENA-BLE_CHANGE_MASK_BIT	Masks POWER_ENABLE_CHANGE_BIT in the INTERRUPT register 0 = POWER_ENABLE_CHANGE_BIT cannot assert INTb 1 = POWER_ENABLE_CHANGE_BIT can assert INTb

The INTERRUPT and INTERRUPT_MASK registers work together to influence the INTb pin logic for any given Quad. Each Si3474 has two Quads, and either Quad can assert the INTb pin independently of each other.

$Quad\_0\_INT = INTERRUPT_{Q0}$ AND $INTERRUPT\_MASK_{Q0}$

$Quad\_1\_INT = INTERRUPT_{Q1}$ AND $INTERRUPT\_MASK_{Q1}$

INTb = NOT (Quad_0_INT OR Quad_1_INT)

Bits in the in the INTERRUPT register can be cleared by a number of actions:

1. Reading CoR EVENT registers
2. Setting PORTn_PORT_MODE to SHUTDOWN
3. Setting PORTn_PB_POWER_OFF
4. Setting RESET_QUAD
5. Setting PORTn_RESET_PORT
6. Set CLEAR_ALL_INTS
7. OSS Emergency Shutdown

It is also possible to negate the INTb pin directly using the CLEAR_INT_PIN. This method does not clear any event register bits, nor does it clear bits in the INTERRUPT register.

4.3 Event Registers

These registers provide event status information. For these event registers, there is an RO register and a separate COR register. The COR version of an event register will clear those events when they are read. Consequently, by clearing the event, the INTERRUPT register bit corresponding to the event register may get cleared as a result. The graphic shows how the various event registers map into the INTERRUPT register bits.

For example, The DISCONNECT_BIT in INTERRUPT sets when either OSS_EVENT in SUPPLY_EVENT is set, or if one or more DISCONNECTION bits are set in the DISCONNECT_PCUT_FAULT. All of these bits are color-coded to illustrate their relationship.

If the SUPPLY_EVENT COR is read, the OSS_EVENT may clear, but if there are still set DISCONNECTION bits in DISCONNECT_PCUT_FAULT, the DISCONNECT_BIT in INTERRUPT will remain asserted. The DISCONNECT_BIT in INTERRUPT will only clear if all event bits, shown in the same color, are all zeroes.

Once the DISCONNECT_BIT in INTERRUPT is cleared, and if there are no other set bits in INTERRUPT on BOTH QUADS, then the INTb is negated.

In addition to reading of the CoR register, PORTn_CLASS_DONE, PORTn_DETECT_CC_DONE, PORTn_DISCONNECTION, PORTn_PCUT_FAULT_2P, PORTn_ILIM_FAULT, PORTn_START_FAULT, PORTnm_PCUT_FAULT_4P can also be cleared by the following:

1. Set PORTn_PORT_MODE to SHUTDOWN
2. Set PORTn_PB_POWER_OFF in PB_POWER_ENABLE
3. Set PORTn_RESET_PORT in PB_RESET
4. OSS_EVENT in SUPPLY_EVENT as a result of an emergency shutdown
5. Set RESET_QUAD
6. Set CLEAR_ALL_INTS

Consequently, INTb may also negate as a result of these event bits being cleared when the COR register is read.

Address	Name	Access	7	6	5	4	3	2	1	0
INTERRUPT REGISTERS										
0x00	INTERRUPT	RO	SUPPLY_EVENT	START_EVENT	P_I_FAULT	CLASS_DONE	DETECT_CC_DONE	DISCONNECT	POWER_GOOD_CHANGE	POWER_ENABLE_CHANGE
0x01	INTERRUPT_MASK	R/W								
EVENT REGISTER BITS ASSOCIATED WITH INTERRUPT REGISTER										
0x02	POWER_EVENT	RO	POWER_GOOD_CHANGE				POWER_ENABLE_CHANGE			
0x03		CoR								
0x04	CLASS_DETECT_EVENT	RO	CLASS_DONE				DETECT_CC_DONE			
0x05		CoR								
0x06	DISCONNECT_PCUT_FAULT	RO	DISCONNECTION				PCUT_FAULT_2P			
0x07		CoR								
0x08	ILIM_START_FAULT	RO	ILIM_FAULT				START_FAULT			
0x09		CoR								
0x0A	SUPPLY_EVENT	RO	OVER_TEMP	VDD_UVLO_FAIL	VDD_UVLO_WARN	VPWR_UVLO	PORTnm_PCUT_FAULT_4P		OSS_EVENT	--
0x0B		CoR								
0x24	POWER_ON_FAULT	RO	PORT4_POWER_ON_FAULT		PORT3_POWER_ON_FAULT		PORT2_POWER_ON_FAULT		PORT1_POWER_ON_FAULT	
0x25		CoR								

4.4 POWER Event and POWER Event CoR (Address 0x02, 0x03)

POWER_EVENT				Register Address: 0x02 Access Type: Read Only Reset: 0000 0000			Register Address: 0x03 Access Type: Clear on Read Reset: 0000 0000
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POWER_GOOD_CHANGE				POWER_ENABLE_CHANGE			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_POWER_GOOD_CHANGE	PORTn_POWER_GOOD_CHANGE PORTn_POWER_GOOD in POWER_STATUS register changed 0 = PORTn_POWER_GOOD did not change 1 = PORTn_POWER_GOOD changed
6	PORT3_POWER_GOOD_CHANGE	
5	PORT2_POWER_GOOD_CHANGE	
4	PORT1_POWER_GOOD_CHANGE	
3	PORT4_POWER_ENABLE_CHANGE	PORTn_POWER_ENABLE_CHANGE PORTn_POWER_ENABLE in POWER_STATUS register changed 0 = PORTn_POWER_ENABLE did not change 1 = PORTn_POWER_ENABLE changed
2	PORT3_POWER_ENABLE_CHANGE	
1	PORT2_POWER_ENABLE_CHANGE	
0	PORT1_POWER_ENABLE_CHANGE	

For a description of what POWER_GOOD and POWER_ENABLE means, refer to the description in the POWER_STATUS register.

PORTn_POWER_GOOD_CHANGE indicates that PORTn_POWER_GOOD in the POWER_STATUS register has changed. Any set PORTn_POWER_GOOD_CHANGE bit will also set the POWER_GOOD_CHANGE_BIT in the INTERRUPT register.

PORTn_POWER_ENABLE_CHANGE indicates that PORTn_POWER_ENABLE in the POWER_STATUS register has changed. Any set PORTn_POWER_ENABLE_CHANGE bit will also set the POWER_ENABLE_CHANGE_BIT in the INTERRUPT register.

4.5 CLASS_DETECT_EVENT and CLASS_DETECT_EVENT CoR (0x04, 0x05)

CLASS_DETECT_EVENT				Register Address: 0x04 Access Type: Read Only Reset: 0000 0000			Register Address: 0x05 Access Type: Clear on Read Reset: 0000 0000
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS_DONE				DETECT_CC_DONE			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_CLASS_DONE	PORTn_CLASS_DONE PORTn_CLASS_STATUS in PORTn_CLASS_DETECT_STATUS register was updated or changed (see also CLASS_CHANGE in 4.17 MISC (0x17)). 0 = PORTn_CLASS_STATUS was not updated nor changed. 1 = PORTn_CLASS_STATUS was updated or changed.
6	PORT3_CLASS_DONE	
5	PORT2_CLASS_DONE	
4	PORT1_CLASS_DONE	
3	PORT4_DETECT_CC_DONE	PORTn_DETECT_CC_DONE PORTn_DETECTION_STATUS in PORTn_CLASS_DETECT_STATUS register was updated or changed (see also DETECT_CHANGE in 4.17 MISC (0x17)). 0 = PORTn_DETECTION_STATUS was not updated nor changed. 1 = PORTn_DETECTION_STATUS was updated or changed.
2	PORT3_DETECT_CC_DONE	
1	PORT2_DETECT_CC_DONE	
0	PORT1_DETECT_CC_DONE	

PORTn_DETECT_CC_DONE indicates whether the PORTn_DETECTION_STATUS in PORTn_CLASS_DETECT_STATUS has valid results. The PORTnm_CONNECTION_CHECK_RESULTS in the AUTOCLASS_CONNECTION_CHECK register also have useful information for 4P Ports. Any set bits in the DETECT_CC_DONE field sets the DETECT_CC_DONE_BIT in the INTERRUPT register.

One common usability issue with enabling the DETECT_CC_DONE_BIT interrupt is that there tends to be a lot of detection events. One good way of reducing the number of interrupts is by also setting the DETECT_CHANGE bit in the MISC register. When this bit is set, the PORTn_DETECT_CC_DONE is only updated whenever there is a change in PORTn_DETECTION_STATUS, thereby reducing the number of interrupts to the system.

PORTn_CLASS_DONE indicates whether PORTn_CLASS_STATUS in PORTn_CLASS_DETECT_STATUS register has valid results. The PORTn_CLASS_DETECT_STATUS will always indicate RGOOD as Class Probe does not occur without RGOOD. PORTnm_CONNECTION_CHECK_RESULTS also will be updated for 4P Ports. Any set PORTn_CLASS_DONE bits also sets CLASS_DONE_BIT in the INTERRUPT register.

4.6 DISCONNECT_PCUT_FAULT and DISCONNECT_PCUT_FAULT CoR (0x06, 0x07)

DISCONNECT_PCUT_FAULT				Register Address: 0x06 Access Type: Read Only Reset: 0000 0000			Register Address: 0x07 Access Type: Clear on Read Reset: 0000 0000
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISCONNECTION				PCUT_FAULT_2P			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_DISCONNECTION	PORTn_DISCONNECTION A PORTn in POWER_GOOD, did not detect sufficient current to meet MPS requirements, leading to a disconnection. 0 = PORTn did not disconnect. 1 = PORTn disconnected.
6	PORT3_DISCONNECTION	
5	PORT2_DISCONNECTION	
4	PORT1_DISCONNECTION	
3	PORT4_PCUT_FAULT_2P	PORTn_PCUT_FAULT_2P PORTn in POWER_GOOD state, was powered off because it exceeded the power threshold defined by the pertinent PORTn_POLICE_2P register. 0 = PORTn did not encounter a PCUT fault. 1 = PORTn encountered a PCUT fault.
2	PORT3_PCUT_FAULT_2P	
1	PORT2_PCUT_FAULT_2P	
0	PORT1_PCUT_FAULT_2P	

PORTn_DISCONNECTION indicates a powered port was formerly in a POWER_GOOD state is now unpowered because the PD drew sufficient current. Any set PORTn_DISCONNECTION bits also set the DISCONNECT_BIT in the INTERRUPT register.

PORTn_PCUT_FAULT_2P indicates a powered port, formerly in a POWER_GOOD state, is now unpowered because the PD exceeded the power limits specified by the various POLICE registers. Any set PORTn_PCUT_FAULT_2P bits will set the P_I_FAULT_BIT in the INTERRUPT register.

4.7 ILIM_START_FAULT and ILIM_START_FAULT CoR (0x08, 0x09)

ILIM_START_FAULT				Register Address: 0x08 Access Type: Read Only Reset: 0000 0000			Register Address: 0x09 Access Type: Clear on Read Reset: 0000 0000
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ILIIM_FAULT				START_FAULT			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_ILIM_FAULT	PORTn_ILIM_FAULT PORTn previously in POWER_GOOD state, encountered an overcurrent event, for longer than tLIM, leading to the port being powered down. 0 = PORTn did not encounter an ILIM fault. 1 = PORTn encountered an ILIM fault.
6	PORT3_ILIM_FAULT	
5	PORT2_ILIM_FAULT	
4	PORT1_ILIM_FAULT	
3	PORT4_START_FAULT	PORTn_START_FAULT PORTn was still powering up encountered an overcurrent condition, for longer than the tINRUSH. PORTn never achieved a POWER_GOOD status and is not powered. 0 = PORTn did not encounter a start fault. 1 = PORTn encountered a start fault.
2	PORT3_START_FAULT	
1	PORT2_START_FAULT	
0	PORT1_START_FAULT	

PORTn_ILIM_FAULT indicates that a powered port in POWER_GOOD state is now unpowered because the port was in a current-limited state for longer than the t_{ILIM} time limit. Any set PORTn_ILIM_FAULT bits will set the P_I_FAULT_BIT in the INTERRUPT register.

PORTn_START_FAULT indicates that a powering port (POWER_ENABLE is set but POWER_GOOD is not set) did not reach POWER_GOOD because PORTn was in a current-limited state for longer than the t_{INRUSH} time limit. Any set PORTn_START_FAULT bits will set the START_FAULT_BIT in the INTERRUPT register.

4.8 SUPPLY_EVENT and SUPPLY_EVENT CoR (0x0A, 0x0B)

SUPPLY_EVENT				Register Address: 0x0A Access Type: Read Only Reset: 0001 0000		Register Address: 0x0B Access Type: Clear on Read Reset: 0001 0000	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_TEMP	VDD_UV-LO_FAIL	VDD_UV-LO_WARN	VPWR_UVLO	PCUT_FAULT_4P		OSS_EVENT	—
—	—	—	—	PORT34	PORT12	—	—

Bit	Name	Description
7	OVER_TEMP	Device temperature monitoring indicator 0 = Normal temperature. 1 = Device case temperature exceeded 125 °C.
6	VDD_UVLO_FAIL	VDD UVLO Failure Status 0 = VDD is greater than 2.25 V. 1 = VDD was measured to be under 2.25 V. Upon entering this condition, VDD needs to be higher than 2.6 V to exit this condition.
5	VDD_UVLO_WARN	VDD UVLO Warning Status 0 = VDD is greater than 2.8 V. 1 = VDD was measured under 2.8 V. Upon entering this condition, VDD needs to be higher than 3.1 V to exit this condition.
4	VPWR_UVLO	VPWR UVLO Status 0 = VPWR is greater than 28 V. 1 = VPWR was measured to be less than 28 V. Upon entering this condition, VPWR needs to be higher than 31 V to exit this condition.
3	PORT34_PCUT_FAULT_4P	The 4PP PD connected to PORT3 and PORT4 exceeded the power threshold defined by PORT34_POLICE_4P register, leading to a disconnection. 0 = PORT34 did not disconnect. 1 = PORT34 encountered a PCUT fault.
2	PORT12_PCUT_FAULT_4P	The 4PP PD connected to PORT1 and PORT2 exceeded the power threshold defined by PORT12_POLICE_4P register, leading to a disconnection. 0 = PORT12 did not disconnect. 1 = PORT12 encountered a PCUT fault.
1	OSS_EVENT	Emergency shutdown affected one of the ports in the quad. 0 = No emergency shutdown event. 1 = At least one low priority port was shut down.

When one of OVER_TEMP, VDD_UVLO_FAIL, VDD_UVLO_WARN, and VPWR_UVLO are set, SUPPLY_EVENT_BIT in the INTERRUPT register is also set. Ports are powered off; no Detection, Classification and Power can occur while these events persist.

When either PORTnm_PCUT_FAULT_4P is set, the P_I_FAULT_BIT in the INTERRUPT register is also set.

When then the OSS_EVENT bit is set, the DISCONNECT_BIT in the INTERRUPT register is also set.

4.9 POWER_ON_FAULT and POWER_ON_FAULT CoR (0x24, 0x25)

POWER_ON_FAULT				Register Address: 0x24 Access Type: Read Only Reset: 0000 0000		Register Address: 0x25 Access Type: Clear on Read Reset: 0000 0000	
7	6	5	4	3	2	1	0
POWER_ON_FAULT		POWER_ON_FAULT		POWER_ON_FAULT		POWER_ON_FAULT	
PORT4		PORT3		PORT2		PORT1	

Bit	Name	Description
7-6	PORT4_POWER_ON_FAULT	PORTn_POWER_ON_FAULT While attempting to turn on a port, a fault occurred even before turning on the FET. 00 = No Event. 01 = Invalid Detection. 10 = Classification Error. 11 = Insufficient power allocation.
5-4	PORT3_POWER_ON_FAULT	
3-2	PORT2_POWER_ON_FAULT	
1-0	PORT1_POWER_ON_FAULT	

When PORTn_POWER_ON_FAULT is set, START_FAULT_BIT in INTERRUPT register is also set.

4.10 CLASS_DETECT_STATUS Registers (0x0C–0x0F)

PORTn_CLASS_DETECT_STATUS Register	Register Address: 0x0C/0x0D/0x0E/0x0F; Port 1/2/3/4 respectively Access Type: Read Only Reset: 0000 0000 for each PORTn_CLASS_DETECT_STATUS

7	6	5	4	3	2	1	0
PORTn_CLASS_STATUS				PORTn_DETECTION_STATUS			

Code	PORTn_CLASS_STATUS	Code	PORTn_DETECTION_STATUS
0000	UNKNOWN	0000	UNKNOWN
0001	Class 1	0001	Short circuit
0010	Class 2	0010	Capacitive[1]
0011	Class 3	0011	RLOW
0100	Class 4	0100	RGOOD
0101	—	0101	RHIGH
0110	Class 0	0110	Open circuit
0111	Overcurrent	0111	PSE to PSE[2]
1000	Class 5 4P SS	1000	—
1001	Class 6 4P SS	1001	—
1010	Class 7 4P SS	1010	—
1011	Class 8 4P SS	1011	—
1100	Class 4+ Type 1 Limited[1]	1100	—
1101	Class 5 DS	1101	—
1110	—	1110	—
1111	Class Mismatch[2]	1111	MOSFET_FAULT

Note:

1. Class 4+ Type 1 Limited is not emitted in Semi Auto Class Probe. It may occur during a Class Power On as a result of PB_POWER_ON
2. The Si3474 automatically performs a Class Reset and repeats classification.

Note:

1. Capacitive status is reported when the load capacitance is bigger than 1.5 µF (Cpd > 1.5 µF).
2. The Si3474 is capable of detecting whether it is cross-connected to another PSE controller of a different type. In this case, the PSE to PSE Status is reported. Detection of another PSE is based on verifying the voltage level on the output (DRAINn pin) during detection.

In SEMI_AUTO mode, the classification process is not initiated unless RGOOD is reported. When reading PORTn_CLASS_STATUS outside of an event handler servicing the PORTn_CLASS_DONE, the classification status can be unknown, or it can be the last classification status after the last RGOOD.

It is generally recommended to only read PORTn_CLASS_STATUS only when PORTn_CLASS_DONE indicates that there is useful information available.

4.11 PORT_POWER_STATUS Register (0x10)

PORT_POWER_STATUS				Register Address: 0x10 Access Type: Read Only Reset: 0000 0000			
7	6	5	4	3	2	1	0
POWER_GOOD				POWER_ENABLE			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_POWER_GOOD	PORTn has passed through the initial inrush period and has successfully powered up the port 0 = OFF 1 = PORTn is in POWER_GOOD state PORTn is in POWER_GOOD state after the initial t_{INRUSH} and that the PORTn Drain is within 2 V of the Si3474 ground reference.
6	PORT3_POWER_GOOD	
5	PORT2_POWER_GOOD	
4	PORT1_POWER_GOOD	
3	PORT4_POWER_ENABLE	PORTn_POWER_ENABLE correlates to PORTn FET ON / OFF Status. 0 = FET is turned OFF. 1 = FET is turned ON. After a PORTn_PB_POWER_ON, the PORTn_POWER_ENABLE is set after the Detection, Connection Check and Class Power On.
2	PORT3_POWER_ENABLE	
1	PORT2_POWER_ENABLE	
0	PORT1_POWER_ENABLE	

The main difference between the POWER_ENABLE and POWER_GOOD concepts is rooted in time delays.

Assume for a moment that both PORTn_POWER_ENABLE and PORTn_POWER_GOOD are both OFF, as an initial condition of this illustration.

When a PORTn_PB_POWER_ON is set, there is typically a delay from that pushbutton setting to when the Si3474 starts drives the GATE of the FET to turn it on. However, between PORTn_PB_POWER_ON and the GATE drive, the Si3474 may need to complete servicing other ports before starting to service the PORTn_PB_POWER_ON. Even if the Si3474 began servicing the PORTn_PB_POWER_ON, the port will still need to go through Detection, Connection Check and Class Power On before turning on the FET.

At the time then the Si3474 drives the FET, this is when PORTn_POWER_ENABLE is declared.

At this point, PORTn_POWER_ENABLE is ON, but PORTn_POWER_GOOD is still OFF. This effectively defines an initial start-up period where the port is allowed to current-limit for short t_{INRUSH} duration in order to charge up the PD capacitors. During this time, it is possible that the FET DRAIN would be folded-back to enforce this start-up current limit. Once the t_{INRUSH} period is over, if the DRAIN voltage is less than 2 V, this is when POWER_GOOD state is declared, and that in the POWER_GOOD state, both PORTn_POWER_ENABLE and PORTn_POWER_GOOD are both ON.

Once in POWER_GOOD state, the port is then monitored for ILIM, PCUT and DISCONNECTION events. Throughout this document, POWER_GOOD state is sometimes used to distinguish between the initial t_{INRUSH} period and the long-term port monitoring of these events.

When a port is turned off, PORTn_POWER_ENABLE and PORTn_POWER_GOOD bits both changes to OFF simultaneously.

The POWER_ENABLE_CHANGE and POWER_GOOD_CHANGE is used to mark the transition time, as these transition times are what marks the status of both the FET, and the actions the Si3474 is performing as part of servicing that port.

4.12 PORT_MODE (0x12)

PORT_MODE				Register Address: 0x12 Access Type: Read / Write Reset: 0000 0000			
7	6	5	4	3	2	1	0
PORT_MODE		PORT_MODE		PORT_MODE		PORT_MODE	
PORT4		PORT3		PORT2		PORT1	

Bit	Name	Description
7-6	PORT4_PORT_MODE	PORTn_PORT_MODE Sets the main port operating mode. SEMI_AUTO is used in managed power use case. AUTO mode is used in unmanaged power use case. MANUAL mode is used generally for debug only. 00 = Set PORTn to SHUTDOWN Mode. 01 = Set PORTn to MANUAL Mode. 10 = Set PORTn to SEMI_AUTO Mode. 11 = Set PORTn to AUTO Mode. See 4.14 DETECT_CLASS_ENABLE (0x14) and 4.19 PB_POWER_ENABLE (0x19).
5-4	PORT3_PORT_MODE	
3-2	PORT2_PORT_MODE	
1-0	PORT1_PORT_MODE	

Setting PORTn_PORT_MODE to SHUTDOWN clears numerous port registers, and possibly the associated INTERRUPT bits. Refer to description of PORTn_PB_POWER_OFF in PB_POWER_ENABLE for this list.

Outside of the host setting PORTn_PORT_MODE, PORTn_PORT_MODE can be set to SHUTDOWN when RESET_QUAD is set.

After setting SEMI_AUTO in PORTn_PORT_MODE, PORTn_CLASS_ENABLE and PORTn_DETECT_CC_ENABLE in DETECT_CC_ENABLE should also be set to begin continuous Detection, Connection Check and Class Probe. Refer to DETECT_CLASS_ENABLE register.

4.13 DISCONNECT_ENABLE (0x13)

DISCONNECT_ENABLE				Register Address: 0x13 Access Type: Read / Write Reset: 0000 1111			
7	6	5	4	3	2	1	0
				DISCONNECT_ENABLE			
				PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
3	PORT4_DISCONNECT_ENABLE	PORTn_DISCONNECT_ENABLE Defines operation of a port in POWER GOOD state, whether or not to allow disconnection if the PD does not draw sufficient current and does not meet MPS requirements. Overcurrent and PCUT faults will still result in a disconnection. 0 = Keep port power even if PD current too low. 1 = Normal Disconnection Monitoring.
2	PORT3_DISCONNECT_ENABLE	
1	PORT2_DISCONNECT_ENABLE	
0	PORT1_DISCONNECT_ENABLE	

4.14 DETECT_CLASS_ENABLE (0x14)

DETECT_CLASS_ENABLE				Register Address: 0x14 Access Type: Read / Write Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLASS_ENABLE				DETECT_CC_ENABLE			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	PORTn_CLASS_ENABLE	PORTn_DETECT_CC_ENABLE	Description
7 / 3	PORT4_CLASS_ENABLE	PORT4_DETECT_CC_ENABLE	PORTn_CLASS_ENABLE / PORTn_DETECT_CC_ENABLE It is more useful to describe CLASS_ENABLE and DETECT_CC_ENABLE together. CLASS_ENABLE is shown on the left; DETECT_CC_ENABLE shown on the right.
6 / 2	PORT3_CLASS_ENABLE	PORT3_DETECT_CC_ENABLE	
5 / 1	PORT2_CLASS_ENABLE	PORT2_DETECT_CC_ENABLE	
4 / 0	PORT1_CLASS_ENABLE	PORT1_DETECT_CC_ENABLE	If PORTn_MODE in SEMI_AUTO 00 = No Operation 01 = Continuous Detection and Connection Check 10 = Not supported 11 = Continuous Detection, Connection Check and Class Probe If PORTn_MODE in AUTO 00 = No Operation 01 = Not supported 10 = Not supported 11 = Continuous Detection, Connection Check and Class Probe until a PD is detected. When a PD is detected, a Class Power On is initiated, followed by a turning on the port. In effect, it is as though the Si3474 received a PORTn_PB_POWER_ON. If PORTn_MODE in MANUAL Use PB_DETECT_CLASS instead If PORTn_MODE in SHUTDOWN Set up PORTn_PORT_MODE first

PORTn_CLASS_ENABLE and PORTn_DETECT_CC_ENABLE are cleared when the following occur:

1. PORTn_PORT_MODE set to SHUTDOWN.
2. PORTn_PB_POWER_OFF in PB_POWER_ENABLE is set.
3. PORTn_RESET_PORT in PB_RESET is set.
4. OSS_EVENT in SUPPLY_EVENT is set as a result of an emergency shutdown.
5. RESET_QUAD is set.

The DETECT_CLASS_ENABLE register is intended for use when PORTn_PORT_MODE is either in SEMI_AUTO or AUTO only.

If PORTn_PORT_MODE is MANUAL, the corresponding bits in PB_DETECT_CLASS are set; refer to PB_DETECT_CLASS for additional operational description.

If PORTn_PORT_MODE is SHUTDOWN, PORTn_PORT_MODE must be initialized first as this is an invalid operation.

4.15 POWER_PRIORITY_PCUT_DISABLE (0x15)

PORT_PRIORITY_PCUT_DISABLE				Register Address: 0x15 Access Type: Read / Write Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PORT_POWER_PRIORITY				DISABLE_PCUT			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_POWER_PRIORITY	PORTn_PORT_POWER_PRIORITY Defines the Port Power Priority for use when MULTIBIT_PRIORITY_ENABLE = 0. 0 = OSS event does not shut down PORTn. 1 = OSS event shuts down PORTn PORTn_PORT_POWER_PRIORITY is cleared when RESET_QUAD is set. An OSS event occurs when the OSS pin goes high. Every lower priority port experiences a PORTn_PB_POWER_OFF. Refer to PORTn_PB_POWER_OFF for additional details of what registers are cleared,
6	PORT3_POWER_PRIORITY	
5	PORT2_POWER_PRIORITY	
4	PORT1_POWER_PRIORITY	
3	PORT4_DISABLE_PCUT	PORTn_DISABLE_PCUT Defines operation of a port in POWER GOOD state, whether or not to power down PORTn if the PD exceeds port power limits defined in PORTn_POLICE_2P or PORTnm_POLICE_4P. For additional 4P behavior, refer to See also 4.28 ILIM_PCUT_DISCONNECT_4P (0x2D). Overcurrent faults and PD Disconnection will still result in a disconnection. 0 = Normal PCUT Monitoring. 1 = Keep port power even if PD exceeds POLICE register limits Although the port power is not removed, PORTn_PCUT_FAULT_2P or PORTnm_PCUT_FAULT_4P events are reported, leading to an interrupt. The interrupt may be cleared by increasing the related PORTn_POLICE_2P or PORTnm_POLICE_4P registers.
2	PORT3_DISABLE_PCUT	
1	PORT2_DISABLE_PCUT	
0	PORT1_DISABLE_PCUT	

4.16 TIMING_CONFIG (0x16)

TLIM	Register Address: 0x16 Access Type: Read / Write Reset: 0000 0000

7	6	5	4	3	2	1	0
TLIM		TSTART		TOVLD		TMPDO	
PORT1 to PORT4		PORT1 to PORT4		PORT1 to PORT4		PORT1 to PORT4	

Bit	Name	Description
7-6	TLIM	ILIM FAULT Timing Specifies minimum t_{LIM} when PORTn_MAX_ILIM is set. This setting defines the minimum period for which an overcurrent event is tolerated without turning off the port. This setting applies for all ports in the quad. 00 = 60 ms 01 = 15 ms 10 = 10 ms 11 = 6 ms When using the Si3474A-A01 or Si3470B-A01, a FLASH Update is required for TLIM to operate as documented. Contact Skyworks for details.
5-4	TSTART	START FAULT Timing When the port is powering up, if the port is still current limiting after the t_{INRUSH} period, the port is shut off. This setting applies for all ports in the quad 00 = 60 ms 01 = 30 ms 10 = 120 ms 11 = Reserved
3-2	TOVLD	PCUT FAULT Timing A PD drawing power that exceeds the policing power limits for longer than t_{OVLD} will result in the port shut off. This setting applies for all ports in the quad. 00 = 60 ms 01 = 30 ms 10 = 120 ms 11 = 240 ms
1-0	TMPDO	DISCONNECTION Delay Timing A PD drawing too little current for longer than the t_{MPDO} will result in a disconnection. This setting applies to all ports in the quad. 00 = 360 ms 01 = 90 ms 10 = 180 ms 11 = 720 ms

4.17 MISC (0x17)

MISC				Register Address: 0x17 Access Type: Read / Write Reset: 1000 0000			
7	6	5	4	3	2	1	0
INTER-RUPT_PIN_ENABLE	CAP_MEAS_ENABLE	—	MULTI-BIT_PRIORI-TY_ENABLE	CLASS_CHANGE	DE-TECT_CHANGE	—	—

Bit	Name	Description
7	INTERRUPT_PIN_ENABLE	Enables INTb pin output drive. 0 = Enable 1 = Disable
6	CAP_MEAS_ENABLE	Enables Capacitance Measurement on PORTn_DETECT_CAPACITANCE. 0 = Enable 1 = Disable When using the Si3474A-A01 or Si3474B-A01, a FLASH Update is needed for Capacitive Measurement to function as documented. Contact Skyworks for more details.
4	MULTIBIT_PRIORITY_ENABLE	Enables Multibit Port Priority. 0 = Single Bit Port Priority. See also PORTn_PORT_POWER_PRIORITY. 1 = Multibit Port Priority. See also PORTn_MULTIBIT_PRIORITY.
3	CLASS_CHANGE	Defines whether CLASS_DONE events in CLASS_DETECT_STATUS register are set whenever the PORTn_CLASS_STATUS is updated, or only when it changes. 0 = Report CLASS_DONE when CLASS_STATUS is updated. 1 = Report CLASS_DONE when CLASS_STATUS changes.
2	DETECT_CHANGE	Defines whether the DETECT_CC_DONE events in CLASS_DETECT_STATUS register are set whenever the PORTn_DETECTION_STATUS is updated, or only if it changes. 0 = Report DETECT_CC_DONE when DETECTION_STATUS is updated. 1 = Report DETECT_CC_DONE when DETECTION_STATUS changes.

4.18 PB_DETECT_CLASS (0x18)

PB_DETECT_CLASS				Register Address: 0x18 Access Type: Write Only Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESTART_CLASS				RESTART_DETECT			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	PORTn_RESTART_CLASS	PORTn_RESTART_DETECT	Description
7 / 3	PORT4_RESTART_CLASS	PORT4_RESTART_DETECT	PORTn_RESTART_CLASS / PORTn_RESTART_DETECT It is best to view these RESTART_CLASS and RESTART_DETECT together. As a shortcut, RESTART_CLASS will be shown below as the 'left bit', while RESTART_DETECT is shown as the 'right' bit. The intended use case of this register is in MANUAL mode. By definition, MANUAL mode is used for debug only. 00 - No operation 01 - Single Detection and Connection Check 10 - Invalid Setting 11 - Single Detection, Connection Check and Classification without powering the port (e.g., Class Probe).
6 / 2	PORT3_RESTART_CLASS	PORT3_RESTART_DETECT	
5 / 1	PORT2_RESTART_CLASS	PORT2_RESTART_DETECT	
4 / 0	PORT1_RESTART_CLASS	PORT1_RESTART_DETECT	

PB_DETECT_CLASS is intended for use when PORTn_PORT_MODE is MANUAL and is not intended for use in SEMI_AUTO or AUTO.

However, if PB_DETECT_CLASS is used while the PORTn_PORT_MODE is SEMI_AUTO or AUTO, the respective bits are transferred over to the DETECT_CLASS_ENABLE.

4.19 PB_POWER_ENABLE (0x19)

PB_POWER_ENABLE				Register Address: 0x19 Access Type: Write Only Reset: 0000 0000			
7	6	5	4	3	2	1	0
PB_POWER_OFF				PB_POWER_ON			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_PB_POWER_OFF	PORTn_PB_POWER_OFF Initiates Pushbutton OFF. 0 = Do Nothing 1 = Power OFF PORT n
6	PORT3_PB_POWER_OFF	
5	PORT2_PB_POWER_OFF	
4	PORT1_PB_POWER_OFF	
3	PORT4_PB_POWER_ON	PORTn_PB_POWER_ON Initiates Pushbutton ON. 0 = Do Nothing 1 = Power ON PORT n
2	PORT3_PB_POWER_ON	
1	PORT2_PB_POWER_ON	
0	PORT1_PB_POWER_ON	

When a PORTn_PB_POWER_OFF is set, all bits associated with the PORTn being Powered OFF are set to its default reset values, which are mostly cleared with a few exceptions. This list also applies to OSS_EVENT, PORTn_RESET_PORT. This list also applies to OSS_EVENT, PORTn_RESET_PORT and when PORTn_PORT_MODE is set to SHUTDOWN.

- PORTn_POWER_ENABLE
- PORTn_POWER_GOOD
- PORTn_CLASS_DONE
- PORTn_DETECT_CC_DONE
- PORTn_DISCONNECTION
- PORTn_PCUT_FAULT_2P
- PORTnm_PCUT_FAULT_4P
- PORTn_ILIM_FAULT
- PORTn_START_FAULT
- PORTn_CLASS_STATUS
- PORTn_DETECTION_STATUS
- PORTn_CLASS_ENABLE
- PORTn_DETECT_CC_ENABLE
- PORTnm_CONNECTION_CHECK_RESULTS
- PORTn_POWER_ON_FAULT
- PORTnm_ILIM_BEHAVIOR
- PORTnm_PCUT_BEHAVIOR
- PORTnm_DISCONNECT_THRESH
- PORTnm_PCUT_ENABLE
- PORTn_CURRENT
- PORTn_VOLTAGE
- PORTn_PGOOD_FOLDBACK
- PORTn_INRUSH_FOLDBACK
- PORTn_DETECT_RESISTANCE
- PORTn_DETECT_CAPACITANCE
- PORTn_ASSIGNED_CLASS
- PORTn_REQUESTED_CLASS

- PORTn_AUTOCLASS_POWER
- PORTn_POLICE_2P
- PORTnm_POLICE_4P

If the host sets a PORTn_PB_POWER_ON, the PORTn_PORT_MODE is in SEMI_AUTO, it is expected that the PORTnm_PORT_ALLOCATION, PORTn_CLASS_ENABLE, and PORTn_DETECT_CC_ENABLE are already initialized.

Prior Detection, Connection Check and Class Probes that has already started are allowed to complete first. A new Detection, Connection Check and Classification are performed before the FET is finally turned on. If any faults occurred prior to the FET turn on, these are reported as PORTn_POWER_ON_FAULT events.

Once the FET is turned on, the PORTn_POWER_ENABLE is set. There is a short tINRUSH period to allow the PD to charge up their capacitors. After the tINRUSH if the PORTn DRAIN voltage does not settle to under 2V, the port is disconnected and a PORTn_START_FAULT is issued.

On the other hand, if the DRAIN voltage is under 2V, PORTn_POWER_GOOD is issued and the port has reaches POWER_GOOD state.

PORTn_POLICE_2P and PORTnm_POLICE_4P are initialized automatically based on PORTn_ASSIGNED_CLASS these registers are used later to check if the PD is exceeding its power budget. If the PD exceeds the negotiated power thresholds dictated by the various PORTn_PCUT_FAULT_2P, PORTnm_PCUT_FAULT_4P events would occur.

If PORTn_AUTO_AUTOCLASS is set and if the PD is Autoclass-capable, the PORTn_POLICE_2P and PORTnm_POLICE_4P are updated based on PORTn_AUTOCLASS_POWER. At any time after the Si3474 updates the PORTn_POLICE_2P and PORTnm_POLICE_4P registers, the host can choose to manage power by overwriting these police registers. The host can compute actual PD power by monitoring PORTn_CURRENT and PORTn_VOLTAGE and may choose to increase or decrease port power as part of power management.

If the host chooses to decrease police registers, it may choose to also set the PORTn_PCUT_DISABLE so that it can be informed that a PD exceeded the police register thresholds without turning off power to the PD.

In addition, the Si3474 also monitors for disconnections (PORTn_DISCONNECTION), current limit events (PORTn_ILIM_FAULT).

Typically, it is expected that PORTn_PB_POWER_ON to be set with both the PORTn_CLASS_ENABLE and the PORTn_DETECT_CC_ENABLE both set also. However, there is a special use case in MANUAL mode that would allow Detection, Connection Check and Classification to be skipped. If the host sets PORTn_PB_POWER_ON with the PORTn_PORT_MODE is in MANUAL Mode, and if PORTn_CLASS_ENABLE = 0 and PORTn_DETECT_CC_ENABLE = 0, Detection, Connection Check and Classification are all skipped and the port is powered on immediately. The PORTn_POLICE_2P and PORTnm_POLICE_4P are initialized based on PORTnm_POWER_ALLOCATION instead of PORTn_ASSIGNED_CLASS.

4.20 PB_RESET (0x1A)

PB_RESET				Register Address: 0x1A Access Type: Write Only Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLEAR_ALL_INTS	CLEAR_INT_PIN		RESET_QUAD	RESET_PORT			
EIGHT PORTS	NONE		PORT1 to PORT4	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	CLEAR_ALL_INTS	Clears the INTb pin by clearing all events on both Quads. 0 = Do Nothing 1 = Clear all events in all ports (both Quads) and negate INTb
6	CLEAR_INT_PIN	Clears the INTb pin directly in hardware without affecting any event bits. 0 = Do Nothing 1 = Clear INTb pin
4	RESET_QUAD	Registers in the current quad are initialized to Reset defaults. Registers in the other quad are unaffected. 0 = Do Nothing 1 = Reset registers in the Quad to reset defaults
3	PORT4_RESET_PORT	PORTn_RESET_PORT Initiates Port Reset 0 = Do Nothing 1 = Associated PORTn Registers are set to Reset Default values Refer to PORTn_PB_POWER_OFF for a list of registers initialized to Reset Default Values. If the port is powered, it will be shut off.
2	PORT3_RESET_PORT	
1	PORT2_RESET_PORT	
0	PORT1_RESET_PORT	

PORTn_RESET_PORT clears event register similar to that of PORTn_PB_POWER_OFF. If PORTn is powered, the port will be shut off. Refer to PORTn_PB_POWER_OFF for the list of register that are set to Reset default values. The main difference between PORTn_RESET_PORT and PORTn_PB_POWER_OFF is that PORTn_RESET_PORT may be used regardless of what the PORTn_PORT_MODE is.

4.21 VENDOR_ID (0x1B), FIRMWARE_REVISION (0x41), CHIP_REVISION (0x43)

VENDOR_ID				Register Address: 0x1B Access Type: Read Only			
7	6	5	4	3	2	1	0
MANUFACTURER_ID					IC_ID		
0	1	0	0	0	1	0	1

FIRMWARE_REVISION				Register Address: 0x41 Access Type: Read Only			
7	6	5	4	3	2	1	0
MAJOR_REVISION				MINOR_REVISION			
?	?	?	?	?	?	?	?

CHIP_REVISION				Register Address: 0x43 Access Type: Read Only			
7	6	5	4	3	2	1	0
CHIP_REVISION							
?	?	?	?	?	?	?	?

The purpose of MANUFACTURER_ID in the VENDOR_ID register is to allow the host to determine the manufacturer of the device in the presence of a multi-source design. This allows the host to make adjustments to the software to make adjustments to system software due to chip behavior across different vendors. The CHIP_ID effectively defines the product as an Si347x-Class device. Together, the MANUFACTURER_ID and the CHIP_ID is an overall identifier of a class of chips that may be similar to competitive offerings.

The VENDOR_ID is therefore static and does not change across revisions in either hardware or firmware.

The CHIP_REVISION tracks Si3474 hardware revisions.

The FIRMWARE_REVISION tracks firmware revisions. The upper nibble is a "major" revision, while the lower nibble is a "minor" revision.

Ordering Part Number	Chip Revision
Si3474A-A01-IM	0x01
Si3474B-A01-IM	0x00

4.22 AUTOCLASS_CONNECTION_CHECK (0x1C)

AUTOCLASS_CONNECTION_CHECK				Register Address: 0x1C Access Type: Read / Write Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AUTOCLASS_DETECTED				CONNECTION_CHECK_RESULTS			
PORT4	PORT3	PORT2	PORT1	PORT34		PORT12	

Bit	Name	Description
7	PORT4_AUTOCLASS_DETECTED	PORTn_AUTOCLASS_DETECTED Indicates that the PD is Autoclass-capable and that the classification occurred on PORTn of a 4P Port 0 = PD not Autoclass-capable 1 = PD is Autoclass-capable
6	PORT3_AUTOCLASS_DETECTED	
5	PORT2_AUTOCLASS_DETECTED	
4	PORT1_AUTOCLASS_DETECTED	
3	PORT34_CONNECTION_CHECK_RESULTS	PORTnm_CONNECTION_CHECK_RESULTS PORTnm Connection Check Results 00 = UNKNOWN 01 = Single Signature 10 = Dual Signature 11 = Invalid Available when PORTn_DETECT_CC_DONE event is set. But since there is no interrupt for this, PORTn_CLASS_DONE can be used instead
2		
1	PORT12_CONNECTION_CHECK_RESULTS	
0		

The AUTOCLASS_CONNECTION_CHECK is set to Reset default values when these occur:

1. PORTn_PORT_MODE = SHUTDOWN
2. PORTn_PB_POWER_OFF = 1
3. PORTn_RESET_PORT = 1
4. OSS_EVENT
5. RESET_QUAD = 1

4.23 PORT1_POLICE_2P to PORT4_POLICE_2P, PORT12_POLICE_4P, PORT34_POLICE_4P (0x1E – 0x21, 0x2A, 0x2B)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_POLICE_2P	0x1E	R/W	1111 1111	PORTn_POLICE_2P Minimum 2P PCUT Threshold (Watts) = PORTn_POLICE_2P * 0.5 W							
PORT2_POLICE_2P	0x1F	R/W	1111 1111								
PORT3_POLICE_2P	0x20	R/W	1111 1111								
PORT4_POLICE_2P	0x21	R/W	1111 1111								
PORT12_POLICE_4P	0x2A	R/W	1111 1111	PORTnm_POLICE_4P Minimum 4P PCUT Threshold (Watts) = PORTnm_POLICE_4P * 0.5 W							
PORT34_POLICE_4P	0x2B	R/W	1111 1111								

PORTn_POLICE_2P and PORTnm_POLICE_4P are registers that are initialized by the Si3474 as part of PORTn_PB_POWER_ON. The PORTnm_POWER_ALLOCATION, in conjunction with the PD Requested Class will negotiate to an ASSIGNED_CLASS. The PCUT thresholds are then set by the Si3474.

For 4PP Ports, the PCUT thresholds are evaluated for individual 2P Ports against the PORTn_POLICE_2P thresholds, then the power from the two 2P ports are then added and evaluated against the PORTnm_POLICE_4P thresholds.

Any of these police registers can be adjusted based on the actual power used by the port. Once the port has achieved a POWER_GOOD state, the police registers can be written and the Si3474 will then evaluate power thresholds as set by these police registers.

It is important to note that the power values represented in the police register interfaces are MINIMUM threshold. The actual internal thresholds are increased by 5%.

PORTn_POLICE_2P are set to Reset Default Values when:

1. Setting PORTn_PORT_MODE = SHUTDOWN
2. Setting PORTn_PB_POWER_OFF
3. Setting PORTn_RESET_PORT
4. Setting RESET_QUAD
5. OSS Event

4.24 PORT_REMAP (0x26)

PORT_REMAP				Register Address: 0x26 Access Type: Read / Write Reset: 11 10 01 00			
7	6	5	4	3	2	1	0
REMAP		REMAP		REMAP		REMAP	
PORT4		PORT3		PORT2		PORT1	

Bit	Name	Description
7-6	PORT4_REMAP	PORTn_REMAP PORTn_REMAP defines the physical pins used when referencing the logical concept called "PORTn" 00 = Use physical pins GATE1, DRAIN1, SENSE1 01 = Use physical pins GATE2, DRAIN2, SENSE2 10 = Use physical pins GATE3, DRAIN3, SENSE3 11 = Use physical pins GATE4, DRAIN4, SENSE4 PORTnm_2P4P_MODE must be written, using a single write, immediately after reset along with PORTnm_2P4P_MODE in POWER_ALLOCATION. For example, the concept called "PORT4", by default, uses DRAIN4. The PORT4_REMAP field is therefore ‘11’.
5-4	PORT3_REMAP	
3-2	PORT2_REMAP	
1-0	PORT1_REMAP	

The port remapping feature allows the host to rearrange the sequencing of the Si3474 ports so that it better aligns to the end product’s port alignment.

There are some restrictions to be aware of:

1. A Physical Port must appear, and may only appear in one Logical Port.
2. If two 2P Ports form a 4P Port, the two 2P Ports must both be listed on the same PORT_REMAP Nibble (e.g., both on upper nibble or both on lower nibble).

Figure 4.1 RJ45 Example Layouts on page 59 shows a graphic illustration of how to create a logical-to-physical mapping by first starting with a sketch of where the DRAIN pins would line up to where your RJ45 jacks would be.

If the same physical pin code is assigned to more than one PORTn_REMAP field, the Si3474 rejects the setting. It is best to confirm if the Si3474 accepted the remap setting by reading back PORT_REMAP register.

The PORT_REMAP register is one of two registers that must be written once immediately after reset. Even if the intention is to use the default PORT_REMAP, PORT_REMAP must be written with 0xE4. Without this, the Si3474 will not function.

Once PORT_REMAP is written, ONLY a hardware reset can be used to allow PORT_REMAP to be written again.

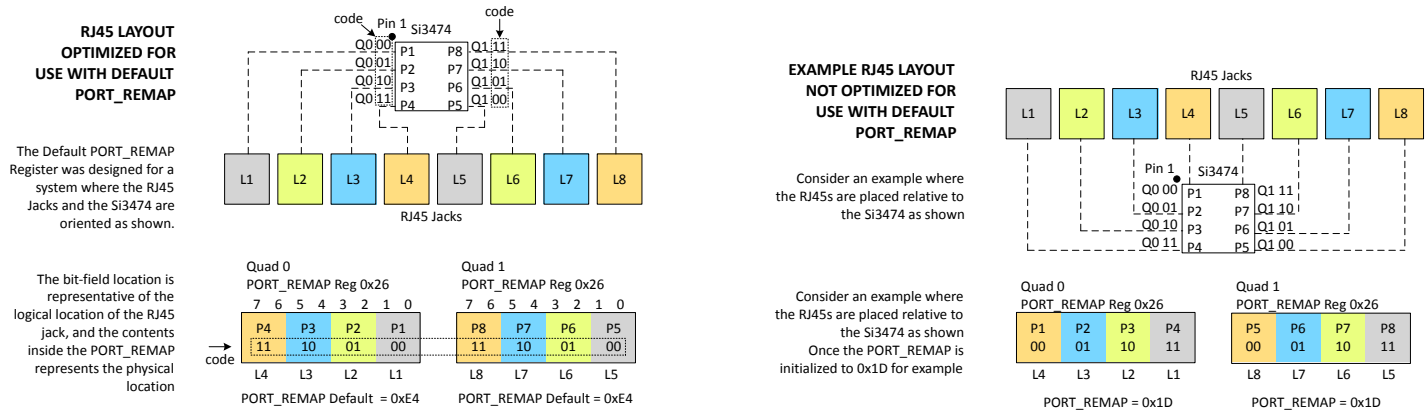


Figure 4.1. RJ45 Example Layouts

4.25 PORTn_MULTIBIT_PRIORITY (0x27, 0x28)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_PORT2_MULTIBIT_PRIORITY	0x27	R/W	0000 0000	PORT2_MULTIBIT_PRIORITY				PORT1_MULTIBIT_PRIORITY			
PORT3_PORT4_MULTIBIT_PRIORITY	0x28	R/W	0000 0000	PORT4_MULTIBIT_PRIORITY				PORT3_MULTIBIT_PRIORITY			

Address	Bit	Name	Description
0x27	6-4	PORT2_MULTIBIT_PRIORITY	PORTn_MULTIBIT_PRIORITY MULTIBIT_PRIORITY_ENABLE in MISC register must be set for PORTn_MULTIBIT_PRIORITY to take effect PORTn_MULTIBIT_PRIORITY defines the OSS Code needed to turn PORTn off. 111 = Receiving OSS Code 111 or lower shuts down PORTn (lowest priority). 110 = Receiving OSS Code 110 or lower shuts down PORTn. 101 = Receiving OSS Code 101 or lower shuts down PORTn. 100 = Receiving OSS Code 100 or lower shuts down PORTn. 011 = Receiving OSS Code 011 or lower shuts down PORTn. 010 = Receiving OSS Code 010 or lower shuts down PORTn. 001 = Receiving OSS Code 001 or lower shuts down PORTn. 000 = Receiving OSS Code 000 shuts down the port (highest priority). Note that the higher the PORTn_MULTIBIT_PRIORITY setting, the more OSS Codes that can shut it down. As such, the lower the PORTn_MULTIBIT_PRIORITY is, the higher the priority of the port.
0x27	2-0	PORT1_MULTIBIT_PRIORITY	
0x28	6-4	PORT4_MULTIBIT_PRIORITY	
0x28	2-0	PORT3_MULTIBIT_PRIORITY	

If MULTIBIT_PRIORITY_ENABLE = 1, then PORT1_PORT2_MULTIBIT_PRIORITY and PORT3_PORT4_MULTIBIT_PRIORITY defines port power priority and governs OSS action. See 2.7.3 Class Power On for figures showing the operation and timing diagram of the OSS pin in multi-bit mode. The most significant bit is sent first. The priority for PORTn is defined by a 3-bit specified by PORTn_MULTIBIT_PRIORITY. A port whose priority setting is ‘000’ has the highest priority; priority setting of ‘111’ has the lowest priority. When the host system wants certain priority ports be shut down, it will transmit the “shutdown code” over the OSS pin Ports whose port priority settings are greater than or equal to the received shutdown code will be turned off For example, a received OSS shutdown code of ‘101’ will shut down ports whose port priority settings are ‘101’, ‘110’ or ‘111’

4.26 POWER_ALLOCATION (0x29)

POWER _ALLOCATION				Register Address: 0x29 Access Type: Read / Write Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
2P4P_MODE	POWER_ALLOCATION			2P4P_MODE	POWER_ALLOCATION		
PORT34				PORT12			

Bit	Name	Description
7	PORT34_2P4P_MODE	PORTnm_2P4P_MODE Assigns whether if PORTn and PORTm should be treated as separate 2P Ports, or should be combined into a single PORTnm 4PP 0 = PORTn and PORTm are separate 2P Ports 1 = PORTn and PORTm combine as PORTnm 4PP PORTnm_2P4P_MODE must be initialized immediately after reset, using a single write, along with PORTn_REMAP
3	PORT12_2P4P_MODE	
6-4	PORT34_POWER_ALLOCATION	PORTnm_POWER_ALLOCATION
2-0	PORT12_POWER_ALLOCATION	

PORTnm_2P4P_MODE	PORTnm_POWER_ALLOCATION			4PP Port Single Signature	4PP Port Dual Signature	2PP Port
	Bit 2	Bit 1	Bit 0			
0	0	0	0			15 W Class 3 + 15 W Class 3
0	0	1	1			30 W Class 4 + 30 W Class 4
0	1	X	X			
1	0	0	0	15 W Class 3	7 W Class 2 + 7 W Class 2	
1	0	0	1			
1	0	1	0			
1	0	1	1	30 W Class 4	15 W Class 3 + 15 W Class 3	
1	1	0	0	45 W Class 5	30 W Class 4 + 15 W Class 3	
1	1	0	1	60 W Class 6	30 W Class 4 + 30 W Class 4	
1	1	1	0	75 W Class 7	45 W Class 5 + 30 W Class 4	
1	1	1	1	90 W Class 8	45 W Class 5 + 45 W Class 5	

4.27 TEMPERATURE (0x2C)

TEMPERATURE				Register Address: 0x2C Access Type: Read Only Reset: ???? ????			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEMPERATURE							
Approximate Chip Temperature in Centigrade is (TEMPERATURE * 0.652) – 20							

4.28 ILIM_PCUT_DISCONNECT_4P (0x2D)

ILIM_PCUT_DISCONNECT_4P							
Register Address: 0x2D Access Type: Read/Write* *The upper nibble of this register is read/write while the lower nibble is read-only. Reset: 00 00 11 00							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ILIM_BEHAVIOR		PCUT_BEHAVIOR		PCUT_ENABLE		DISCONNECT_THRESH	
PORT34	PORT12	PORT34	PORT12	PORT34	PORT12	PORT34	PORT12

Bit	Name	Description
7	PORT34_ILIM_BEHAVIOR	PORTnm_ILIM_BEHAVIOR Defines 4PP ILIM Behavior when an ILIM fault occurs on one of the 2PP ports 0 = Only the faulting port is turned off 1 = Both ports are turned off
6	PORT12_ILIM_BEHAVIOR	
5	PORT34_PCUT_BEHAVIOR	PORTnm_PCUT_BEHAVIOR Defines 4PP ILIM Behavior when a PCUT fault occurs on one of the 2PP ports 0 = Only the faulting port is turned off 1 = Both ports are turned off
4	PORT12_PCUT_BEHAVIOR	
3	PORT34_PCUT_ENABLE	PORTnm_PCUT_ENABLE Defines 4PP PCUT Enable 0 = 4PP PCUT is disabled 1 = 4PP PCUT is enabled
2	PORT12_PCUT_ENABLE	
1	PORT34_DISCON-NECT_THRESH	PORTnm_DISCONNECT_THRESH Status of which 4PP Disconnection Threshold the Si3474 chose 0 = Si3474 chose disconnection threshold for SS Class 0-4 1 = Si3474 chose disconnection threshold for SS Class 5-8
0	PORT12_DISCON-NECT_THRESH	

ILIM_PCUT_DISCONNECT_4P is initialized to Reset default behavior when the following occurs:

1. PORTn_PORT_MODE = SHUTDOWN
2. PORTn_PB_POWER_OFF = 1
3. PORTn_RESET_PORT = 1
4. OSS_EVENT
5. RESET_QUAD = 1

4.29 Parametric Measurement Registers (0x2E – 0x3F)

VPWR, PORTn_VOLTAGE and PORTn_CURRENT are each 14-bit registers straddled across two bytes.

The host must use an SMBus Burst Read of 16-bits so for proper the proper LSB / MSB pairing. An improper LSB / MSB pairing will result in a 256 code error if the measurement happens to be near a multiple of 256.

All of the 16-bit registers begin at an even byte. The SMBus Burst Read should therefore have an even Register Address. The first byte returned from the SMBus Read would be the LSB, followed by the MSB.

VPWR can be read at any time.

PORTn_VOLTAGE and PORTn_CURRENT can be read as long as the port is in POWER_GOOD state. PORTn_VOLTAGE and PORTn_CURRENT are cleared when the following occurs:

1. PORTn_PORT_MODE = SHUTDOWN
2. PORTn_PB_POWER_OFF = 1
3. PORTn_RESET_PORT = 1
4. OSS_EVENT
5. RESET_QUAD = 1

4.30 VPWR, PORT1_VOLTAGE, PORT2_VOLTAGE, PORT3_VOLTAGE, PORT4_VOLTAGE (0x2E/0x2F, 0x32/0x33, 0x36/0x37, 0x3A/0x3B, 0x3E/0x3F)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
VPWR_LSB	0x2E	RO	???? ????	VPWR Voltage (in volts) = 60 * ((VPWR_MSB << 8) + VPWR_LSB) / 16384							
VPWR_MSB	0x2F	RO	00?? ????								
PORT1_VOLTAGE_LSB	0x32	RO	0000 0000	PORTn Voltage (in volts) = 60 * ((PORTn_VOLTAGE_MSB << 8) + PORTn_VOLTAGE_LSB) / 16384							
PORT1_VOLTAGE_MSB	0x33	RO	0000 0000								
PORT2_VOLTAGE_LSB	0x36	RO	0000 0000								
PORT2_VOLTAGE_MSB	0x37	RO	0000 0000								
PORT3_VOLTAGE_LSB	0x3A	RO	0000 0000								
PORT3_VOLTAGE_MSB	0x3B	RO	0000 0000								
PORT4_VOLTAGE_LSB	0x3E	RO	0000 0000								
PORT4_VOLTAGE_MSB	0x3F	RO	0000 0000								

4.31 PORT1_CURRENT, PORT2_CURRENT, PORT3_CURRENT, PORT4_CURRENT (0x30/0x31, 0x34/0x35, 0x38/0x39, 0x3C/0x3D)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_CURRENT_LSB	0x30	RO	0000 0000	PORTn Current (in mA) = 1000 * ((PORTn_CURRENT_MSB << 8) + PORTn_CURRENT_LSB) / 16384							
PORT1_ CURRENT _MSB	0x31	RO	0000 0000								
PORT2_ CURRENT _LSB	0x34	RO	0000 0000								
PORT2_ CURRENT _MSB	0x35	RO	0000 0000								
PORT3_ CURRENT _LSB	0x38	RO	0000 0000								
PORT3_ CURRENT _MSB	0x39	RO	0000 0000								
PORT4_ CURRENT _LSB	0x3C	RO	0000 0000								
PORT4_ CURRENT _MSB	0x3D	RO	0000 0000								

4.32 MAX_ILIM_MANUAL_POLICE (0x40)

MAX_ILIM_MANUAL_POLICE				Register Address: 0x40 Access Type: Read / Write Reset: 0000 0000			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX_ILIM				MANUAL_POLICE			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_MAX_ILIM	PORTn_MAX_ILIM Allows increasing of the port's current limit setting to the maximum possible setting allowed by the Si3474 0 = Port Current Limit not yet maximized 1 = Max Port Current Limit When the port is powered up to POWER_GOOD state, the PORTn_MAX_ILIM is set by the device if the highest 1275 mA current limit setting is used. For the ports whose PORTn_MAX_ILIM is zero, the host can set it to 1 to maximize the current limit to 1275 mA. When set, the PORTn_TLIM setting is enforced. The PORTn_PGOOD_FOLDBACK is also used. When using the Si3474A-A01 or Si3474B-A01, a FLASH Update is needed for PORTn_MAX_ILIM to function as documented. Contact Skyworks for more details.
6	PORT3_MAX_ILIM	
5	PORT2_MAX_ILIM	
4	PORT1_MAX_ILIM	
3	PORT4_MANUAL_POLICE	PORTn_MANUAL_POLICE Defines ports for which the police register settings are manually set 0 = The police registers are updated automatically based on PD Assigned Class 1 = The police registers are initialized by the host before PORTn_PB_POWER_ON. The host is responsible for maintaining the police registers
2	PORT3_MANUAL_POLICE	
1	PORT2_MANUAL_POLICE	
0	PORT1_MANUAL_POLICE	

4.33 I2C_WATCHDOG (0x42)

I2C_WATCHDOG	Register Address: 0x42 Access Type: Read / Write Reset: 000 1011 0

7	6	5	4	3	2	1	0
0	0	0	WATCHDOG_DISABLE				WATCHDOG_STATUS

Bit	Name	Description
4-1	WATCHDOG_DISABLE	WATCHDOG_DISABLE Enables the I²C Watchdog 1011 = Disable the I²C Watchdog NOT 1011 = Enable the I²C Watchdog
0	WATCHDOG_STATUS	0 = I²C Watchdog did not occur 1 = I²C Watchdog occurred

The Si3474 implements an I²C transaction watchdog. The I²C transaction watchdog is disabled by default and can be enabled by setting WATCHDOG_DISABLE to any bit pattern except 0xB. When WATCHDOG_DISABLE bit is set, the transaction watchdog will begin a 50 ms timer whenever an I²C Start Bit is detected. If an I²C Stop Bit is not detected within the 50 ms time period, the Si3474 restarts the I²C subsystem and performs an action equivalent to RESET_QUAD. This results in all ports being shut off.

Once the WATCHDOG_STATUS bit is set, it remains set until the host sets it to 0.

The main benefit of enabling the I²C WATCHDOG feature is to allow recovery if an I²C miscommunication results in the Si3474 is in a stuck state, continuously asserting the SDA pin.

Consider this condition as an example of how the Si3474 could end up asserting the SDA continuously:

Let's say that during an SMBUS Read during which the Si3474 is driving SDA to supply data to the host. Let's say that for some reason, the Si3474 somehow misses an SCL clock transition. If this occurs, the Si3474 may be expecting more SCL transitions as it believes that it needs to send more data bits. So, it drives the SDA pin believing that there would be additional SCL clocks. The Si3474 in this case could be driving the SDA low, thereby hanging the I²C Bus. By enabling the I²C WATCHDOG feature, the I²C Bus is unlocked, and all ports are effectively placed in a reset state so that the host has a known starting point to begin again.

Although an I²C fault would lead to powering down ports all ports, it places the Si3474 in a known state, ready for the host to reinitialize and start anew.

4.34 DETECT_RESISTANCE (0x44 – 0x47)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_DETECT_RESISTANCE	0x44	RO	0000 0000	PORTn PD RESISTANCE (in kΩ) = (50/256) * PORTn_DETECT_RESISTANCE Updated when PORTn_DETECT_CC_DONE event is set.							
PORT2_DETECT_RESISTANCE	0x45	RO	0000 0000								
PORT3_DETECT_RESISTANCE	0x46	RO	0000 0000								
PORT4_DETECT_RESISTANCE	0x47	RO	0000 0000								

4.35 DETECT_CAPACITANCE (0x48 – 0x4B)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_DETECT_CAPACITANCE	0x48	RO	0000 0000	PORTn PD Capacitance (in uF) = PORTn_DETECT_CAPACITANCE * 0.05 CAP_MEAS_ENABLE must be set for these registers to be updated. Capacitance Measurement is initiated when the detection result is 'Capacitive'. PORTn_DETECT_CAPACITANCE is ready once PORTn_DETECT_CC_DONE event is set.							
PORT2_DETEC_CAPACITANCE	0x49	RO	0000 0000								
PORT3_DETECT_CAPACITANCE	0x4A	RO	0000 0000								
PORT4_DETECT_CAPACITANCE	0x4B	RO	0000 0000								

When using the Si3474A-A01 or Si3474B-A01, a FLASH Update is needed for this register to function as documented. Contact Skyworks for more details.

4.36 CLASS_RESULTS (0x4C – 0x4F)

Name	Address	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_CLASS_RESULTS	0x4C	RO	0000 0000	ASSIGNED_CLASS				REQUESTED_CLASS			
PORT2_CLASS_RESULTS	0x4D	RO	0000 0000	ASSIGNED_CLASS				REQUESTED_CLASS			
PORT3_CLASS_RESULTS	0x4E	RO	0000 0000	ASSIGNED_CLASS				REQUESTED_CLASS			
PORT4_CLASS_RESULTS	0x4F	RO	0000 0000	ASSIGNED_CLASS				REQUESTED_CLASS			

Address	Bit	Name	Description
0x4C	7 - 4	PORT1_ASSIGNED_CLASS	PORTn_ASSIGNED_CLASS The assigned class represents the result of Class Power On initiated by a PORTn_PB_POWER_ON
0x4D	7 – 4	PORT2_ASSIGNED_CLASS	
0x4E	7 – 4	PORT3_ASSIGNED_CLASS	
0x4F	7 – 4	PORT4_ASSIGNED_CLASS	
0x4C	3 - 0	PORT1_REQUESTED_CLASS	PORTn_REQUESTED_CLASS When a PORTn_PB_POWER_ON is issued, the most recent Class Probe results are stored here. The Class Probe is effectively the requested class.
0x4D	3 - 0	PORT2_REQUESTED_CLASS	
0x4E	3 - 0	PORT3_REQUESTED_CLASS	
0x4F	3 - 0	PORT4_REQUESTED_CLASS	

The following table aims to provide a summary of when to expect values in the various fields that may contain Classification information.

Table 4.2. Classification Event Timing

Classification Code	PORTn_CLASS_STATUS	PORTn_REQUESTED_CLASS	PORTn_ASSIGNED_CLASS	Comments
0000	UNKNOWN	UNKNOWN	UNKNOWN	
0001	Class 1	Class 1	Class 1	
0010	Class 2	Class 2	Class 2	
0011	Class 3	Class 3	Class 3	
0100	Class 4	Class 4	Class 4	
0101				
0110	Class 0	Class 0		If a Class 0 is requested, it is converted to Class 3
0111	Overcurrent			
1000	Class 5 - 4P SS	Class 5 - 4P SS	Class 5 - 4P SS	
1001	Class 6 - 4P SS	Class 6 - 4P SS	Class 6 - 4P SS	
1010	Class 7 - 4P SS	Class 7 - 4P SS	Class 7 - 4P SS	
1011	Class 8 - 4P DS	Class 8 - 4P DS	Class 8 - 4P DS	
1100	Class 4+ Type 1 limited			Requested Class ≥ CLASS_4, demoted to CLASS_3
1101	Class 5 - 4P DS	Class 5 - 4P DS	Class 5 - 4P DS	
1110	—	—	—	
1111	Class mismatch			This is temporary status setting as the classification is repeated

Note:

1. Red Text: Possible if unsuccessful Class Power On (PORTn_POWER_ON_FAULT in POWER_ON_FAULT register).
2. Green Text: Updated during Class Probe (PORTn_CLASS_DONE in CLASS_DETECT_STATUS).
3. Blue Text: Updated during Class Power On (PORTn_POWER_GOOD in POWER_STATUS register).
4. All Initialized to UNKNOWN:
   - PORTn_PORT_MODE = SHUTDOWN
   - PORTn_PB_POWER_OFF = 1
   - PORTn_RESET_PORT = 1
   - OSS_EVENT
   - RESET_QUAD = 1

4.37 AUTOCLASS_CONTROL (0x50)

AUTOCLASS_CONTROL				Register Address: 0x50 Access Type: Read / Write Reset: 0000 0000			
7	6	5	4	3	2	1	0
MANUAL_AUTOCLASS				AUTO_AUTOCLASS			
PORT4	PORT3	PORT2	PORT1	PORT4	PORT3	PORT2	PORT1

Bit	Name	Description
7	PORT4_MANUAL_AUTO-CLASS	PORTn_MANUAL_AUTOCLASS Initiate an autoclass measurement. 0 = No Action 1 = Manually initiate an Autoclass power measurement. Once set, PORTn_MANUAL_AUTOCLASS clears itself once the results in PORTn_AUTOCLASS_POWER is ready. It is recommended that the host makes use of this auto-clearing behavior to determine that PORTn_AUTOCLASS_POWER is ready to be read. Once the PORTn_AUTOCLASS_POWER is updated, the host may then add some margin, then update the related PORTn_POLICE_2P and/or PORTnm_POLICE_4P registers.
6	PORT3_MANUAL_AUTO-CLASS	
5	PORT2_MANUAL_AUTO-CLASS	
4	PORT1_MANUAL_AUTO-CLASS	
3	PORT4_AUTO_AUTOCLASS	PORTn_AUTO_AUTOCLASS PORTn_AUTO_AUTOCLASS Enable 0 = Disable AUTO Autoclass 1 = Enables AUTO Autoclass Must be initialized before initiating PORTn_PB_POWER_ON In the presence of an autoclass-capable PD, the related PORTn_POLICE_2P and/or PORTnm_POLICE_4P registers are updated based on some margin in addition to the measurement stored in PORTn_AUTOCLASS_POWER.
2	PORT3_AUTO_AUTOCLASS	
1	PORT2_AUTO_AUTOCLASS	
0	PORT1_AUTO_AUTOCLASS	

PORTn_AUTO_AUTOCLASS must be set prior to a PORTn_PB_POWER_ON.

An Autoclass procedure is performed during the Class Power On that occurs due to a PORTn_PB_POWER_ON. If the Si3474 detects an Autoclass request from a PD, the PORTn_AUTOCLASS_DETECTED is set.

Once the PORT has reached POWER_GOOD, the PD is expected to draw its maximum power during the first few seconds after powering up. The Si3474 automatically measures the PD power and updates the police registers based on the measured power.

In the 802.3bt standard, it is possible to negotiate a manual autoclass procedure between the PSE and PD through Data Link Layer messaging. The host can set the PORTn_MANUAL_AUTOCLASS at the time when the PD is expected to be drawing full power as part of this Data Link Layer Autoclass protocol. Once PORTn_MANUAL_AUTOCLASS is set, the Si3474 performs a power measurement. Once the power measurement is ready, the PORTn_MANUAL_AUTOCLASS is cleared as an indicator to the host that the PORTn_AUTOCLASS_POWER is ready.

In a MANUAL AUTOCLASS measurement is made, the police registers are not updated, and it is the host's responsibility to set up the various police registers based on the PORTn_AUTOCLASS_POWER results.

4.38 PORT1_AUTOCLASS_RESULTS, PORT2_AUTOCLASS_RESULTS, PORT3_AUTOCLASS_RESULTS, PORT4_AUTOCLASS_RESULTS (0x51 – 0x54)

Name	Addr	Access Type	Reset	7	6	5	4	3	2	1	0
PORT1_AUTOCLASS_RESULTS	0x51	RO	0000 0000	0	AUTOCLASS_POWER						
PORT2_AUTOCLASS_RESULTS	0x52	RO	0000 0000	0	AUTOCLASS_POWER						
PORT3_AUTOCLASS_RESULTS	0x53	RO	0000 0000	0	AUTOCLASS_POWER						
PORT4_AUTOCLASS_RESULTS	0x54	RO	0000 0000	0	AUTOCLASS_POWER						

Addr	Bit	Name	Description
0x51	6 - 0	PORT1_AUTOCLASS_POWER	PORTn_AUTOCLASS_POWER Holds the AUTOCLASS_POWER information Power (in Watts) = PORTn_AUTOCLASS_POWER * 0.5
0x52	6 - 0	PORT2_AUTOCLASS_POWER	
0x53	6 - 0	PORT3_AUTOCLASS_POWER	
0x54	6 - 0	PORT4_AUTOCLASS_POWER	

4.39 ALTERNATIVE_FOLDBACK (0x55)

ALTERNATIVE_FOLDBACK

Register Address: 0x50

Access Type: Read / Write

Reset: 0000 0000

7	6	5	4	3	2	1	0
PGOOD_FOLDBACK				—			
PORT4	PORT3	PORT2	PORT1				

Bit	Name	Description
7	PORT4_PGOOD_FOLDBACK	PORTn_PGOOD_FOLDBACK When PORTn is in POWER_GOOD state and the PD momentarily increases its current draw, setting this bit decreases the level at which the PORTn fold-backs the port voltage so the current can be supplied at a higher port voltage, thereby increasing the maximum power delivery to the PD 0 = Normal Voltage Foldback for port in POWER_GOOD state 1 = Decrease level of Port Voltage Foldback
6	PORT3_PGOOD_FOLDBACK	
5	PORT2_PGOOD_FOLDBACK	
4	PORT1_PGOOD_FOLDBACK	

4.40 FLASH REGISTERS (0x5F – 0x63)

Refer to 2.13.1 Updating Si3474 Flash for information on the use of these registers.

5. Electrical Characteristics Si3474

Table 5.1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
VPWR Input Supply Voltage	V_{PWR}	IEEE Type 3 when port is ON	50	—	57	V
		IEEE Type 4 when port is ON	52	—	57	V
VPWR Slew Rate	$V_{PWRSLEW}$		—	—	1	V/µs
VDD Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Operating Ambient Temperature[2]	T_{AMB}		–40	—	85	°C

Note:

1. All specification voltages are referenced with respect to DGND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise.
2. The Si3474 includes internal thermal shutdown above 125 °C.

Table 5.2. Electrical Specifications

These specifications apply over the recommended operating voltage and temperature ranges of the device specified in Table 5.1 Recommended Operating Conditions[1] on page 70 unless otherwise noted. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and VPWR at 54 V. V_{PORTn}, V_{CLASS}, and V_{MARK} voltages are referenced with respect to V_{DRAIN}. All other voltages are referenced with respect to GND.

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Power Supply Voltages						
VPWR Under Voltage Lock Out	V_{PWR_UVLO}	Level below which chip is not operational	25	31	34	V
VPWR UVLO Input Voltage (to turn on)	V_{UVLO_ON}		25	28	—	V
VPWR UVLO Input Voltage (to turn off)	V_{UVLO_OFF}		—	31	34	V
VDD UVLO Warning Voltage	$V_{DD\_UVLO\_WARN}$	Digital interface still responds, but VDD_UVLO bit will be set as an indication of an imminent problem.	2.6	2.8	3.0	V
VDD UVLO Failure Voltage	$V_{DD\_UVLO\_FAIL}$	Level below which digital parts of the chip will not respond	2.1	2.25	2.4	V
Hardware Reset Voltage	V_{RESET}	V_{DD} voltage causing reset	—	1.8	—	V
Power Supply Currents[1]						
VPWR Supply Current	I_{VPWR}	During normal operation	—	2	5	mA
		V_{PWR} = 8 V, V_{DD} = 0 V	—	—	100	µA
VDD Supply Current	I_{DD}	During normal operation	—	17	25	mA
MOSFET Fault Specifications						
MOSFET Fault Threshold	V_{PORT}	When FET is driven OFF, if either condition is met, a MOSFET fault is reported.	—	15	—	V
	I_{FET}		—	2.5	—	mA

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Detection Specifications						
Detection Short Circuit Current	I_{DET_SC}	Measured when Vdrain is shorted to V_{PWR}	—	3.0	4.9	mA
Detection voltage when RDET = 25.5 kΩ	V_{PORTn}	Primary detection voltage	2.8	4.0	—	V
		Secondary detection voltage	—	8.0	10.0	V
Signature Resistance	R_{GOOD}		—	25	—	kΩ
Minimum Signature Resistance @ PD	R_{DET_MIN}		15	17	19	kΩ
Maximum Signature Resistance @ PD	R_{DET_MAX}		26.5	30	33	kΩ
Reject Signature Capacitance	C_{REJECT}		—	—	10	µF
Open Port Threshold	R_{OPEN_PORT}	Threshold between R_HIGH and R_OPEN	100	—	400	kΩ
Shorted Port Threshold	R_{SHORT}		150	—	400	Ω
High Detection Signature Resistance	R_{HIGH}		33	—	100	kΩ
Low Detection Signature Resistance	R_{LOW}		0.4	—	15	kΩ
Classification Specifications						
Class Event Voltage	V_{CLASS}	0 mA < I_{CLASS} < 51 mA	15.5	—	20.5	V
Classification Short Circuit Current	I_{CLASS_SC}	Measured when Vdrain is shorted to V_{PWR}	55	—	95	mA
Classification Current Region	I_{CLASS_REGION}	Class Signature 0	0	—	5	mA
		Threshold between Class Signature 0 or 1	5	—	8	mA
		Class Signature 1	8	—	13	mA
		Threshold between Class Signature 1 or 2	13	—	16	mA
		Class Signature 2	16	—	21	mA
		Threshold between Class Signature 2 or 3	21	—	25	mA
		Class Signature 3	25	—	31	mA
		Threshold between Class Signature 3 or 4	31	—	35	mA
		Class Signature 4	35	—	45	mA
		Threshold between Class Signature 4 or invalid class	45	—	51	mA
Classification Mark Specifications						
Mark Event Voltage	V_{MARK}	Mark current between 0 and 5 mA	7	—	10	V
Mark Event Current Limitation	I_{MARK_LIM}		5	—	100	mA
Output Voltage						
Threshold Voltage for Power Good Sense	V_{PGOOD}	Measured at V_{DRAINn} to AGND	1	2	3	V
Bias Current of DRAINn Pin	I_{DRAINn}	V_{DRAINn} = 0 V	—	–25	—	µA

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Current Limit Detection Threshold	V_{DRAIN_ILIM}	Measured at V_{DRAIN} with respect to AGND	—	—	3.00	V
Resistance from DRAIN to AGND	R_{DRAIN}		—	2.5	—	MΩ
Current Sense[2]						
Power Limit	P_{CUT}	Class 0, 2-pair power, 15.4 W nominal	—	16.275	—	W
		Class 1, 2-pair power, 4 W nominal	—	4.2	—	W
		Class 2, 2-pair power, 7 W nominal	—	7.35	—	W
		Class 3, 2-pair power, 15.4 W nominal	—	16.275	—	W
		Class 4, 2 or 4-pair power[3], 30 W nominal[4]	—	31.5	—	W
		Class 5, dual signature, 2 pair power, 45 W nominal[5]	—	47.25	—	W
		Class 5, single signature, 4 pair power[3], 45 W nominal	—	47.25	—	W
		Class 6, 4-pair power[3], 60 W nominal	—	63	—	W
		Class 7, 4-pair power[3], 75 W nominal	—	78.75	—	W
		Class 8, 4-pair power[3], 90 W nominal	—	94.5	—	W
PCUT Tolerance	P_{CUT}	Policy settings < 15 W	0	5	10	%
		Policy settings ≥ 15 W	0	2.5	5	%
Current Limit[6]	I_{LIM}	Inrush, all assigned PD classes, Vport > 30 V	400	425	450	mA
		Power-on, assigned PD Class 0, 1, 2, 3, 4+ Type 1 limited	—	425	—	mA
		Power-on, assigned PD Class 4, 5, 6 [7]	—	850	—	mA
		Power-on, assigned PD Class 7, 8 [7]	—	1275	—	mA
		Power-on, assigned dual-signature PD Class 1, 2, 3	—	425	—	mA
		Power-on, assigned dual-signature PD Class 4	—	850	—	mA
		Power-on, assigned dual-signature PD Class 5	—	1275	—	mA
Disconnect with power provided over two pairs[8]	$I_{PORT\_DIS\_2P}$	Current per pairset	—	6.5	—	mA
Disconnect with power provided over four pairs[8]	$I_{PORT\_DIS\_4P}$	Current per pairset. While powering over four pairs, if either pairset current is above this threshold, the PD is considered to be presenting the MPS signal.	—	3.5	—	mA
MOSFET Gate Drive[9]						
Drive Current from GATEn Pin (Active)		GATEn pin active V_{GATEn} = AGND	–70	–50	–20	µA
Drive Current from GATEn Pin (Off)		GATEn pin shut off V_{GATEn} = AGND+ 5 V	—	50	—	mA

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Voltage Difference Between any GATEn and AGND Pin		I_{GATEn} = –1 µA	10	11.5	13	V

Note:

1. Positive values indicate currents flowing into the device. Negative currents indicate current flowing out of the device.
2. Current sense resistor, R_{SENSE}, has a value of 0.255 Ω.
3. P_{CUT} is within 802.3bt specified unbalance limits.
4. Class 4 can be powered over either 4-pair or 2-pair power. When powered over 4-pair, the total current across both alternatives is used for P_{CUT} measurements, when powered over a single pair PCUT is taken from the lone alternative.
5. Class 5 dual signature is on a per-alternative basis. The summed P_{CUT} of both alternatives are held to Class 8 Single Signature power levels.
6. Setting applies to each active alternative.
7. When powered in 4-pair mode, the ILIM value applies to each alternative; so, the total ILIM for the load is effectively doubled.
8. An MPS signal is considered present on an alternative when the current on that alternative is above these thresholds.
9. See "AN1228: FET Selection Guide for Si347x PSE Families" for detailed information on FET selection.

Table 5.3. I²C Bus Timing Specifications[1, 2, 3, 4]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Serial Bus Clock Frequency	f_{SCL}	See Figure 5.1 I²C Bus Interface Timing on page 74.	0	—	800	kHz
SCL High Time	t_{SKH}	See Figure 5.1 I²C Bus Interface Timing on page 74.	300	—	—	ns
SCL Low Time	t_{SKL}	See Figure 5.1 I²C Bus Interface Timing on page 74.	650	—	—	ns
Bus Free Time	t_{BUF}	Between STOP and START conditions. See Figure 5.1 I²C Bus Interface Timing on page 74.	650	—	—	ns
Start Hold Time	t_{STH}	Between START and first low SCL. See Figure 5.1 I²C Bus Interface Timing on page 74.	300	—	—	ns
Repeated Start Setup Time	t_{STS}	Between SCL high and START condition. See Figure 5.1 I²C Bus Interface Timing on page 74.	300	—	—	ns
Stop Setup Time	t_{SPS}	Between SCL high and STOP condition. See Figure 5.1 I²C Bus Interface Timing on page 74.	300	—	—	ns
Data Hold Time	t_{DH}	See Figure 5.1 I²C Bus Interface Timing on page 74.	75	—	—	ns
Data Setup Time	t_{DS}	See Figure 5.1 I²C Bus Interface Timing on page 74.	100	—	—	ns
Time from Hardware or Software Reset until Start of I²C Traffic	t_{RESET}	Reset to start condition	5	—	—	ms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. All specification voltages are referenced with respect to AGND and DGND at ground.
2. Not production tested (guaranteed by design).
3. All timing references measured at V_{IL} and V_{IH}.
4. SCL and SDA rise and fall times depend on bus pull-up resistance and bus capacitance.

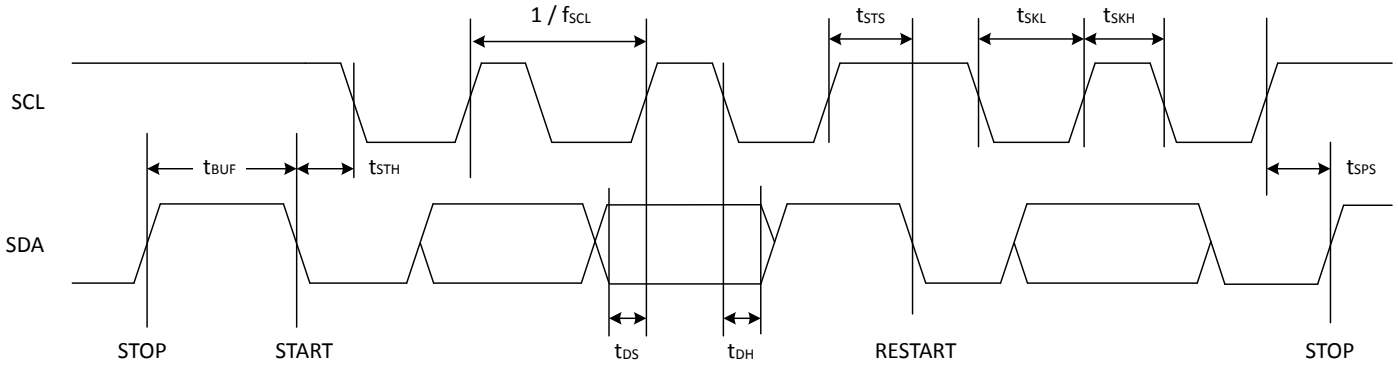


Figure 5.1. I²C Bus Interface Timing

Table 5.4. Digital Pin Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Pins	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		A1-A4, SCL, SDA, RESETb, OSS	—	—	0.3 x VDD	V
Input High Voltage	V_{IH}		A1-A4, SCL, SDA, RESETb, OSS	0.7 x VDD	—	—	V
Output Low Voltage	V_{OL}	IOL = 13.5 mA, VDD > 3.0 IOL = 3.6 mA, 1.71 < VDD < 2.2 V	SDA, INTb			VDD x 0.2	V
Input Leakage	I_{LK}	VDD < Vpin < VDD + 2.5 V	A1-A4, SCL, SDA, RESETb, OSS	0	5	150	µA
Pullup Current to VDD	I_{PU}		RESET, OSS, INT, SCL, SDA, A1–A4	—	–20	—	µA
Pulse Width of spikes which must be suppressed by input filter	t_{SP}		SCL, SDA	0	—	10	ns

Note:

1. All specification voltages are referenced with respect to DGND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise.
2. SDA and INTb are open drain outputs. Tie each pin to VDD with a 1 kΩ resistor for normal operation
3. Note that VIL and VIH are shown as fractions of VDD. This is intended to allow the I²C interface to operate with CMOS levels. These values will be higher than the standard TTL interface.

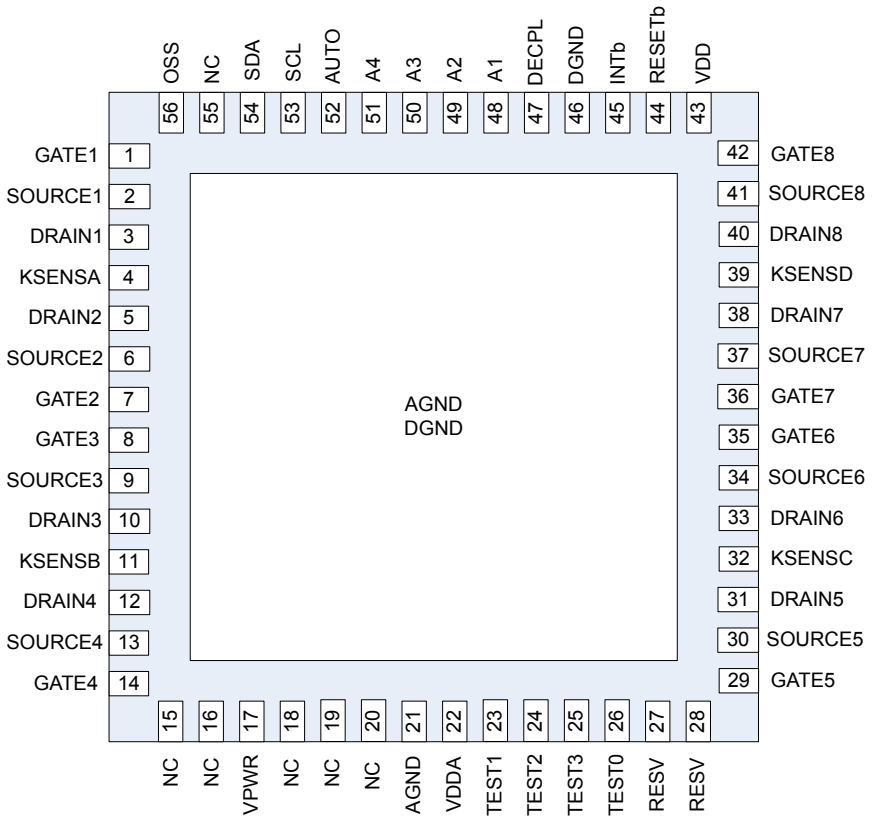
Table 5.5. Absolute Maximum Ratings[1]

Parameter	Range	Unit
Supply Voltage		
VDD	–0.3 to 4.0	V
VPWR	–0.3 to 80.0	V
DGND with Respect to AGND	0	V
Digital Signals		
All	–0.3 to 3.6	V
Analog Signals		
GATEn with Respect to AGND	–0.3 to 20.0	V
SENSEn with Respect to AGND	–0.3 to 3.0	V
DRAINn with Respect to AGND	–3 to 80	V
Temperature		
Junction	+150	°C
Storage	–55 to +150	°C

Note:

1. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.

6. Pin Descriptions



Pin #	Name	Type	Description
44	RESETb	Digital input with 20 µA pull-up to VDD	Active low device reset input. Generally, RESETb is used at initial power up. If RESETb is asserted (pulled to DGND), the MCU is disabled, all internal registers of the device are set to their default (power-up) state, and all output ports are shut off. Valid RESETb timing pulses must be >10 µs. If RESETb is not used, RESETb should either be tied directly to VDD or through a 10 kΩ resistor to VDD.
45	INTb	Digital output (open drain)	Interrupt output. This open drain output pin is asserted low (to DGND) if a fault condition occurs on any of the four ports. The state of INTb is updated for use by the host controller between valid I^2C commands. Refer to the “Interrupts” section of for more information. Tie INTb to VDD through a 10 kΩ resistor for normal operation.
53	SCL	Digital input	Serial clock input. Should be tied directly to the SCL (clock) connection on the I^2C bus.
54	SDA	I^2C input/output	Bidirectional I^2C input/output.
51, 50, 49, 48	A4, A3, A2, A1	Digital input with 20 µA pull-up to VDD	I^2C address input. Used to set the base I^2C address for the Si3474 in the following (binary) format: 010[A4][A3][A2][A1]b. The three MSB bits of the address are set to 010. Address values are latched after the deassertion of RESETB or when VDD ramps and VPWR exceeds the UVLO threshold voltage. Each address pin should be tied to either VDD or DGND.
46, ePAD	DGND	Digital ground	Ground connection for 3.3 V digital supply (VDD). DGND and AGND are tied together inside the Si3474 package.

Pin #	Name	Type	Description
21, ePAD	AGND	Analog ground	Ground connection for VPWR supply. DGND and AGND are tied together inside the Si3474 package
43	VDD	Digital power	3.3 V digital supply (relative to DGND). Bypass VDD with a 0.1 µF capacitor to DGND as close as possible to the Si3474 power supply pins; tied with VDDA.
22	VDDA	Analog power	3.3 V supply to the analog side; tied with VDD at the PCB level.
17	VPWR	Analog power	Positive PoE voltage (+44 to +56 V) relative to AGND.
41	SENSE8	Analog input	Current sense inputs for external MOSFETs. The SENSEn pin measures current through an external sense resistor tied between the AGND supply rail and the SENSEn input. If the I_{CUT} limit (the overcurrent limit) is exceeded, the current limit fault timer is incremented. If the voltage across the sense resistor subsequently triggers (the overcurrent limit), the voltage driven onto the GATEn pin is modulated to provide constant current through the external MOSFET. Tie the SENSEn pin to AGND when the port is not used. To accommodate 802.3at (PoE Plus) classification, both the I_{CUT} and Ilim values can be scaled. See 4.24 PORT_REMAP (0x26) for more information.
37	SENSE7		
34	SENSE6		
30	SENSE5		
13	SENSE4		
9	SENSE3		
6	SENSE2		
2	SENSE1		
42	GATE8	Analog output	Gate drive outputs to external MOSFETs. Connect the GATEn outputs to the external MOSFET gate node gate. A 50 µA pull-up source is used to turn on the external MOSFET. When a current limit is detected, the GATEn voltage is reduced to maintain constant current through the external MOSFET. If the fault timer limit is reached, GATEn pulls down, shutting off the external MOSFET. GATEn will clamp to 11.5 V (typical) above AGND. If the port is unused, leave the GATEn pin disconnected or tie to AGND.
36	GATE7		
35	GATE6		
29	GATE5		
14	GATE4		
8	GATE3		
7	GATE2		
1	GATE1		
40	DRAIN8	Analog input with 25 µA pull-up to VPWR	MOSFET drain output voltage sense. The Power Good bit is set on each port when the voltage between DRAINn and AGND drops below 2 V (typical). See 4.4 POWER Event and POWER Event CoR (Address 0x02, 0x03) for further information. DRAINn pins should be left floating if the port is unused.
38	DRAIN7		
33	DRAIN6		
31	DRAIN5		
12	DRAIN4		
10	DRAIN3		
5	DRAIN2		
3	DRAIN1		
56	OSS	Over supply signal	A positive going edge on this pin shuts down ports that have been identified as low priority by setting Register 0x15. This pin has a 20 µA pull-up. Do not leave this pin unconnected.
4	KSENSA	Input	Kelvin points for accurate measurement of voltage across the sense resistor for ports 1 and 2.
11	KSENSB	Input	Kelvin points for accurate measurement of voltage across the sense resistor for ports 3 and 4.
32	KSENSC	Input	Kelvin points for accurate measurement of voltage across the sense resistor for ports 5 and 6.

Pin #	Name	Type	Description
39	KSENSD	Input	Kelvin points for accurate measurement of voltage across the sense resistor for ports 7 and 8.
26	TEST4	Input/Output	Test pin for internal use by Skyworks. Leave floating.
25	TEST3		
24	TEST2		
23	TEST1		
47	DECPL	Decoupling	Place a 0.1 µF capacitor between DECPL and GND.
52	AUTO-MODE	Automode	Enables Automode. Refer to 2.10.1 AUTO Pin Autonomous Mode.
28, 27	RESV	Reserved	Reserved for future use. Leave floating.
19, 18, 16, 15, 55, 20	NC	No Connect	No connections or nets allowed. Leave floating.

7. Package Outline: 56-Pin QFN

The figure below illustrates the package details for the Si3474. The table lists the values for the dimensions shown in the illustration. The Si3474 is packaged in an industry-standard, RoHS-compliant, 56-pin QFN package.

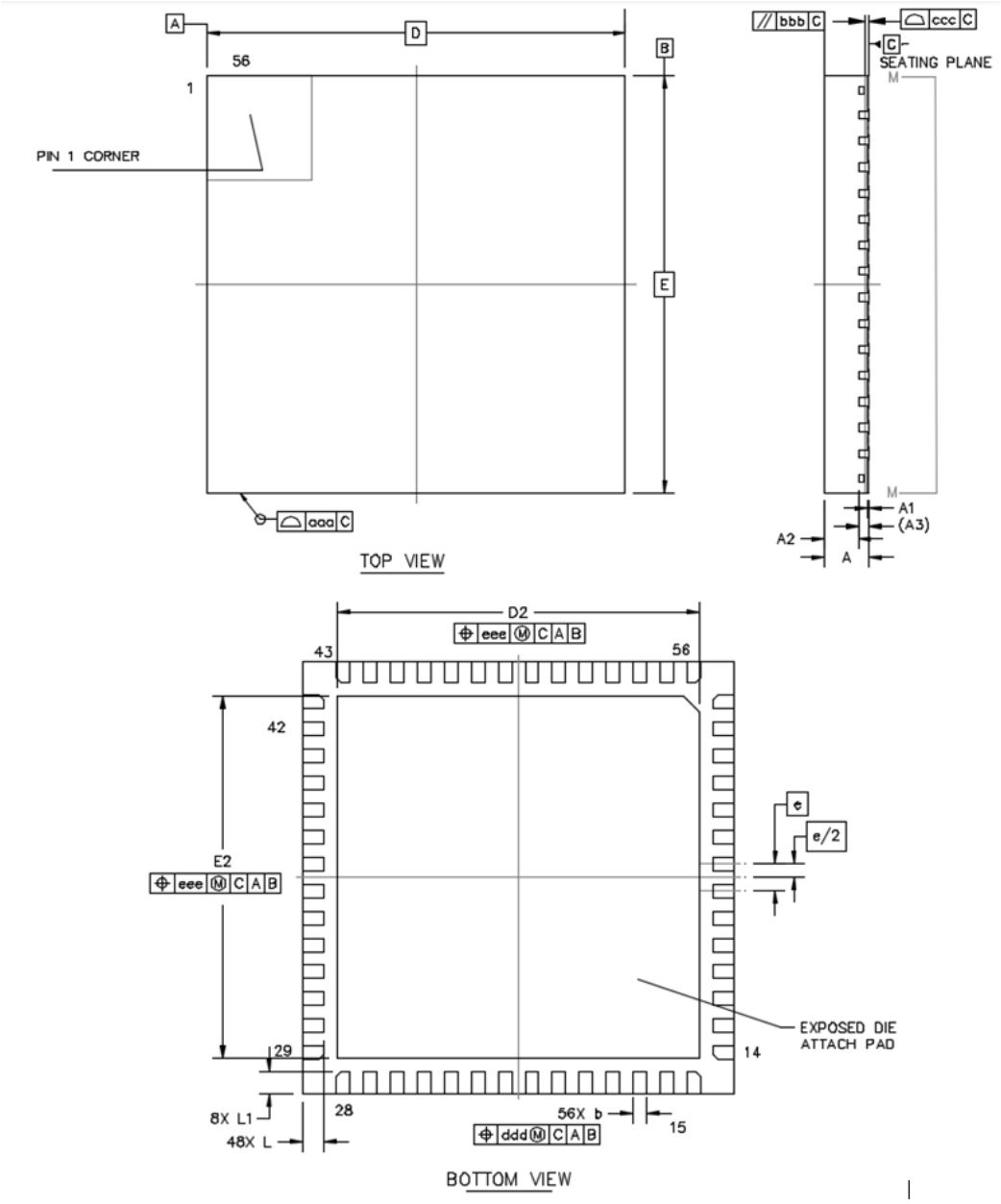


Figure 7.1. 56-Pin QFN Package

Table 7.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	6.60	6.70	6.80
E2	6.60	6.70	6.80
e		0.50 BSC	
L	0.35	0.40	0.45
L1	0.30	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VLLD-5.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Land Pattern

The following figure illustrates the land pattern details for the Si3474. The table lists the values for the dimensions shown in the illustration. The stencil design and notes are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

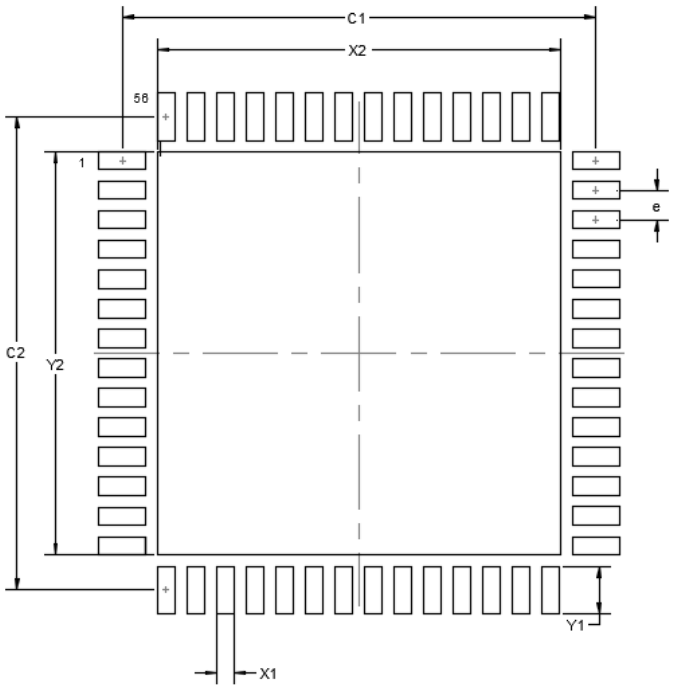


Figure 8.1. Si3474 Recommended Land Pattern

Table 8.1. PCB Land Pattern Dimensions

Symbol	mm
C1	8.00
C2	8.00
e	0.50
X1	0.30
Y1	0.80
X2	6.80
Y2	6.80

Symbol	mm

Notes:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
4. A 3 x 3 array of 1.50 mm square openings on a 2.1 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Marking

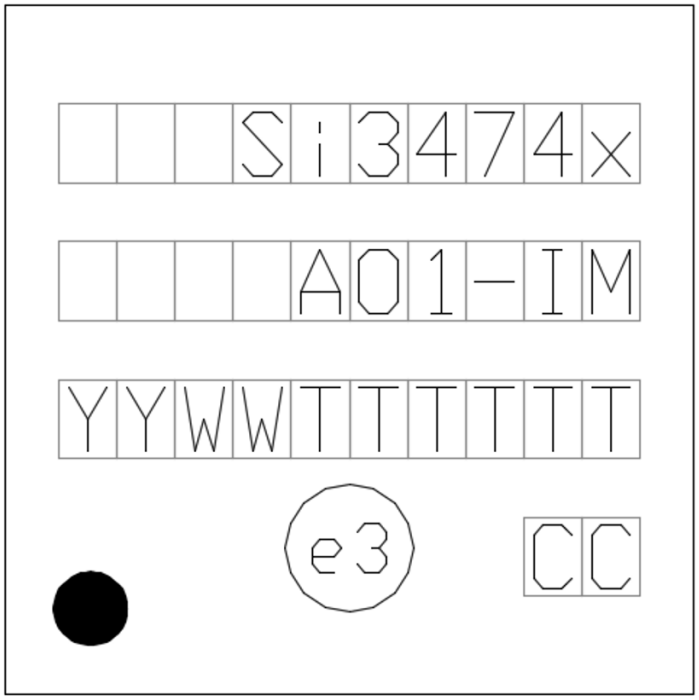


Figure 9.1. Si3474 Top Marking (QFN)

Table 9.1. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Bottom-Left-Justified	
Line 1 Mark Format:	Device Part Number	Si3474x x = A (255 mΩ sense resistor) x = B (200 mΩ sense resistor)
Line 2 Mark Format:	Device Revision Package Type	A01 IM
Line 3 Mark Format:	YY = Year WW = Work Week TTTTTT = Mfg Code	Year and Work Week of Assembly Manufacturing Code
Line 4 Mark Format:	Circle = 1.3 mm Diameter Country of Origin	“e3” Pb-Free Symbol TW = Taiwan

10. Revision History

Revision 0.5

May, 2020

- Initial release.

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