UCC21540-Q1 Reinforced Isolation Dual-Channel Gate Driver

1 Features

- AEC Q100 qualified with:
  - Device temperature grade 1
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C6
- Functional Safety Quality-Managed
  - Documentation available to aid functional safety system design
- Junction temperature range –40°C to 150°C
- Up to 18-V VDD output drive supply
  - 5-V and 8-V VDD UVLO Options
- CMTI greater than 100 V/ns
- Switching parameters:
  - 40-ns maximum propagation delay
  - 5-ns maximum delay matching
  - 5.5-ns maximum pulse-width distortion
  - 35-µs maximum VDD power-up delay
- Safety-related certifications:
  - 8000-V_{PK} reinforced isolation per DIN V VDE V 0884-11:2017-01
  - 5700-V_{RMS} isolation for 1 minute per UL 1577
  - CQC certification per GB4943.1-2011

2 Applications

- HEV and EV battery chargers
- Isolated converters in AC-to-DC and DC-to-DC power supplies
- Motor drives and inverters
- Uninterruptible power supply (UPS)

3 Description

The UCC21540-Q1 device is an isolated dual channel gate driver with programmable dead time and wide temperature range. This device exhibits consistent performance and robustness under extreme temperature conditions. It is designed with 4-A peak-source and 6-A peak-sink current to drive power MOSFET, IGBT, and GaN transistors.

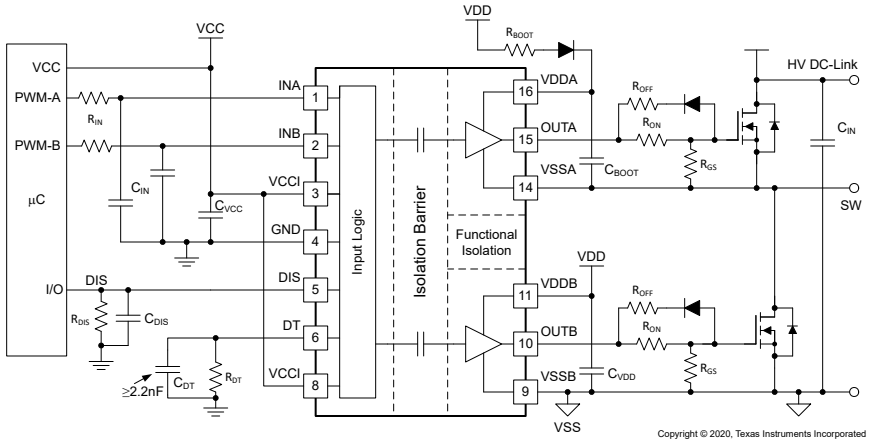
The UCC21540-Q1 can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. The input side is isolated from the two output drivers by a 5.7-kV_{RMS} isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI).

Protection features include: resistor programmable dead time, disable feature to shut down both outputs simultaneously, integrated de-glitch filter that rejects input transients shorter than 5ns, and negative voltage handling for up to –2V spikes for 200ns on input and output pins. All supplies have UVLO protection.

Device Information(1)

PART NUMBER	I_{PK}	Rec. VDD Supply Min.	PACKAGE
UCC21540QDWKQ1	4.0-A/6.0-A	9.2-V	SOIC (14)
UCC21540AQDWKQ1	4.0-A/6.0-A	6.0-V	SOIC (14)

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2021) to Revision C (February 2021)	Page
• Updated Reinforced Isolation Capcitor Life Time Projection Figure	9

Changes from Revision A (July 2020) to Revision B (February 2021)	Page
• Added functional safety quality-managed to features list	1
• Changed Features, Applications, and Description sections	1
• Added initial release of UCC21540A-Q1 device	1
• Added UCC21540A-Q1 UVLO thresholds	7
• Added UCC21540A-Q1 UVLO threshold plots	9

Changes from Revision * (May 2020) to Revision A (July 2020)	Page
• Changed marketing status from Advance Information to initial release.	1

5 Device Comparison Table

DEVICE OPTIONS	UVLO	PEAK CURRENT	PACKAGE
UCC21540QDWKQ1	8.0-V	4-A Source, 6-A Sink	SOIC-14
UCC21540AQDWKQ1	5.0-V	4-A Source, 6-A Sink	SOIC-14

6 Pin Configuration and Functions

UCC21540-Q1 Pin Functions

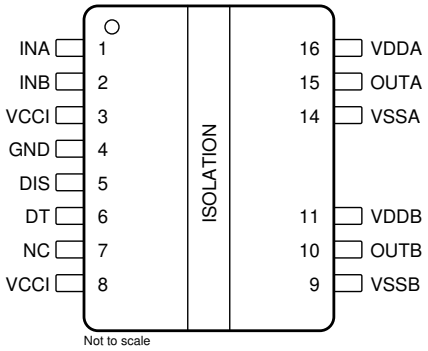


Figure 6-1. DWK Package 14-Pin SOIC Top View

PIN		I/O (1)	Description
NAME	NO.		
DIS	5	I	Disables both driver outputs if asserted high, enables if set low. It is recommended to tie this pin to ground if not used to achieve better noise immunity. Bypass using a ≈ 1-nF low ESR/ESL capacitor close to DIS pin when connecting to a µC with distance.
DT	6	I	DT pin configuration: • Tying DT to VCCI disables the DT feature and allows the outputs to overlap. • Placing a resistor (R_{DT}) between DT and GND adjusts dead time according to the equation: DT (in ns) = 10 × R_{DT} (in kΩ). TI recommends bypassing this pin with a ceramic capacitor, 2.2 nF or greater, close to DT pin to achieve better noise immunity.
GND	4	P	Primary-side ground reference. All signals in the primary side are referenced to this ground.
INA	1	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
INB	2	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
NC	7	-	No internal connection. This pin can be left floating, tied to VCCI, or tied to GND.
NC	12	-	For SOIC-14 DWK Package, pin 12 and pin 13 are removed.
	13		
OUTA	15	O	Output of driver A. Connect to the gate of the A channel FET or IGBT.
OUTB	10	O	Output of driver B. Connect to the gate of the B channel FET or IGBT.
VCCI	3	P	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
VCCI	8	P	This pin is internally shorted to pin 3. Preference should be given to bypassing pin 3-4 instead of pins 8-4.
VDDA	16	P	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.
VDDB	11	P	Secondary-side power for driver B. Locally decoupled to VSSB using a low ESR/ESL capacitor located as close to the device as possible.
VSSA	14	P	Ground for secondary-side driver A. Ground reference for secondary side A channel.
VSSB	9	P	Ground for secondary-side driver B. Ground reference for secondary side B channel.

(1) P = power, I = input, O = output

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input bias pin supply voltage	VCCI to GND	–0.5	6	V
Driver bias supply	VDDA-VSSA, VDDB-VSSB	–0.5	20	V
Output signal voltage	OUTA to VSSA, OUTB to VSSB	–0.5	V_{VDDA}+0.5, V_{VDDB}+0.5	V
	OUTA to VSSA, OUTB to VSSB, Transient for 200 ns	–2	V_{VDDA}+0.5, V_{VDDB}+0.5	V
Input signal voltage	INA, INB, DIS and DT to GND	–0.5	V_{VCCI}+0.5	V
	INA, INB Transient to GND for 200ns	–2	V_{VCCI}+0.5	V
Channel to channel isolation voltage	|VSSA-VSSB| in DWK Package		1850	V
Junction temperature, T_J (2)		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To maintain the recommended operating conditions for T_J, see the Section 7.4.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
VCCI	VCCI Input supply voltage		3	5.5	V
VDDA, VDDB	Driver output bias supply	UCC21540-Q1	9.2	18	
		UCC21540A-Q1	6.0	18	
T_J	Junction Temperature		–40	150	°C
T_A	Ambient Temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		UCC21540-Q1 DWK (SOIC)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Power Ratings

			VALUE	UNIT
P_D	Power dissipation	VCCI = 5.5 V, VDDA/B = 12 V, INA/B = 3.3 V, 2.7 MHz 50% duty cycle square wave 1.0-nF load	915	mW
P_{DI}	Power dissipation by transmitter side		15	mW
P_{DA}, P_{DB}	Power dissipation by each driver side		450	mW

7.6 Insulation Specifications

	PARAMETER	TEST CONDITIONS	VALUE	UNIT
CLR	External clearance[1]	Shortest pin-to-pin distance through air	> 8	mm
CPG	External creepage[1]	Shortest pin-to-pin distance across the package surface	> 8	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 8.5 µm)	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB), test (See Figure 7-1)	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification) V_{TEST} = 1.2 × V_{IOTM}, t = 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} = 12800 V_{PK} (qualification)	8000	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After I/O safety test subgroup 2/3. V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 X V_{IORM} = 1697 V_{PK}, t_m = 10 s	<5	pC
		Method a, After environmental tests subgroup 1. V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 X V_{IORM} = 2262 V_{PK}, t_m = 10 s	<5	
		Method b1; At routine test (100% production) and preconditioning (type test) V_{ini} = 1.2 × V_{IOTM}; t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 * V_{IORM} = 2651 V_{PK} , t_m = 1 s	<5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 sin (2πft), f =1 MHz	1.2	pF

7.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S =150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 sec. (qualification), V_{TEST} = 1.2 × V_{ISO} = 6840V_{RMS}, t = 1 sec (100% production)	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications..
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

7.7 Safety-Related Certifications

VDE	UL	CQC
Certified according to DIN V VDE V 0884-11:2017-01	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011
Reinforced Insulation Maximum Transient Isolation Voltage, 8000 V_{PK}; Maximum Repetitive Peak Voltage, 1414 V_{PK}; Maximum Surge Isolation Voltage, 8000 V_{PK}	Single protection, 5700 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate
Certification number: 40040142	File number: E181974	Certificate number: CQC19001226951

7.8 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
I_S	Safety output supply current	θ_{JA} = 69.7°C/W, $V_{VDDA/B}$ = 12 V, T_J = 150°C, T_A = 25°C See Figure 7-2	DRIVER A, DRIVER B			73	mA
P_S	Safety supply power	θ_{JA} = 69.7°C/W, V_{VCCI} = 5.5 V, T_J = 150°C, T_A = 25°C See Figure 7-3	INPUT			15	mW
			DRIVER A			880	
			DRIVER B			880	
			TOTAL			1775	
T_S	Safety temperature (1)					150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Section 7.4* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

7.9 Electrical Characteristics

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitor from VCCI to GND and 1-µF capacitor from VDDA/B to VSSA/B, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, DT pin tied to VCCI, C_L = 0 pF, T_J = –40°C to +150°C unless otherwise noted(1) (2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCCI}	VCCI quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		1.5	2.0	mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		1.0	1.8	mA
I_{VCCI}	VCCI operating current	current per channel (f = 500-kHz, 50% duty cycle)		2.5		mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB operating current	current per channel (f = 500 kHz, 50% duty cycle), C_L = 100 pF		2.5		mA
VCC SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VCCI_ON}	UVLO Rising threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	UVLO Falling threshold		2.35	2.5	2.65	V
V_{VCCI_HYS}	UVLO Threshold hysteresis			0.2		V
UCC21540A-Q1 VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold		5.0	5.5	5.9	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold		4.7	5.2	5.6	V
V_{VDDA_HYS}, V_{VDDB_HYS}	UVLO Threshold hysteresis			0.3		V
UCC21540-Q1 VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold		8	8.5	9	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold		7.5	8	8.5	V
V_{VDDA_HYS}, V_{VDDB_HYS}	UVLO Threshold hysteresis			0.5		V
INA, INB AND DISABLE						
V_{INAH}, V_{INBH}, V_{DISH}	Input high threshold voltage		1.6	1.8	2	V
V_{INAL}, V_{INBL}, V_{DISL}	Input low threshold voltage		0.8	1	1.25	V
V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}	Input threshold hysteresis			0.8		V
OUTPUT						
I_{OA+}, I_{OB+}	Peak output source current	C_{VDD} = 10 µF, C_{LOAD} = 0.18 µF, f = 1 kHz, bench measurement	2	4		A
I_{OA-}, I_{OB-}	Peak output sink current		3	6		A
R_{OHA}, R_{OHB}	Output resistance at high state	I_{OUT} = –10 mA, R_{OHA}, R_{OHB} do not represent drive pull-up performance. See t_{RISE} in and Section 9.3.4 for details.		5	10	Ω
R_{OLA}, R_{OLB}	Output resistance at low state	I_{OUT} = 10 mA		0.55	1.1	Ω
V_{OHA}, V_{OHB}	Output voltage at high state	V_{VDDA}, V_{VDDB} = 12 V, I_{OUT} = –10 mA	11.9	11.95		V
V_{OLA}, V_{OLB}	Output voltage at low state	V_{VDDA}, V_{VDDB} = 12 V, I_{OUT} = 10 mA		5.5	11	mV
V_{OAPDA}, V_{OAPDB}	Driver output (V_{OUTA}, V_{OUTB}) active pull down	V_{VDDA} and V_{VDDB} unpowered, I_{OUTA}, I_{OUTB} = 200 mA		1.75	2.1	V
DEAD TIME AND OVERLAP PROGRAMMING						

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitor from VCCI to GND and 1-µF capacitor from VDDA/B to VSSA/B, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, DT pin tied to VCCI, C_L = 0 pF, T_J = –40°C to +150°C unless otherwise noted(1) (2).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dead time, DT	DT pin tied to VCCI	Overlap determined by INA, INB			-
	R_{DT} = 10 kΩ	80	100	120	ns
	R_{DT} = 20 kΩ	160	200	240	
	R_{DT} = 50 kΩ	400	500	600	
Dead time matching, $\|DT_{AB}-DT_{BA}\|$	R_{DT} = 10 kΩ	-	0	10	ns
	R_{DT} = 20 kΩ	-	0	20	
	R_{DT} = 50 kΩ	-	0	65	

(1) Current direction in the testing conditions are defined to be positive into the pin and negative out of the specified terminal (unless otherwise noted)
(2) Parameters with only a typical value are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.10 Switching Characteristics

V_{VCCI} = 3.3 V or 5.5 V, 0.1-µF capacitor from VCCI to GND, V_{VDDA} = V_{VDDB} = 12 V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, load capacitance C_{OUT} = 0 pF, T_J = –40°C to +150°C unless otherwise noted(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output rise time, see Figure 8-4	C_{VDD} = 10 µF, C_{OUT} = 1.8 nF, V_{VDDA}, V_{VDDB} = 12 V, f = 1 kHz		5	16	ns
t_{FALL}	Output fall time, see Figure 8-4	C_{VDD} = 10 µF, C_{OUT} = 1.8 nF , V_{VDDA}, V_{VDDB} = 12 V, f = 1 kHz		6	12	ns
t_{PWmin}	Minimum input pulse width that passes to output, see Figure 8-1 and Figure 8-2	Output does not change the state if input signal less than t_{PWmin}		10	20	ns
t_{PDHL}	Propagation delay at falling edge, see Figure 8-3	INx high threshold, V_{INH}, to 10% of the output		28	40	ns
t_{PDLH}	Propagation delay at rising edge, see Figure 8-3	INx low threshold, V_{INL}, to 90% of the output		28	40	ns
t_{PWD}	Pulse width distortion	$\|t_{PDLHA} - t_{PDHLA}\|$, $\|t_{PDLHB} - t_{PDHLB}\|$ see Figure 8-3			5.5	ns
t_{DM}	Propagation delays matching, $\|t_{PDLHA} - t_{PDLHB}\|$, $\|t_{PDHLA} - t_{PDHLB}\|$, see Figure 8-3	f = 250kHz			5	ns
$t_{VCCI+ to OUT}$	VCCI Power-up Delay Time: UVLO Rise to OUTA, OUTB, See Figure 8-7	INA or INB tied to VCCI		40	59	µs
$t_{VDD+ to OUT}$	VDDA, VDDB Power-up Delay Time: UVLO Rise to OUTA, OUTB See Figure 8-8	INA or INB tied to VCCI		23	35	
$\|CM_H\|$	High-level common-mode transient immunity (See Section 8.7)	Slew rate of GND vs. VSSA/B, INA and INB both are tied to VCCI; V_{CM}=1000 V;	100			V/ns
$\|CM_L\|$	Low-level common-mode transient immunity (See Section 8.7)	Slew rate of GND vs. VSSA/B, INA and INB both are tied to GND; V_{CM}=1000 V;	100			

(1) Parameters with only a typical value are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.11 Insulation Characteristics Curves

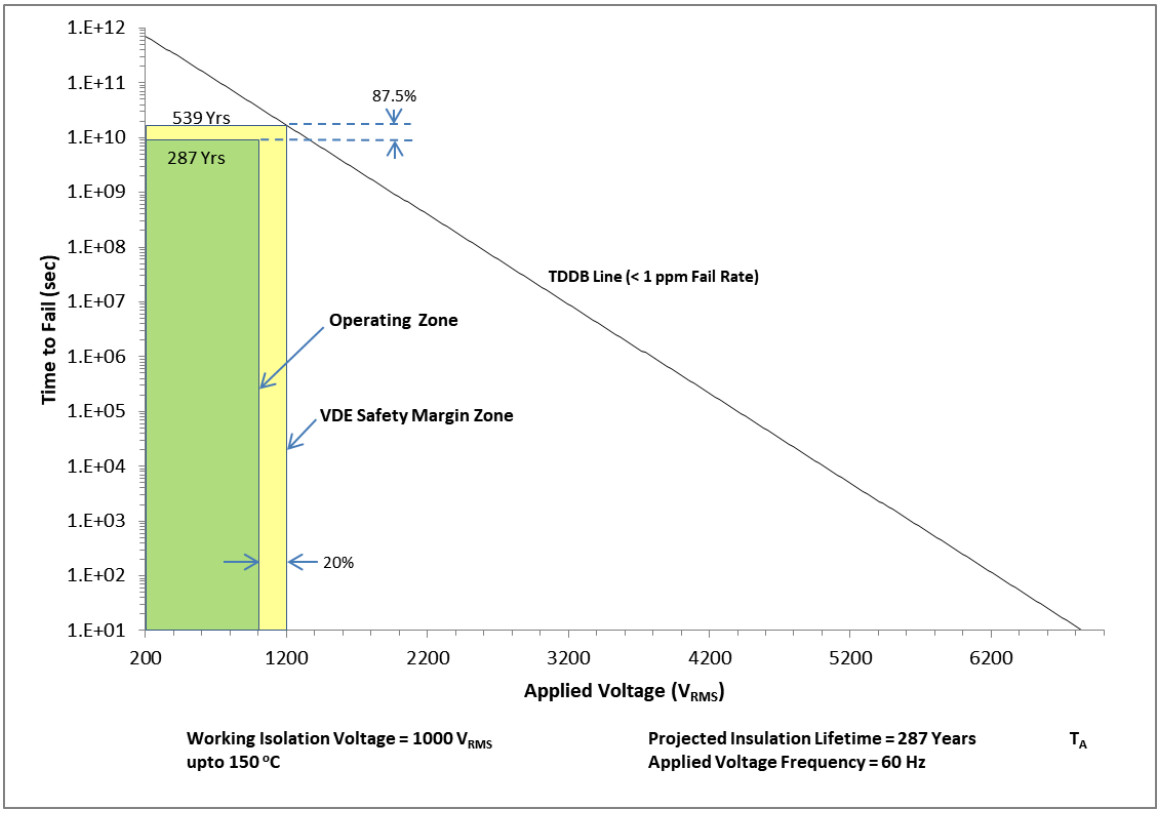
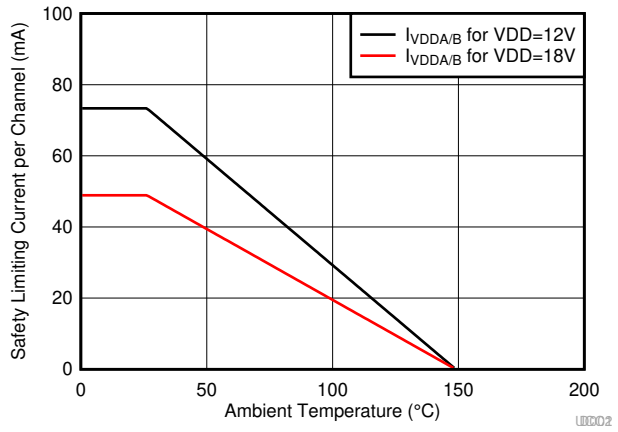


Figure 7-1. Reinforced Isolation Capacitor Life Time Projection



Current in Each Channel with Both Channels Running Simultaneously

Figure 7-2. Thermal Derating Curve for Limiting Current Per VDE

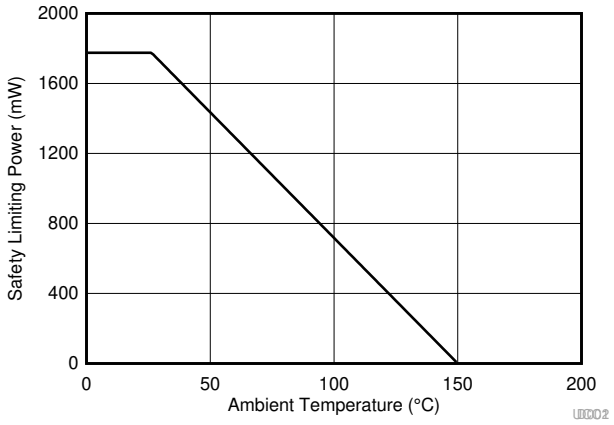
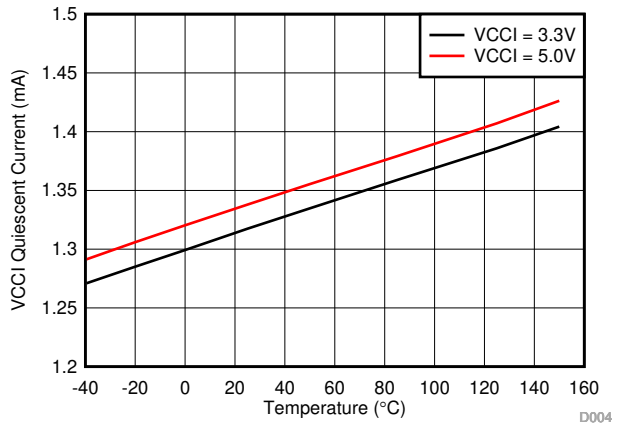


Figure 7-3. Thermal Derating Curve for Limiting Power Per VDE

7.12 Typical Characteristics

VDDA = VDDB = 12 V, VCCI = 3.3 V or 5.0 V, DT pin tied to VCCI, T_A = 25°C, C_L = 0 pF unless otherwise noted.



No Load INA = INB = GND

Figure 7-4. VCCI Quiescent Current

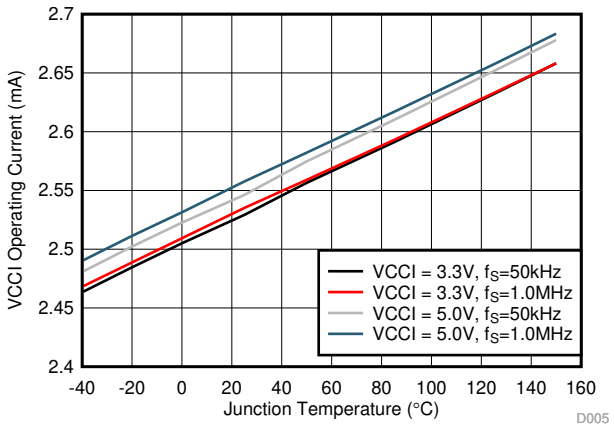


Figure 7-5. VCCI Operating Current - I_{VCCI}

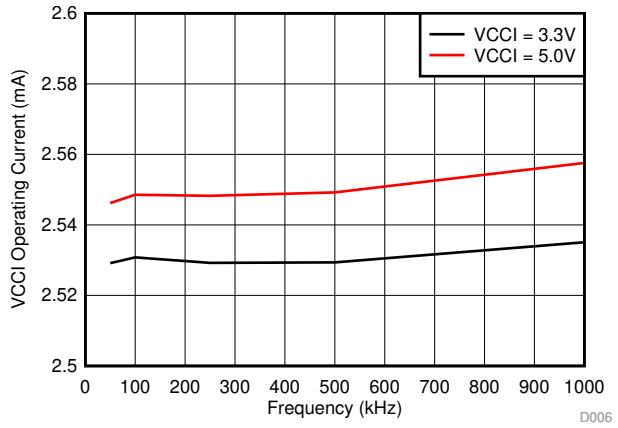
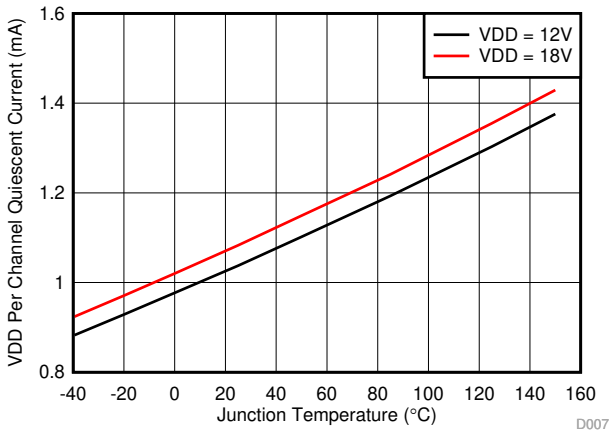
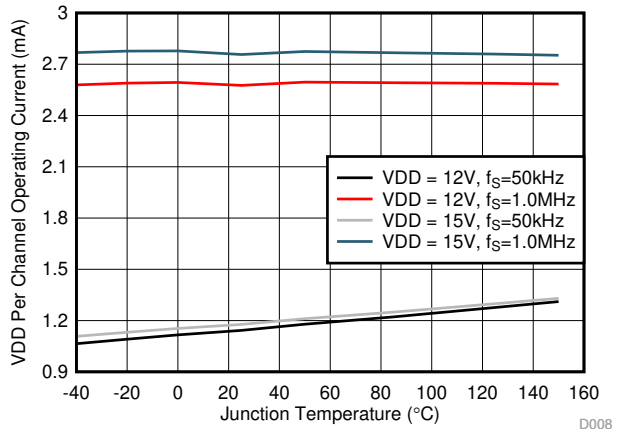


Figure 7-6. VCCI Operating Current vs. Frequency



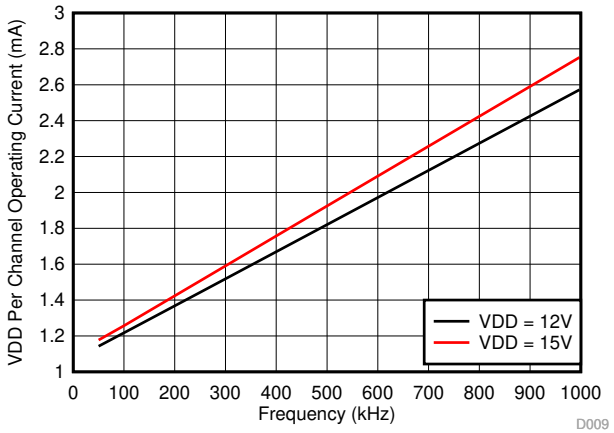
No Load INA = INB = GND

Figure 7-7. VDD Per Channel Quiescent Current (I_{VDDA}, I_{VDDB})



No Load

Figure 7-8. VDD Per Channel Operating Current - $I_{VDDA/B}$



No Load INA and INB both switching

Figure 7-9. Per Channel Operating Current ($I_{VDDA/B}$) vs. Frequency

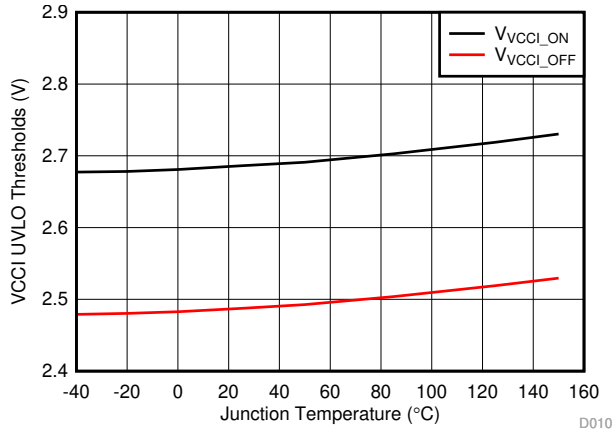


Figure 7-10. VCCI UVLO Threshold Voltage

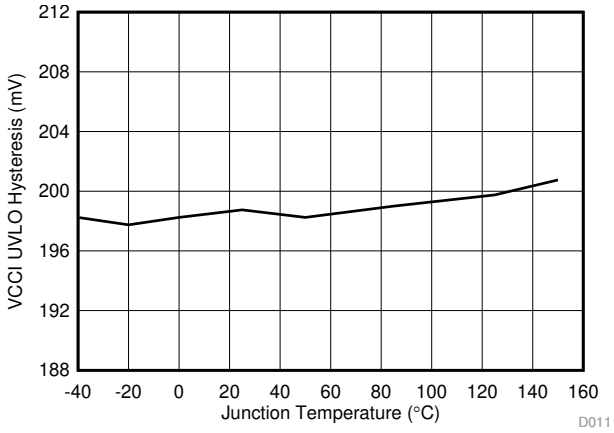


Figure 7-11. VCCI UVLO Threshold Hysteresis Voltage

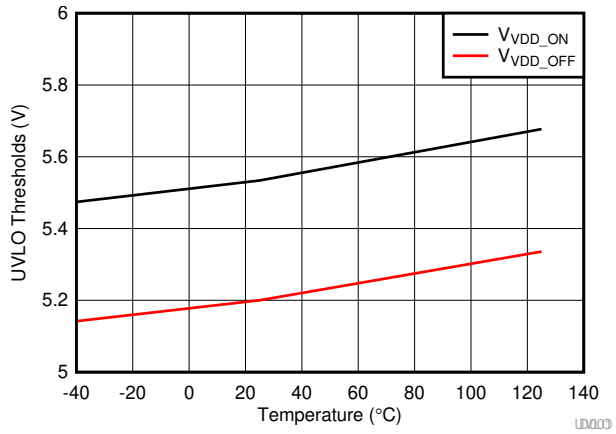


Figure 7-12. 5-V VDD UVLO Threshold Voltage

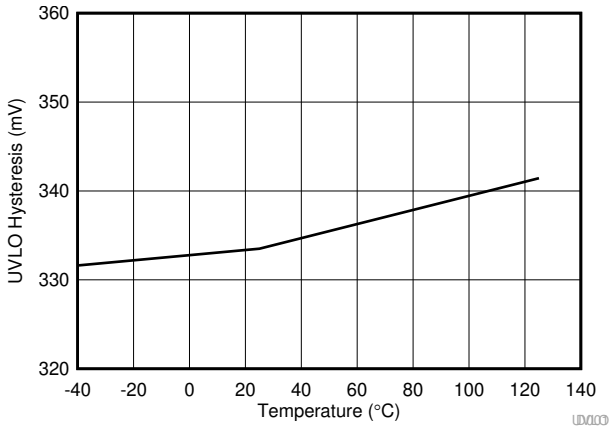


Figure 7-13. 5-V VDD UVLO Hysteresis Voltage

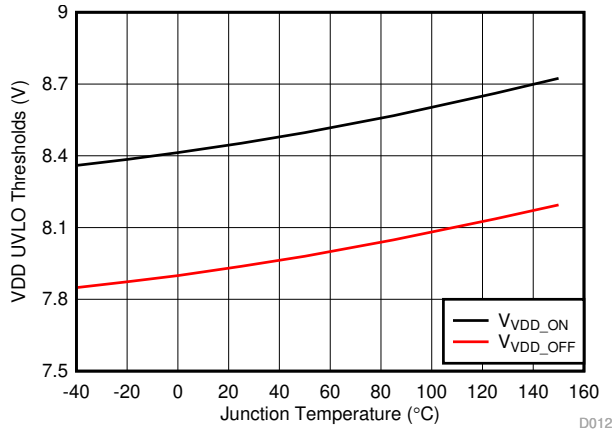


Figure 7-14. 8-V VDD UVLO Threshold Voltage

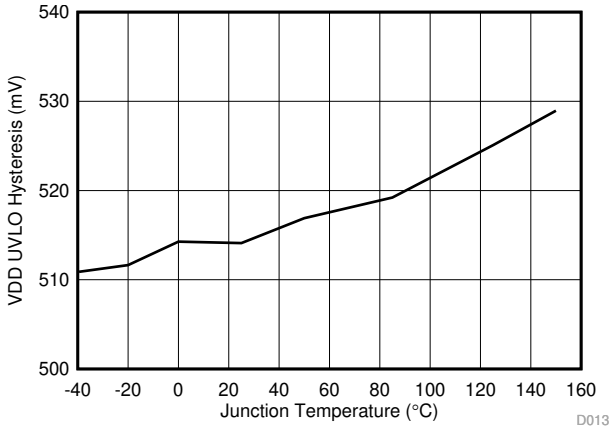


Figure 7-15. 8-V VDD UVLO Threshold Hysteresis Voltage

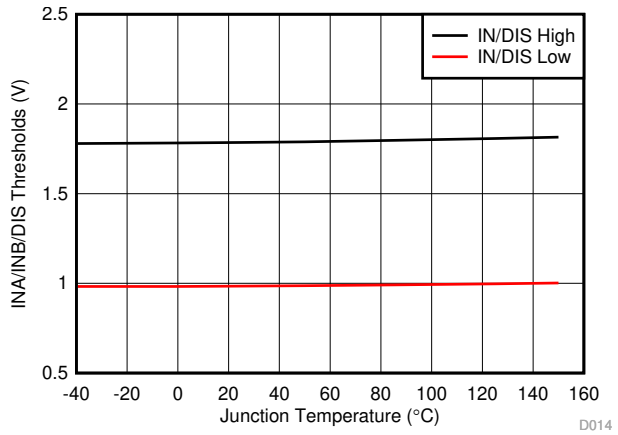


Figure 7-16. INA/INB/DIS High and Low Threshold Voltage

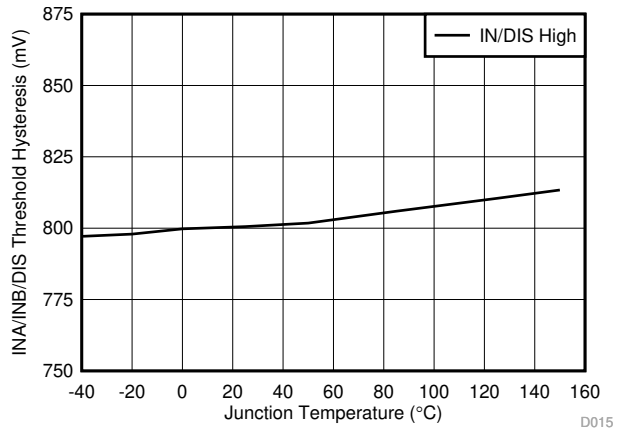


Figure 7-17. INA/INB/DIS High and Low Threshold Hysteresis

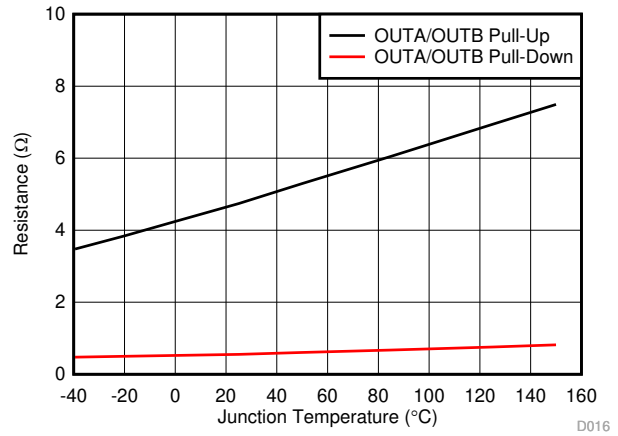


Figure 7-18. OUT Pullup and Pulldown Resistance

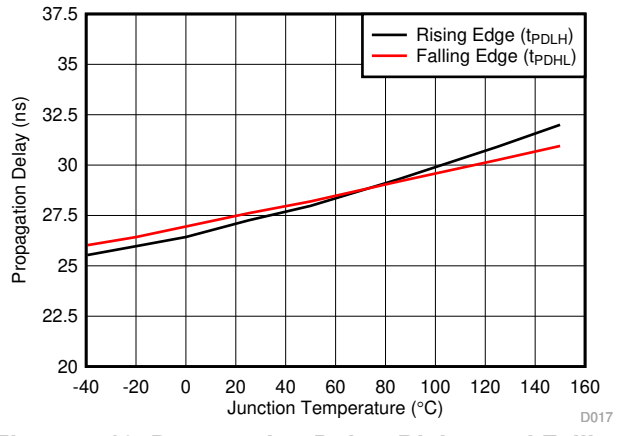


Figure 7-19. Propagation Delay, Rising and Falling Edge

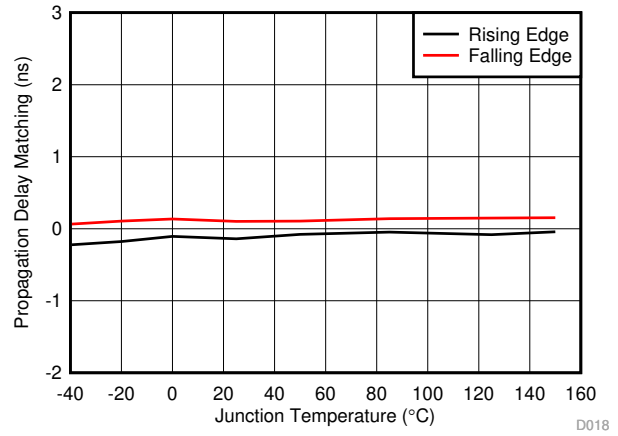
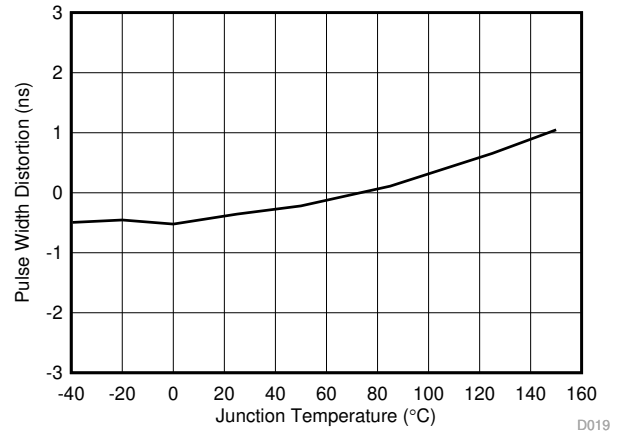
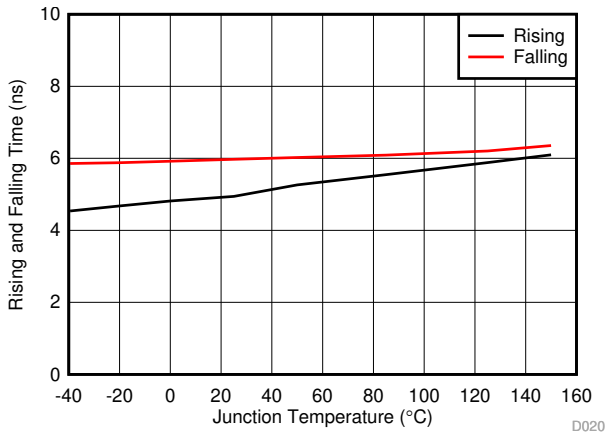


Figure 7-20. Propagation Delay Matching, Rising and Falling Edge



$t_{PDLH} - t_{PDHL}$

Figure 7-21. Pulse Width Distortion



C_L = 1.8 nF

Figure 7-22. Rise Time and Fall Time

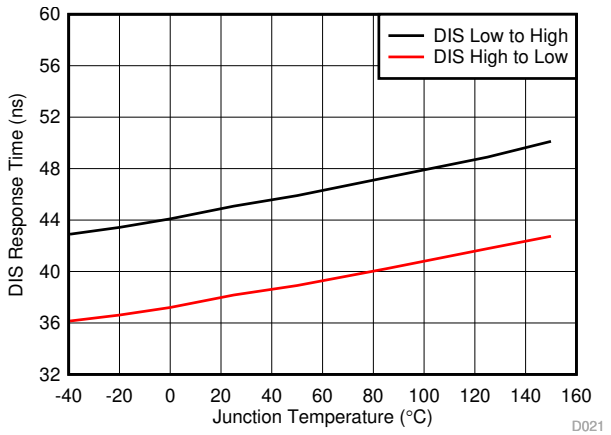


Figure 7-23. DISABLE Response Time

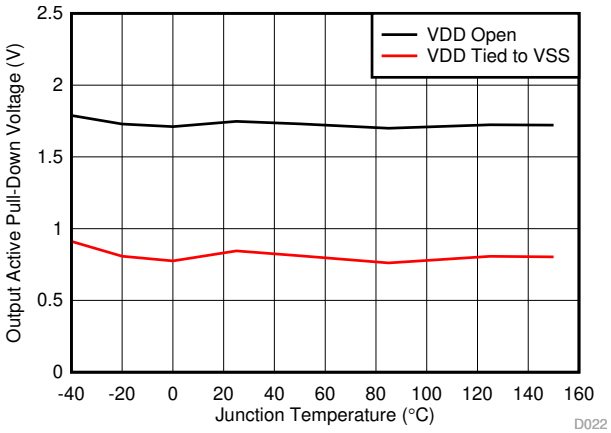


Figure 7-24. OUTPUT Active Pulldown Voltage

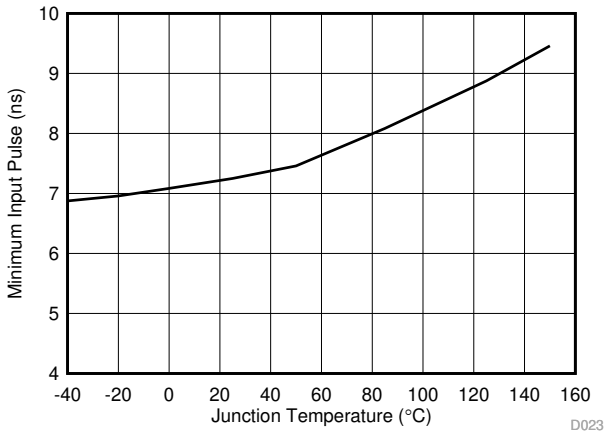


Figure 7-25. Minimum Pulse that Changes Output

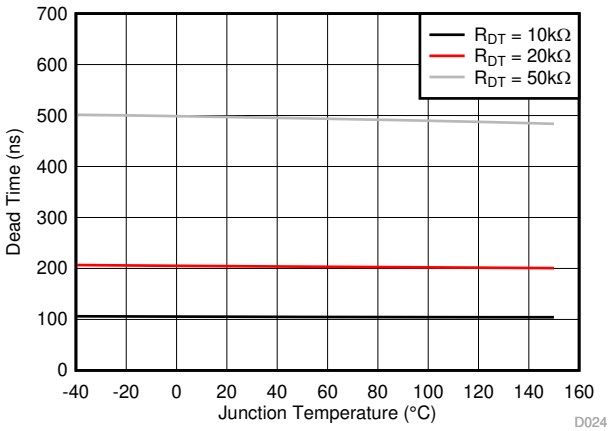


Figure 7-26. Dead Time Temperature Drift

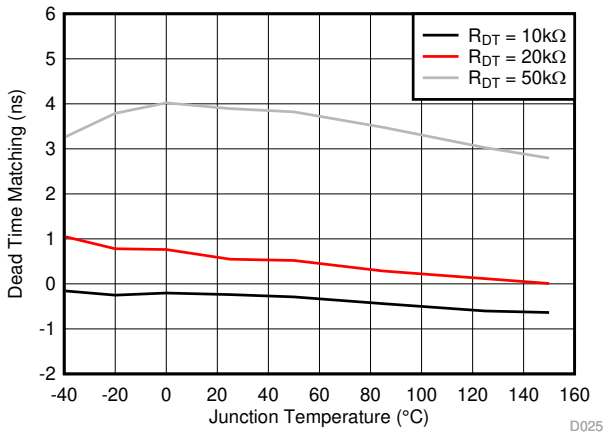


Figure 7-27. Dead Time Matching

8 Parameter Measurement Information

8.1 Minimum Pulses

A typical 5-ns deglitch filter removes small input pulses introduced by ground bounce or switching transients. An input pulse with duration longer than t_{PWmin}, typically 10 ns, must be asserted on INA or INB to guarantee an output state change at OUTA or OUTB. See Figure 8-1 and Figure 8-2 for detailed information of the operation of deglitch filter.

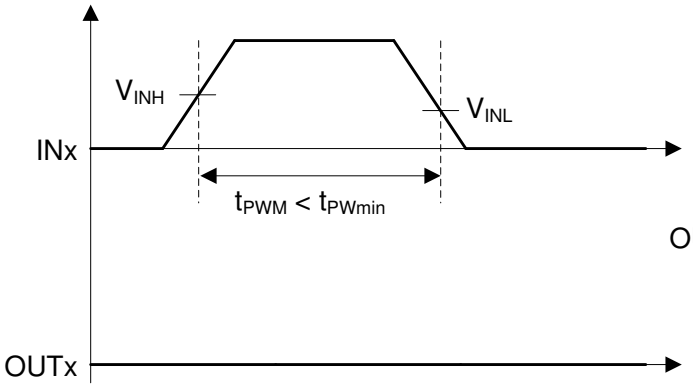


Figure 8-1. Deglitch Filter – Turn ON

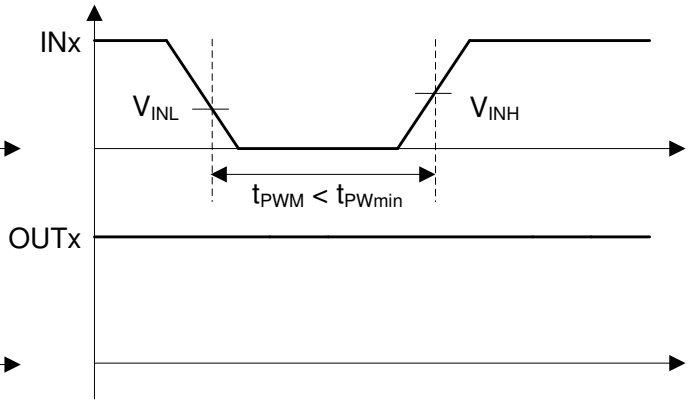


Figure 8-2. Deglitch Filter – Turn OFF

8.2 Propagation Delay and Pulse Width Distortion

Figure 8-3 shows calculation of pulse width distortion (t_{PWD}) and delay matching (t_{DM}) from the propagation delays of channels A and B. To measure delay matching, both inputs must be in phase, and the DT pin must be shorted to VCCI to enable output overlap.

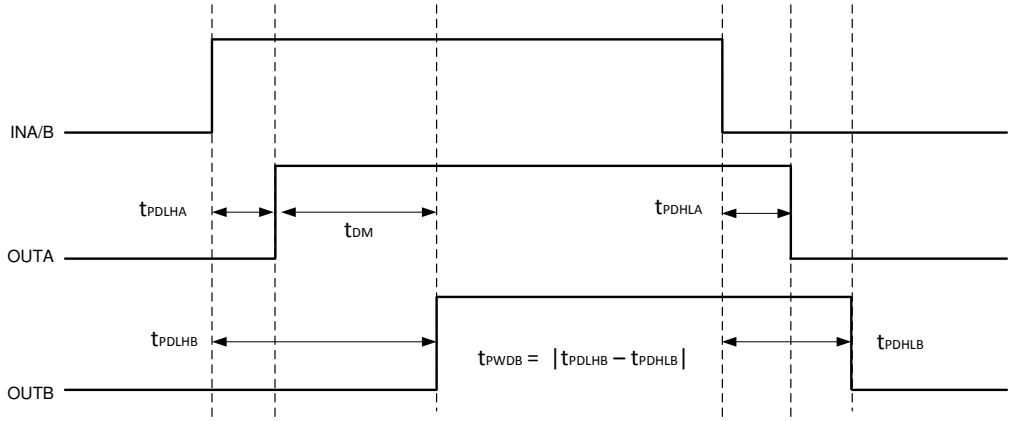


Figure 8-3. Delay Matching and Pulse Width Distortion

8.3 Rising and Falling Time

Figure 8-4 shows the criteria for measuring rising (t_{RISE}) and falling (t_{FALL}) times. For more information on how short rising and falling times are achieved see Section 9.3.4.

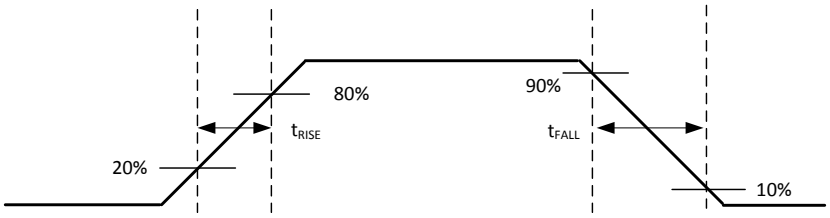


Figure 8-4. Rising and Falling Time Criteria

8.4 Input and Disable Response Time

Figure 8-5 shows the response time of the disable function. For more information, see Section 9.4.1.

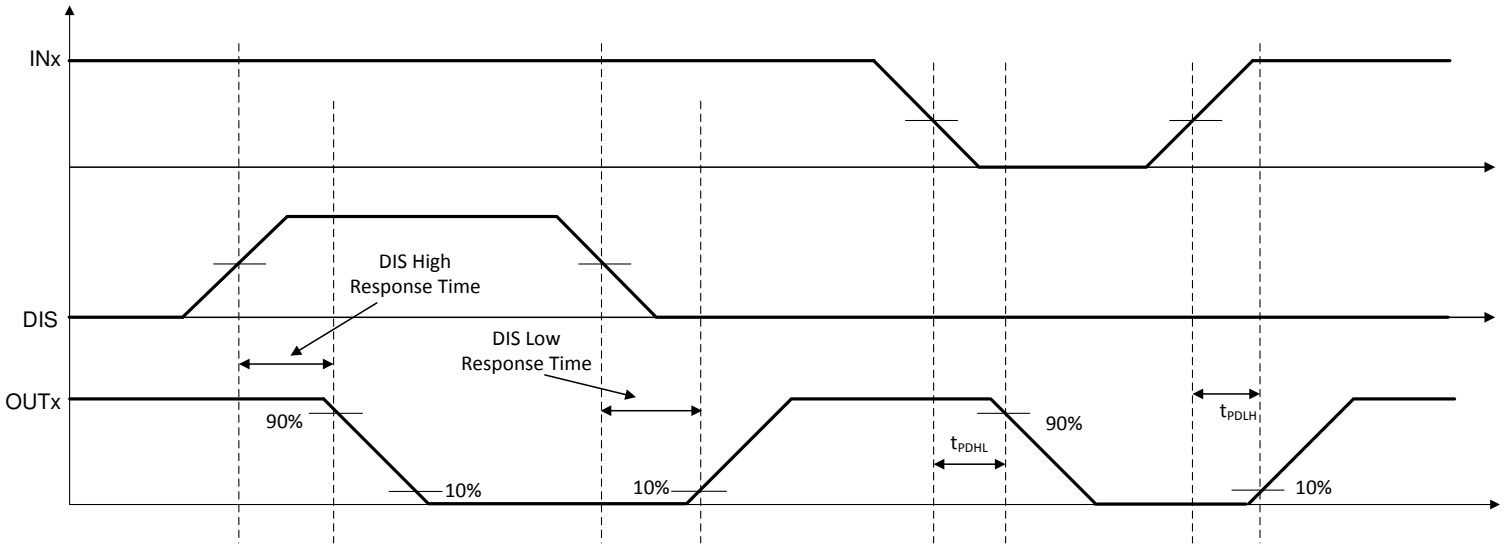


Figure 8-5. Disable Pin Timing

8.5 Programmable Dead Time

Tying DT to VCCI disables DT feature and allows the outputs to overlap. Placing a resistor (R_{DT}) between DT and GND adjusts dead time according to the equation: DT (in ns) = 10 × R_{DT} (in kΩ). TI recommends bypassing this pin with a ceramic capacitor, 2.2 nF or greater, close to DT pin to achieve better noise immunity. For more details on dead time, refer to Section 9.4.2.

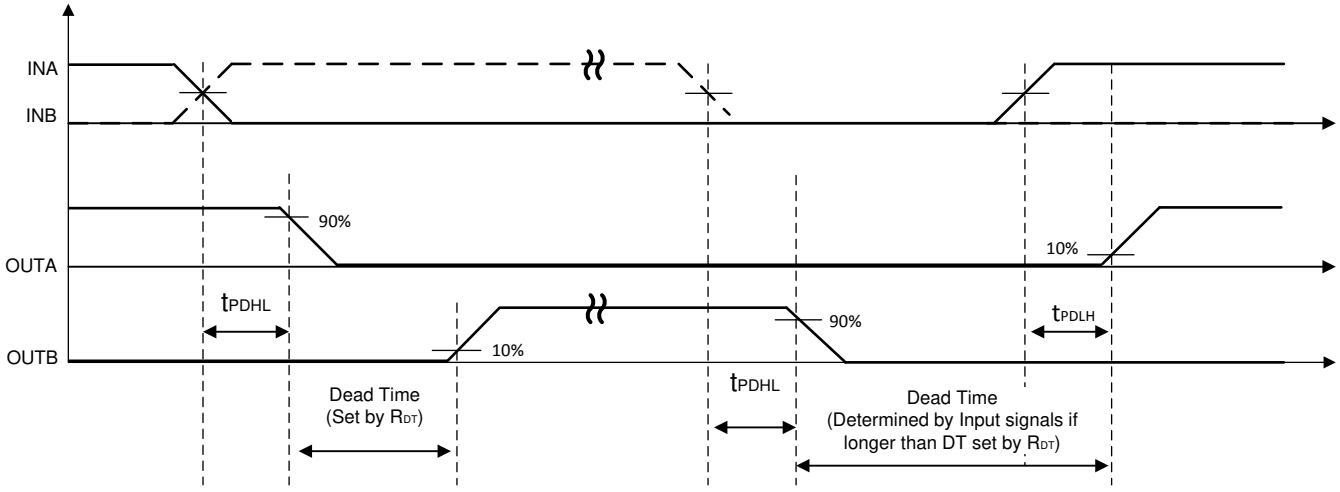


Figure 8-6. Dead Time Switching Parameters

8.6 Power-up UVLO Delay to OUTPUT

Whenever the supply voltage VCCI crosses from below the falling threshold V_{VCCI_OFF} to above the rising threshold V_{VCCI_ON}, and whenever the supply voltage VDDx crosses from below the falling threshold V_{VDDx_OFF} to above the rising threshold V_{VDDx_ON}, there is a delay before the outputs begin responding to the inputs. For VCCI UVLO this delay is defined as $t_{VCCI+ to OUT}$, and is typically 40 µs. For VDDx UVLO this delay is defined as $t_{VDD+ to OUT}$, and is typically 23 µs. TI recommends allowing some margin before driving input signals, to ensure the driver VCCI and VDD bias supplies are fully activated. Figure 8-7 and Figure 8-8 show the power-up UVLO delay timing diagram for VCCI and VDD.

Whenever the supply voltage VCCI crosses below the falling threshold V_{VCCI_OFF}, or VDDx crosses below the falling threshold V_{VDDx_OFF}, the outputs stop responding to the inputs and are held low within 1 µs. This asymmetric delay is designed to ensure safe operation during VCCI or VDDx brownouts.

When VCCI goes away but VDDx is present, outputs are held low; when VDDx is gone, outputs are CLAMPED low through the active pull down feature. For more detailed UVLO feature description, please check session Section 9.3.1.

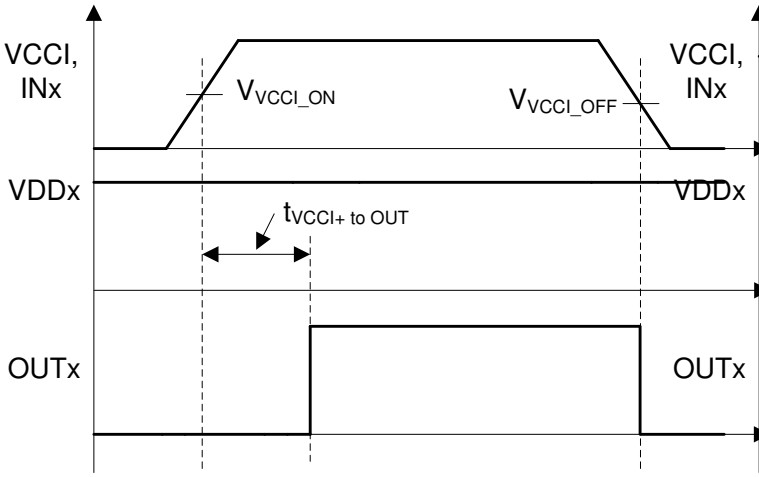


Figure 8-7. VCCI Power-up UVLO Delay

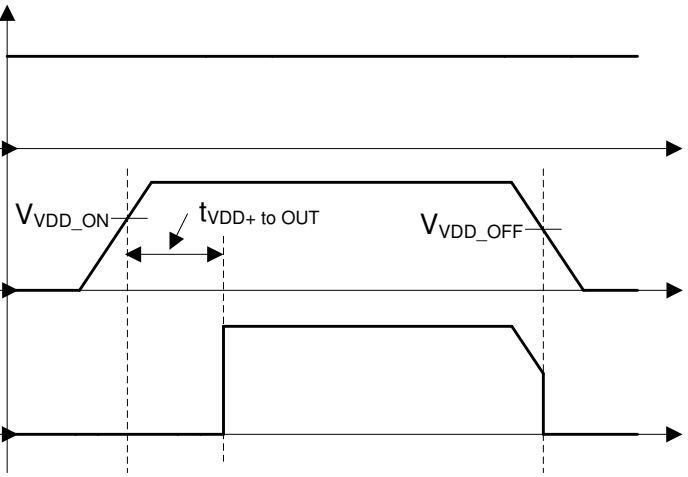


Figure 8-8. VDDA/B Power-up UVLO Delay

8.7 CMTI Testing

Figure 8-9 is a simplified diagram of the CMTI testing configuration.

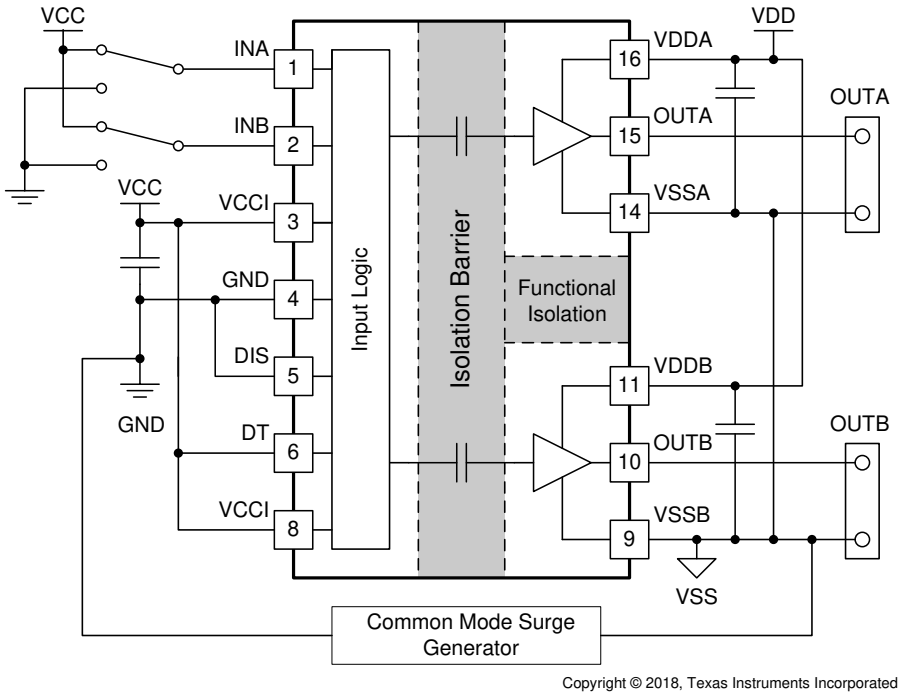


Figure 8-9. Simplified CMTI Testing Setup

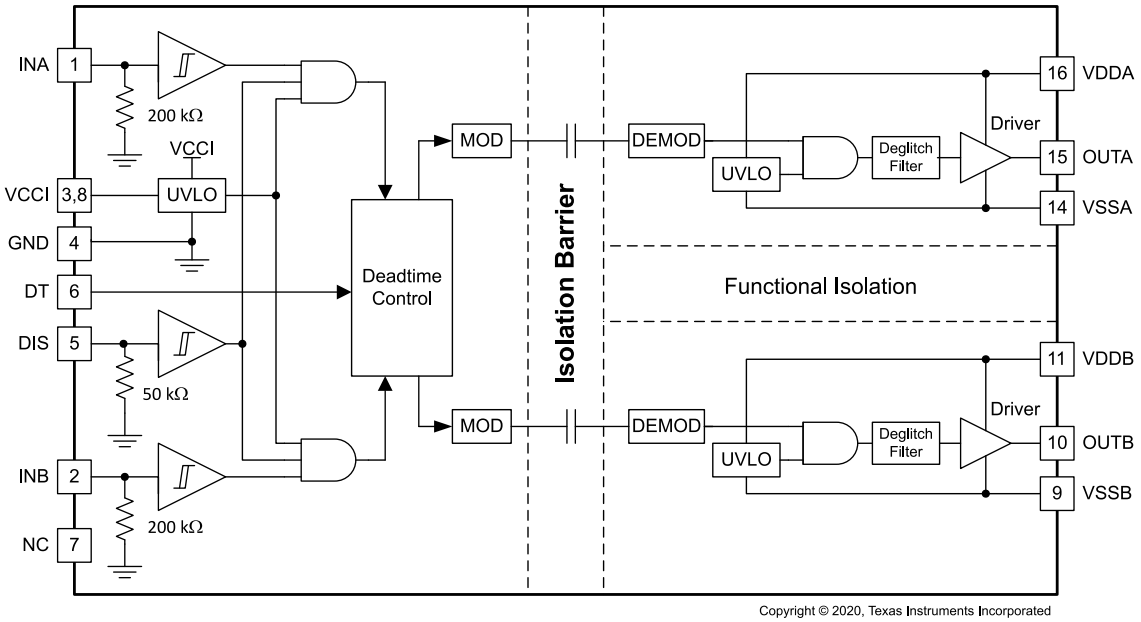
9 Detailed Description

9.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC21540-Q1 is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors. The UCC21540-Q1 has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor-programmable dead time (DT) control, disable pin, and under voltage lock out (UVLO) for both input and output supplies. The UCC21540-Q1 also holds its outputs low when the inputs are left open or when the input pulse duration is too short. The driver inputs are CMOS and TTL compatible for interfacing with digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each of the outputs.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 VDD, VCCI, and Under Voltage Lock Out (UVLO)

The UCC21540-Q1 has an internal under voltage lock out (UVLO) protection feature on each supply voltage between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the channel output low, regardless of the status of the input pins. The VDDx UVLO feature operates independently between CHA and CHB, allowing for bootstrapped systems where low-side output is required before high-side bias can be charged up.

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (illustrated in Figure 9-1). In this condition, the upper PMOS is resistively held off by R_{Hi-Z} while the lower NMOS gate is tied to the driver output through R_{CLAMP}. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.75V, regardless of whether bias power is available.

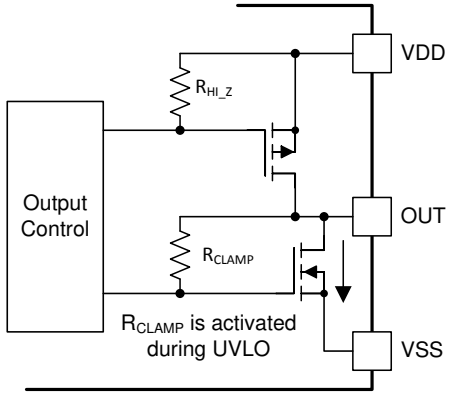


Figure 9-1. Simplified Representation of Active Pull Down Feature

The VDD UVLO protection has a hysteresis feature (V_{VDD_HYS}). This hysteresis prevents chatter when there is ground noise from the power supply. This also allows the device to accept small drops in bias voltage, which commonly occurs when the device starts switching and operating current consumption increases suddenly.

The inputs of the UCC21540-Q1 also has an internal under voltage lock out (UVLO) protection feature. The inputs cannot affect the outputs unless the supply voltage VCCI exceeds V_{VCCI_ON} on start-up. The outputs are held low and cannot respond to inputs when the supply voltage VCCI drops below V_{VCCI_OFF} after start-up. Like the UVLO for VDD, there is hystersis (V_{VCCI_HYS}) to ensure stable operation.

Table 9-1. VCCI UVLO Feature Logic(1)

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	H	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L	L

(1) VDDx > VDD_ON.

Table 9-2. VDDx UVLO Feature Logic(1)

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	H	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L	L	L

(1) VCCI > VCCI_ON.

9.3.2 Input and Output Logic Table

Table 9-3. INPUT/OUTPUT Logic Table(1) (2)

Assume VCCI, VDDA, VDDB are powered up (see Section 9.3.1 for more information on UVLO operation modes). Table 9-3 shows the operation with INA, INB and DIS and the corresponding output state.

INPUTS		DIS	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	L	L	L	If the dead time function is used, output transitions occur after the dead time expires. See Section 9.4.2.
L	H	L	L	H	
H	L	L	H	L	
H	H	L	L	L	DT is programmed with R_{DT}.
H	H	L	H	H	DT pin pulled high to VCCI
Left Open	Left Open	L	L	L	
X	X	H	L	L	Bypass using a ≥1-nF low ESR/ESL capacitor close to DIS pin when connecting to a micro-controller with distance.

(1) "X" means L, H or left open.
(2) For improved noise immunity, TI recommends connecting INA, INB, and DIS to GND, and DT to VCCI, when these pins are not used.

9.3.3 Input Stage

The input pins (INA, INB, and DIS) of the UCC21540-Q1 is based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage of the output channels. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers), since the UCC21540-Q1 has a typical high threshold (V_{INAH}) of 1.8 V and a typical low threshold of 1 V, which vary little with temperature (see and). A wide hysterisis (V_{INA_HYS}) of 0.8 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 200 kΩ for INA/B and 50 kΩ for DIS (see Section 9.2). TI recommends grounding any unused inputs.

The amplitude of any signal applied to the inputs should not exceed the voltage at the VCCI pin. The UCC21540-Q1 cannot be driven from an analog controller with an output voltage greater than the VCCI voltage.

9.3.4 Output Stage

The UCC21540-Q1 output stage features a pull-up structure which delivers the highest peak-source current when it is most needed: during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high.

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *pull-up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC21540-Q1 pull-up stage during this brief turn-on phase is much lower than what is represented by the R_{OH} parameter.

The pull-down structure of the UCC21540-Q1 is composed of an N-channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. The output voltage swings between VDD and VSS for rail-to-rail operation.

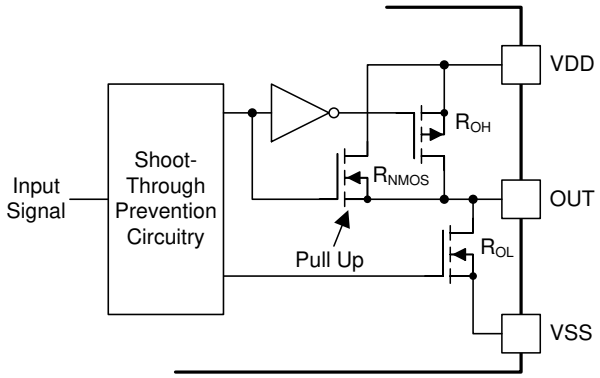


Figure 9-2. Output Stage

9.3.5 Diode Structure in the UCC21540-Q1

Figure 9-3 illustrates the multiple diodes involved in the ESD protection components. This provides a pictorial representation of the absolute maximum rating for the device.

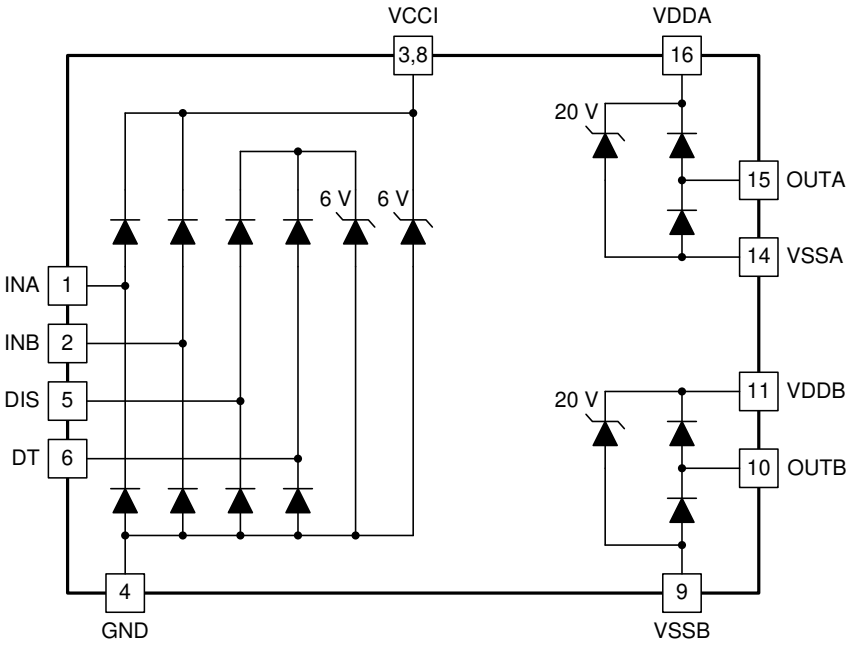


Figure 9-3. ESD Structure

9.4 Device Functional Modes

9.4.1 Disable Pin

When the DIS pin is set high, both outputs are shut down simultaneously. When the DIS pin is set low, the UCC21540-Q1 operates normally. Bypass using a ≈ 1-nF low ESR/ESL capacitor close to DIS pin when connecting to a micro-controller with distance. The DIS circuit logic structure is similar compared to INA or INB, and the propagation delay typical performance can be found in . The DIS pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to GND if the DIS pin is not used to achieve better noise immunity.

9.4.2 Programmable Dead Time (DT) Pin

The UCC21540-Q1 allows the user to adjust dead time (DT) in the following ways:

9.4.2.1 DT Pin Tied to VCCI

Outputs completely match inputs, so no minimum dead time is asserted. This allows the outputs to overlap. TI recommends connecting this pin directly to VCCI if it is not used to achieve better noise immunity.

9.4.2.2 Connecting a Programming Resistor between DT and GND Pins

Program t_{DT} by placing a resistor, R_{DT}, between the DT pin and GND. TI recommends bypassing this pin with a ceramic capacitor, 2.2 nF or greater, close to DT pin to achieve better noise immunity. The appropriate R_{DT} value can be determined from:

$$t_{DT} \approx 10 \times R_{DT} \quad (1)$$

where

- t_{DT} is the programmed dead time, in nanoseconds.
- R_{DT} is the value of resistance between DT pin and GND, in kilo-ohms.

The steady state voltage at the DT pin is about 0.8 V. R_{DT} programs a small current at this pin, which sets the dead time. As the value of R_{DT} increases, the current sourced by the DT pin decreases. The DT pin current will be less than 10 µA when R_{DT} = 100 kΩ. For larger values of R_{DT}, TI recommends placing R_{DT} and a ceramic capacitor, 2.2 nF or greater, as close to the DT pin as possible to achieve greater noise immunity and better dead time matching between both channels.

The falling edge of an input signal initiates the programmed dead time for the other signal. The programmed dead time is the minimum enforced duration in which both outputs are held low by the driver. The outputs may also be held low for a duration greater than the programmed dead time, if the INA and INB signals include a dead time duration greater than the programmed minimum. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent shoot-through in half-bridge applications, and it does not affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in Input and Output Logic Relationship with Input Signals.

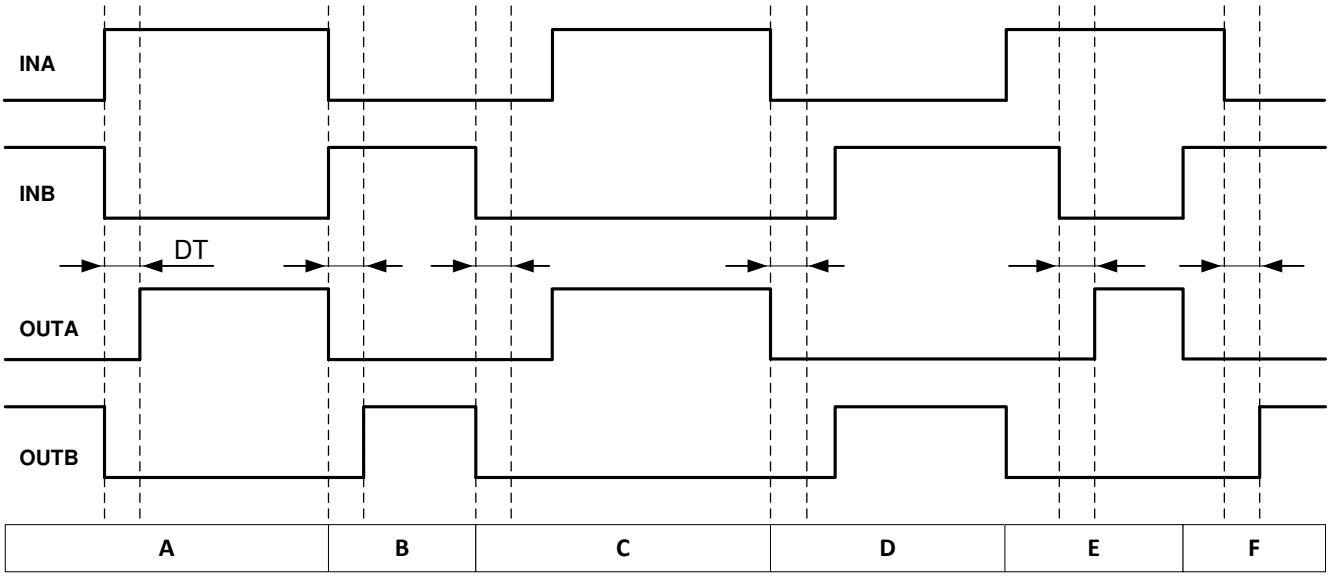


Figure 9-4. Input and Output Logic Relationship with Input Signals

Condition A: INB goes low, INA goes high. INB sets OUTB low immediately and assigns the programmed dead time to OUTA. OUTA is allowed to go high after the programmed dead time.

Condition B: INB goes high, INA goes low. Now INA sets OUTA low immediately and assigns the programmed dead time to OUTB. OUTB is allowed to go high after the programmed dead time.

Condition C: INB goes low, INA is still low. INB sets OUTB low immediately and assigns the programmed dead time for OUTA. In this case, the input signal dead time is longer than the programmed dead time. When INA goes high after the duration of the input signal dead time, it immediately sets OUTA high.

Condition D: INA goes low, INB is still low. INA sets OUTA low immediately and assigns the programmed dead time to OUTB. In this case, the input signal dead time is longer than the programmed dead time. When INB goes high after the duration of the input signal dead time, it immediately sets OUTB high.

Condition E: INA goes high, while INB and OUTB are still high. To avoid overshoot, OUTB is immediately pulled low. After some time OUTB goes low and assigns the programmed dead time to OUTA. OUTB is already low. After the programmed dead time, OUTA is allowed to go high.

Condition F: INB goes high, while INA and OUTA are still high. To avoid overshoot, OUTA is immediately pulled low. After some time OUTA goes low and assigns the programmed dead time to OUTB. OUTA is already low. After the programmed dead time, OUTB is allowed to go high.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The UCC21540-Q1 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC21540-Q1 (with up to 5.5-V VCCI and 18-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or GaN transistor. With integrated components, advanced protection features (UVLO, dead time, and disable) and optimized switching performance, the UCC21540-Q1 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

10.2 Typical Application

The circuit in Figure 10-1 shows a reference design with the UCC21540-Q1 driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

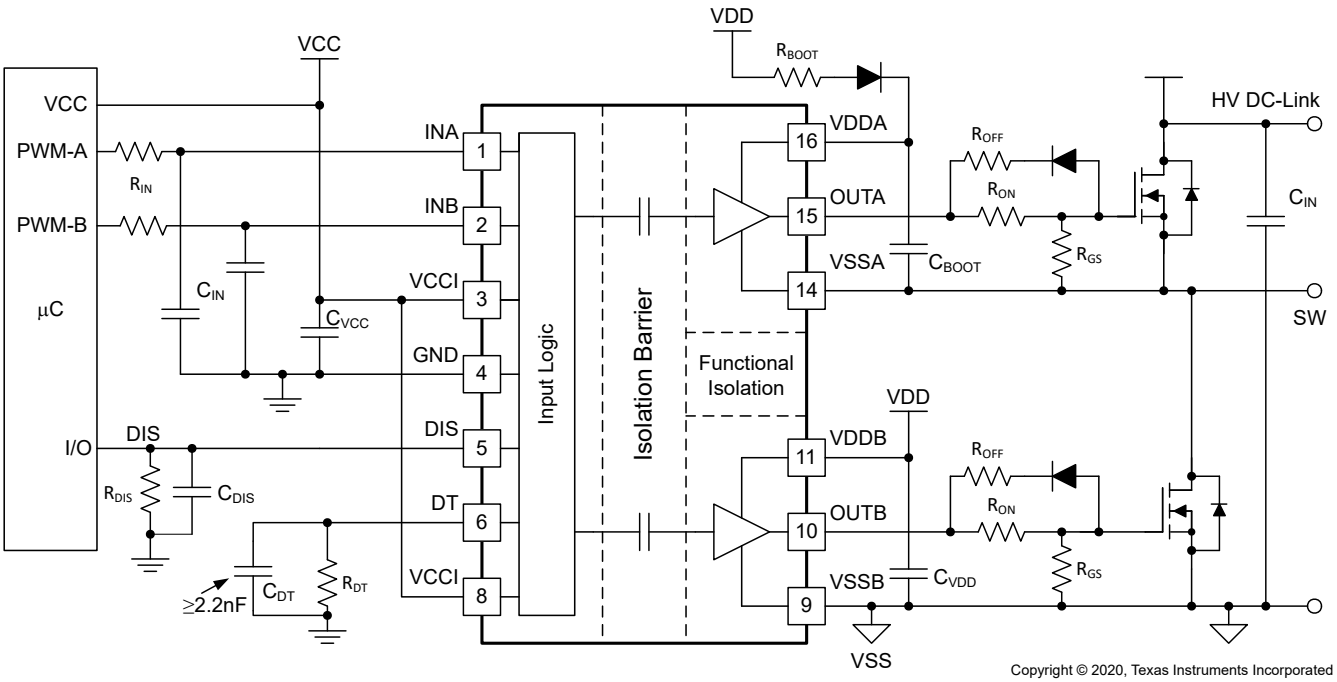


Figure 10-1. Typical Application Schematic

10.2.1 Design Requirements

Table 10-1 lists reference design parameters for the example application: UCC21540-Q1 driving 650-V MOSFETs in a high side-low side configuration.

Table 10-1. UCC21540-Q1 Design Requirements

PARAMETER	VALUE	UNITS
Power transistor	650-V, 150-mΩ R_{DS_ON} with 12-V V_{GS}	-
VCC	5.0	V
VDD	12	V
Input signal amplitude	3.3	V
Switching frequency (f_s)	100	kHz
Dead Time	200	ns
DC link voltage	400	V

10.2.2 Detailed Design Procedure

10.2.2.1 Designing INA/INB Input Filter

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input R_{IN}-C_{IN} filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an R_{IN} in the range of 0 Ω to 100 Ω and a C_{IN} between 10 pF and 100 pF. In the example, an R_{IN} = 51 Ω and a C_{IN} = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

10.2.2.2 Select Dead Time Resistor and Capacitor

From Equation 1, a 20-kΩ resistor is selected to set the dead time to 200 ns. A 2.2-nF capacitor is placed in parallel close to the DT pin to improve noise immunity.

10.2.2.3 Select External Bootstrap Diode and its Series Resistor

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode's forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, TI recommends choosing high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 400 V_{DC}. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 600-V ultrafast diode, MURA160T3G, is chosen in this example.

A bootstrap resistor, R_{BOOT}, is used to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle, especially when the VSSA(SW) pin has an excessive negative transient voltage. The recommended value for R_{BOOT} is between 1 Ω and 20 Ω depending on the diode used. In the example, a current limiting resistor of 2.7 Ω is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through D_{Boot} is,

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} = \frac{12V - 1.5V}{2.7\Omega} \approx 4A \quad (2)$$

where

- V_{BDF} is the estimated bootstrap diode forward voltage drop around 4 A.

Failure to limit the voltage to VDDx-VSSx to less than the Absolute Maximum Ratings of the FET and UCC21540-Q1 may result in permanent damage to the device in certain cases.

10.2.2.4 Gate Driver Output Resistor

The external gate driver resistors, R_{ON}/R_{OFF}, are used to:

- Limit ringing caused by parasitic inductances/capacitances.
- Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
- Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
- Reduce electromagnetic interference (EMI).

As mentioned in Section 9.3.4, the UCC21540-Q1 has a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{OA+} = \min\left(4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \tag{3}$$

$$I_{OB+} = \min\left(4A, \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \tag{4}$$

where

- R_{ON}: External turn-on resistance.
- R_{GFET_INT}: Power transistor internal gate resistance, found in the power transistor datasheet.
- I_{O+} = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

In this example:

$$I_{OA+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{12V - 0.8V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 1.5\Omega} \approx 2.3A \tag{5}$$

$$I_{OB+} = \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{12V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 1.5\Omega} \approx 2.5A \tag{6}$$

Therefore, the high-side and low-side peak source current is 2.3 A and 2.5 A respectively. Similarly, the peak sink current can be calculated with:

$$I_{OA-} = \min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right) \tag{7}$$

$$I_{OB-} = \min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right) \tag{8}$$

where

- R_{OFF}: External turn-off resistance, R_{OFF}=0 in this example;

- V_{GDF}: The anti-parallel diode forward voltage drop which is in series with R_{OFF}. The diode in this example is an MSS1P4.
- I_{O-}: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

In this example,

$$I_{OA-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{12V - 0.8V - 0.85V}{0.55\Omega + 0\Omega + 1.5\Omega} \approx 5.0A \quad (9)$$

$$I_{OB-} = \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{12V - 0.85V}{0.55\Omega + 0\Omega + 1.5\Omega} \approx 5.4A \quad (10)$$

Therefore, the high-side and low-side peak sink current is 5.0 A and 5.4A respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

Failure to control OUTx voltage to less than the Absolute Maximum Ratings in the datasheet (including transients) may result in permanent damage to the device in certain cases. To reduce excessive gate ringing, it is recommended to use a ferrite bead near the gate of the FET. External clamping diodes can also be added in the case of extended overshoot/undershoot, in order to clamp the OUTx voltage to the VDDx and VSSx voltages.

10.2.2.5 Gate to Source Resistor Selection

A gate to source resistor, RGS, is recommended to pull down the gate to the source voltage when the gate driver output is unpowered and in an indeterminate state. This resistor also helps to mitigate the risk of dv/dt induced turn-on due to Miller current before the gate driver is able to turn on and actively pull low. This resistor is typically sized between 5.1kΩ and 20kΩ, depending on the Vth and ratio of CGD to CGS of the power device.

10.2.2.6 Estimating Gate Driver Power Loss

The total loss, P_G, in the gate driver subsystem includes the power losses of the UCC21540-Q1 (P_{GD}) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in P_G and not discussed in this section.

P_{GD} is the key power loss which determines the thermal safety-related limits of the UCC21540-Q1, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. P_{GDQ} is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. and show the operating current consumption vs. operating frequency with no load. In this example, V_{VCCI} = 5 V and V_{VDD} = 12 V. The current on each power supply, with INA/INB switching from 0 V to 3.3 V at 100 kHz is measured to be I_{VCCI} ≈ 2.5 mA, and I_{VDDA} = I_{VDDB} ≈ 1.5 mA. Therefore, the P_{GDQ} can be calculated with

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{VDDB} \times I_{DDB} = 50mW \quad (11)$$

The second component is switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, P_{GSW}, can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW} \tag{12}$$

where

- Q_G is the gate charge of the power transistor.

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 12V \times 100nC \times 100kHz = 240mW \tag{13}$$

Q_G represents the total gate charge of the power transistor switching 480 V at 14 A provided by the datasheet, and is subject to change with different testing conditions. The UCC21540-Q1 gate driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} will be equal to P_{GSW} if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC21540-Q1. If there are external turn-on and turn-off resistances, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2} \times \left(\frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} \right) \tag{14}$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC21540-Q1 gate driver loss can be estimated with:

$$P_{GDO} = \frac{240mW}{2} \times \left(\frac{5\Omega \,||\, 1.47\Omega}{5\Omega \,||\, 1.47\Omega + 2.2\Omega + 1.5\Omega} + \frac{0.55\Omega}{0.55\Omega + 0\Omega + 1.5\Omega} \right) \approx 60mW \tag{15}$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = 2 \times f_{SW} \times \left[4A \times \int_0^{T_{R\_Sys}} \left(V_{DD} - V_{OUTA/B}(t) \right) dt + 6A \times \int_0^{T_{F\_Sys}} V_{OUTA/B}(t)\, dt \right] \tag{16}$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted.

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the P_{GDO} will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC21540-Q1 P_{GD}, is:

$$P_{GD} = P_{GDQ} + P_{GDO} \tag{17}$$

which is equal to 127 mW in the design example.

10.2.2.7 Estimating Junction Temperature

The junction temperature of the UCC21540 UCC21540-Q1 can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{GD} \tag{18}$$

where

- T_J is the junction temperature.
- T_C is the UCC21540-Q1 case-top temperature measured with a thermocouple or some other instrument.
- ψ_{JT} is the junction-to-top characterization parameter from the Section 7.4 table.

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\Theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). $R_{\Theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of $R_{\Theta JC}$ will inaccurately estimate the true junction temperature. Ψ_{JT} is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius. For more information, see the Section 12.1 and Semiconductor and IC Package Thermal Metrics application report.

10.2.2.8 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. TI recommends choosing low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 V_{DC} is applied.

10.2.2.8.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 25-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

10.2.2.8.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 4-A, the source peak current, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with

$$Q_{Total} = Q_G + \frac{I_{VDD}@100kHz(\text{No Load})}{f_{SW}} = 100nC + \frac{1.5mA}{100kHz} = 115nC \tag{19}$$

where

- Q_{Total}: Total charge needed
- Q_G: Gate charge of the power transistor.
- I_{VDD}: The channel self-current consumption with no load at 100kHz.
- f_{SW}: The switching frequency of the gate driver

Therefore, the absolute minimum C_{Boot} requirement is:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{VDDA}} = \frac{115nC}{0.5V} = 230nF \quad (20)$$

where

- ΔV_{VDDA} is the voltage ripple at VDDA, which is 0.5 V in this example.

In practice, the value of C_{Boot} is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a margin in the C_{Boot} value and place it as close to the VDD and VSS pins as possible. A 50-V 1-µF capacitor is chosen in this example.

$$C_{Boot} = 1\mu F \quad (21)$$

Care should be taken when selecting the bootstrap capacitor to ensure that the VDD to VSS voltage does not drop below the recommended minimum operating level listed in section 6.3. The value of the bootstrap capacitor should be sized such that it can supply the initial charge to switch the power device, and then continuously supply the gate driver quiescent current for the duration of the high-side on-time.

If the high-side supply voltage drops below the UVLO falling threshold, the high-side gate driver output will turn off and switch the power device off. Uncontrolled hard-switching of power devices can cause high di/dt and high dv/dt transients on the output of the driver and may result in permanent damage to the device.

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor placed very close to VDDx - VSSx pins with a low ESL/ESR. In this example a 100 nF, X7R ceramic capacitor, is placed in parallel with C_{Boot} to optimize the transient performance.

Note

Too large C_{BOOT} is not good. C_{BOOT} may not be charged within the first few cycles and V_{BOOT} could stay below UVLO. As a result, the high-side FET does not follow input signal command. Also during initial C_{BOOT} charging cycles, the bootstrap diode has highest reverse recovery current and losses.

10.2.2.8.3 Select a VDDB Capacitor

Channel B has the same current requirements as channel A, therefore, a VDDB capacitor (shown as C_{VDD} in Figure 10-1) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-µF MLCC and a 50-V, 220-nF MLCC are chosen for C_{VDD}. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor with a value over 10 µF, should be used in parallel with C_{VDD}.

10.2.2.9 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (e.g. TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

Figure 10-2 shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, V_A, is equal to 17 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 17 V – 5.1 V ≈ 12 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from R_Z.

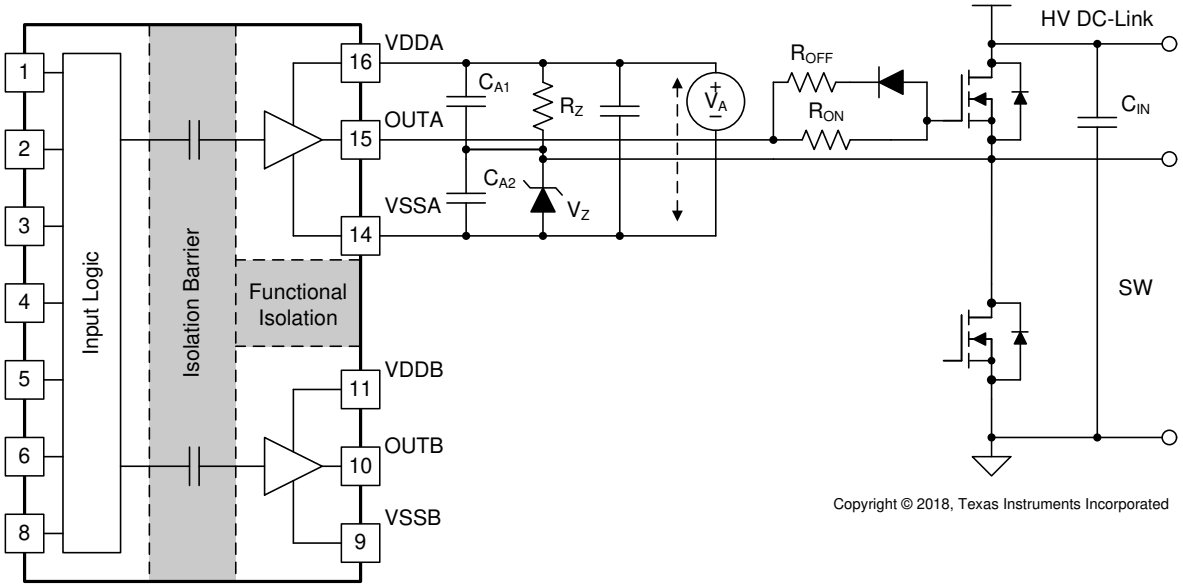


Figure 10-2. Negative Bias with Zener Diode on Iso-Bias Power Supply Output

Figure 10-3 shows another example which uses two supplies (or single-input-double-output power supply). Power supply V_{A+} determines the positive drive output voltage and $V_{A–}$ determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

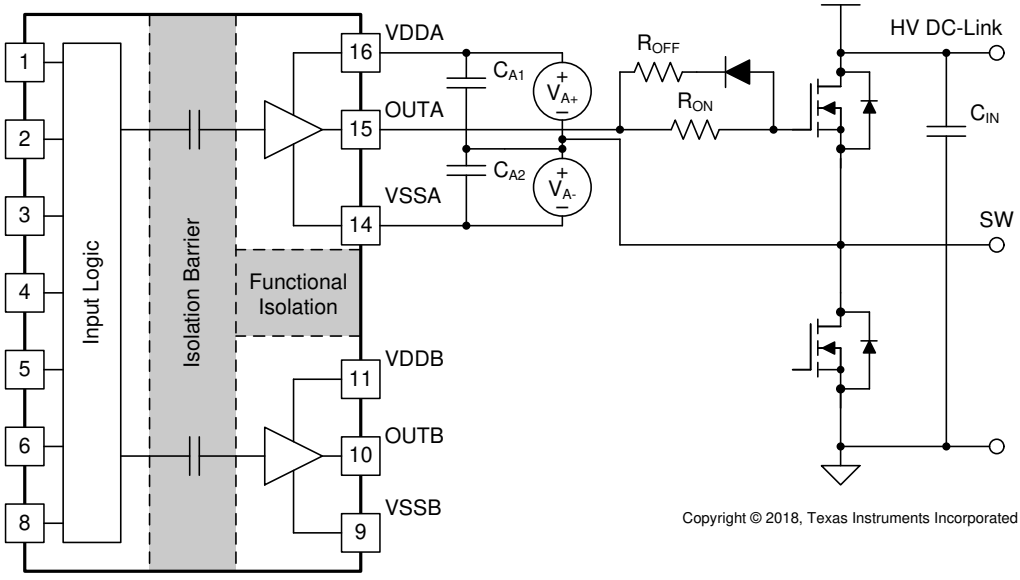


Figure 10-3. Negative Bias with Two Iso-Bias Power Supplies

The last example, shown in Figure 10-4, is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant convertors or phase shift convertors will favor this solution.

2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

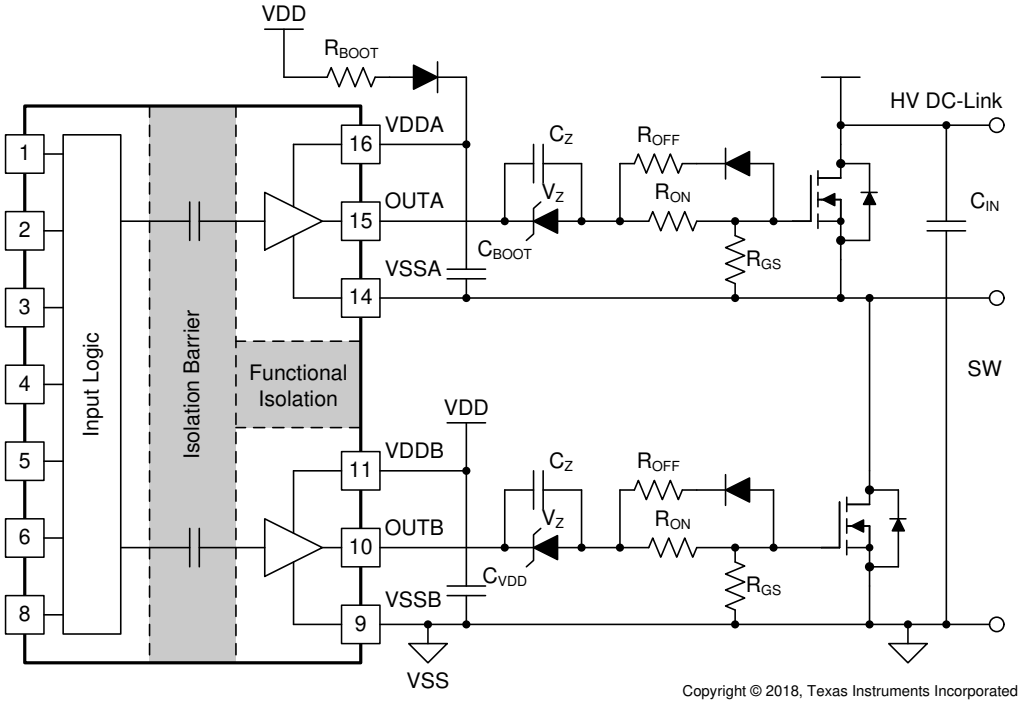


Figure 10-4. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path

10.2.3 Application Curves

Figure 10-5 and Figure 10-6 shows the bench test waveforms for the design example shown in Figure 10-1 under these conditions: VCC = 5.0 V, VDD = 12 V, f_{SW} = 100 kHz, $V_{DC-Link}$ = 400 V.

Channel 1 (Blue): Gate-source signal on the high side power transistor.

Channel 2 (Cyan): Gate-source signal on the low side power transistor.

Channel 3 (Pink): INA pin signal.

Channel 4 (Green): INB pin signal.

In Figure 10-5, INA and INB are sent complimentary 3.3-V, 20%/80% duty-cycle signals. The gate drive signals on the power transistor have a 200-ns dead time with 400V high voltage on the DC-Link, shown in the measurement section of Figure 10-5. Note that with high voltage present, lower bandwidth differential probes are required, which limits the achievable accuracy of the measurement.

Figure 10-6 shows a zoomed-in version of the waveform of Figure 10-5, with measurements for propagation delay and dead time. Importantly, the output waveform is measured between the power transistors' gate and source pins, and is not measured directly from the driver OUTA and OUTB pins.

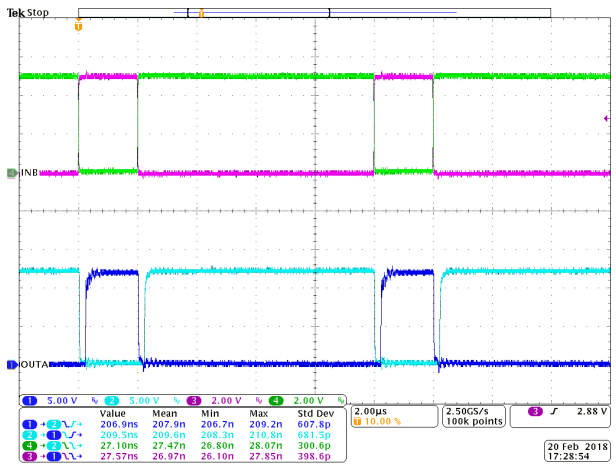


Figure 10-5. Bench Test Waveform for INA/B and OUTA/B

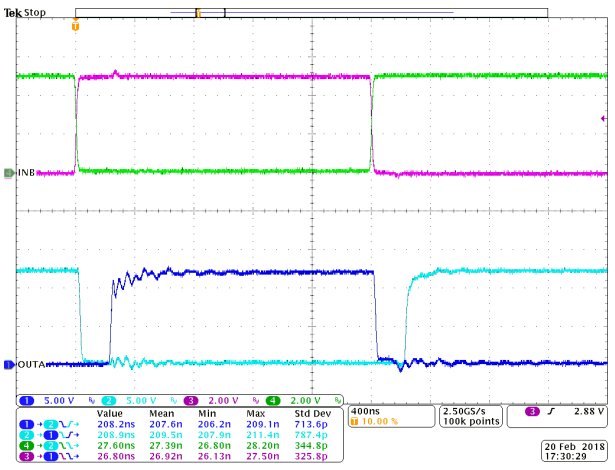


Figure 10-6. Zoomed-In bench-test waveform

11 Power Supply Recommendations

The recommended input supply voltage (VCCI) for the UCC21540-Q1 is between 3 V and 5.5 V. The output bias supply voltage (VDDA/VDDB) ranges from 6.0 V to 18 V. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. VDD and VCCI must not fall below their respective UVLO thresholds during normal operation. (For more information on UVLO see Section 9.3.1). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by the UCC21540-Q1. The recommended maximum VDDA/VDDB is 18 V.

A local bypass capacitor should be placed between the VDD and VSS pins, to supply current when the output goes high into a capacitive load. This capacitor should be positioned as close to the device as possible to minimize parasitic impedance. A low ESR, ceramic surface mount capacitor is recommended. If the bypass capacitor impedance is too large, resistive and inductive parasitics could cause the supply voltage seen at the IC pins to dip below the UVLO threshold unexpectedly. To filter high frequency noise between VDD and VSS, it can be helpful to place a second capacitor with lower impedance at higher frequency. As an example, the primary bypass capacitor could be 1 µF, with a secondary high frequency bypass capacitor of 100 nF.

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC21540-Q1, this bypass capacitor has a minimum recommended value of 100 nF.

12 Layout

12.1 Layout Guidelines

Consider these PCB layout guidelines for in order to achieve optimum performance for the UCC21540-Q1.

12.1.1 Component Placement Considerations

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin in bridge configurations, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- To improve noise immunity when driving the DIS pin from a distant micro-controller or high impedance source, TI recommends adding a small bypass capacitor, ≥ 1000 pF, between the DIS pin and GND.
- If the dead time feature is used, TI recommends placing the programming resistor R_{DT} and bypassing capacitor close to the DT pin of the UCC21540-Q1 to prevent noise from unintentionally coupling to the internal dead time circuit. The capacitor should be ≥ 2.2 nF.

12.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical loop area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

12.1.3 High-Voltage Considerations

- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the isolation performance.
- For half-bridge or high-side/low-side configurations, maximize the clearance distance of the PCB layout between the high and low-side PCB traces. The DWK package has pin12 and pin13 removed and has a minimum 3.3mm creepage distance which allows higher bus voltage.

12.1.4 Thermal Considerations

- A large amount of power may be dissipated by the UCC21540-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high (refer to Section 10.2.2.6 for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB (see Figure 12-2 and Figure 12-3). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. Ensure that no traces or copper from different high-voltage planes overlap.

12.2 Layout Example

Figure 12-1 shows a 2-layer PCB layout example with the signals and key components labeled for the SOIC-14 DW package, which has Pin 12 and Pin 13 removed. For more detailed information, please refer to the UCC21540EVM design - "Using the UCC21540EVM - TI"

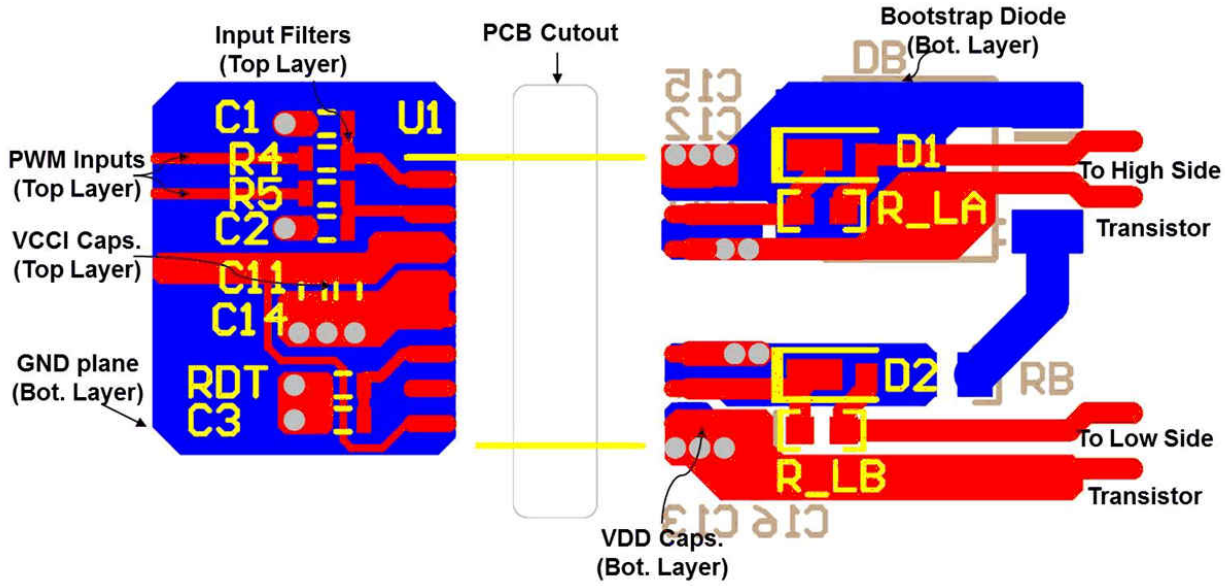


Figure 12-1. Layout Example

Figure 12-2 and Figure 12-3 shows top and bottom layer traces and copper.

Note

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

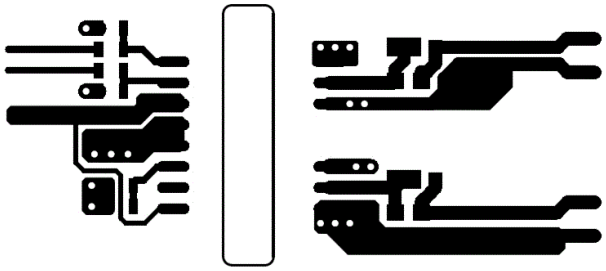


Figure 12-2. Top Layer Traces and Copper

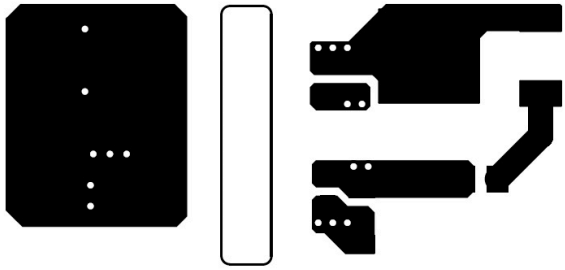


Figure 12-3. Bottom Layer Traces and Copper (Flipped)

Figure 12-4 and Figure 12-5 are 3-D layout pictures with top view and bottom views.

Note

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

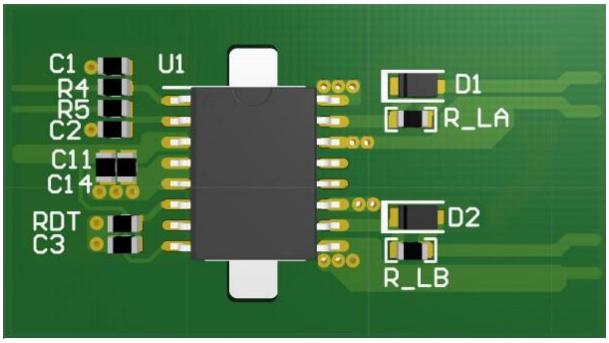


Figure 12-4. 3-D PCB Top View

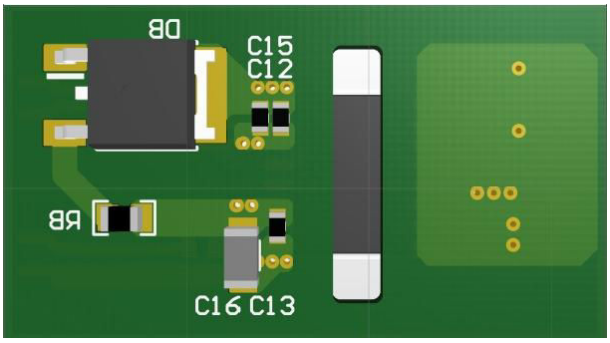


Figure 12-5. 3-D PCB Bottom View

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the Isolation Glossary

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC21540AQDWKRQ1	ACTIVE	SOIC	DWK	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21540AQ	Samples
UCC21540QDWKRQ1	ACTIVE	SOIC	DWK	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21540Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC21540-Q1, UCC21540A-Q1 :

- Catalog: UCC21540, UCC21540A

NOTE: Qualified Version Definitions:

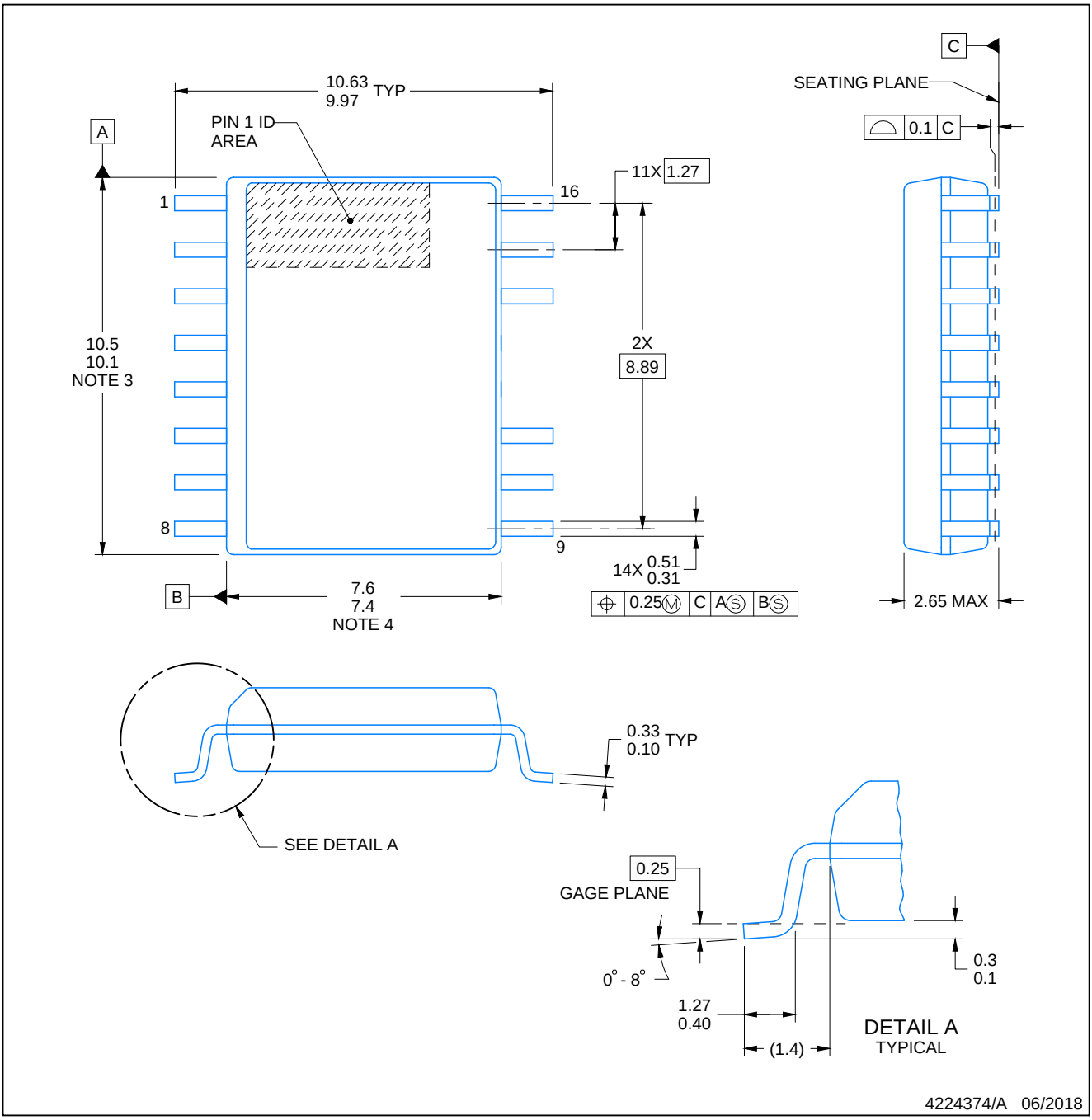
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DWK0014A

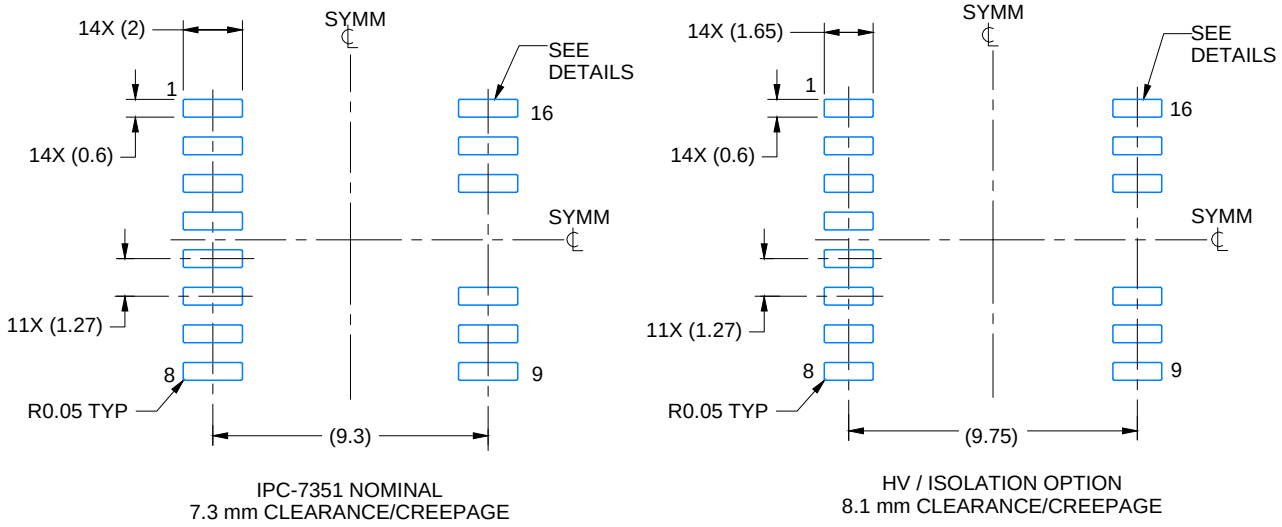
SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

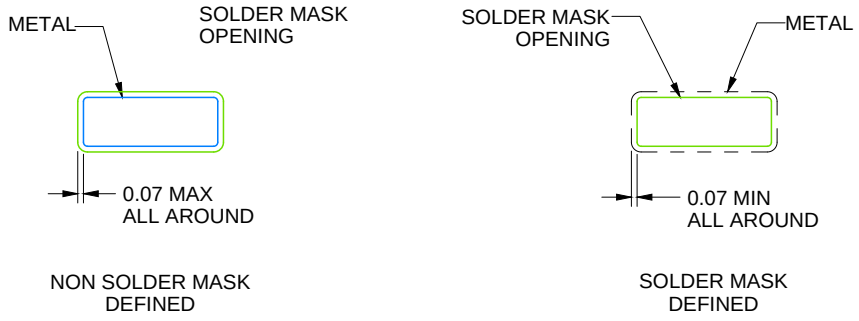


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

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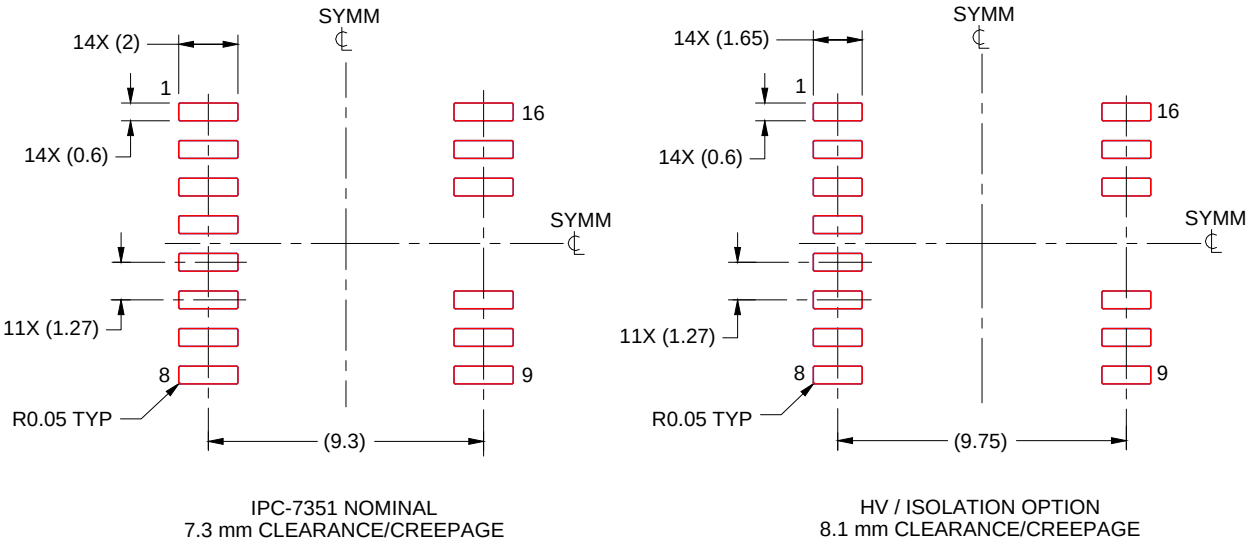
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4224374/A 06/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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