TEXAS INSTRUMENTS

SN75ALS174A
SLLS122F – JULY 1991 – REVISED JANUARY 2018

SN75ALS174A Quadruple Differential Line Driver

1 Features

- Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and RS-485
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for up to 20-Mbit/s Operation in Both Serial and Parallel Applications
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply Current Requirements 55 mA Max
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity: 60 mA
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Functionally Interchangeable With SN75174

2 Applications

- Motor Drives
- Factory Automation and Control

3 Description

The SN75ALS174A is a quadruple line driver with tri-state differential outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485. This device is optimized for balanced multipoint bus transmission at rates of up to 20 Mbit/s.

Each driver features wide positive and negative common-mode output voltage ranges that make them suitable for party-line applications in noisy environments.

The SN75ALS174A provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

The SN75ALS174A is characterized for operation from 0°C to 70°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75ALS174A	PDIP (N) (16)	19.3 mm x 6.50 mm
	SOIC (DW) (20)	12.8 mm x 7.50 mm
	TSSOP (PW) (20)	6.50 mm x 4.40 mm

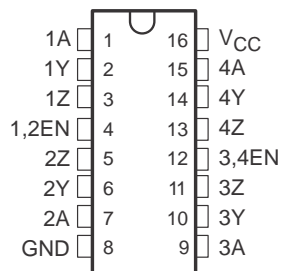(1) For all available packages, see the orderable addendum at the end of the data sheet.

Function Table
(each driver)[1] [2]

INPUT A	ENABLES	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant.

(2) Z = high impedance (off)

N Package
(Top View)

1A	1	16	V_CC
1Y	2	15	4A
1Z	3	14	4Y
1,2EN	4	13	4Z
2Z	5	12	3,4EN
2Y	6	11	3Z
2A	7	10	3Y
GND	8	9	3A

DW, PW Package
(Top View)

1A	1	20	V_CC
1Y	2	19	4A
NC	3	18	4Y
1Z	4	17	NC
1,2EN	5	16	4Z
2Z	6	15	3,4EN
NC	7	14	3Z
2Y	8	13	NC
2A	9	12	3Y
GND	10	11	3A
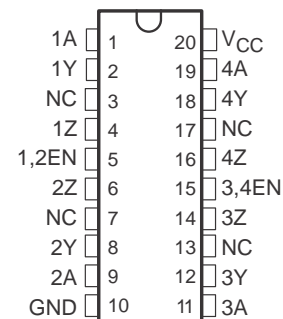
NC – No internal connection

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 1998) to Revision F   **Page**

- Added the PW package, *Applications* list, *Device Information* table, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

Product Folder Links: *SN75ALS174A*

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage, V_{CC}[2]		7	V
Input voltage, V_I		7	V
Output voltage range, V_O	−9	14	V
Continuous total dissipation	See the *Dissipation Rating* table		
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network GND.

5.2 Dissipation Rating Table

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	596 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OC}	Common-mode output voltage			12	V
				−7	V
I_{OH}	High-level output current			−60	mA
I_{OL}	Low-level output current			60	mA
T_A	Operating free-air temperature	0		70	°C

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$|V_{OD1}|$	Differential output voltage	$I_O = 0$		1.5		6	V
$|V_{OD2}|$	Differential output voltage	$R_L = 100$ Ω	See Note Figure 1	1/2 V_{OD1} or 2[2]			V
		$R_L = 54$ Ω		1.5	2.5	5	V
$|V_{OD3}|$	Differential output voltage	See [3]		1.5		5	V
$\Delta|V_{OD}|$	Change in magnitude of differential output voltage[4]	$R_L = 54$ Ω or 100 Ω	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage[5]	$R_L = 54$ Ω or 100 Ω	See Figure 1			3	V
						−1	V
$\Delta|V_{OC}|$	Change in magnitude of common-mode output voltage[4]	$R_L = 54$ Ω or 100 Ω	See Figure 1			±0.2	V
I_O	Output current with power off	$V_{CC} = 0$, $V_O = -7$ V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V				±100	µA
I_{IH}	High-level input current	$V_I = 2.7$ V				20	µA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−100	µA
I_{OS}	Short-circuit output current	$V_O = -7$ V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		16	30	mA

(1) All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
(2) The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
(3) See EIA Standard RS-485, Figures 3-5, Test Termination Measurement 2.
(4) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(5) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

5.5 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), $C_L = 50$ pF

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54$ Ω, See Figure 2	9	15	22	ns
t_{PZH}	Output enable time to high level	$R_L = 110$ Ω, See Figure 3	30	45	70	ns
t_{PZL}	Output enable time to low level	$R_L = 110$ Ω, See Figure 4	25	40	65	ns
t_{PHZ}	Output disable time from high level	$R_L = 110$ Ω, See Figure 3	10	20	35	ns
t_{PLZ}	Output disable time from low level	$R_L = 110$ Ω, See Figure 4	10	30	45	ns

6 Parameter Measurement Information
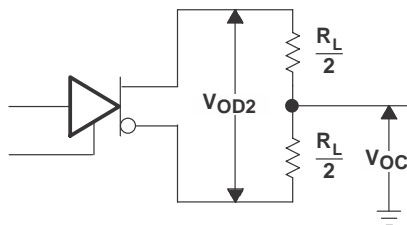
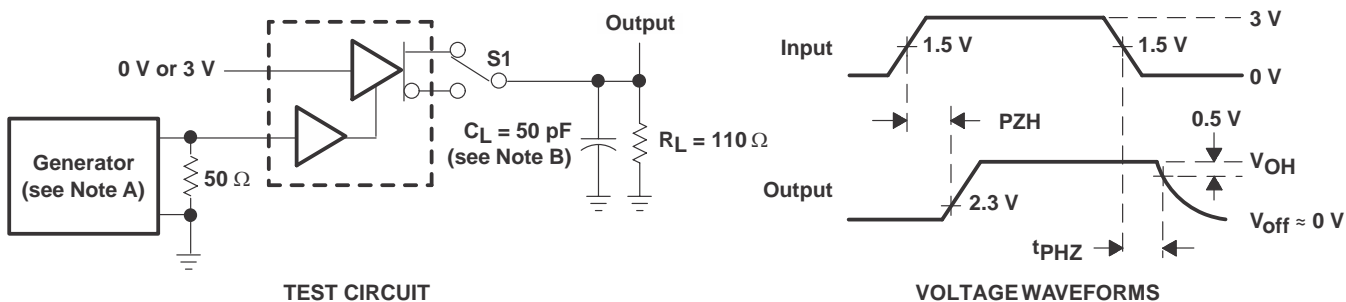Copyright © 2018, Texas Instruments Incorporated

Figure 1. Differential and Common-Mode Output Voltages
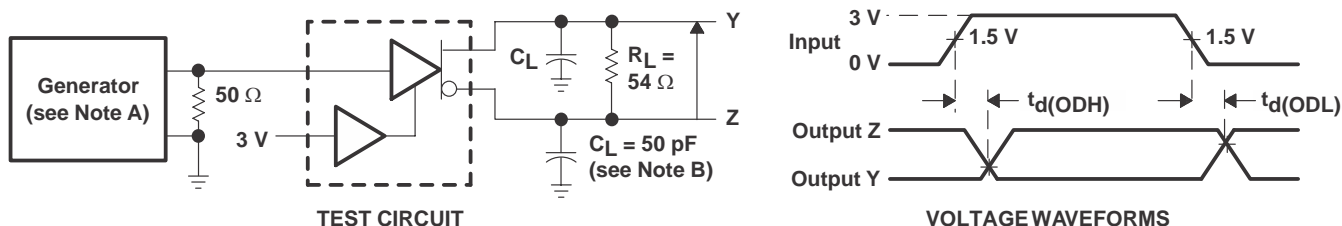
Copyright © 2018, Texas Instruments Incorporated

A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, t_f 5 ns, t_r 5 ns.

B. C_L includes probe and stray capacitance.

Figure 2. Differential-Output Test Circuit and Delay and Transition Times Voltage Waveforms
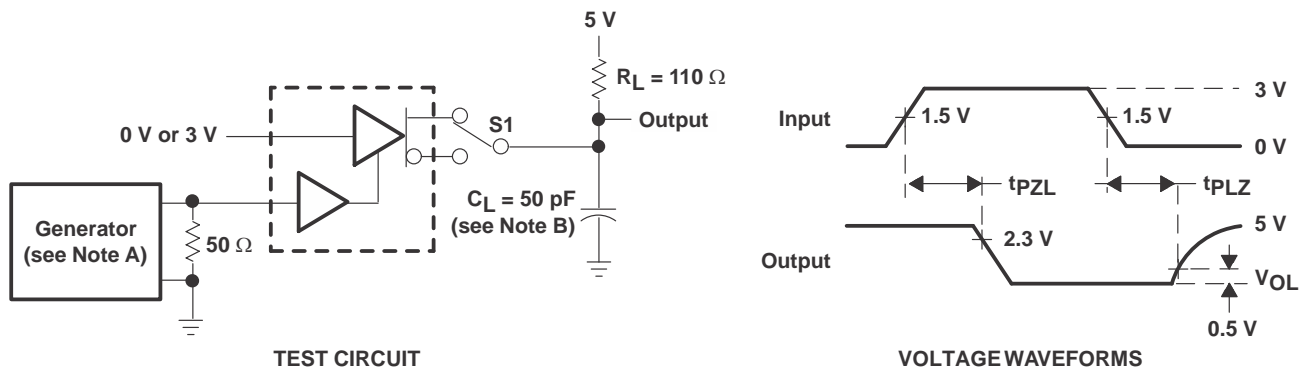

Copyright © 2018, Texas Instruments Incorporated

A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, t_f 5 ns, t_r 5 ns.

B. C_L includes probe and stray capacitance.

**Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}**

Parameter Measurement Information (continued)

TEST CIRCUIT

VOLTAGE WAVEFORMS

Copyright © 2018, Texas Instruments Incorporated

A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, t_f 5 ns, t_r 5 ns.
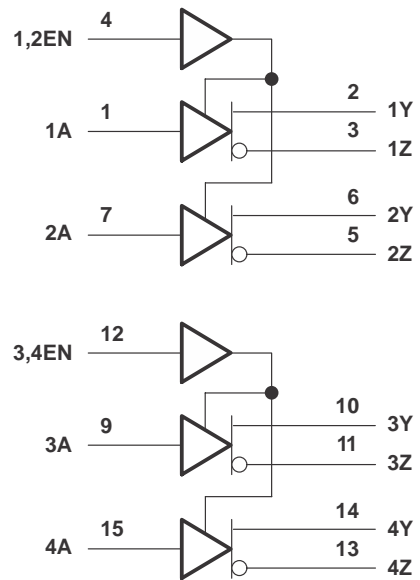
B. C_L includes probe and stray capacitance.

Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}
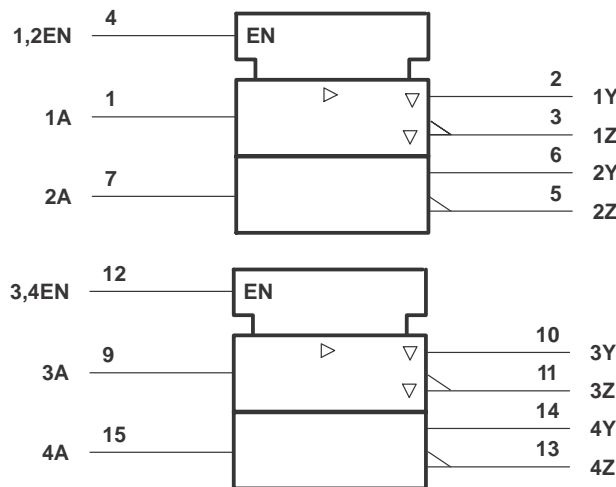
(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

(2) Pin numbers shown are for the N package.
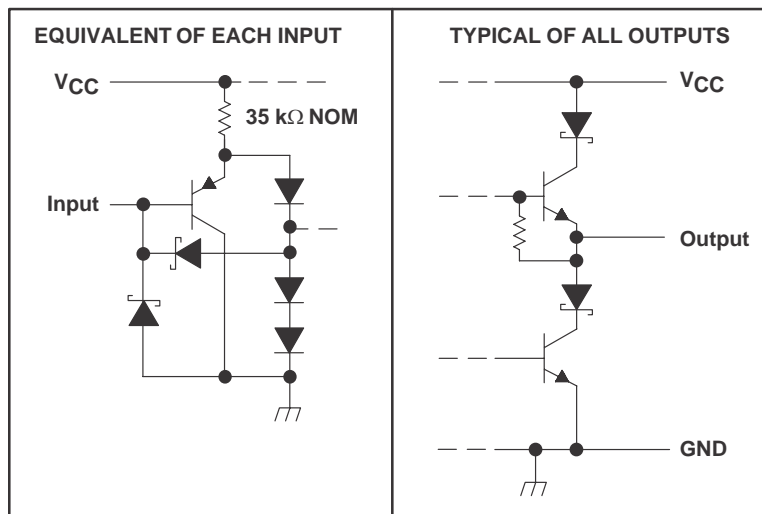
Figure 5. Logic Symbol

Product Folder Links: *SN75ALS174A*

Parameter Measurement Information (continued)

(1) Pin numbers shown are for the N package.

Figure 6. Logic Diagram (Positive Logic)

Copyright © 2018, Texas Instruments Incorporated

Figure 7. Schematics of Inputs and Outputs

7 Device and Documentation Support

7.1 Documentation Support

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS174ADW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	
SN75ALS174ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
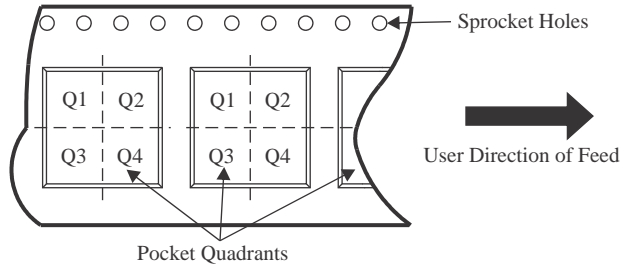
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width		
B0	Dimension designed to accommodate the component length		
K0	Dimension designed to accommodate the component thickness		
W	Overall width of the carrier tape		
P1	Pitch between successive cavity centers		

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS174ADWR	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE

T - Tube
height

L - Tube length

W - Tube
width

B - Alignment groove width
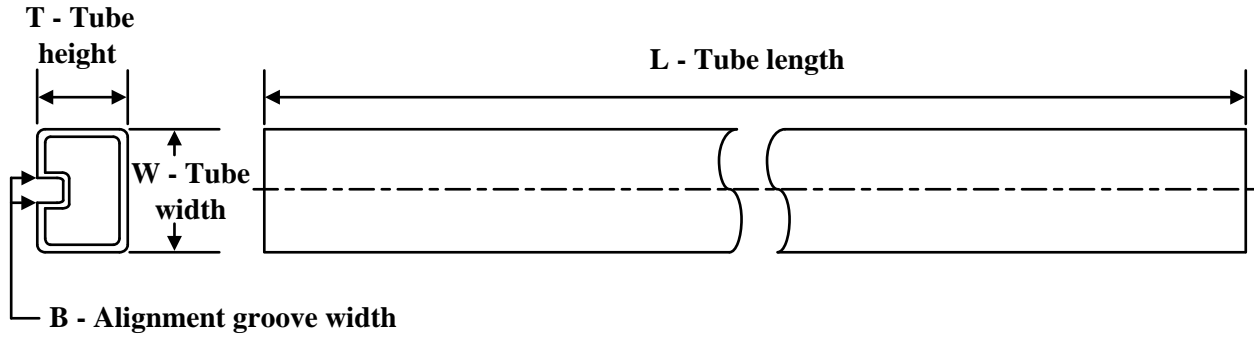
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS174ADW	DW	SOIC	20	25	506.98	12.7	4826	6.6

SEATING PLANE

C

⬠ 0.1 C

10.63 / 9.97 TYP

PIN 1 ID AREA

A

1

18X 1.27

20

13.0 / 12.6 NOTE 3

2X 11.43

10

11

20X 0.51 / 0.31

B

7.6 / 7.4 NOTE 4

⊕ 0.25 Ⓜ C A B

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25

GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

TEXAS INSTRUMENTS
www.ti.com

20X (2)

SYMM
¢

1

20

20X (0.6)

18X (1.27)

SYMM
¢

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10   11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER