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FAIRCHILD™

August 2014

FCD5N60 / FCU5N60

N-Channel SuperFET® MOSFET

600 V, 4.6 A, 950 mΩ

Features

- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 810 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 16 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 32 pF)
- 100% Avalanche Tested
- RoHS Compliant

Application

- LCD/LED TV and Monitor
- Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.
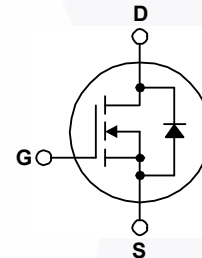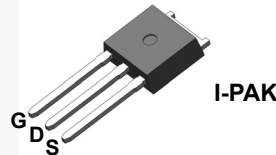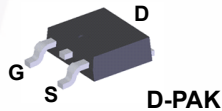
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FCD5N60TM FCD5N60TM_WS FCU5N60TU	Unit
V_{DSS}	Drain to Source Voltage			600	V
I_D	Drain Current	- Continuous (T_C = 25°C)		4.6	A
		- Continuous (T_C = 100°C)		2.9	
I_{DM}	Drain Current	- Pulsed	(Note 1)	13.8	A
V_{GSS}	Gate to Source Voltage			±30	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	159	mJ
I_{AR}	Avalanche Current		(Note 1)	4.6	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	5.4	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)		54	W
		- Derate Above 25°C		0.43	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	FCD5N60TM FCD5N60TM_WS FCU5N60TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	83	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD5N60TM	FCD5N60	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FCD5N60TM_WS	FCD5N60	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FCU5N60TU	FCU5N60	IPAK	Tube	N/A	N/A	75 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA, T_C = 25°C	600	-	-	V
		V_{GS} = 0 V, I_D = 250 µA, T_C = 150°C	-	650	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	-	0.6	-	V/°C
BV_{DS}	Drain to Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 4.6 A	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 480 V, T_C = 125°C	-	-	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2.3 A	-	0.81	0.95	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 2.3 A	-	3.8	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	-	470	600	pF
C_{oss}	Output Capacitance		-	250	320	pF
C_{rss}	Reverse Transfer Capacitance		-	22	-	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	-	12	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	32	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 4.6 A, V_{GS} = 10 V, R_G = 25 Ω	-	12	30	ns
t_r	Turn-On Rise Time		-	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		-	47	95	ns
t_f	Turn-Off Fall Time	(Note 4)	-	22	55	ns
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 480 V, I_D = 4.6 A, V_{GS} = 10 V	-	16	-	nC
Q_{gs}	Gate to Source Gate Charge		-	2.8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	7	-	nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4.6	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	13.8	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 4.6 A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 4.6 A, dI_F/dt = 100 A/µs	-	295	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.7	-	µC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.

2. I_{AS} = 2.3 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25℃.

3. $I_{SD} \leq$ 4.6 A, di/dt $\leq$ 200 A/µs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25℃.

4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics
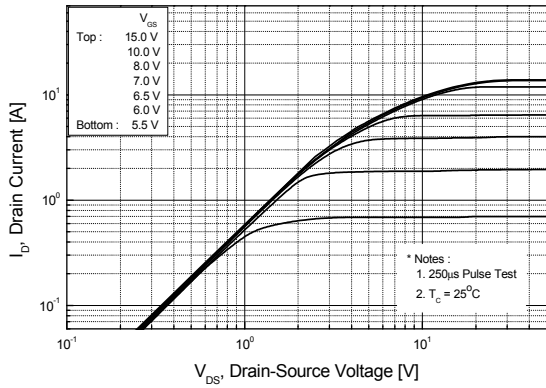
Figure 1. On-Region Characteristics

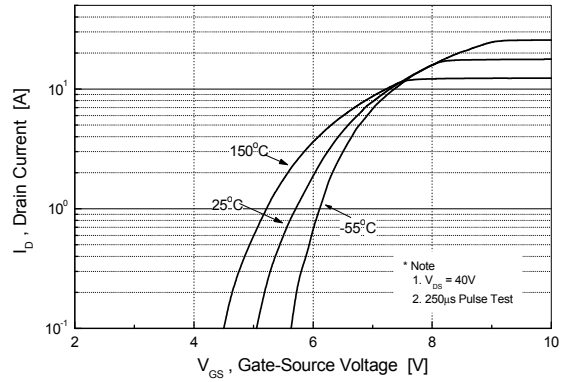**Figure 2. Transfer Characteristics**

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage
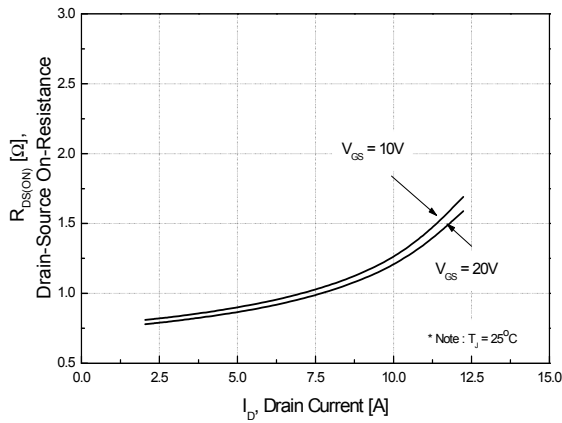

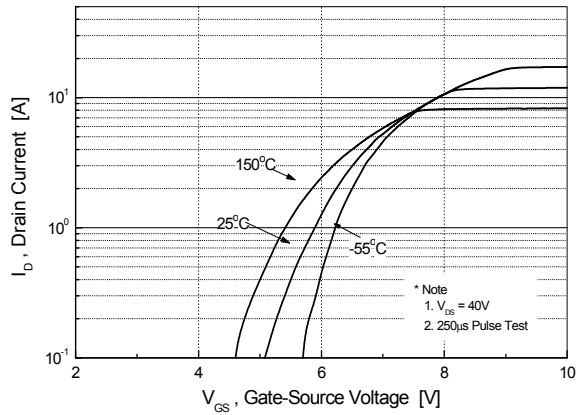**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue**
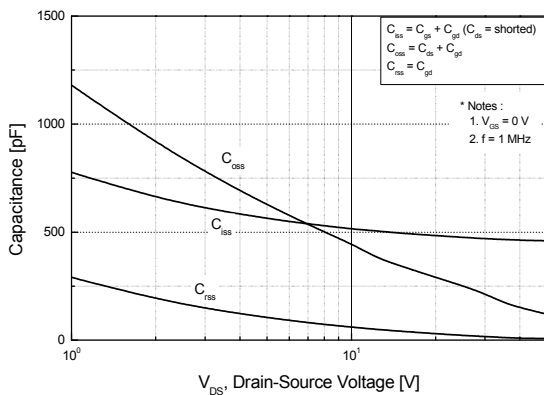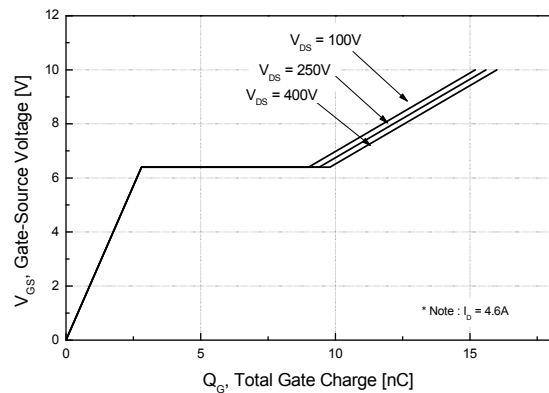

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

Typical Performance Characteristics (Continued)
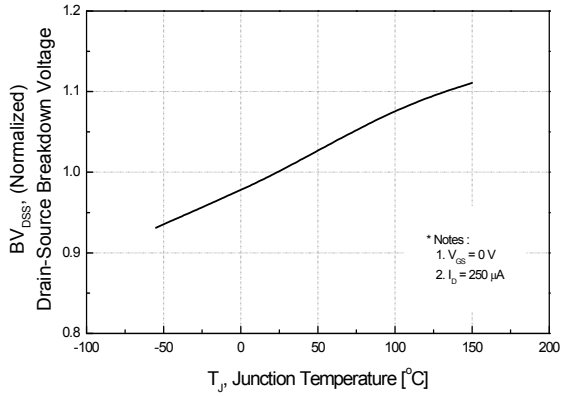
Figure 7. Breakdown Voltage Variation vs. Temperature

* Notes :
1. V_{GS} = 0 V
2. I_D = 250 μA

Y-axis: BV_{DSS}, (Normalized) Drain-Source Breakdown Voltage
X-axis: T_J, Junction Temperature [°C]

Figure 8. On-Resistance Variation vs. Temperature

* Notes :
1. V_{GS} = 10 V
2. I_D = 2.3 A

Y-axis: $R_{DS(ON)}$, (Normalized) Drain-Source On-Resistance
X-axis: T_J, Junction Temperature [°C]
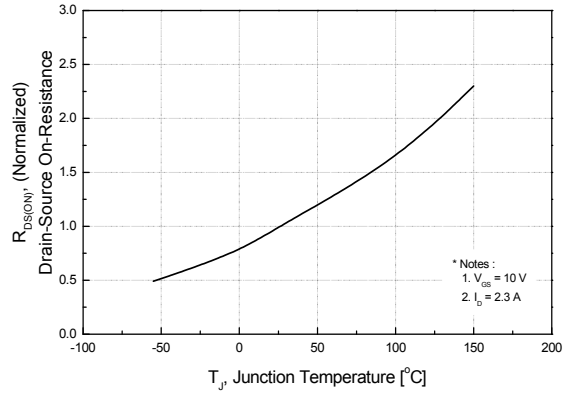
Figure 9. Maximum Safe Operating Area

Operation in This Area is Limited by $R_{DS(on)}$

10 us
100 us
1 ms
10 ms
100 ms
DC

* Notes :
1. T_C = 25 °C
2. T_J = 150 °C
3. Single Pulse

Y-axis: I_D, Drain Current [A]
X-axis: V_{DS}, Drain-Source Voltage [V]
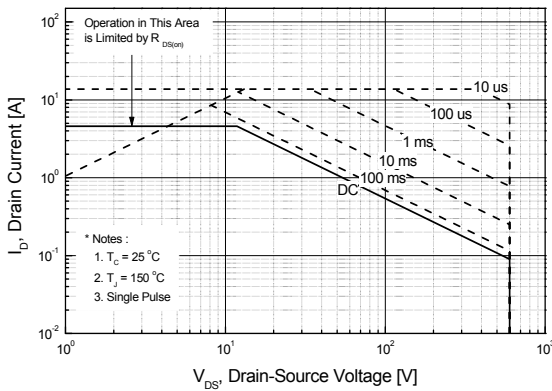
Figure 10. Maximum Drain Current vs. Case Temperature

Y-axis: I_D, Drain Current [A]
X-axis: T_C, Case Temperature [°C]
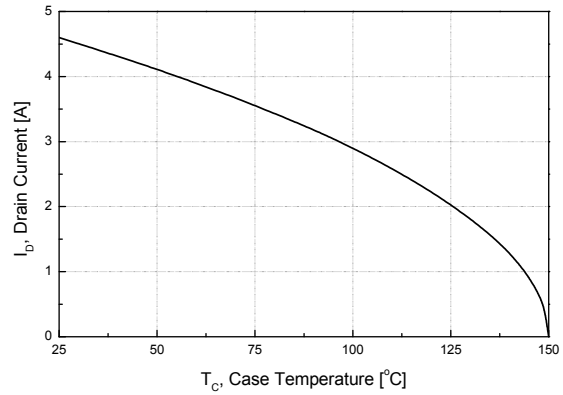
Figure 11. Transient Thermal Response Curve

D = 0.5
0.2
0.1
0.05
0.02
0.01
single pulse

* Notes :
1. $Z_{\theta JC}(t)$ = 2.3 °C/W Max.
2. Duty Factor, D = t_1/t_2
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

P_{DM}
t_1
t_2

Y-axis: $Z_{\theta JC}(t)$, Thermal Response [°C/W]
X-axis: t_1, Square Wave Pulse Duration [sec]
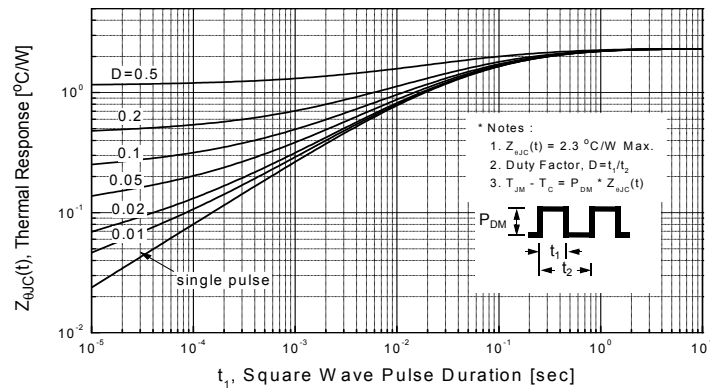
Figure 12. Gate Charge Test Circuit & Waveform

Figure 13. Resistive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \ \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{Gate\ Pulse\ Width}{Gate\ Pulse\ Period}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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