

## FEATURES

Ultralow on resistance ( $R_{DS(on)}$ )

50 m $\Omega$  @ 3.6 V

55 m $\Omega$  @ 2.5 V

65 m $\Omega$  @ 1.8 V

100 m $\Omega$  @ 1.2 V

Input voltage range: 1.1 V to 3.6 V

1.1 A maximum continuous operating current

Low enable control logic threshold can be operated from  
1.2 V to 3.3 V

Low 1  $\mu$ A (typical) ground current @ 1.8 V

Low 4  $\mu$ A (maximum) reverse current @ 3.6 V

Ultralow shutdown current: 0.7  $\mu$ A (typical) @ 1.8 V

Reverse current blocking

Tiny 4-ball wafer level chip scale package (WLCSP)

1.0 mm  $\times$  1.0 mm, 0.5 mm pitch

Tiny 6-lead lead frame chip scale package (LFCSP)

2.0 mm  $\times$  2.0 mm  $\times$  0.55 mm, 0.65 mm pitch

## APPLICATIONS

Mobile phones

Digital cameras and audio devices

GPS devices

Personal media players

Portable and battery-powered equipment

## TYPICAL APPLICATIONS CIRCUIT

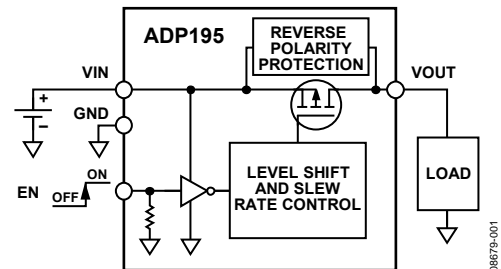


Figure 1.

## GENERAL DESCRIPTION

The ADP195 is a high-side load switch designed for operation between 1.1 V to 3.6 V and protected against reverse current flow from output to input. This load switch provides power domain isolation helping extended power domain isolation. The device contains a low on-resistance, P-channel MOSFET that supports over 1.1 A of continuous current and minimizes power loss. The low 1  $\mu$ A of quiescent current and ultralow shutdown current make the ADP195 ideal for battery-operated portable equipment. The built-in level shifter for enable logic makes the ADP195 compatible with many processors and GPIO controllers.

In addition to operating performance, the ADP195 occupies minimal printed circuit board (PCB) space with an area of less than 1.0 mm<sup>2</sup> and a height of 0.60 mm.

It is available in an ultrasmall 1 mm  $\times$  1 mm, 4-ball, 0.5 mm pitch WLCSP. A 6-lead 2 mm  $\times$  2 mm  $\times$  0.55 mm, 0.65 mm pitch LFCSP is also available.

## Rev. C

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## REVISION HISTORY

### 1/12—Rev. B to Rev. C

Changes to General Description Section .....	1
Changes to Table 2 .....	4
Updated Outline Dimensions .....	12

### 2/11—Rev. A to Rev. B

Added 6-Lead LFCSP .....	Universal
Changes to Features, Applications, and General Description Sections .....	1
Added $V_{IN}$ to $V_{OUT}$ Resistance, LFCSP Parameter, Table 1 .....	3
Changes to Table 2 and Table 3 .....	4
Added Figure 4; Renumbered Sequentially .....	5
Added Table 5; Renumbered Sequentially .....	5
Added Figure 6, Figure 8, and Figure 10 .....	6
Changes to Theory of Operation Section .....	9
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	12

### 7/10—Rev. 0 to Rev. A

Changes to Features and Applications Sections .....	1
Changed 10 $\mu$ A Ground Current to 1 $\mu$ A Ground Current in General Description Section .....	1
Changes to Table 2 and Thermal Resistance Section .....	4
Added Thermal Data Section .....	4

### 3/10—Revision 0: Initial Version

## SPECIFICATIONS

$V_{IN} = 1.8\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 200\text{ mA}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	$V_{IN}$	$T_J = -40^\circ\text{C to } +85^\circ\text{C}$	1.1		3.6	V
EN INPUT						
EN Input Threshold	$V_{IH}$	$1.1\text{ V} \leq V_{IN} < 1.8\text{ V}$ , $T_J = -40^\circ\text{C to } +85^\circ\text{C}$ $1.8\text{ V} \leq V_{IN} \leq 3.6\text{ V}$ , $T_J = -40^\circ\text{C to } +85^\circ\text{C}$	0.29		1.0	V
EN Input Pull-Down Current	$I_{EN}$	$V_{IN} = 1.8\text{ V}$		500		nA
$V_{IN}$ Shutdown Current		$V_{EN} = 0\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{OUT} = 3.6\text{ V}$		-10		nA
REVERSE BLOCKING						
$V_{OUT}$ Current		$V_{EN} = 0\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{OUT} = 3.6\text{ V}$		4		$\mu\text{A}$
Hysteresis		$ V_{IN} - V_{OUT} $		75		mV
CURRENT						
Ground Current	$I_{GND}$	$V_{OUT} = 0$ , includes $V_{EN}$ pull-down and reverse blocking bias current, $V_{IN} = 3.6\text{ V}$ , $T_J = -40^\circ\text{C to } +85^\circ\text{C}$			10	$\mu\text{A}$
		$V_{OUT} = 0$ , includes $V_{EN}$ pull-down and reverse blocking bias current, $V_{IN} = 1.8\text{ V}$		1		$\mu\text{A}$
Off State Current	$I_{OFF}$	$V_{EN} = \text{GND}$ (includes reverse blocking bias current), $V_{OUT} = 0\text{ V}$ $V_{EN} = \text{GND}$ , $T_J = -40^\circ\text{C to } +85^\circ\text{C}$ , $V_{OUT} = 0\text{ V}$		0.7		$\mu\text{A}$
					5	$\mu\text{A}$
$V_{IN}$ to $V_{OUT}$ RESISTANCE	$R_{DS(ON)}$					
WLCSP		$V_{IN} = 3.6\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 3.6\text{ V}$		0.050		$\Omega$
		$V_{IN} = 2.5\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 2.5\text{ V}$		0.055		$\Omega$
		$V_{IN} = 1.8\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 1.8\text{ V}$		0.065		$\Omega$
		$V_{IN} = 1.8\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 1.8\text{ V}$ , $T_J = -40^\circ\text{C to } +85^\circ\text{C}$			0.095	$\Omega$
		$V_{IN} = 1.5\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 1.5\text{ V}$		0.075		$\Omega$
		$V_{IN} = 1.2\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 1.2\text{ V}$		0.100		$\Omega$
LFCSP		$V_{IN} = 3.6\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 3.6\text{ V}$		0.070		$\Omega$
		$V_{IN} = 2.5\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 2.5\text{ V}$		0.078		$\Omega$
		$V_{IN} = 1.8\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 1.8\text{ V}$		0.090		$\Omega$
		$V_{IN} = 1.8\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 1.8\text{ V}$ , $T_J = -40^\circ\text{C to } +85^\circ\text{C}$			0.130	$\Omega$
		$V_{IN} = 1.5\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 1.5\text{ V}$		0.097		$\Omega$
		$V_{IN} = 1.2\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 1.2\text{ V}$		0.125		$\Omega$
$V_{OUT}$ TURN-ON DELAY TIME						
Turn-On Delay Time	$t_{ON\_DLY}$	$V_{IN} = 1.8\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 1.8\text{ V}$ , $C_{LOAD} = 1\text{ }\mu\text{F}$ $V_{IN} = 3.6\text{ V}$ , $I_{LOAD} = 200\text{ mA}$ , $V_{EN} = 3.6\text{ V}$ , $C_{LOAD} = 1\text{ }\mu\text{F}$		5		$\mu\text{s}$
				1.5		$\mu\text{s}$

## TIMING DIAGRAM

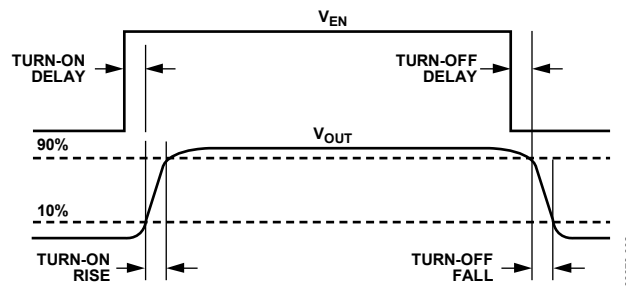


Figure 2. Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, VIN1, VIN2 to GND	−0.3 V to +4.0 V
VOUT, VOUT1, VOUT2 to GND	−0.3 V to +4.0 V
EN to GND	−0.3 V to +4.0 V
Continuous Drain Current	
$T_A = 25^\circ\text{C}$	±2 A
$T_A = 85^\circ\text{C}$	±1.1 A
Continuous Diode Current	−50 mA
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Operating Ambient Temperature Range	−40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP195 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that  $T_J$  is within the specified temperature limits. In applications with high power dissipation and poor PCB thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature ( $T_J$ ) of the device is dependent on the ambient temperature ( $T_A$ ), the power dissipation of the device ( $P_D$ ), and the junction-to-ambient thermal resistance of the package ( $\theta_{JA}$ ).

Maximum junction temperature ( $T_J$ ) is calculated from the ambient temperature ( $T_A$ ) and power dissipation ( $P_D$ ) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of  $\theta_{JA}$  may vary, depending on PCB material, layout, and environmental conditions. The specified values of  $\theta_{JA}$  are based on a 4-layer, 4 inch × 3 inch PCB. See JESD51-7 and JESD51-9 for detailed information regarding board construction. For additional information, see the AN-617 application note, *MicroCSP™ Wafer Level Chip Scale Package*.

$\Psi_{JB}$  is the junction-to-board thermal characterization parameter with units of °C/W.  $\Psi_{JB}$  of the package is based on modeling and calculation using a 4-layer board. The JESD51-12 document, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances.  $\Psi_{JB}$  measures the component power flowing through multiple thermal paths rather than through a single path, as in thermal resistance ( $\theta_{JB}$ ). Therefore,  $\Psi_{JB}$  thermal paths include convection from the top of the package as well as radiation from the package, factors that make  $\Psi_{JB}$  more useful in real-world applications. Maximum junction temperature ( $T_J$ ) is calculated from the board temperature ( $T_B$ ) and the power dissipation ( $P_D$ ) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8, JESD51-9, and JESD51-12 for more detailed information about  $\Psi_{JB}$ .

### THERMAL RESISTANCE

$\theta_{JA}$  and  $\Psi_{JB}$  are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	$\theta_{JA}$	$\Psi_{JB}$	Unit
4-Ball, 0.5 mm Pitch WLCSF	260	58.4	°C/W
6-Lead, 2 mm × 2 mm LFCSP	72.1	24.0	°C/W

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

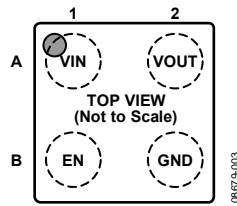
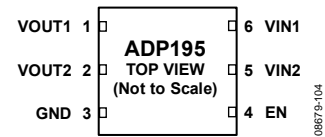


Figure 3. 4-Ball WLCSP Pin Configuration



### NOTES

1. THE EXPOSED PAD MUST BE CONNECTED TO GND.

Figure 4. 6-Lead LFCSP Pin Configuration

Table 4. WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VIN	Input Voltage.
A2	VOUT	Output Voltage.
B1	EN	Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.
B2	GND	Ground.

Table 5. LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VOUT1	Output Voltage. Connect VOUT1 and VOUT2 together.
2	VOUT2	Output Voltage. Connect VOUT1 and VOUT2 together.
3	GND	Ground.
4	EN	Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.
5	VIN2	Input Voltage. Connect VIN1 and VIN2 together.
6	VIN1	Input Voltage. Connect VIN1 and VIN2 together.
EP	EP	The exposed pad must be connected to ground.

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 1.8\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

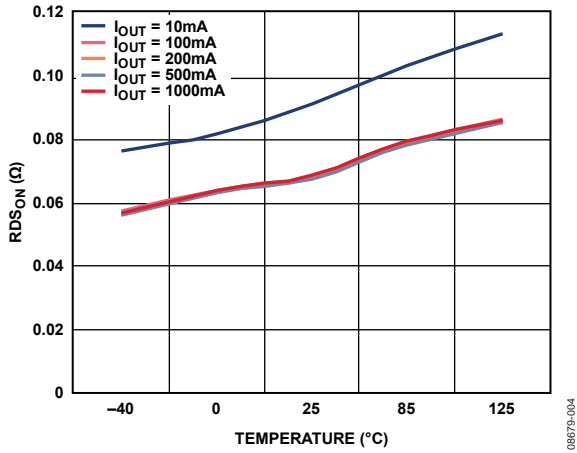


Figure 5.  $R_{DS(on)}$  vs. Temperature, WLCSPP

08679-004

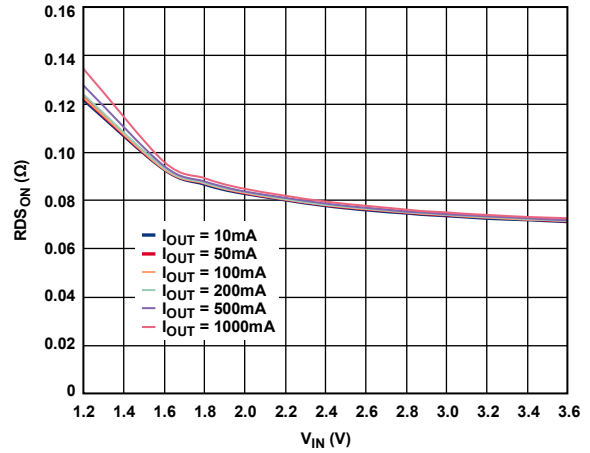


Figure 8.  $R_{DS(on)}$  vs. Input Voltage ( $V_{IN}$ ), LFCSP

08679-108

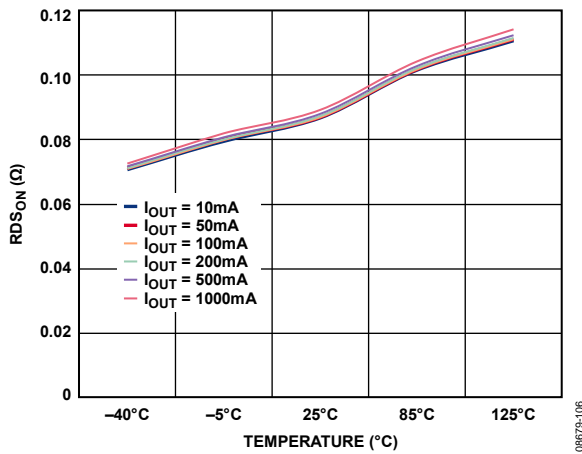


Figure 6.  $R_{DS(on)}$  vs. Temperature, LFCSP

08679-106

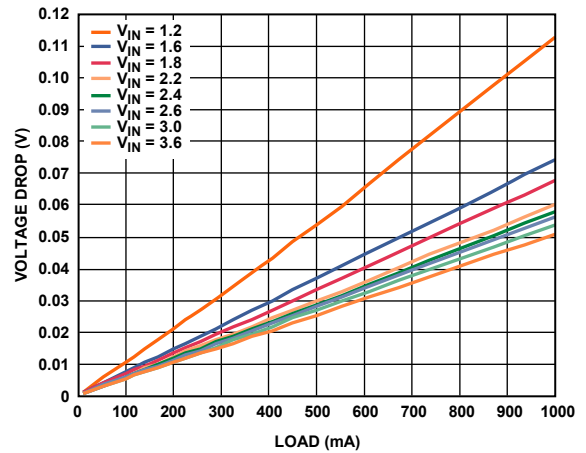


Figure 9. Voltage Drop vs. Load Current, WLCSPP

08679-006

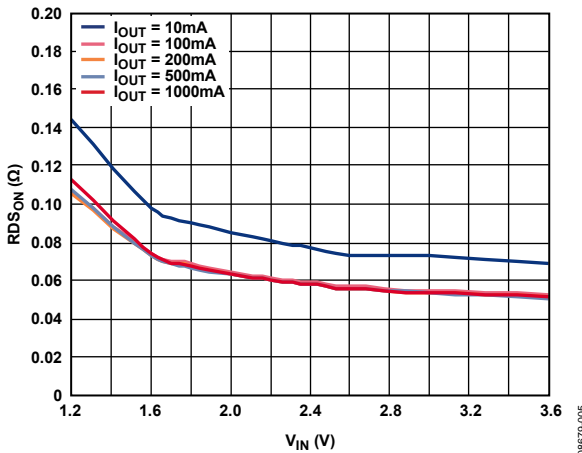


Figure 7.  $R_{DS(on)}$  vs. Input Voltage ( $V_{IN}$ ), WLCSPP

08679-005

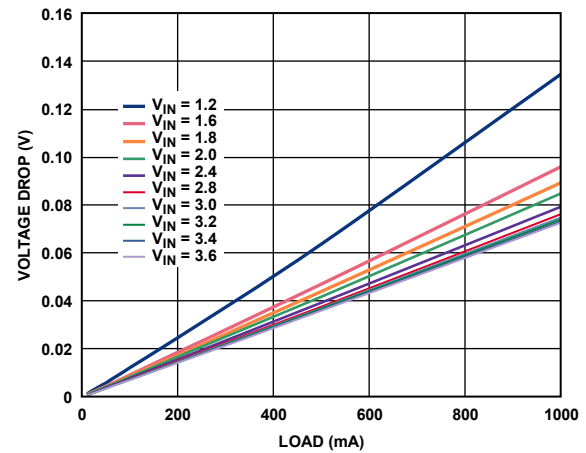


Figure 10. Voltage Drop vs. Load Current, LFCSP

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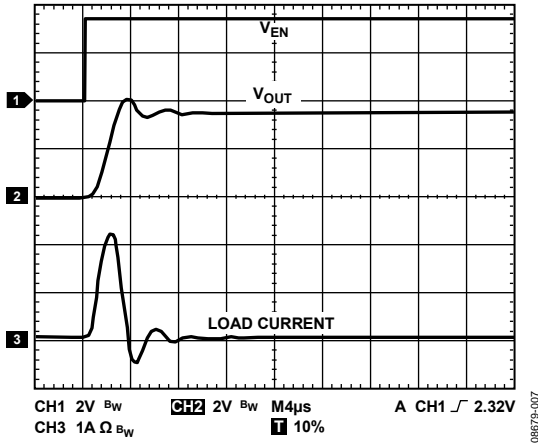


Figure 11. Typical Rise Time and Inrush Current,  $V_{IN} = 3.6\text{ V}$ , No Load

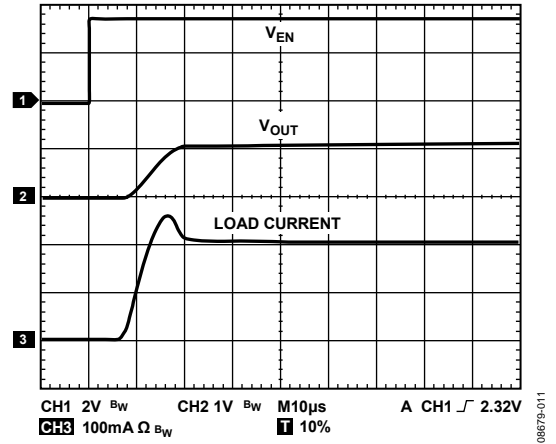


Figure 14. Typical Rise Time and Inrush Current,  $V_{IN} = 1.2\text{ V}$ , Load = 200 mA

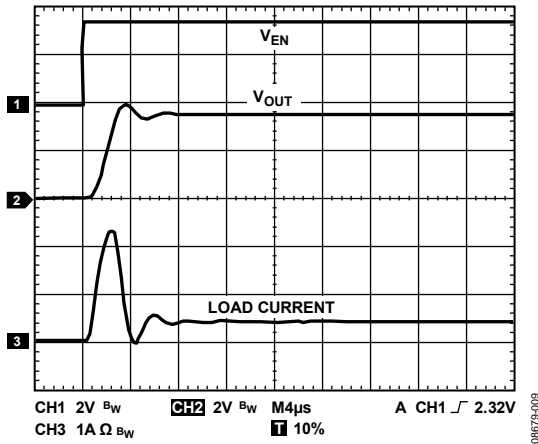


Figure 12. Typical Rise Time and Inrush Current,  $V_{IN} = 3.6\text{ V}$ , Load = 200 mA

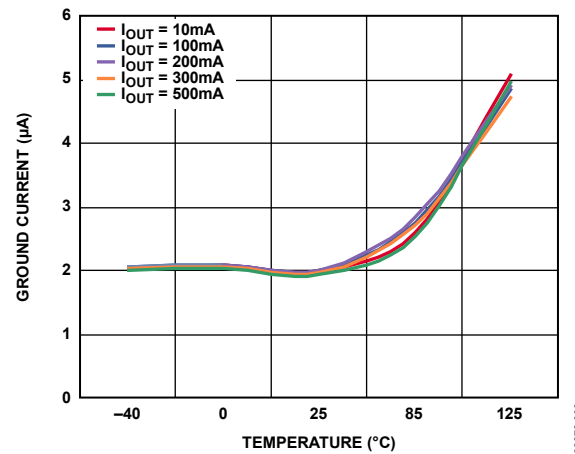


Figure 15. Ground Current vs. Temperature

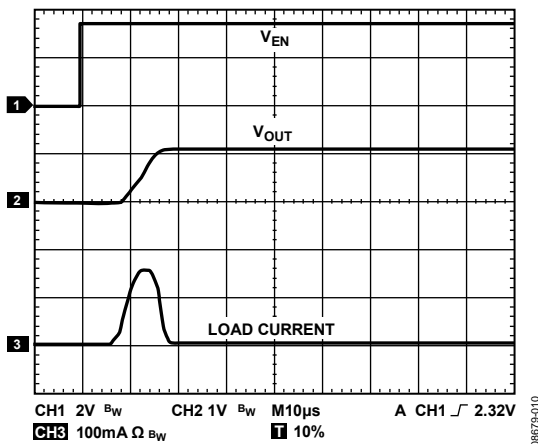


Figure 13. Typical Rise Time and Inrush Current,  $V_{IN} = 1.2\text{ V}$ , No Load

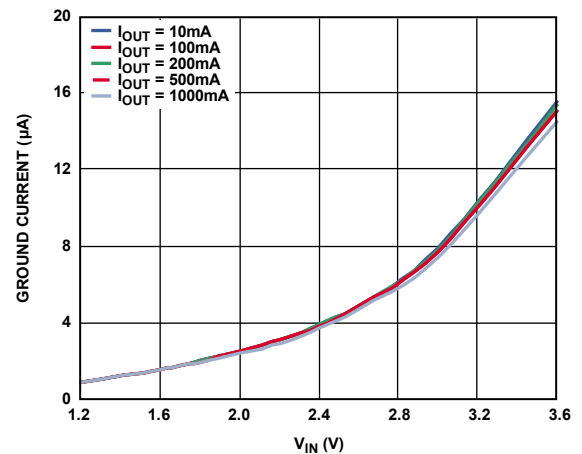


Figure 16. Ground Current vs. Input Voltage ( $V_{IN}$ )

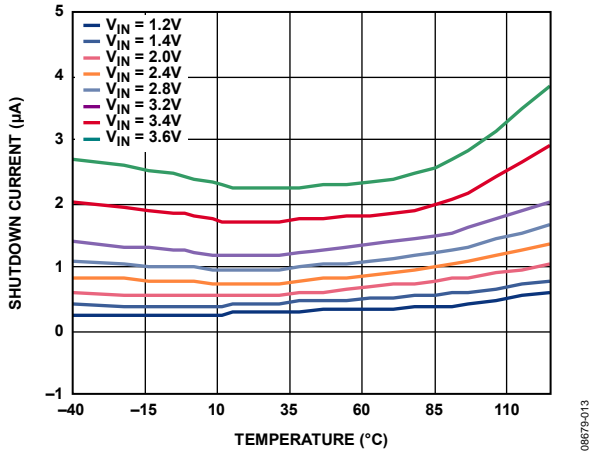


Figure 17. Shutdown Current vs. Temperature

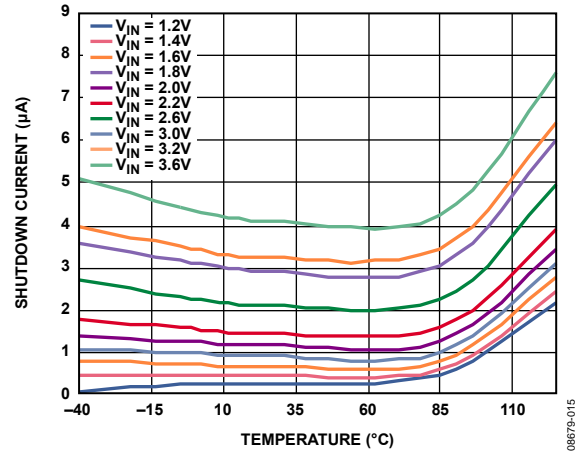


Figure 19. Reverse Output Shutdown Current vs. Temperature

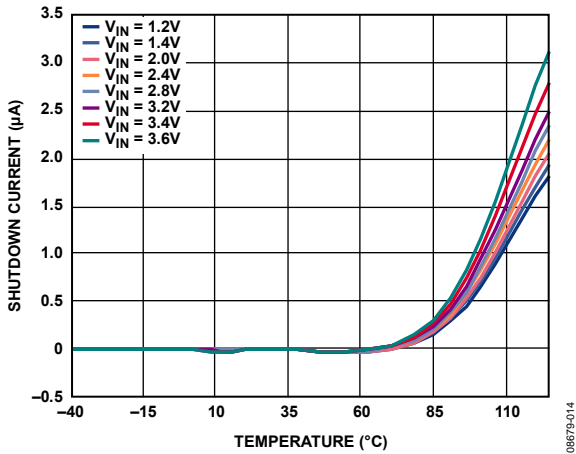


Figure 18. Reverse Input Shutdown Current vs. Temperature

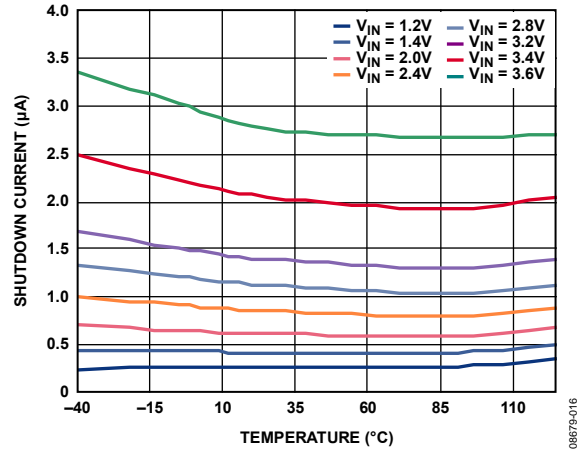


Figure 20. Reverse Shutdown Current vs. Temperature



## THEORY OF OPERATION

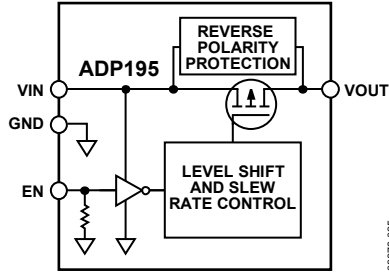


Figure 21. Functional Block Diagram

The ADP195 is a high-side PMOS load switch. It is designed for supply operation between 1.1 V to 3.6 V. The PMOS load switch is designed for low on resistance, 65 m $\Omega$  at  $V_{IN} = 1.8$  V and supports greater than 1 A of continuous current. It is a low

quiescent current device with a nominal 4 M $\Omega$  pull-down resistor on its enable pin (EN).

The reverse current protection circuitry prevents current flow backward through the ADP195 when the output voltage is greater than the input voltage. A comparator senses the difference between the input and output voltages. When the difference between the input voltage and output voltage exceeds 75 mV, the body of the pFET is switched to  $V_{OUT}$  and is turned off or opened; that is, the gate is connected to  $V_{OUT}$ .

The packaging is a space-saving 1.0 mm  $\times$  1.0 mm, 4-ball WLCSP. The ADP195 is also available in a 2 mm  $\times$  2 mm  $\times$  0.55 mm, 0.65 mm pitch LFCSP.

## APPLICATIONS INFORMATION

### GROUND CURRENT

The major source for ground current in the ADP195 is an internal 4 MΩ pull-down on the enable pin. Figure 22 shows the typical ground current when  $V_{EN} = V_{IN}$  and varies from 1.2 V to 3.6 V.

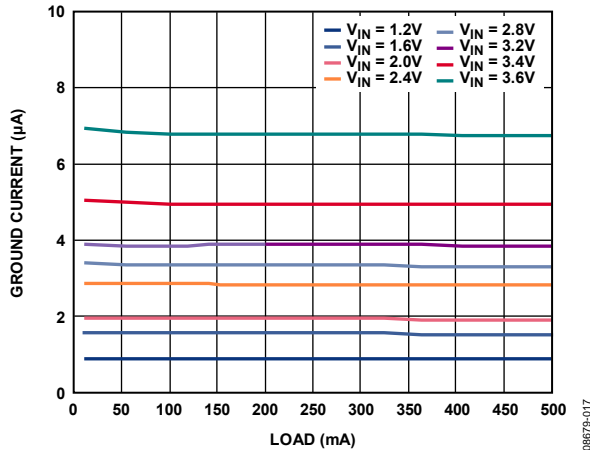


Figure 22. Ground Current vs. Load Current

As shown in Figure 23, an increase in quiescent current can occur when  $V_{EN} \neq V_{IN}$ . This is caused by the CMOS logic nature of the level shift circuitry as it translates an  $V_{EN}$  signal  $\geq 1.2$  V to a logic high. This increase is a function of the  $V_{IN} - V_{EN}$  delta.

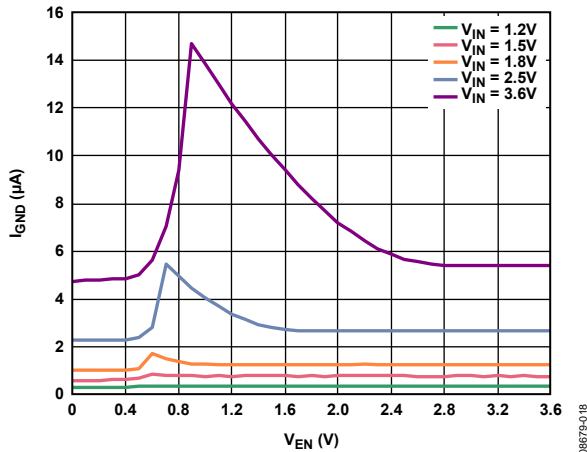


Figure 23. Typical Ground Current when  $V_{EN} \neq V_{IN}$

### ENABLE FEATURE

The ADP195 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 24, when a rising voltage on  $V_{EN}$  crosses the active threshold,  $V_{OUT}$  turns on. When a falling voltage on  $V_{EN}$  crosses the inactive threshold,  $V_{OUT}$  turns off.

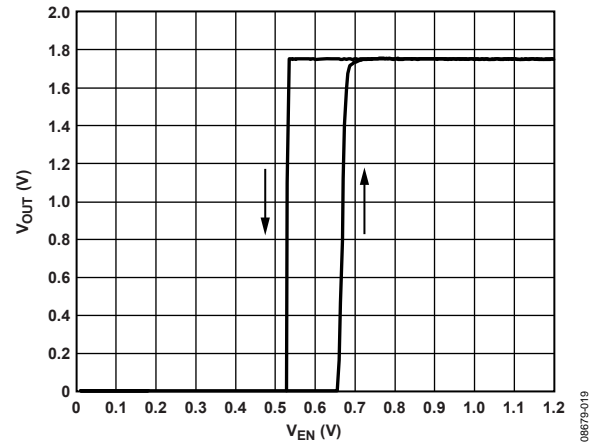


Figure 24. Typical EN Operation

As shown in Figure 24, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds derive from the  $V_{IN}$  voltage; therefore, these thresholds vary with the changing input voltage. Figure 25 shows the typical EN active/inactive thresholds when the input voltage varies from 1.2 V to 3.6 V.

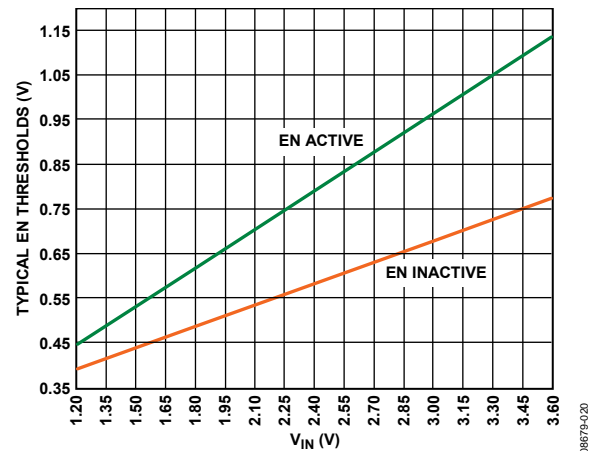


Figure 25. Typical EN Thresholds vs. Input Voltage ( $V_{IN}$ )

**TIMING**

Turn-on delay is defined as the delta between the time that  $V_{EN}$  reaches  $>1.2\text{ V}$  until  $V_{OUT}$  rises to  $\sim 10\%$  of its final value. The ADP195 includes circuitry to have typical  $5\text{ }\mu\text{s}$  turn-on delay at  $3.6\text{ V } V_{IN}$  to limit the  $V_{IN}$  inrush current. As shown in Figure 26, the turn-on delay is dependent on the input voltage.

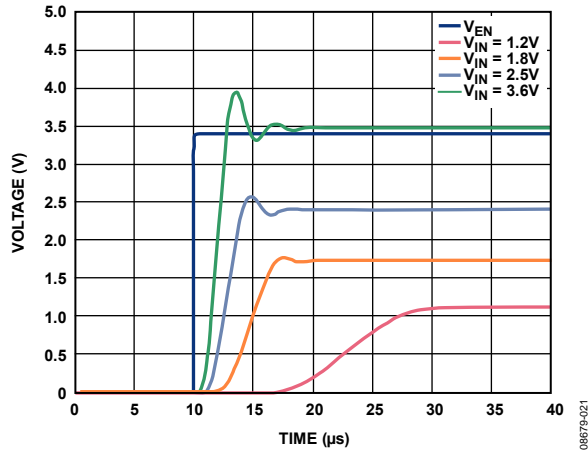


Figure 26. Typical Turn-On Delay Time with Varying Input Voltage

The rise time is defined as the delta between the time from 10% to 90% of  $V_{OUT}$  reaching its final value. It is dependent on the RC time constant where  $C = \text{load capacitance } (C_{LOAD})$  and  $R = R_{DS(ON)} || R_{LOAD}$ . Because  $R_{DS(ON)}$  is usually smaller than  $R_{LOAD}$ , an adequate approximation for RC is  $R_{DS(ON)} \times C_{LOAD}$ . An input or load capacitor is not needed for the ADP195; however, capacitors can be used to suppress noise on the board. If significant load capacitance is connected, inrush current is a concern.

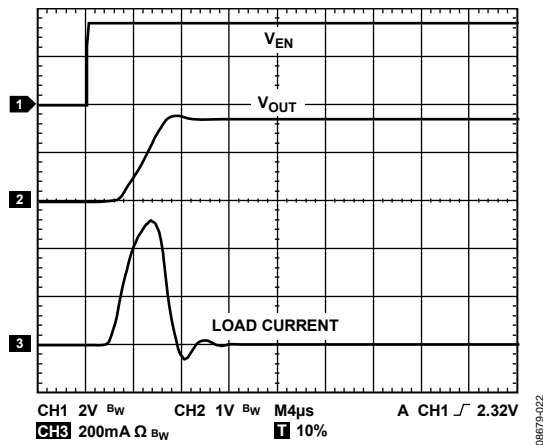


Figure 27. Typical Rise Time and Inrush Current,  $C_{LOAD} = 1\text{ }\mu\text{F}$ ,  $V_{IN} = 1.8\text{ V}$ , No Load

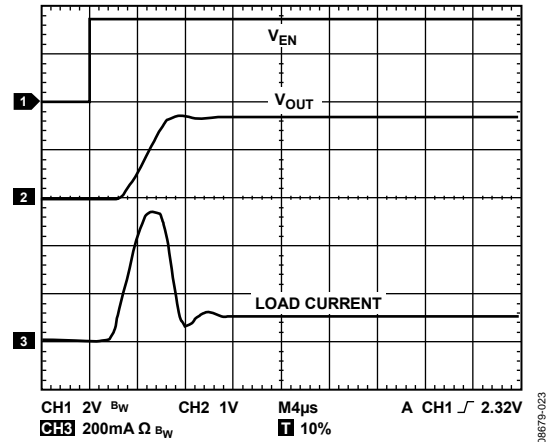


Figure 28. Typical Rise Time and Inrush Current,  $C_{LOAD} = 1\text{ }\mu\text{F}$ ,  $V_{IN} = 1.8\text{ V}$ , Load = 200 mA

The turn-off time is defined as the delta between the time from 90% to 10% of  $V_{OUT}$  reaching its final value. It is also dependent on the RC time constant.

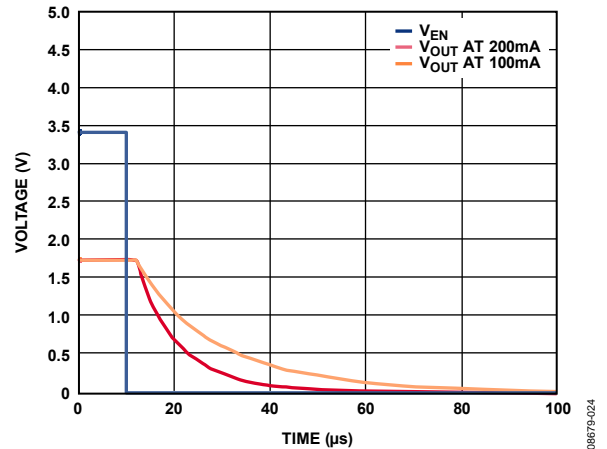


Figure 29. Typical Turn-Off Time

OUTLINE DIMENSIONS

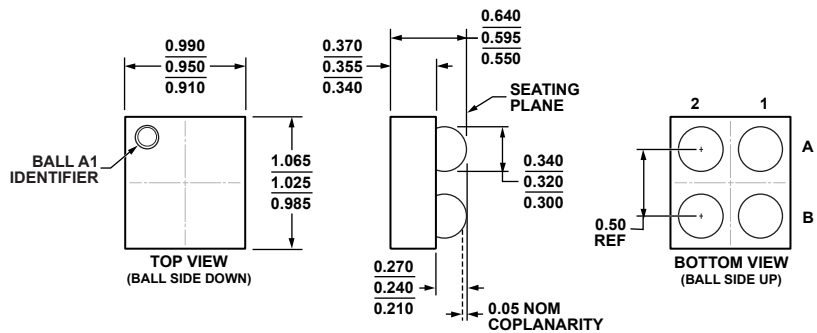


Figure 30. 4-Ball Wafer Level Chip Scale Package [WLCSP] (CB-4-4)

Dimensions shown in millimeters

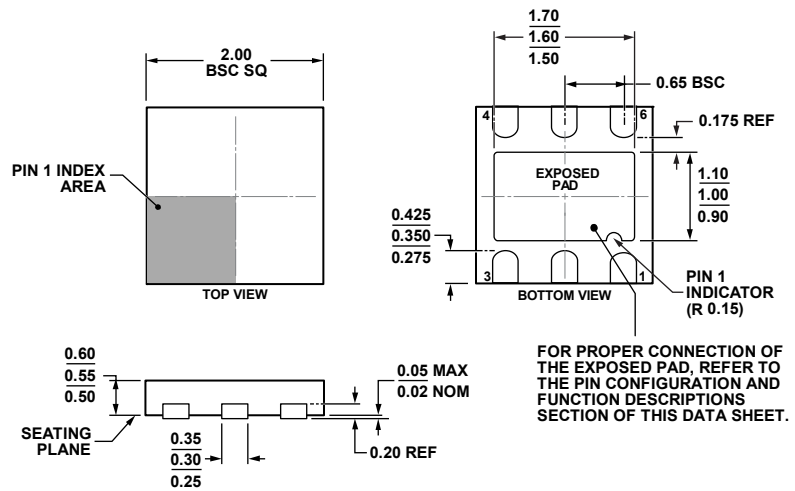


Figure 31. 6-Lead Lead Frame Chip Scale Package [LFCSP\_UD] 2.00 x 2.00 mm Body, Ultra Thin, Dual Lead (CP-6-3)

Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
ADP195ACBZ-R7	-40°C to +85°C	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-4	5Y
ADP195ACPZ-R7	-40°C to +85°C	6-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-6-3	LJ6
ADP195-EVALZ		Evaluation Board		
ADP195-CP-EVALZ		Evaluation Board		

<sup>1</sup> Z = RoHS Compliant Part.

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