# FAIRCHILD

SEMICONDUCTOR

# FST3253 Dual 4:1 Multiplexer/Demultiplexer Bus Switch

#### **General Description**

The Fairchild Switch FST3253 is a dual 4:1 high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When  $\overline{\text{OE}}$  is LOW, S<sub>0</sub> and S<sub>1</sub> connect the A Port to the selected B Port output. When  $\overline{\text{OE}}$  is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

#### Features

•  $4\Omega$  switch connection between two ports.

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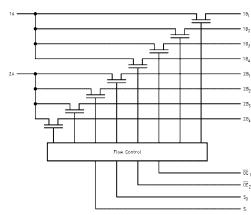
- Minimal propagation delay through the switch.
- Low I<sub>CC</sub>.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

### **Ordering Code:**

Order Number	Package Number	Package Description
FST3253M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
FST3253QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150 Wide
FST3253MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Device also available in	T 18 10 11	

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Logic Diagram



# Connection Diagram

OE 1	1	 16	— v <sub>cc</sub>
s <sub>1</sub> —	2	15	— 002
1 B <sub>4</sub> —	3	14	— s <sub>o</sub>
1B3 —	4	13	— 2B <sub>4</sub>
1B <sub>2</sub> —	5	12	— 2B <sub>3</sub>
1 B <sub>1</sub> —	6	11	— 2B <sub>2</sub>
1A —	7	10	— 2B <sub>1</sub>
GND —	8	9	<b>—</b> 2A

#### Pin Descriptions

Pin Name	Description
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enables
S <sub>0</sub> , S <sub>1</sub>	Select Inputs
A	Bus A
B <sub>1</sub> , B <sub>2</sub> , B <sub>3</sub> , B <sub>4</sub>	Bus B

#### **Truth Table**

Function	OE <sub>2</sub>	OE <sub>1</sub>	S <sub>0</sub>	S <sub>1</sub>
Disconnect 1A	Х	Н	Х	Х
Disconnect 2A	н	Х	Х	Х
$A = B_1$	L	L	L	L
$A = B_2$	L	L	н	L
$A = B_3$	L	L	L	н
$A = B_4$	L	L	н	н

#### Absolute Maximum Ratings(Note 1)

Supply Voltage (V <sub>CC</sub> )	-0.5V to +7.0V
DC Switch Voltage (V <sub>S</sub> )	-0.5V to +7.0V
DC Input Voltage (VIN)(Note 2)	-0.5V to +7.0V
DC Input Diode Current (I <sub>IK</sub> ) $V_{IN}$ <0V	–50mA
DC Output (I <sub>OUT</sub> ) Sink Current	128mA
DC V <sub>CC</sub> /GND Current (I <sub>CC</sub> /I <sub>GND</sub> )	+/- 100mA
Storage Temperature Range (T <sub>STG</sub> )	–65°C to +150 $^\circ\text{C}$

# Recommended Operating Conditions (Note 3)

Power Supply Operating (V <sub>CC)</sub>	4.0V to 5.5V
Input Voltage (V <sub>IN</sub> )	0V to 5.5V
Output Voltage (V <sub>OUT</sub> )	0V to 5.5V
Input Rise and Fall Time $(t_r, t_f)$	
Switch Control Input	0ns/V to 5ns/V
Switch I/O	0ns/V to DC
Free Air Operating Temperature (T <sub>A</sub> )	–40 °C to –85 °C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

### **DC Electrical Characteristics**

	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> =	-40 °C to +	85 °C	Units	
Symbol			Min	Typ (Note 4)	Мах		Conditions
V <sub>IK</sub>	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18 \text{mA}$
V <sub>IH</sub>	High Level Input Voltage	4.0-5.5	2.0			V	
V <sub>IL</sub>	Low Level Input Voltage	4.0-5.5			0.8	V	
l <sub>l</sub>	Input Leakage Current	5.5			±1.0	μA	0≤ V <sub>IN</sub> ≤5.5V
I <sub>OZ</sub>	OFF-STATE Leakage Current	5.5			±1.0	μA	$0 \leq A, B \leq V_{CC}$
R <sub>ON</sub>	Switch On Resistance	4.5		4	7	Ω	$V_{IN} = 0V, I_{IN} = 64mA$
	(Note 5)	4.5		4	7	Ω	$V_{IN} = 0V$ , $I_{IN} = 30mA$
		4.5		8	15	Ω	$V_{IN} = 2.4V, I_{IN} = 15mA$
		4.0		11	20	Ω	$V_{IN} = 2.4V, I_{IN} = 15mA$
I <sub>CC</sub>	Quiescent Supply Current	5.5			3	μA	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
Δ I <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V <sub>CC</sub> or GND

Note 4: Typical values are at  $V_{CC}$  = 5.0V and  $T_A$  = +25  $^\circ C$ 

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

## **AC Electrical Characteristics**

		$T_A = -40$ °C to +85 °C $C_L = 50$ pF, RU = RD = 500 $\Omega$						
Symbol	Parameter	$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$		Units	Conditions	Figure No.
		Min	Max	Min	Max			
t <sub>PHL</sub> ,t <sub>PLH</sub>	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V <sub>I</sub> = OPEN	Figure 1
	Prop Delay, Select to Bus A	1.0	5.3		6.3	115	Figur	Figure 2
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time, Select to Bus B	1.0	5.3		6.0	ns	$V_I = 7V$ for $t_{PZL}$	Figure 1 Figure 2
	Output Enable Time, I <sub>OE</sub> to Bus A, B	1.0	5.3		6.2	115	$V_I = OPEN$ for $t_{PZH}$	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time., Select to Bus B	1.0	5.8		6.2		$V_I = 7V$ for $t_{PLZ}$	Figure 1 Figure 2
	Output Disable Time, I <sub>OE</sub> to Bus A, B	1.0	5.5		6.2	ns	$V_I = OPEN \text{ for } t_{PHZ}$	

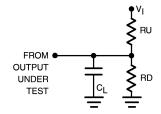
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

#### Capacitance (Note 7)

Symbol		Parameter	Тур	Max	Units	Conditions
CIN		Control Pin Input Capacitance	3		pF	$V_{CC} = 5.0V$
Cure	A Port	Input/Output Capacitance	13		pF	$V_{CC}, \overline{OE} = 5.0V$
C <sub>I/O</sub>	B Port	5		pF	VCC, OL = 0.0V	

Note 7:  $T_A = +25^{\circ}C$ , f = 1 MHz, Capacitance is characterized but not tested.

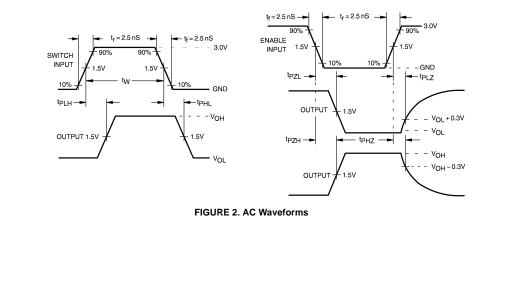
## AC Loading and Waveforms



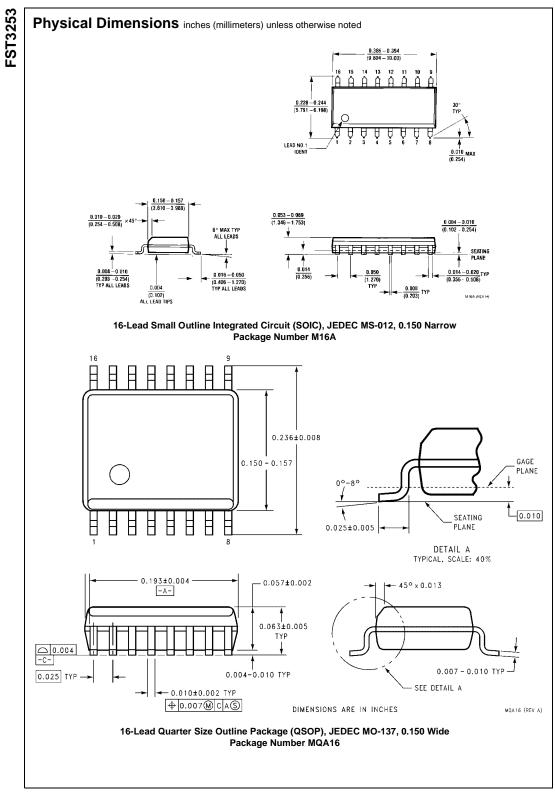
Note: Input driven by 50  $\Omega$  source terminated in 50  $\Omega$  Note: CL includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t<sub>W</sub> = 500 ns

#### FIGURE 1. AC Test Circuit



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