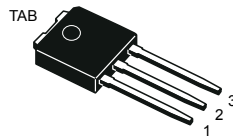
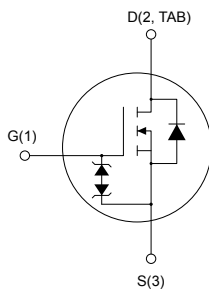


## N-channel 1050 V, 6 $\Omega$ typ., 1.5 A MDmesh K5 Power MOSFET in an IPAK package


**IPAK**


AM01476v1\_tab


**Product status link**
[STU2N105K5](#)
**Product summary**

<b>Order code</b>	STU2N105K5
<b>Marking</b>	2N105K5
<b>Package</b>	IPAK
<b>Packing</b>	Tube

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STU2N105K5	1050 V	8 $\Omega$	1.5 A

- Industry's lowest  $R_{DS(on)}$  x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	1.5	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	0.95	
$I_{DM}^{(1)}$	Drain current (pulsed)	6	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 1.5\text{ A}$ ,  $di/dt = 100\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ .
3.  $V_{DS} \leq 840\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	2.08	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	100	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)	0.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	90	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	1050			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 1050\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 1050\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			50	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 0.75\text{ A}$		6	8	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	115	-	pF
$C_{oss}$	Output capacitance		-	15	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(tr)}$ <sup>(1)</sup>	Equivalent output capacitance time related	$V_{DS} = 0\text{ to }840\text{ V}$ , $V_{GS} = 0\text{ V}$	-	17	-	pF
$C_{o(er)}$ <sup>(2)</sup>	Equivalent output capacitance energy related		-	6	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	20	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 840\text{ V}$ , $I_D = 1.5\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	10	-	nC
$Q_{gs}$	Gate-source charge		-	1.5	-	nC
$Q_{gd}$	Gate-drain charge		-	8	-	nC

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 525\text{ V}$ , $I_D = 0.75\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	14.5	-	ns
$t_r$	Rise time		-	8.5	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	35	-	ns
$t_f$	Fall time		-	38.5	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		1.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		6	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 1.5\text{ A}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	326		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	1.19		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	7.3		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	525		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	1.83		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	7		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

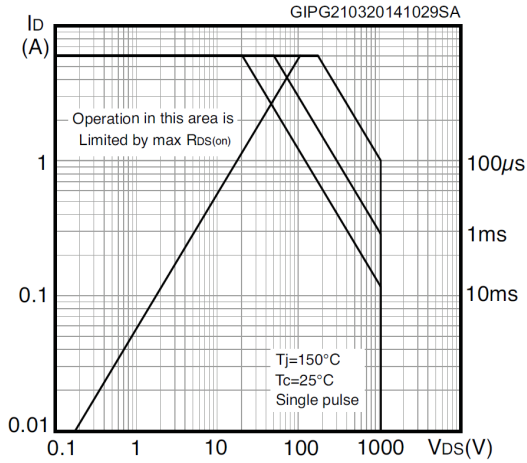


Figure 2. Normalized transient thermal impedance

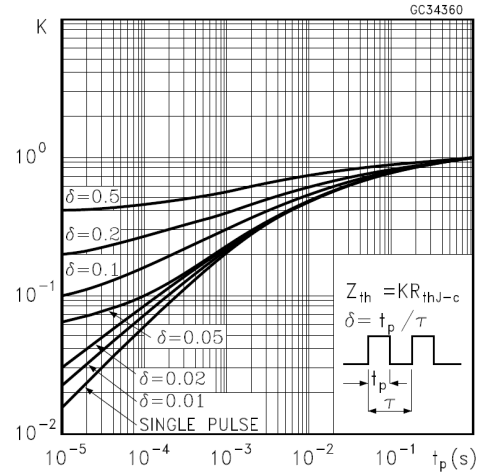


Figure 3. Typical output characteristics

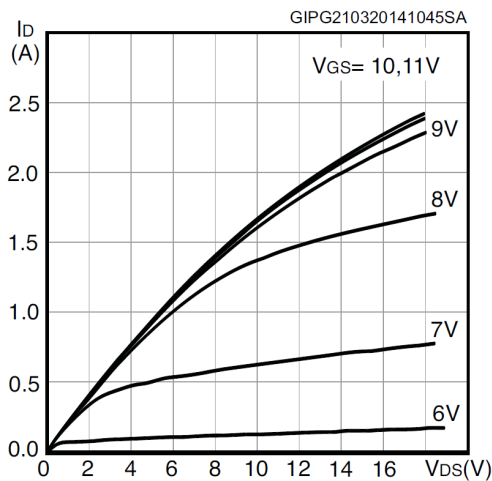


Figure 4. Typical transfer characteristics

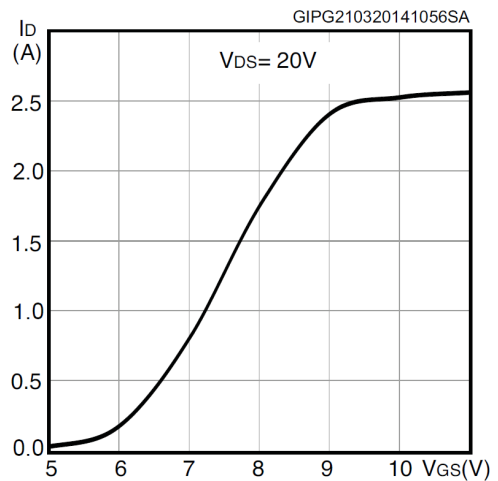


Figure 5. Typical gate charge characteristics

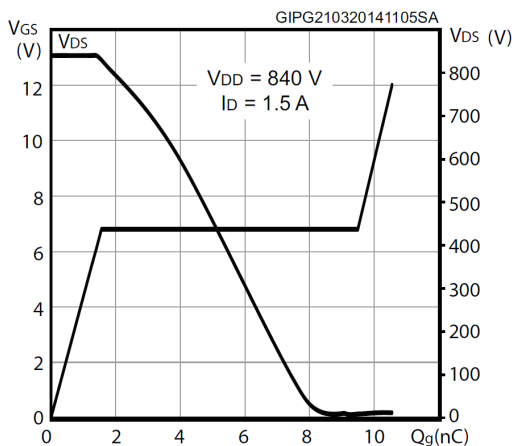


Figure 6. Typical drain-source on-resistance

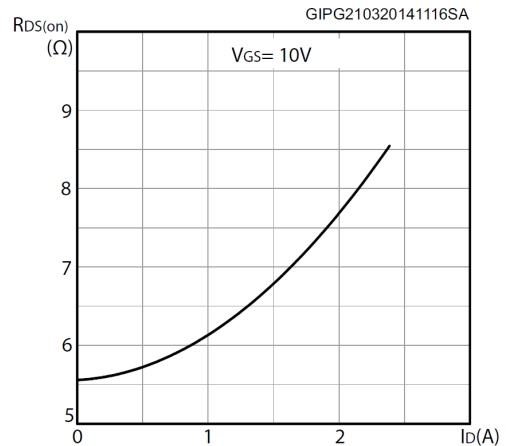


Figure 7. Typical capacitance characteristics

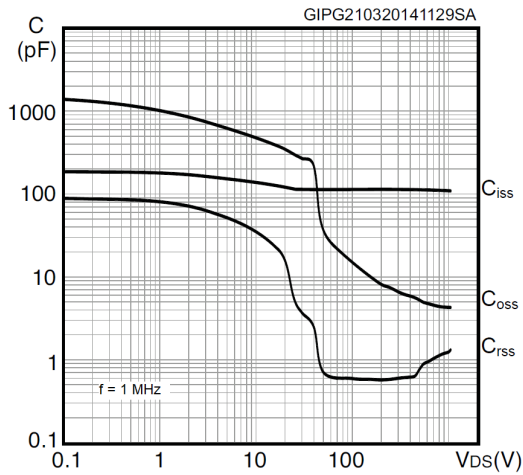


Figure 8. Typical output capacitance stored energy

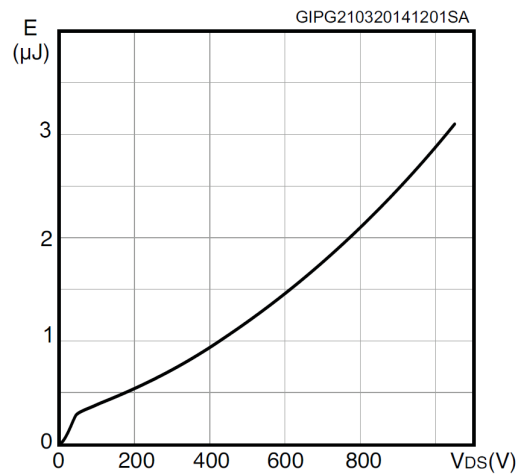


Figure 9. Normalized breakdown voltage vs temperature

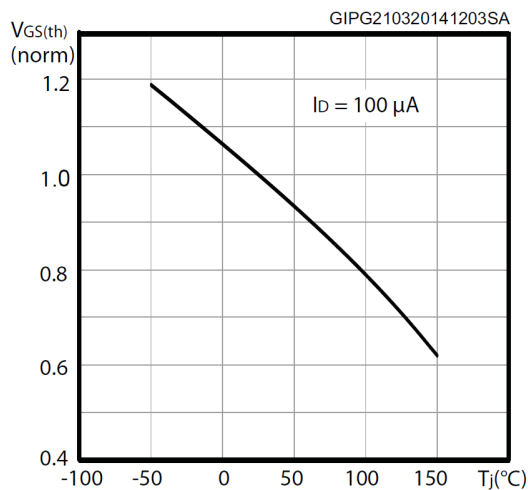


Figure 10. Normalized on-resistance vs temperature

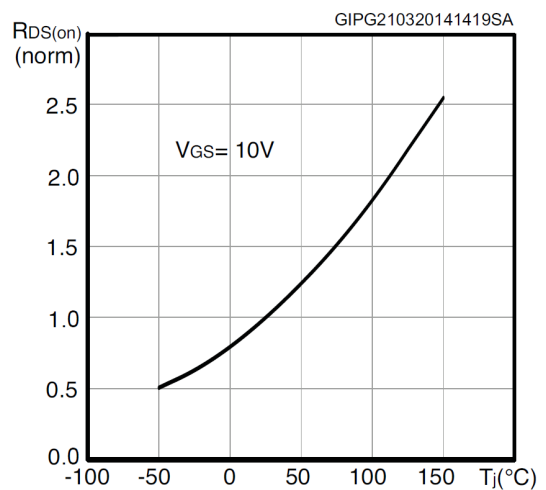


Figure 11. Typical reverse diode forward characteristics

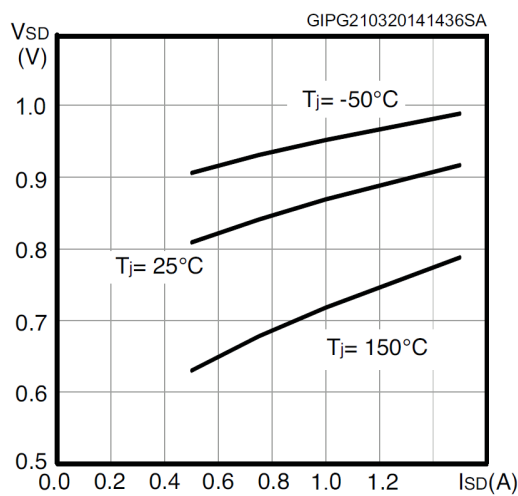
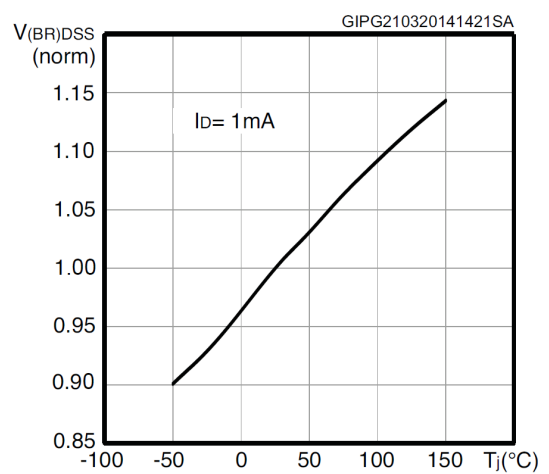
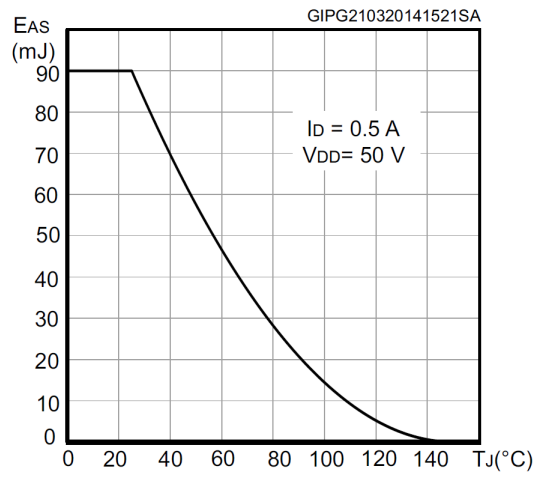


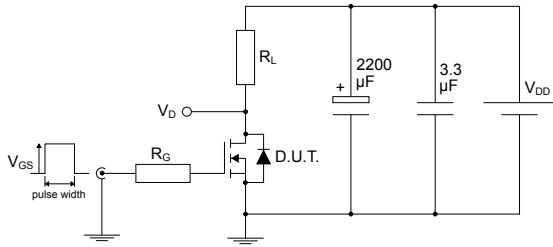
Figure 12. Normalized breakdown voltage vs temperature



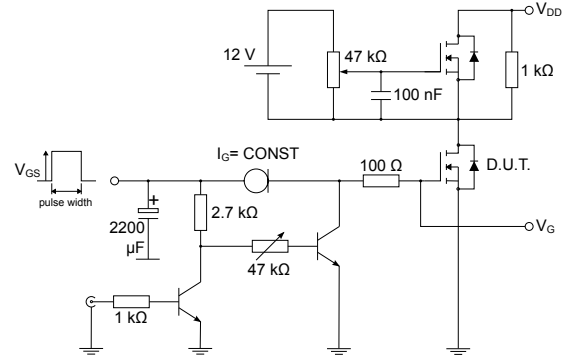
**Figure 13. Maximum avalanche energy vs starting  $T_J$**



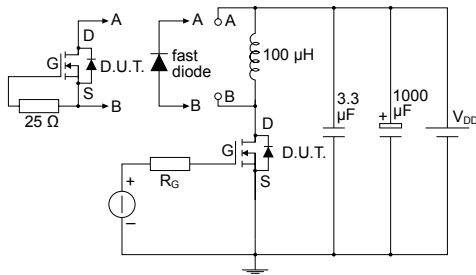
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


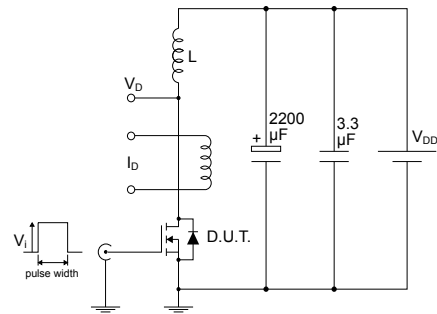
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**Figure 15. Test circuit for gate charge behavior**


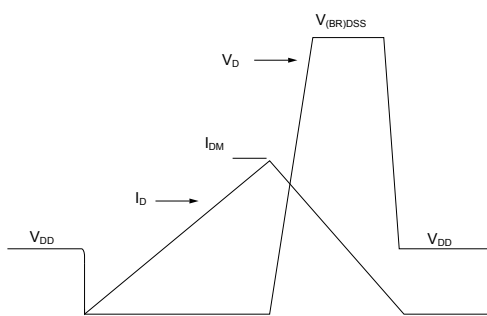
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


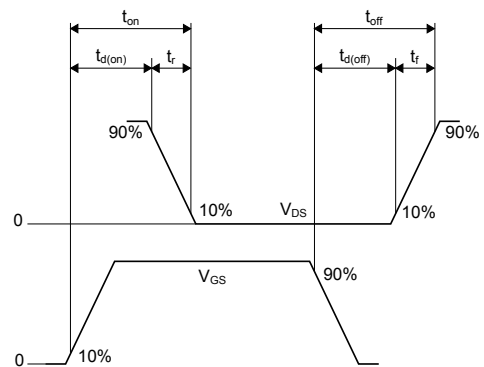
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**Figure 17. Unclamped inductive load test circuit**


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**Figure 18. Unclamped inductive waveform**


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**Figure 19. Switching time waveform**


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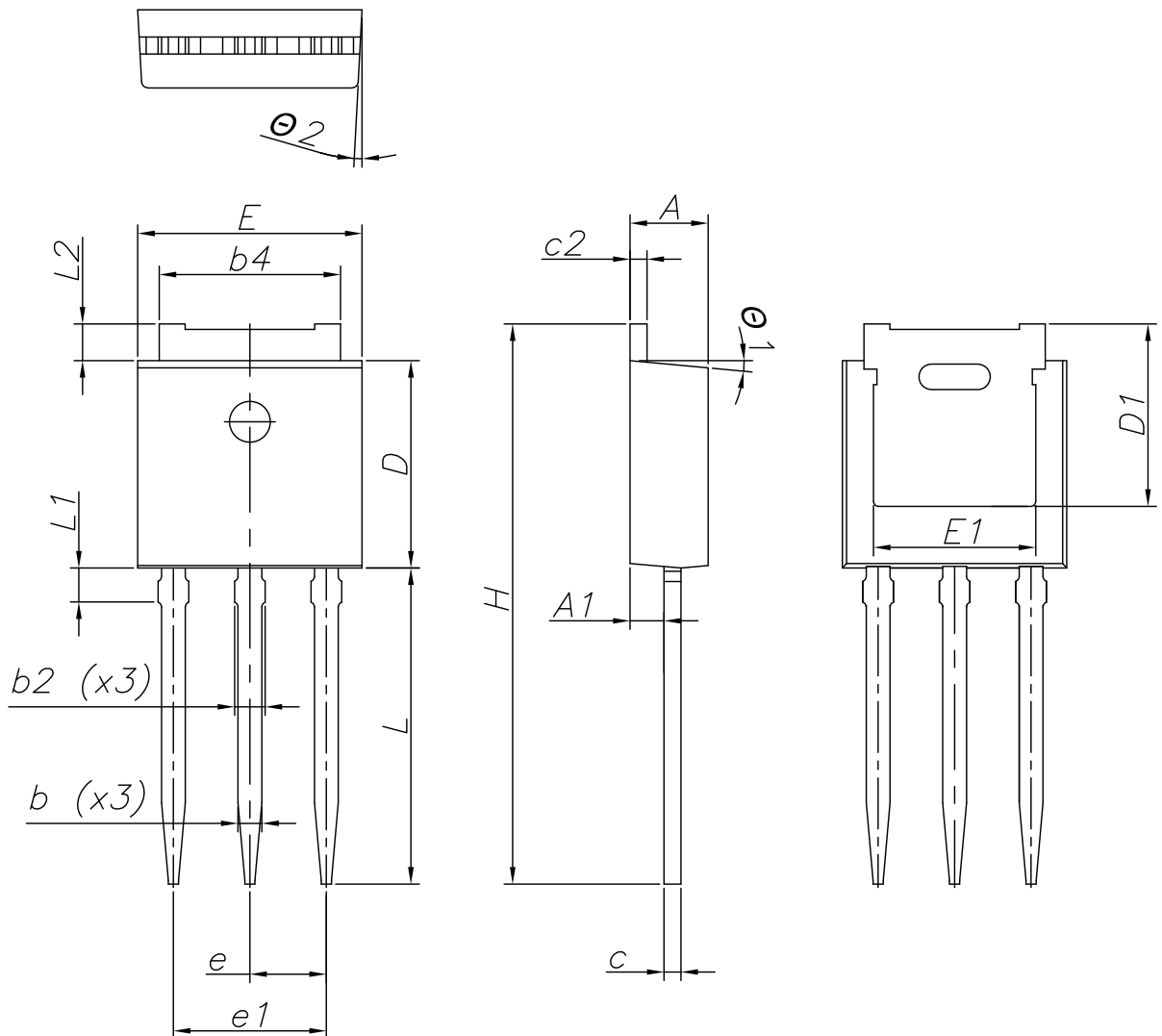


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 IPAK (TO-251) type C package information

Figure 20. IPAK (TO-251) type C package outline



0068771\_IK\_typeC\_rev16

**Table 8. IPAK (TO-251) type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
06-Jul-2023	1	First release. The part number STU2N105K5 was previously inserted in the DS10323.

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