

ADG821/ADG822/ADG823

FEATURES

- 0.8 Ω maximum on resistance @ 125°C**
- 0.3 Ω maximum on resistance flatness @ 125°C**
- 1.8 V to 5.5 V single supply**
- 200 mA current carrying capability**
- Automotive temperature range: -40°C to +125°C**
- Rail-to-rail operation**
- 8-lead MSOP**
- 33 ns switching times**
- Typical power consumption: <0.01 μ W**
- TTL-/CMOS-compatible inputs**
- Pin-compatible with the ADG721/ADG722/ADG723**

APPLICATIONS

- Power routing**
- Battery-powered systems**
- Communication systems**
- Data acquisition systems**
- Audio and video signal routing**
- Cellular phones**
- Modems**
- PCMCIA cards**
- Hard drives**
- Relay replacement**

GENERAL DESCRIPTION

The ADG821/ADG822/ADG823 are monolithic CMOS single-pole, single-throw (SPST) switches. These switches are designed on an advanced submicron process that provides low power dissipation, yet gives high switching speed, low on resistance, and low leakage currents.

The ADG821/ADG822/ADG823 are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery-powered instruments.

Each switch of the ADG821/ADG822/ADG823 conducts equally well in both directions when on. The ADG821/ADG822/ADG823 contain two independent SPST switches. The ADG821 and ADG822 differ only in that both switches are normally open and normally closed, respectively. In the ADG823, Switch 1 is normally open and Switch 2 is normally closed. The ADG823 exhibits break-before-make switching action.

The ADG821/ADG822/ADG823 are available in an 8-lead MSOP.

Rev. A

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FUNCTIONAL BLOCK DIAGRAMS

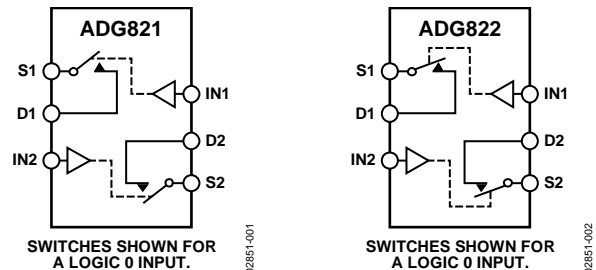


Figure 1.

Figure 2.

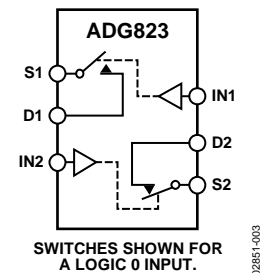


Figure 3.

PRODUCT HIGHLIGHTS

1. Very Low On Resistance: 0.5 Ω typ.
2. On Resistance Flatness ($R_{FLAT(ON)}$): 0.15 Ω typ.
3. Automotive Temperature Range: -40°C to +125°C.
4. Current Carrying Capability: 200 mA.
5. Low Power Dissipation. CMOS construction ensures low power dissipation.
6. 8-Lead MSOP.

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REVISION HISTORY

4/08—Rev. 0 to Rev. A

Updated Format.....	Universal
Added Table 6.....	6
Updated Outline Dimensions	12
Changes to Ordering Guide	12

8/02—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$; $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.5			Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$, see Figure 17
	0.6	0.7	0.8	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.16			Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$
	0.2	0.25	0.28	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.15			Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = 100\text{ mA}$
	0.23	0.26	0.3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.01			nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$, see Figure 18
	± 0.25	± 3	± 25	nA max	
Drain Off Leakage, I_D (Off)	± 0.01			nA typ	$V_S = 4.5\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/4.5\text{ V}$, see Figure 18
	± 0.25	± 3	± 25	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.01			nA typ	$V_S = V_D = 1\text{ V}$, or $V_S = V_D = 4.5\text{ V}$, see Figure 19
	± 0.25	± 3	± 25	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{ON}	33			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$, see Figure 20
	45	48	52	ns max	
t_{OFF}	11			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$, see Figure 20
	16	19	21	ns max	
Break-Before-Make Time Delay, t_{BBM} (ADG823 Only)	32		1	ns typ ns min	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$, see Figure 21
Charge Injection	15			pC typ	$V_S = 2.5\text{ V}$; $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 22
Off Isolation	-52			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 23
Channel-to-Channel Crosstalk	-82			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 24
Bandwidth -3 dB	24			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 25
C_S (Off)	85			pF typ	$f = 1\text{ MHz}$
C_D (Off)	98			pF typ	$f = 1\text{ MHz}$
C_D , C_S (On)	230			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = 5.5\text{ V}$, digital inputs = 0 V or 5.5 V
		1.0	2.0	μA max	

¹ On resistance parameters tested with $I_S = 10\text{ mA}$.

² Guaranteed by design, not subject to production test.

ADG821/ADG822/ADG823

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.7			Ω typ	$V_S = 0\text{ V to }V_{DD}$, $I_S = 100\text{ mA}$, see Figure 17
	1.4	1.5	1.6	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.16			Ω typ	$V_S = 0\text{ V to }V_{DD}$, $I_S = 100\text{ mA}$
	0.2	0.25	0.28	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.3		0.33	Ω typ	$V_S = 0\text{ V to }V_{DD}$, $I_S = 100\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.01			nA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 3.3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3.3\text{ V}$, see Figure 18
	± 0.25	± 3	± 15	nA max	
Drain Off Leakage, I_D (Off)	± 0.01			nA typ	$V_S = 3.3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3.3\text{ V}$, see Figure 18
	± 0.25	± 3	± 25	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.01			nA typ	$V_S = V_D = 1\text{ V}$, or 3.3 V , see Figure 19
	± 0.25	± 3	± 25	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{ON}	48			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 1.5\text{ V}$, see Figure 20
	67	74	78	ns max	
t_{OFF}	12			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 1.5\text{ V}$, see Figure 20
	18	20	23	ns max	
Break-Before-Make Time Delay, t_{BBM} (ADG823 Only)	40		1	ns typ ns min	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 1.5\text{ V}$, see Figure 21
Charge Injection	± 2			pC typ	$V_S = 1.5\text{ V}$; $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 22
Off Isolation	-52			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 23
Channel-to-Channel Crosstalk	-82			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 24
Bandwidth -3 dB	24			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 25
C_S (Off)	85			pF typ	$f = 1\text{ MHz}$
C_D (Off)	98			pF typ	$f = 1\text{ MHz}$
C_D , C_S (On)	230			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = 3.6\text{ V}$, digital inputs = 0 V or 3.6 V
		1.0	2.0	μA max	

¹ On resistance parameters tested with $I_S = 10\text{ mA}$.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V _{DD} to GND	−0.3 V to +7 V
Analog Inputs ¹	−0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs ¹	−0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	400 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	200 mA
Operating Temperature Range	
Automotive	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T _J max)	150°C
Package Power Dissipation	(T _J max − T _A)/θ _{JA}
8-Lead MSOP Thermal Impedance	
θ _{JA}	206°C/W
θ _{JC}	44°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Truth Table for the ADG821/ADG822

ADG821 INx	ADG822 INx	Switch x Condition
0	1	Off
1	0	On

Table 5. Truth Table for the ADG823

IN1	IN2	Switch S1	Switch S2
0	0	Off	On
0	1	Off	Off
1	0	On	On
1	1	On	Off

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG821/ADG822/ADG823

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1	Source Terminal. This pin can be an input or output.
2	D1	Drain Terminal. This pin can be an input or output.
3	IN2	Logic Control Input.
4	GND	Ground (0 V) Reference.
5	S2	Source Terminal. This pin can be an input or output.
6	D2	Drain Terminal. This pin can be an input or output.
7	IN1	Logic Control Input.
8	V _{DD}	Most Positive Power Supply Potential.

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 5. On Resistance vs. V_D , V_S



Figure 8. On Resistance vs. V_D , V_S for Different Temperatures, $V_{DD} = 3V$

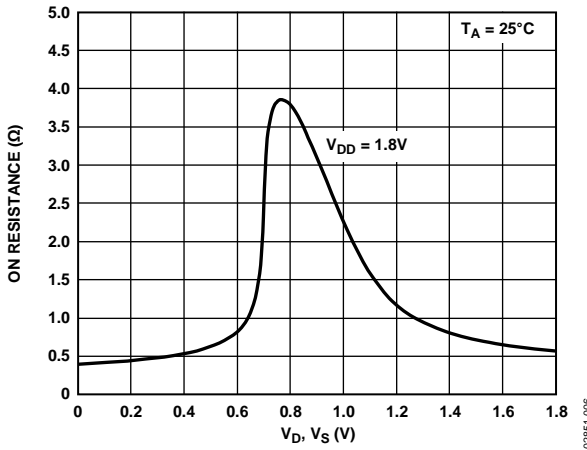


Figure 6. On Resistance vs. V_D , V_S ; $V_{DD} = 1.8V$

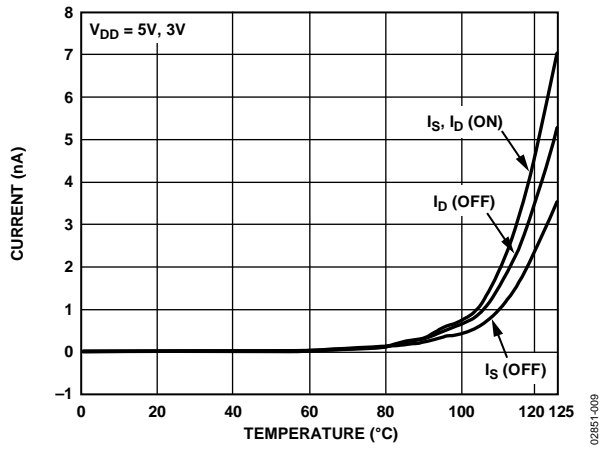


Figure 9. Leakage Current vs. Temperature

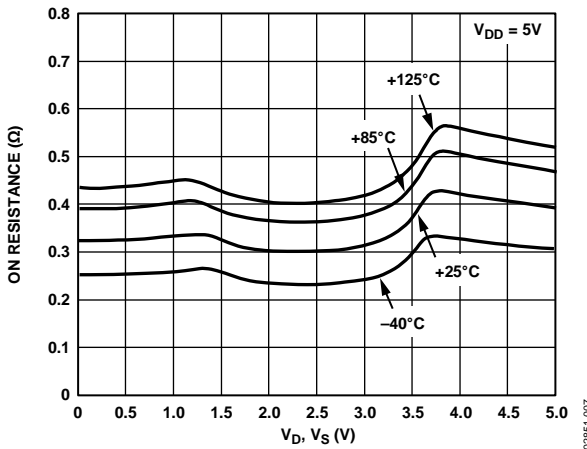


Figure 7. On Resistance vs. V_D , V_S for Different Temperatures, $V_{DD} = 5V$

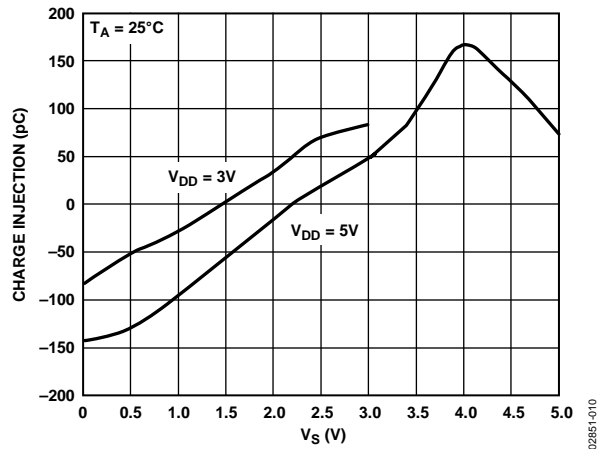


Figure 10. Charge Injection vs. Source Voltage

ADG821/ADG822/ADG823



Figure 11. t_{ON}/t_{OFF} vs. Temperature

02851-011

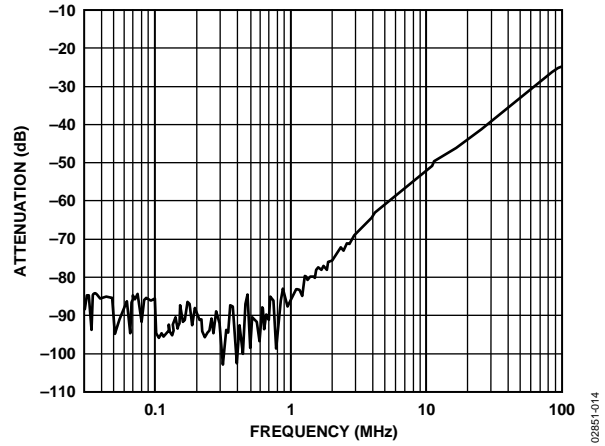


Figure 14. Crosstalk vs. Frequency

02851-014

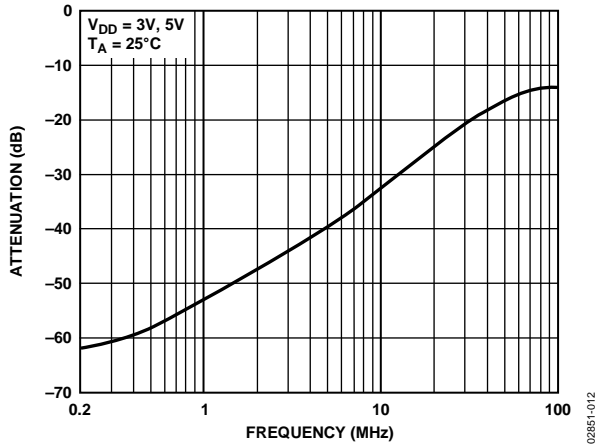


Figure 12. Off Isolation vs. Frequency

02851-012

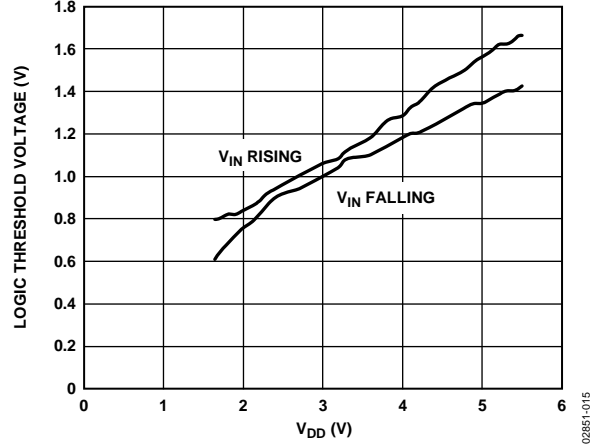


Figure 15. Logic Threshold Voltage vs. Supply Voltage

02851-015

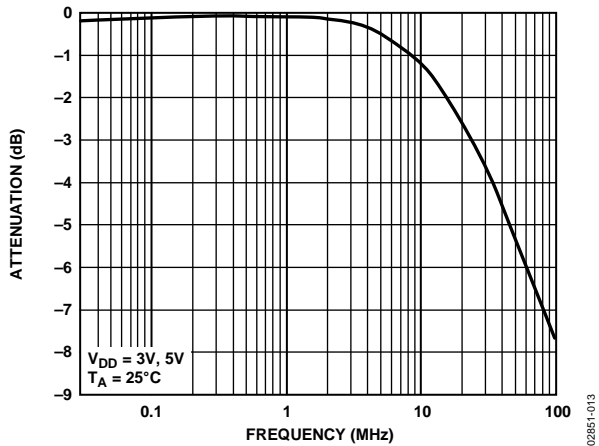


Figure 13. On Response vs. Frequency

02851-013

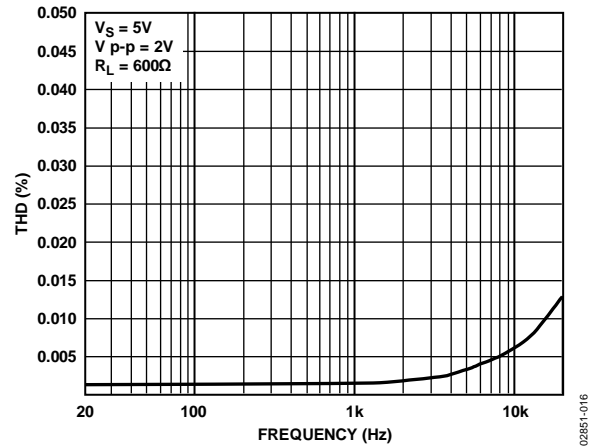


Figure 16. THD vs. Frequency

02851-016

TEST CIRCUITS

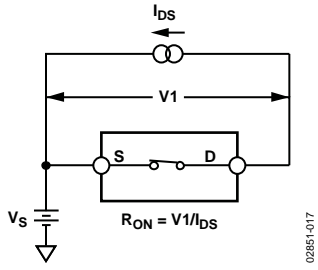


Figure 17. On Resistance

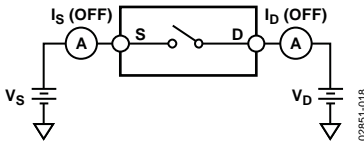


Figure 18. Off Leakage

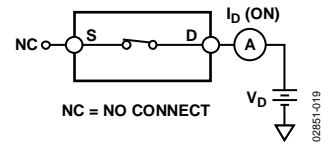


Figure 19. On Leakage



Figure 20. Switching Times

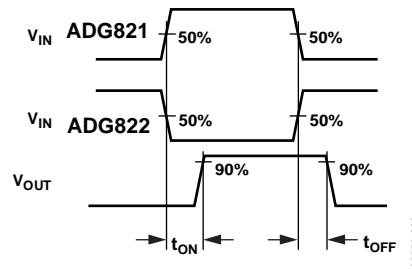


Figure 21. Break-Before-Make Time Delay, t_{BBM} (ADG823 only)

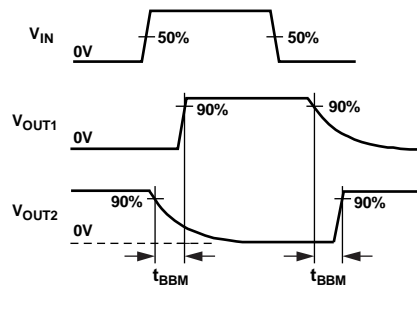
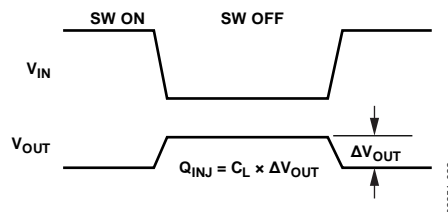


Figure 22. Charge Injection



ADG821/ADG822/ADG823



Figure 23. Off Isolation

02851-023



Figure 25. Bandwidth

02851-025



Figure 24. Channel-to-Channel Crosstalk

02851-024

TERMINOLOGY

V_{DD}

Most positive power supply potential.

GND

Ground (0 V) reference.

I_{DD}

Positive supply current.

S

Source terminal. May be an input or output.

D

Drain terminal. May be an input or output.

IN

Logic control input.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

On resistance match between any two channels (that is, $R_{ON\ max} - R_{ON\ min}$).

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)

Source leakage current with the switch off.

I_D (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_D, V_S

Analog voltage on Terminal D and Terminal S.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (Off)

Off switch source capacitance.

C_D (Off)

Off switch drain capacitance.

C_D, C_S (On)

On switch capacitance.

t_{ON}

Delay between applying the digital control input and the output switching on.

t_{OFF}

Delay between applying the digital control input and the output switching off.

t_{BBM}

Off time or on time measured between the 90% points of both switches, when switching from one address state to another.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Bandwidth

The frequency at which the output is attenuated by -3 dBs.

On Response

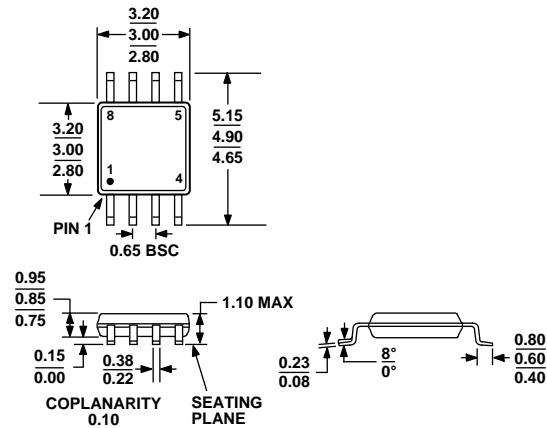
The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

ADG821/ADG822/ADG823

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 26. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG821BRM	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SQB
ADG821BRM-REEL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SQB
ADG821BRMZ ¹	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SOP
ADG821BRMZ-REEL ⁷	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SOP
ADG822BRM	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SRB
ADG822BRM-REEL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SRB
ADG822BRM-REEL7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SRB
ADG822BRMZ ¹	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S1J
ADG822BRMZ-REEL ⁷	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S1J
ADG823BRM	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SSB
ADG823BRM-REEL	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SSB
ADG823BRMZ ¹	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SSB#
ADG823BRMZ-REEL ⁷	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SSB#

¹ Z = RoHS Compliant Part, # denotes RoHS compliant product may be top or bottom marked.

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