



FEATURES

- 1.8 V to 5.5 V single-supply operation
- ±2.5 V dual-supply operation
- On resistance: 4 Ω at 25°C (+5 V single supply/±2.5 V dual supply)
- 0.5 Ω on-resistance flatness at 25°C (+5 V single supply/±2.5 V dual supply)
- Rail-to-rail operation
- Transition times: 23 ns typical at 25°C
- Single 32-to-1 channel multiplexer
- Dual/differential 16-to-1 channel multiplexer
- TTL-/CMOS-compatible inputs
- 48-lead TQFP or 48-lead, 7 mm × 7 mm LFCSP

APPLICATIONS

- Optical applications
- Data acquisition systems
- Communication systems
- Relay replacement
- Audio and video switching
- Battery-powered systems
- Medical instrumentation
- Automatic test equipment (ATE)

GENERAL DESCRIPTION

The [ADG726/ADG732](#) are monolithic, complementary metal oxide semiconductor (CMOS) 32-channel and dual 16-channel analog multiplexers. The [ADG732](#) switches one of 32 inputs (S1 to S32) to a common output, D, as determined by the 5-bit binary address lines A0, A1, A2, A3, and A4. The [ADG726](#) switches one of 16 inputs as determined by the 4-bit binary address lines A0, A1, A2, and A3.

On-chip latches facilitate microprocessor interfacing. The [ADG726](#) may also be configured for differential operation by tying \overline{CSA} and \overline{CSB} together. An \overline{EN} input is used to enable or disable the devices. When disabled, all channels are switched off.

These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance, and leakage currents. They operate from a single supply of +1.8 V to +5.5 V and a ±2.5 V dual supply, making them ideally suited to a variety of applications. On resistance is in the region of a few ohms and is

Rev. C

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FUNCTIONAL BLOCK DIAGRAMS

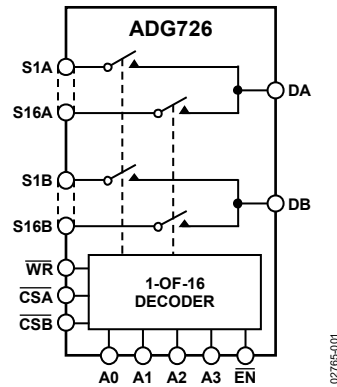


Figure 1.

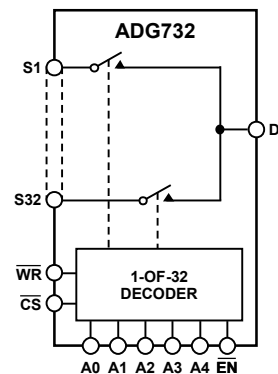


Figure 2.

closely matched between switches and very flat over the full signal range. These devices can operate equally well as either multiplexers or demultiplexers and have an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

The [ADG726/ADG732](#) are available in a 48-lead LFCSP or a 48-lead TQFP. For functionally equivalent devices with serial interface, see the [ADG725/ADG731](#).

PRODUCT HIGHLIGHTS

- +1.8 V to +5.5 V single- or ±2.5 V dual-supply operation. These devices are specified and guaranteed with +5 V ± 10%, +3 V ± 10% single-supply, and ±2.5 V ± 10% dual-supply rails.
- An on resistance of 4 Ω.
- Guaranteed break-before-make switching action.
- 48-lead LFCSP package or 48-lead TQFP package.

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REVISION HISTORY

2/2021—Rev. B to Rev. C

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7/2002—Revision 0: Initial Version

SPECIFICATIONS

+5 V SINGLE SUPPLY

$V_{DD} = 5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $GND = 0 \text{ V}$, unless otherwise noted.

Table 1.

| Parameter | Symbol | ADG726/ADG732 | | ADG732 | Unit | Test Conditions/Comments |
|--|---|---------------|-----------------|-----------------|-------------------|---|
| | | +25°C | −40°C to +85°C | −40°C to +125°C | | |
| ANALOG SWITCH | | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | | V | |
| On Resistance | R_{ON} | 4 | 5 | | Ω typ | $V_S = 0 \text{ V to } V_{DD}$, $I_{DS} = 10 \text{ mA}$, see Figure 20 |
| | | 5.5 | 6 | 7 | Ω max | |
| On Resistance Match Between Channels | ΔR_{ON} | | 0.3 | | Ω typ | $V_S = 0 \text{ V to } V_{DD}$, $I_{DS} = 10 \text{ mA}$ |
| | | | 0.8 | 1 | Ω max | |
| On Resistance Flatness | $R_{FLAT(ON)}$ | 0.5 | | | Ω typ | $V_S = 0 \text{ V to } V_{DD}$, $I_{DS} = 10 \text{ mA}$ |
| | | | 1 | 1.2 | Ω max | |
| LEAKAGE CURRENTS | | | | | | |
| Source Off Leakage | I_S (Off) | ± 0.01 | | | nA typ | $V_{DD} = 5.5 \text{ V}$ $V_D = 4.5 \text{ V}/1 \text{ V}$, $V_S = 1 \text{ V}/4.5 \text{ V}$, see Figure 21 |
| | | ± 0.25 | ± 1 | ± 2 | nA max | |
| Drain Off Leakage | I_D (Off) | ± 0.05 | | | nA typ | $V_D = 4.5 \text{ V}/1 \text{ V}$, $V_S = 1 \text{ V}/4.5 \text{ V}$, see Figure 24 |
| | | ± 0.5 | ± 2.5 | | nA max | |
| | | ± 1 | ± 5 | ± 10 | nA max | |
| Channel On Leakage | I_D, I_S (On) | ± 0.05 | | | nA typ | $V_D = V_S = 1 \text{ V}$, or 4.5 V, see Figure 25 |
| | | ± 0.5 | ± 2.5 | | nA max | |
| | | ± 1 | ± 5 | ± 10 | nA max | |
| DIGITAL INPUTS | | | | | | |
| Input High Voltage | V_{INH} | | 2.4 | 2.4 | V min | |
| Input Low Voltage | V_{INL} | | 0.8 | 0.8 | V max | |
| Input Current | | | | | | |
| Low or High | I_{INL} or I_{INH} | 0.005 | | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | | ± 0.5 | ± 0.5 | μA max | |
| Digital Input Capacitance | C_{IN} | 5 | | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | | | |
| Transition Time | $t_{TRANSITION}$ | 23 | | | ns typ | $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, see Figure 27 |
| | | 34 | 40 | 48 | ns max | $V_{S1} = 3 \text{ V}/0 \text{ V}$, $V_{S32} = 0 \text{ V}/3 \text{ V}$ |
| Break-Before-Make Time Delay | t_D | 18 | | | ns typ | $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$; $V_S = 3 \text{ V}$, see Figure 28 |
| | | | 1 | 1 | ns min | |
| On Time (\overline{CS} , \overline{WR}) | $t_{ON}(\overline{CS}, \overline{WR})$ | 18 | | | ns typ | $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$; $V_S = 3 \text{ V}$, see Figure 29 |
| | | 25 | 32 | 38.5 | ns max | |
| Off Time (\overline{CS} , \overline{WR}) | $t_{OFF}(\overline{CS}, \overline{WR})$ | 17 | | | ns typ | $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$; $V_S = 3 \text{ V}$, see Figure 29 |
| | | 23 | 29 | 33 | ns max | |
| On Time (\overline{EN}) | $t_{ON}(\overline{EN})$ | 24 | | | ns typ | $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$; $V_S = 3 \text{ V}$, see Figure 30 |
| | | 32 | 40 | 43 | ns max | |
| Off Time (\overline{EN}) | $t_{OFF}(\overline{EN})$ | 16 | | | ns typ | $R_L = 300 \Omega$, $C_L = 35 \text{ pF}$; $V_S = 3 \text{ V}$, see Figure 30 |
| | | 22 | 25 | 25 | ns max | |
| Charge Injection | Q_{INJ} | 5 | | | pC typ | $V_S = 2.5 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$, see Figure 31 |
| Off Isolation | I_{SO} | −72 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 22 |
| Channel-to-Channel Crosstalk | C_{TK} | −72 | | | dB typ | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$, see Figure 23 |
| −3 dB Bandwidth | BW | | | | | $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, see Figure 26 |
| | | 34 | | | MHz typ | |
| | | 18 | | | MHz typ | |

| Parameter | Symbol | ADG726/ADG732 | | ADG732 | Unit | Test Conditions/Comments |
|-------------------------------------|--------------------------------------|---------------|----------------|-----------------|------------------|--|
| | | +25°C | -40°C to +85°C | -40°C to +125°C | | |
| Off Switch Source Capacitance | C _S (Off) | 13 | | | pF typ | f = 1 MHz |
| Off Switch Drain Capacitance | C _D (Off) | 170 | | | pF typ | f = 1 MHz |
| ADG726 | | 340 | | | pF typ | f = 1 MHz |
| ADG732 | | | | | | |
| On Switch Drain, Source Capacitance | C _D , C _S (On) | 175 | | | pF typ | f = 1 MHz |
| ADG726 | | 350 | | | pF typ | f = 1 MHz |
| ADG732 | | | | | | |
| POWER REQUIREMENTS | | | | | | |
| Positive Supply Current | I _{DD} | 10 | 20 | 20 | μA typ μA max | V _{DD} = 5.5 V Digital inputs = 0 V or 5.5 V |

¹ Guaranteed by design; not subject to production test.

+3 V SINGLE SUPPLY

$V_{DD} = 3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | Symbol | ADG726/ADG732 | | ADG732 | Unit | Test Conditions/Comments |
|--|---|------------------------------------|---------------------------------|----------------------|--|--|
| | | +25°C | −40°C to +85°C | −40°C to +125°C | | |
| ANALOG SWITCH | | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | | V | |
| On Resistance | R_{ON} | 7 | 12 | 13 | Ω typ Ω max | $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 10\text{ mA}$, see Figure 20 |
| On Resistance Match Between Channels | ΔR_{ON} | 11 | 0.35 | | Ω typ | $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 10\text{ mA}$ |
| On Resistance Flatness | $R_{FLAT(ON)}$ | | 1 3 | 1 | Ω max Ω typ | $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = 10\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | | |
| Source Off Leakage | I_S (Off) | ± 0.01 ± 0.25 | ± 1 | ± 2 | nA typ nA max | $V_{DD} = 3.3\text{ V}$ $V_S = 3\text{ V}/1\text{ V}$, $V_D = 1\text{ V}/3\text{ V}$, see Figure 21 |
| Drain Off Leakage | I_D (Off) | ± 0.05 ± 0.5 | ± 2.5 | | nA typ nA max | $V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$, see Figure 24 |
| Channel On Leakage | I_D, I_S (On) | ± 0.05 ± 0.5 ± 1 | ± 5 ± 2.5 ± 5 | ± 10 ± 10 | nA max nA typ nA max | $V_S = V_D = 1\text{ V or }3\text{ V}$, see Figure 25 |
| DIGITAL INPUTS | | | | | | |
| Input High Voltage | V_{INH} | | 2.0 | 2.0 | V min | |
| Input Low Voltage | V_{INL} | | 0.7 | 0.7 | V max | |
| Input Current | I_{INL} or I_{INH} | 0.005 | ± 0.5 | ± 0.5 | μA typ μA max | $V_{IN} = V_{INL}$ or V_{INH} |
| Digital Input Capacitance | C_{IN} | 5 | | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | | | |
| Transition Time | $t_{TRANSITION}$ | 34 52 | 62 | 69 | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 27 $V_{S1} = 2\text{ V}/0\text{ V}$, $V_{S32} = 0\text{ V}/2\text{ V}$ |
| Break-Before-Make Time Delay | t_D | 26 | 1 | 1 | ns typ ns min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 2\text{ V}$, see Figure 28 |
| On Time (\overline{CS} , \overline{WR}) | $t_{ON}(\overline{WR}, \overline{CS})$ | 29 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 2\text{ V}$, see Figure 29 |
| Off Time (\overline{CS} , \overline{WR}) | $t_{OFF}(\overline{WR}, \overline{CS})$ | 43 26 | 52 | 60 | ns max ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 2\text{ V}$, see Figure 29 |
| On Time (\overline{EN}) | $t_{ON}(\overline{EN})$ | 38 33 | 42 | 55.5 | ns max ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 2\text{ V}$, see Figure 30 |
| Off Time (\overline{EN}) | $t_{OFF}(\overline{EN})$ | 48 19 | 55 | 63.5 | ns max ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 2\text{ V}$, see Figure 30 |
| Charge Injection | Q_{INJ} | 25 | 28 | 28 | ns max pC typ | $V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 31 |
| Off Isolation | I_{SO} | 1 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 22 |
| Channel-to-Channel Crosstalk | C_{TK} | −72 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 23 |
| −3 dB Bandwidth | BW | −72 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 26 |
| | | 34 | | | MHz typ | |
| | | 18 | | | MHz typ | |

| Parameter | Symbol | ADG726/ADG732 | | ADG732 | Unit | Test Conditions/Comments |
|-------------------------------------|--------------------------------------|---------------|----------------|-----------------|------------------|--|
| | | +25°C | -40°C to +85°C | -40°C to +125°C | | |
| Off Switch Source Capacitance | C _S (Off) | 13 | | | pF typ | f = 1 MHz |
| Off Switch Drain Capacitance | C _D (Off) | 170 | | | pF typ | f = 1 MHz |
| | | 340 | | | pF typ | f = 1 MHz |
| On Switch Drain, Source Capacitance | C _D , C _S (On) | | | | | |
| | | 175 | | | pF typ | f = 1 MHz |
| | | 350 | | | pF typ | f = 1 MHz |
| POWER REQUIREMENTS | | | | | | |
| Positive Supply Current | I _{DD} | 5 | 10 | 10 | μA typ μA max | V _{DD} = 3.3 V Digital inputs = 0 V or 3.3 V |

¹ Guaranteed by design; not subject to production test.

±2.5 V DUAL SUPPLY

$V_{DD} = +2.5\text{ V} \pm 10\%$, $V_{SS} = -2.5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

| Parameter | Symbol | ADG726/ADG732 | | ADG732 | Unit | Test Conditions/Comments |
|--|---|--|---|----------------------|--|--|
| | | +25°C | −40°C to +85°C | −40°C to +125°C | | |
| ANALOG SWITCH | | | | | | |
| Analog Signal Range | | | V_{SS} to V_{DD} | | V | |
| On Resistance | R_{ON} | 4 5.5 | 6 | 7 | Ω typ Ω max | $V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$, see Figure 20 |
| On Resistance Match Between Channels | ΔR_{ON} | | 0.3 | | Ω typ | $V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$ |
| On Resistance Flatness | $R_{FLAT(ON)}$ | 0.5 | 0.8 1 | 1 1.2 | Ω max Ω typ Ω max | $V_S = V_{SS}$ to V_{DD} , $I_{DS} = 10\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | | |
| Source Off Leakage | I_S (Off) | ± 0.01 | | | nA typ | $V_{DD} = +2.75\text{ V}$, $V_{SS} = -2.75\text{ V}$ $V_S = +2.25\text{ V}/-1.25\text{ V}$, $V_D = -1.25\text{ V}/+2.25\text{ V}$, see Figure 21 |
| Drain Off Leakage | I_D (Off) | ± 0.25 ± 0.05 | ± 0.5 | ± 1 | nA max nA typ | $V_S = +2.25\text{ V}/-1.25\text{ V}$, $V_D = -1.25\text{ V}/+2.25\text{ V}$, see Figure 24 |
| Channel On Leakage | I_D, I_S (On) | ± 0.5 ± 1 ± 0.05 ± 0.5 ± 1 | ± 2.5 ± 5 ± 2.5 ± 2.5 ± 5 | ± 10 ± 10 | nA max nA max nA typ nA max nA max | $V_S = V_D = +2.25\text{ V}/-1.25\text{ V}$, see Figure 25 |
| DIGITAL INPUTS | | | | | | |
| Input High Voltage | V_{INH} | | 1.7 | 1.7 | V min | |
| Input Low Voltage | V_{INL} | | 0.7 | 0.7 | V max | |
| Input Current | I_{INL} or I_{INH} | 0.005 | ± 0.5 | ± 0.5 | μA typ μA max | $V_{IN} = V_{INL}$ or V_{INH} |
| Digital Input Capacitance | C_{IN} | 5 | | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | | | |
| Transition Time | $t_{TRANSITION}$ | 33 45 | 51 | 56 | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, see Figure 27 $V_{S1} = 1.5\text{ V}/0\text{ V}$, $V_{S32} = 0\text{ V}/1.5\text{ V}$ |
| Break-Before-Make Time Delay | t_D | 15 | 1 | 1 | ns typ ns min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, see Figure 28 |
| On Time (\overline{CS} , \overline{WR}) | $t_{ON}(\overline{WR}, \overline{CS})$ | 21 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, see Figure 29 |
| Off Time (\overline{CS} , \overline{WR}) | $t_{OFF}(\overline{WR}, \overline{CS})$ | 30 20 | 37 | 43 | ns max ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.5\text{ V}$, see Figure 29 |
| On Time (\overline{EN}) | $t_{ON}(\overline{EN})$ | 29 26 | 35 | 38 | ns max ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.8\text{ V}$, see Figure 30 |
| Off Time (\overline{EN}) | $t_{OFF}(\overline{EN})$ | 37 18 | | 50 | ns max ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = 1.8\text{ V}$, see Figure 30 |
| Charge Injection | Q_{INJ} | 26 1 | 29 | 29 | ns max pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 31 |
| Off Isolation | I_{SO} | −72 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 22 |
| Channel-to-Channel Crosstalk | C_{TK} | −72 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 23 |
| −3 dB Bandwidth | BW | | | | | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 26 |
| | | 34 | | | MHz typ | |
| | | 18 | | | MHz typ | |

| Parameter | Symbol | ADG726/ADG732 | | ADG732 | Unit | Test Conditions/Comments |
|-------------------------------------|--------------------------------------|---------------|----------------|-----------------|--------|--------------------------------|
| | | +25°C | -40°C to +85°C | -40°C to +125°C | | |
| Off Switch Source Capacitance | C _S (Off) | 13 | | | pF typ | |
| Off Switch Drain Capacitance | C _D (Off) | | | | pF typ | f = 1 MHz |
| ADG726 | | 137 | | | pF typ | f = 1 MHz |
| ADG732 | | 275 | | | pF typ | f = 1 MHz |
| On Switch Drain, Source Capacitance | C _D , C _S (On) | | | | pF typ | f = 1 MHz |
| ADG726 | | 150 | | | pF typ | f = 1 MHz |
| ADG732 | | 300 | | | pF typ | f = 1 MHz |
| POWER REQUIREMENTS | | | | | | |
| Positive Supply Current | I _{DD} | 10 | | | μA typ | V _{DD} = 2.75 V |
| Negative Supply Current | I _{SS} | 10 | 20 | 20 | μA max | Digital inputs = 0 V or 2.75 V |
| | | | 20 | 20 | μA typ | V _{DD} = -2.75 V |
| | | | | | μA max | Digital inputs = 0 V or 2.75 V |

¹ Guaranteed by design; not subject to production test.

TIMING CHARACTERISTICS

Table 4.

| Parameter ^{1, 2, 3} | Limit at T _{MIN} , T _{MAX} | Unit | Test Conditions/Comments |
|------------------------------|--|--------|---|
| t ₁ | 0 | ns min | \overline{CS} to \overline{WR} setup time |
| t ₂ | 0 | ns min | \overline{CS} to \overline{WR} hold time |
| t ₃ | 10 | ns min | \overline{WR} pulse width |
| t ₄ | 10 | ns min | Time between \overline{WR} cycles |
| t ₅ | 5 | ns min | Address, enable setup time |
| t ₆ | 2 | ns min | Address, enable hold time |

¹ See Figure 3.

² All input signals are specified with t_r = t_f = 1 ns (10% to 90% of V_{DD}).

³ Guaranteed by design and characterization, not production tested.

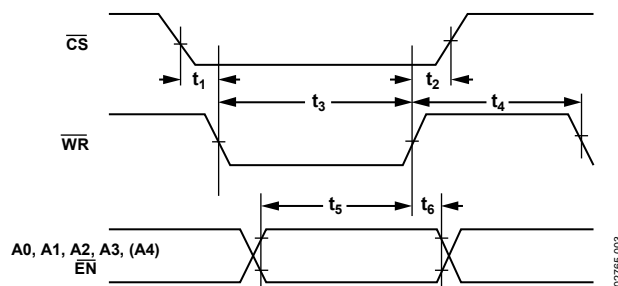


Figure 3. Timing Diagram

Figure 3 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while \overline{WR} is held low, the latches are transparent and the switches respond to changing the address and enable the inputs.

Input data is latched on the rising edge of \overline{WR} . The ADG726 has two \overline{CS} inputs. This enables the device to be used either as a dual 16-to-1 channel multiplexer or a differential 16-channel multiplexer. If a differential output is required, tie \overline{CSA} and \overline{CSB} together.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 5.

| Parameter | Rating |
|--|---|
| V_{DD} to V_{SS} | 7 V |
| V_{DD} to GND | -0.3 V to +7 V |
| V_{SS} to GND | +0.3 V to -7 V |
| Analog Inputs ¹ | $V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first |
| Digital Inputs ¹ | -0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first |
| Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum) | 60 mA |
| Continuous Current, S or D | 30 mA |
| Operating Temperature Range | |
| ADG726 | -40°C to +85°C |
| ADG732 | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| Thermal Impedance θ_{JA} (4-Layer Board) | |
| 48-Lead LFCSP | 25°C/W |
| 48-Lead TQFP | 54.6°C/W |
| Reflow Soldering Peak Temperature, Pb Free | As per JEDEC J-STD-020 |

¹ Overvoltages at A, \overline{EN} , \overline{WR} , \overline{CS} , S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

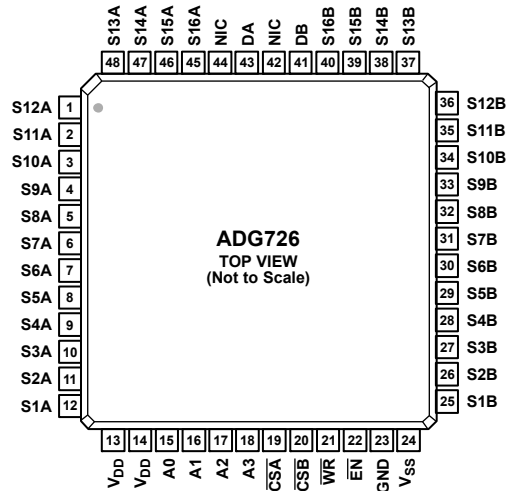
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTION
48-LEAD TQFP

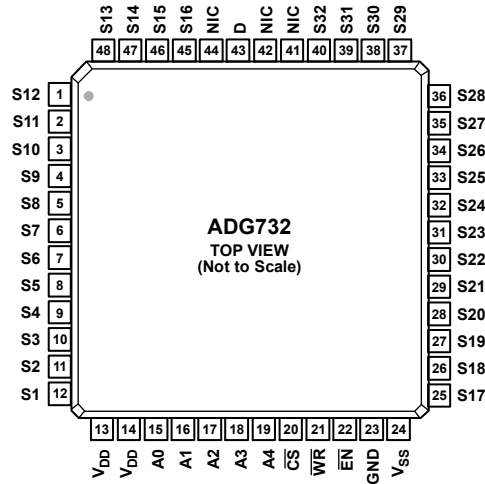


NOTES
 1. NIC = NOT INTERNALLY CONNECTED. DO NOT CONNECT TO THIS PIN.

Figure 4. ADG726 Pin Configuration

Table 6. ADG726 Pin Function Description

| Pin No. | Mnemonic | Description |
|-------------------|------------------|--|
| 1 to 12, 45 to 48 | S16A to S1A | Source Terminal. This pin may be an input or output. |
| 13, 14 | V _{DD} | Most Positive Power Supply Potential. |
| 15 to 18 | A0 to A3 | Logic Control Inputs. |
| 19 | \overline{CSA} | Chip Select Pin A. \overline{CSA} is active low. If a differential output configuration is required, tie \overline{CSA} and \overline{CSB} together. |
| 20 | \overline{CSB} | Chip Select Pin B. \overline{CSB} is active low. If a differential output configuration is required, tie \overline{CSB} and \overline{CSA} together. |
| 21 | \overline{WR} | Write pin. When \overline{WR} is low, the logic control inputs (A0 to A3) control which state the switches are in. On the rising edge of \overline{WR} , the logic control input data is latched. |
| 22 | \overline{EN} | Active Low, Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, the Ax logic control inputs determine the on switches. The \overline{EN} input signal is not latched by \overline{WR} . |
| 23 | GND | Ground (0 V) Reference. |
| 24 | V _{SS} | Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect this pin to GND. |
| 25 to 40 | S1B to S16B | Source Terminal. This pin may be an input or output. |
| 41 | DB | Drain Terminal. This pin may be an input or output. |
| 42, 44 | NIC | Not Internally Connected. Do not connect to this pin. |
| 43 | DA | Drain Terminal. This pin may be an input or output. |



NOTES
 1. NIC = NOT INTERNALLY CONNECTED. DO NOT CONNECT TO THIS PIN.

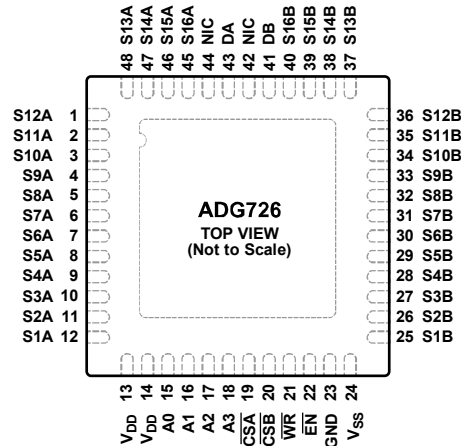
Figure 5. ADG732 Pin Configuration

02765-104

Table 7. ADG732 Pin Function Description

| Pin No. | Mnemonic | Description |
|-------------------|-----------------|--|
| 1 to 12, 45 to 48 | S16 to S1 | Source Terminal. This pin may be an input or output. |
| 13, 14 | V _{DD} | Most Positive Power Supply Potential. |
| 15 to 19 | A0 to A4 | Logic Control Inputs. |
| 20 | \overline{CS} | Chip Select Pin. \overline{CS} is active low. |
| 21 | \overline{WR} | Write Pin. When \overline{WR} is low, the logic control inputs (A0 to A4) control which state the switches are in. On the rising edge of \overline{WR} , the logic control input data is latched. |
| 22 | \overline{EN} | Active Low, Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, the A _x logic control inputs determine the on switches. The \overline{EN} input signal is not latched by \overline{WR} . |
| 23 | GND | Ground (0 V) Reference. |
| 24 | V _{SS} | Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect this pin to GND. |
| 25 to 40 | S17 to S32 | Source Terminal. This pin may be an input or output. |
| 41, 42, 44 | NIC | Not Internally Connected. Do not connect to this pin. |
| 43 | D | Drain Terminal. This pin may be an input or output. |

48-LEAD LFCSP

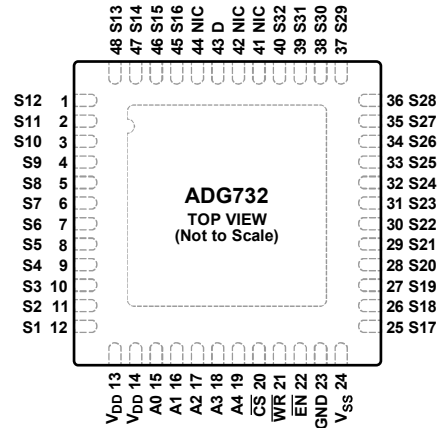


NOTES
 1. NIC = NOT INTERNALLY CONNECTED. DO NOT CONNECT TO THIS PIN.
 2. THE EXPOSED PAD MUST BE CONNECTED TO GND.

Figure 6. ADG726 Pin Configuration

Table 8. ADG726 Pin Function Description

| Pin No. | Mnemonic | Description |
|-------------------|------------------|---|
| 1 to 12, 45 to 48 | S16A to S1A | Source Terminal. This pin may be an input or output. |
| 13, 14 | V _{DD} | Most Positive Power Supply Potential. |
| 15 to 18 | A0 to A3 | Logic Control Inputs. |
| 19 | \overline{CSA} | Chip Select Pin A. \overline{CSA} is active low. If a differential output configuration is required, tie \overline{CSA} and \overline{CSB} together. |
| 20 | \overline{CSB} | Chip Select Pin B. \overline{CSB} is active low. If a differential output configuration is required, tie \overline{CSB} and \overline{CSA} together. |
| 21 | \overline{WR} | Write pin. When \overline{WR} is low, the logic control inputs (A0 to A3) control which state the switches are in. On the rising edge of \overline{WR} , the logic control input data is latched. |
| 22 | \overline{EN} | Active Low, Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, the Ax logic control inputs determine the on switches. The EN input signal is not latched by \overline{WR} . |
| 23 | GND | Ground (0 V) Reference. |
| 24 | V _{SS} | Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect this pin to GND. |
| 25 to 40 | S1B to S16B | Source Terminal. This pin may be an input or output. |
| 41 | DB | Drain Terminal. This pin may be an input or output. |
| 42, 44 | NIC | Not Internally Connected. Do not connect to this pin. |
| 43 | DA | Drain Terminal. This pin may be an input or output. |
| | EPAD | Exposed Pad. The exposed pad must be connected to GND. |



- NOTES**
 1. NIC = NOT INTERNALLY CONNECTED. DO NOT CONNECT TO THIS PIN.
 2. THE EXPOSED PAD MUST BE CONNECTED TO GND.

Figure 7. ADG732 Pin Configuration

02765-004

Table 9. ADG732 Pin Function Description

| Pin No. | Mnemonic | Description |
|-----------------------------|------------------------------|---|
| 1 to 12, 45 to 48 13, 14 | S16 to S1 V _{DD} | Source Terminal. This pin may be an input or output. Most Positive Power Supply Potential. |
| 15 to 19 | A0 to A4 | Logic Control Inputs. |
| 20 | \overline{CS} | Chip Select Pin. \overline{CS} is active low. |
| 21 | \overline{WR} | Write Pin. When \overline{WR} is low, the logic control inputs (A0 to A4) control which state the switches are in. On the rising edge of \overline{WR} , the logic control input data is latched. |
| 22 | \overline{EN} | Active Low, Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, the Ax logic control inputs determine the on switches. The EN input signal is not latched by \overline{WR} . |
| 23 | GND | Ground (0 V) Reference. |
| 24 | V _{SS} | Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect this pin to GND. |
| 25 to 40 | S17 to S32 | Source Terminal. This pin may be an input or output. |
| 41, 42, 44 | NIC | Not Internally Connected. Do not connect to this pin. |
| 43 | D | Drain Terminal. This pin may be an input or output. |
| | EPAD | Exposed Pad. The exposed pad must be connected to GND. |

Truth Tables

Table 10. ADG726 Truth Table

| A3 ¹ | A2 ¹ | A1 ¹ | A0 ¹ | \overline{EN} ¹ | \overline{CSA} | \overline{CSB} | \overline{WR} ¹ | On Switch |
|-----------------|-----------------|-----------------|-----------------|------------------------------|------------------|------------------|------------------------------|-------------------------------|
| X | X | X | X | X | 1 | 1 | L → H | Latches control input data |
| X | X | X | X | X | 1 | 1 | X | No change in switch condition |
| X | X | X | X | 1 | X | X | X | None |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | S1A to DA, S1B to DB |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | S2A to DA, S2B to DB |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | S3A to DA, S3B to DB |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | S4A to DA, S4B to DB |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | S5A to DA, S5B to DB |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | S6A to DA, S6B to DB |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | S7A to DA, S7B to DB |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | S8A to DA, S8B to DB |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | S9A to DA, S9B to DB |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | S10A to DA, S10B to DB |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | S11A to DA, S11B to DB |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | S12A to DA, S12B to DB |

| A3 ¹ | A2 ¹ | A1 ¹ | A0 ¹ | EN ¹ | CSA | CSB | WR ¹ | On Switch |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----|-----|-----------------|------------------------|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | S13A to DA, S13B to DB |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | S14A to DA, S14B to DB |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | S15A to DA, S15B to DB |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | S16A to DA, S16B to DB |

¹ X is don't care, L is low, and H is high.

Table 11. ADG732 Truth Table

| A4 ¹ | A3 ¹ | A2 ¹ | A1 ¹ | A0 ¹ | EN ¹ | CS | WR ¹ | Switch Condition |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----|-----------------|-------------------------------|
| X | X | X | X | X | X | 1 | L → H | Latches control input data |
| X | X | X | X | X | X | 1 | X | No change in switch condition |
| X | X | X | X | X | 1 | X | X | None |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 2 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 3 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 4 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 5 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 6 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 8 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 9 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 10 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 11 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 12 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 13 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 14 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 15 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 16 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 17 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 18 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 19 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 20 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 21 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 22 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 23 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 24 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 25 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 26 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 27 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 28 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 29 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 30 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 31 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 32 |

¹ X is don't care, L is low, and H is high.

TYPICAL PERFORMANCE CHARACTERISTICS

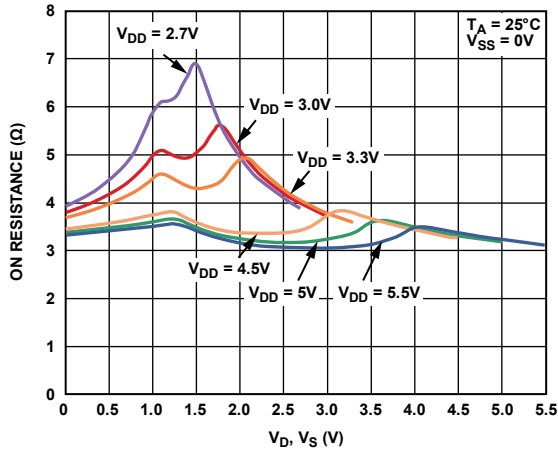


Figure 8. On Resistance vs. V_D (V_S), Single Supply

02765-006

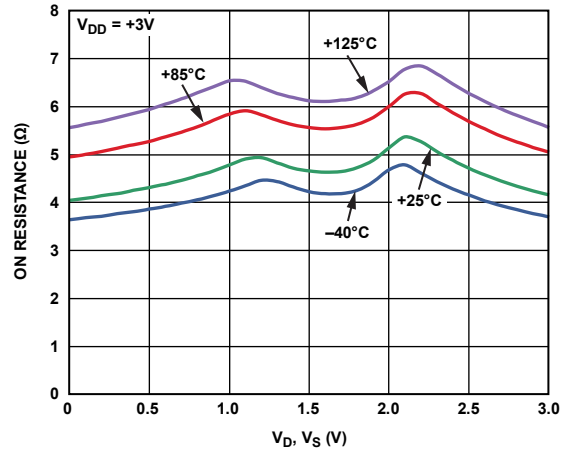


Figure 11. On Resistance vs. V_D (V_S), Single Supply

02765-009

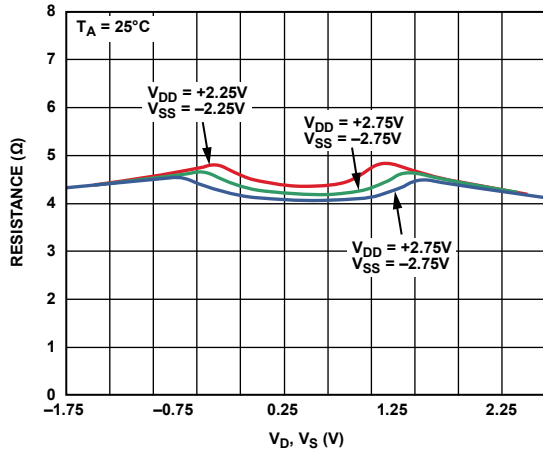


Figure 9. On Resistance vs. V_D (V_S), Dual Supply

02765-007

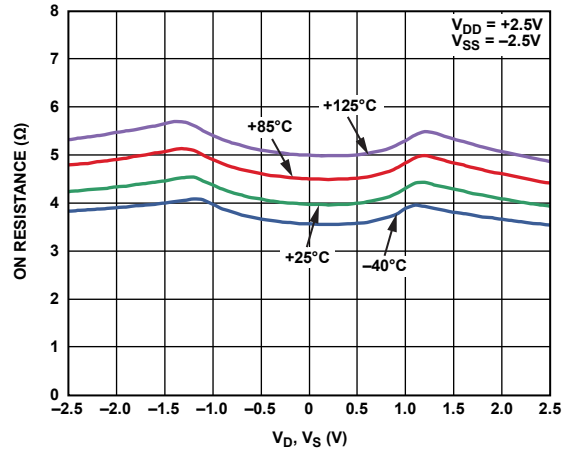


Figure 12. On Resistance vs. V_D (V_S), Dual Supply

02765-010

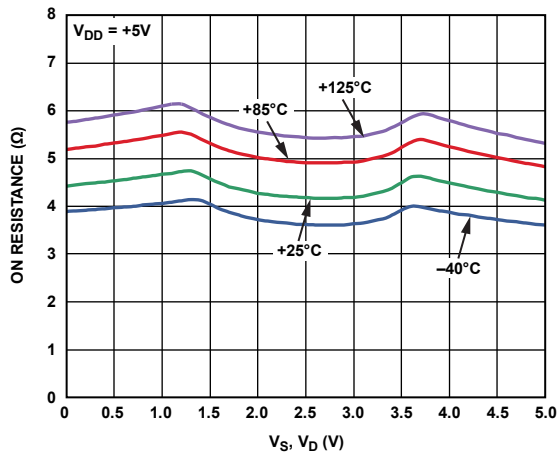


Figure 10. On Resistance vs. V_D (V_S) for Different Temperatures, Single Supply

02765-008

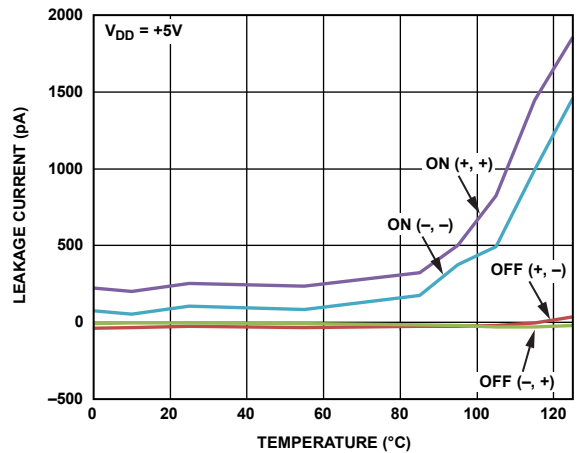


Figure 13. Leakage Currents vs. Temperature

02765-011

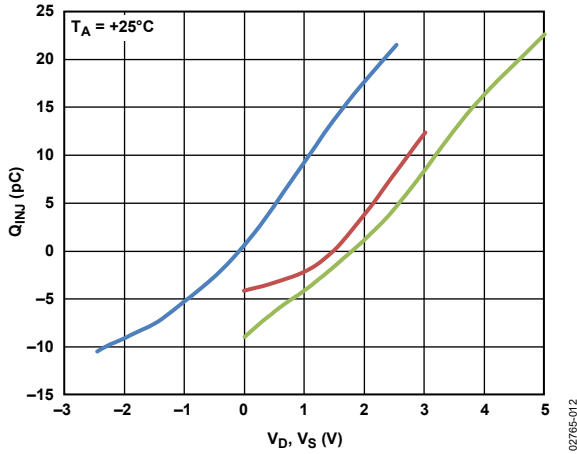


Figure 14. ADG732 Charge Injection (Q_{INJ}) vs. V_D , V_S

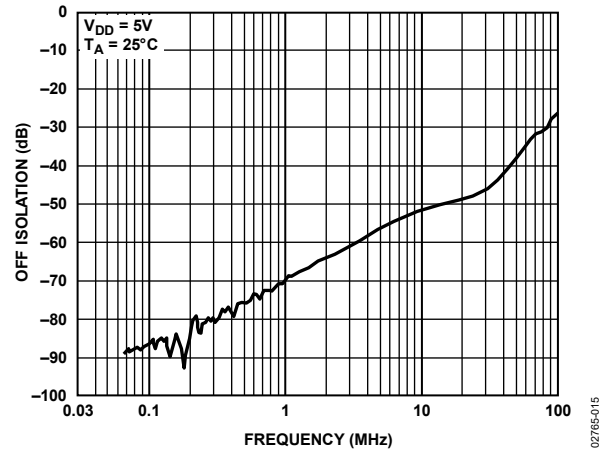


Figure 17. Off Isolation vs. Frequency

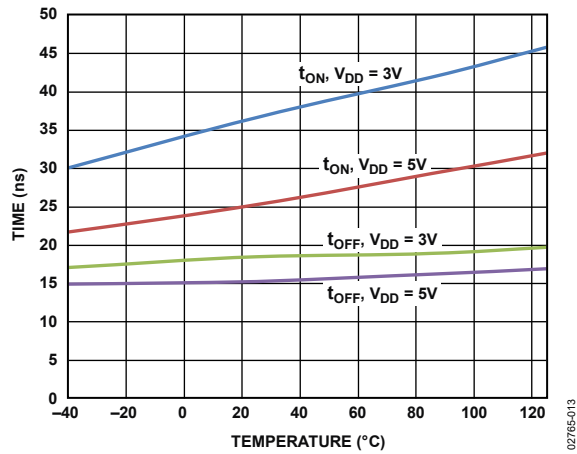


Figure 15. t_{ON}/t_{OFF} (\overline{EN}) Time vs. Temperature

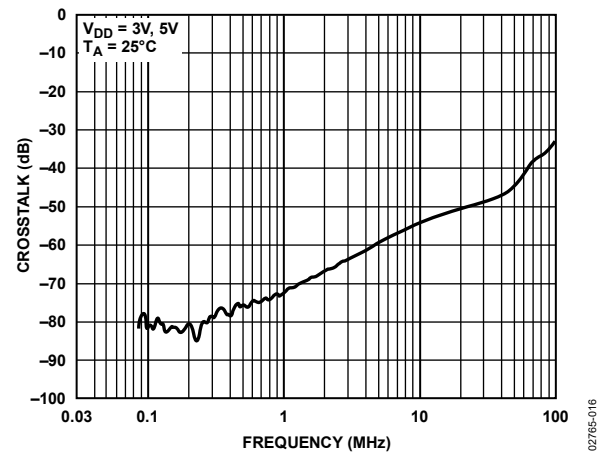


Figure 18. Crosstalk vs. Frequency

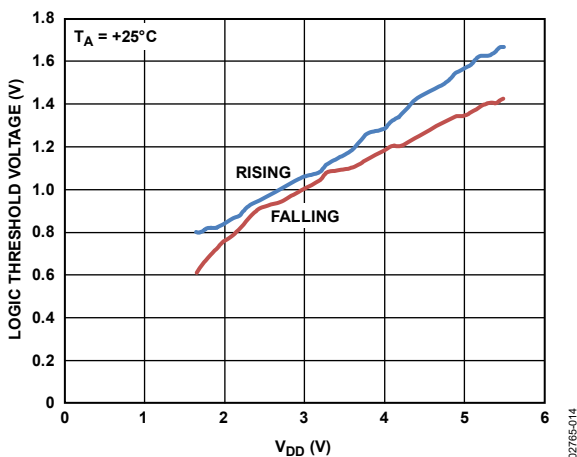


Figure 16. Logic Threshold Voltage vs. Supply Voltage (V_{DD})

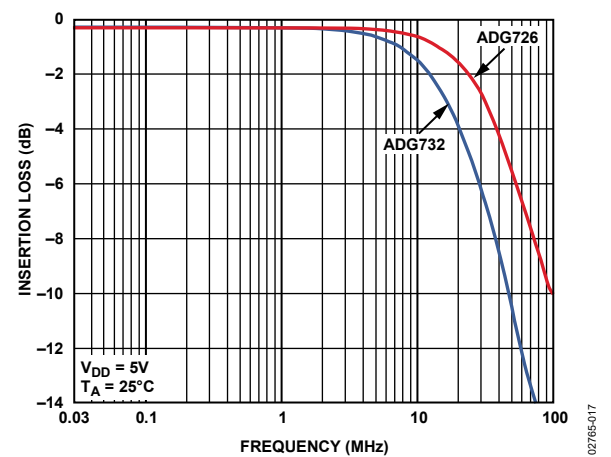


Figure 19. Insertion Loss vs. Frequency

TEST CIRCUITS

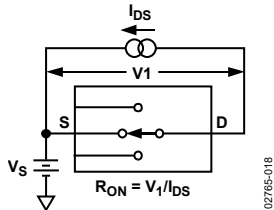


Figure 20. On Resistance

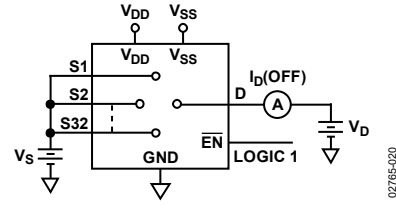


Figure 24. Ib (Off)

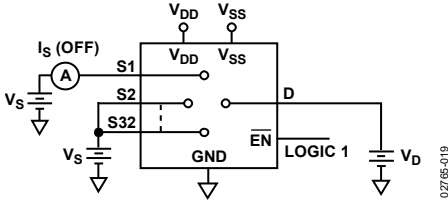


Figure 21. Is (Off)

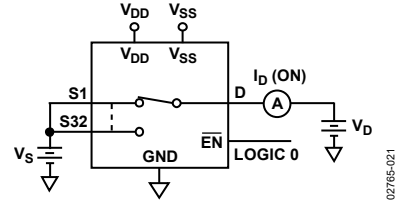
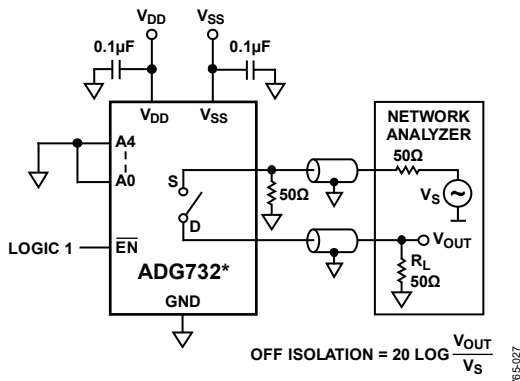
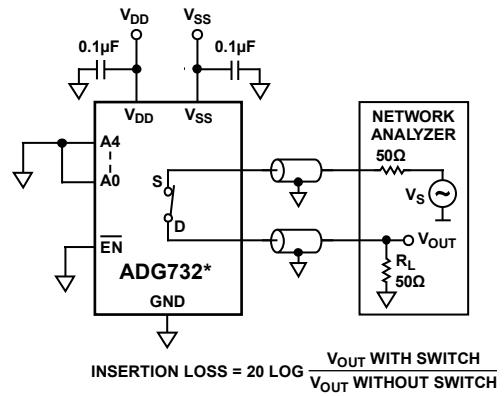


Figure 25. Ib (On)



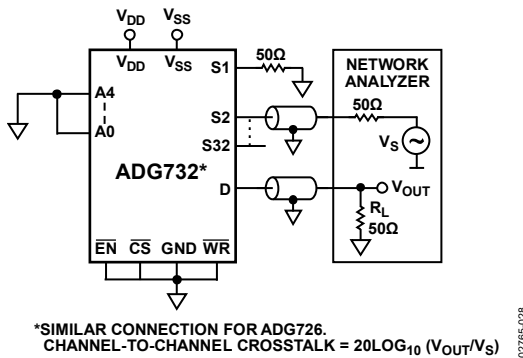
*SIMILAR CONNECTION FOR ADG726.

Figure 22. Off Isolation



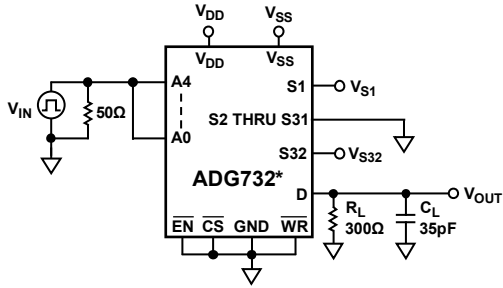
*SIMILAR CONNECTION FOR ADG726.

Figure 26. Bandwidth



*SIMILAR CONNECTION FOR ADG726.
CHANNEL-TO-CHANNEL CROSSTALK = 20LOG₁₀ (V_{OUT}/V_S)

Figure 23. Channel-to-Channel Crosstalk



*SIMILAR CONNECTION FOR ADG726.

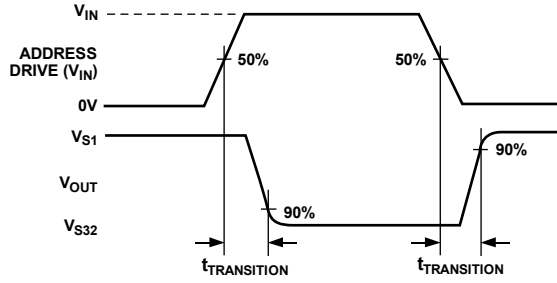
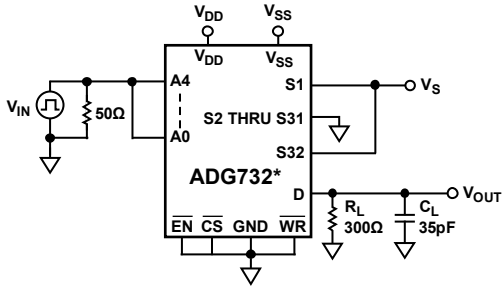


Figure 27. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$

02765-022



*SIMILAR CONNECTION FOR ADG726.

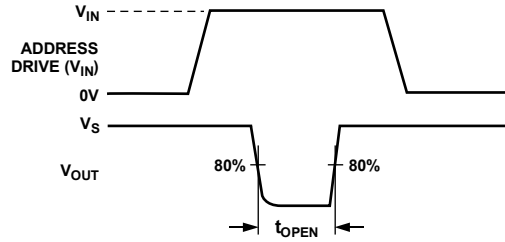
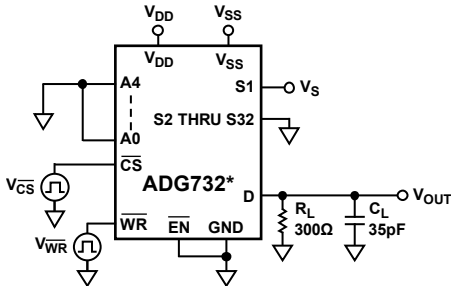


Figure 28. Break-Before-Make Delay, t_{OPEN}

02765-023



*SIMILAR CONNECTION FOR ADG726.

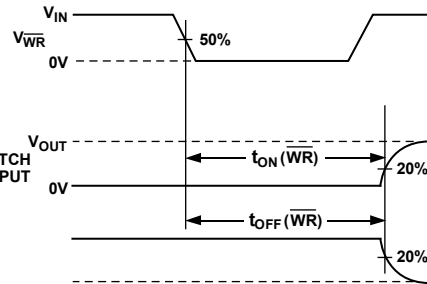
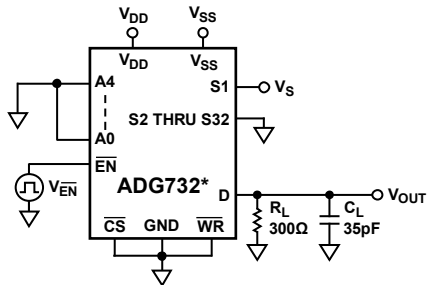


Figure 29. Write Turn-On and Turn-Off Time, $t_{\text{ON}}(\overline{\text{WR}})$, $t_{\text{OFF}}(\overline{\text{WR}})$

02765-024



*SIMILAR CONNECTION FOR ADG726.

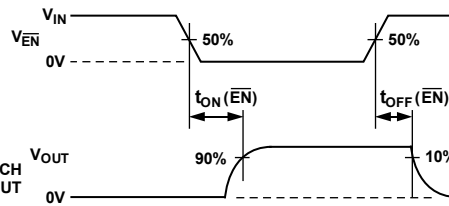
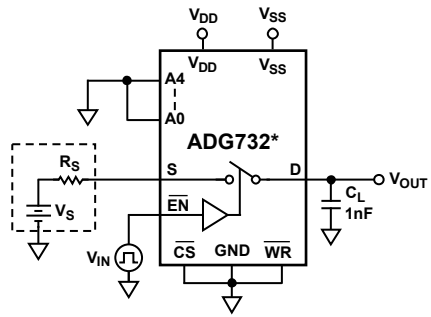
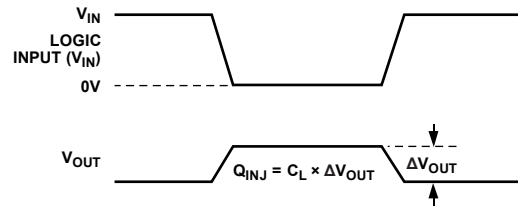


Figure 30. Enable Delay, $t_{\text{ON}}(\overline{\text{EN}})$, $t_{\text{OFF}}(\overline{\text{EN}})$

02765-025



*SIMILAR CONNECTION FOR ADG726.



02785-028

Figure 31. Charge Injection

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

IN

IN represents the logic control input.

V_D (V_S)

V_D and V_S represent the analog voltage on the Dx pins and the Sx pins, respectively.

R_{ON}

R_{ON} represents the ohmic resistance between the Dx pins and the Sx pins.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

$R_{FLAT(ON)}$ is the flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

I_S (Off) represents the source leakage current with the switch off.

I_D (Off)

I_D (Off) represents the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL} , I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_S (Off)

C_S (Off) represents the off switch source capacitance. It is measured with a reference to ground.

C_D (Off)

C_D (Off) represents the off switch drain capacitance. It is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent the on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} is the digital input capacitance.

$t_{TRANSITION}$

$t_{TRANSITION}$ is the delay time measured between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{ON} (\overline{EN})

t_{ON} (\overline{EN}) is the delay time between the 50% and 90% points of the \overline{EN} digital input and the switch on condition.

t_{OFF} (\overline{EN})

t_{OFF} (\overline{EN}) is the delay time between the 50% and 90% points of the \overline{EN} digital input and the switch off condition.

t_{OPEN}

t_{OPEN} is the off time measured between the 80% points of both switches when switching from one address state to another

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

Off isolation is a measure of the unwanted signal coupling through an off switch.

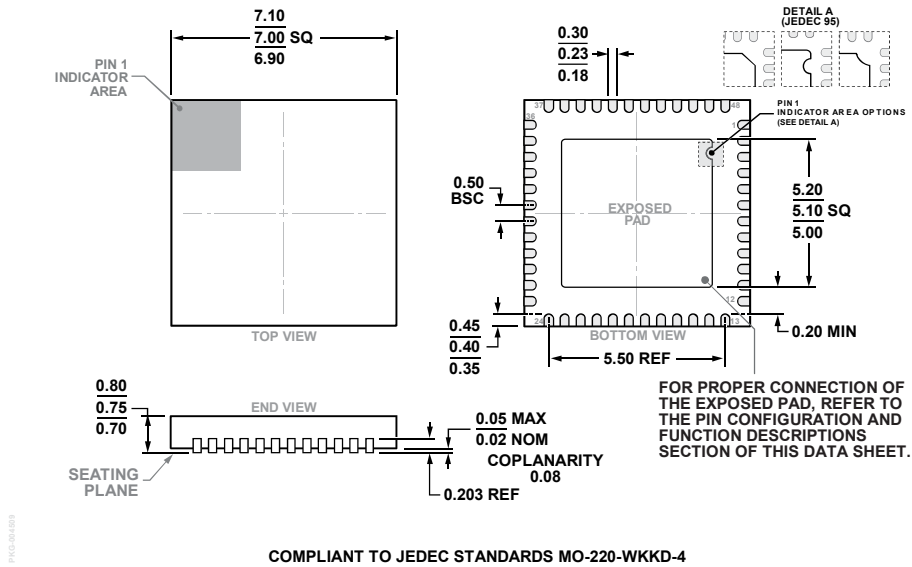
Channel-to-Channel Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

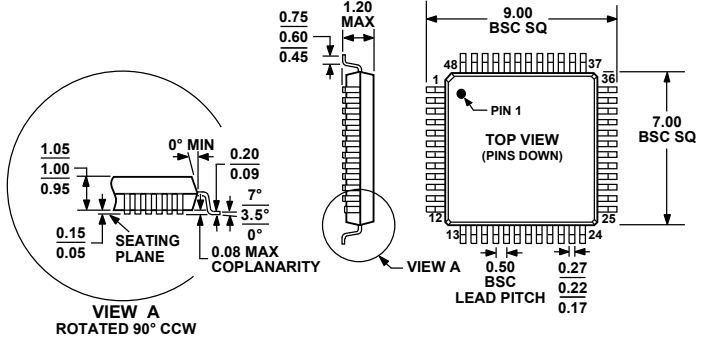
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKGD-4

Figure 32. 48-Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-4)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026ABC

Figure 33. 48-Lead Thin Plastic Quad Flat Package [TQFP]
(SU-48)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADG726BCPZ | -40°C to +85°C | 48-Lead Frame Chip Scale Package [LFCSP] | CP-48-4 |
| ADG726BCPZ-REEL | -40°C to +85°C | 48-Lead Frame Chip Scale Package [LFCSP] | CP-48-4 |
| ADG726BSUZ | -40°C to +85°C | 48-Lead Thin Plastic Quad Flat Package [TQFP] | SU-48 |
| ADG726BSUZ-REEL | -40°C to +85°C | 48-Lead Thin Plastic Quad Flat Package [TQFP] | SU-48 |
| ADG732BCPZ | -40°C to +125°C | 48-Lead Frame Chip Scale Package [LFCSP] | CP-48-4 |
| ADG732BCPZ-REEL | -40°C to +125°C | 48-Lead Frame Chip Scale Package [LFCSP] | CP-48-4 |
| ADG732BSUZ | -40°C to +125°C | 48-Lead Thin Plastic Quad Flat Package [TQFP] | SU-48 |
| ADG732BSUZ-REEL | -40°C to +125°C | 48-Lead Thin Plastic Quad Flat Package [TQFP] | SU-48 |

¹ Z = RoHS-Compliant Part

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