

FEATURES

44 V supply maximum ratings

V_{SS} to V_{DD} analog signal range

Low on resistance (<70 Ω)

Low ΔR_{ON} (9 Ω max)

Low R_{ON} match (3 Ω max)

Low power dissipation

Fast switching times

t_{ON} < 110 ns

t_{OFF} < 60 ns

Low leakage currents (3 nA max)

Low charge injection (6 pC max)

Break-before-make switching action

Latch-up proof A grade

**Plug-in upgrade for DG201A/ADG201A, DG202A/ADG202A,
DG211/ADG211A**

Plug-in replacement for DG441/DG442/DG444

APPLICATIONS

Audio and video switching

Automatic test equipment

Precision data acquisition

Battery-powered systems

Sample-and-hold systems

Communication systems

GENERAL DESCRIPTION

The [ADG441](#), [ADG442](#), and [ADG444](#) are monolithic CMOS devices that comprise of four independently selectable switches. They are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals. High switching speed also makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments. The [ADG441](#), [ADG442](#), and [ADG444](#) contain four independent SPST switches. Each switch of the [ADG441](#) and [ADG444](#) turns on when a logic low is applied to the appropriate control input. The [ADG442](#) switches are turned on with logic high on the appropriate control input. The [ADG441](#) and [ADG444](#) switches differ in that the [ADG444](#) requires a 5 V logic power supply that is applied to the V_L pin. The [ADG441](#) and [ADG442](#) do not have a V_L pin, the logic power supply is generated internally by an on-chip voltage generator.

Rev. B

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FUNCTIONAL BLOCK DIAGRAM

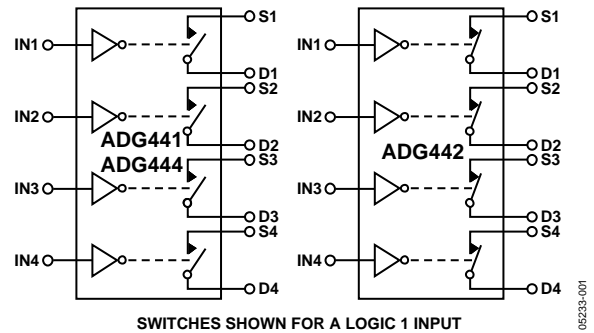


Figure 1.

Each switch conducts equally well in both directions when ON and has an input signal range that extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is the low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended signal range. The [ADG441A/ADG442A/ADG444A](#) are fabricated on an enhanced LC²MOS, trench-isolated process, giving an increased signal range that extends to the supply rails.
2. Low power dissipation.
3. Low R_{ON}.
4. Trench isolation guards against latch-up for A grade parts. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
5. Break-before-make switching. This prevents channel shorting when the switches are configured as a multiplexer.
6. Single-supply operation. For applications where the analog signal is unipolar, the [ADG441/ADG442/ADG444](#) can be operated from a single-rail power supply. The parts are fully specified with a single 12 V power supply.

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REVISION HISTORY

5/14—Rev. A to Rev. B

Updated Outline Dimensions	13
Changes to Ordering Guide	14

5/05—Rev. 0 to Rev. A

Changes to Format	Universal
Deleted CERDIP Package and T Grade	Universal
Changes to Features and Product Highlights	1
Changes to Test Conditions in Table 2	4
Changes to Figure 11	8
Changes to Trench Isolation Section	12
Updated Outline Dimensions	13
Changes to Ordering Guide	14

4/94—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY¹

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $V_L = +5\text{ V} \pm 10\%$ (ADG444), GND = 0 V, unless otherwise noted.

Table 1.

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
R_{ON}	40		Ω typ	$V_D = \pm 8.5\text{ V}$, $I_S = -10\text{ mA}$
	70	85	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
ΔR_{ON}		4	Ω typ	$-8.5\text{ V} \leq V_D \leq +8.5\text{ V}$
		9	Ω max	
R_{ON} Match		1	Ω typ	$V_D = 0\text{ V}$, $I_S = -10\text{ mA}$
		3	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.5	± 3	nA max	$V_D = \pm 15.5\text{ V}$, $V_S = \mp 15.5\text{ V}$
Drain OFF Leakage I_D (OFF)	± 0.01		nA typ	$V_D = \pm 15.5\text{ V}$, $V_S = \mp 15.5\text{ V}$
	± 0.5	± 3	nA max	See Figure 15
Channel ON Leakage I_D , I_S (ON)	± 0.08		nA typ	$V_S = V_D = \pm 15.5\text{ V}$
	± 0.5	± 3	nA max	See Figure 16
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}		± 0.00001	μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.5	μA max	
DYNAMIC CHARACTERISTICS²				
t_{ON}	85		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$;
	110	170	ns max	$V_S = \pm 10\text{ V}$; see Figure 17
t_{OFF}	45		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$;
	60	80	ns max	$V_S = \pm 10\text{ V}$; see Figure 17
t_{OPEN}	30		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$;
Charge Injection	1		pC typ	$V_S = 0\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$;
	6		pC max	$V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$; see Figure 18
OFF Isolation	60		dB typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$; $f = 1\text{ MHz}$; see Figure 19
Channel-to-Channel Crosstalk	100		dB typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$; $f = 1\text{ MHz}$; see Figure 20
C_S (OFF)	4		pF typ	$f = 1\text{ MHz}$
C_D (OFF)	4		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	16		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}				$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
		80	μA max	Digital Inputs = 0 V or 5 V
ADG441/ADG442			μA typ	
ADG444	0.001		μA max	
	1	2.5	μA max	
I_{SS}	0.0001		μA typ	
	1	2.5	μA max	
I_L (ADG444 Only)	0.001		μA typ	$V_L = 5.5\text{ V}$
	1	2.5	μA max	

¹ Temperature range is: B Version: -40°C to +85°C.

² Guaranteed by design, not subject to production test.

SINGLE SUPPLY¹

$V_{DD} = +12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $V_L = +5\text{ V} \pm 10\%$ (ADG444), $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
R_{ON}	70		Ω typ	$V_D = +3\text{ V}, +8\text{ V}, I_S = -5\text{ mA}$
	110	130	Ω max	$V_{DD} = 10.8\text{ V}$
ΔR_{ON}		4	Ω typ	$3\text{ V} \leq V_D \leq 8\text{ V}$
		9	Ω max	
R_{ON} Match		1	Ω typ	$V_D = +6\text{ V}, I_S = -5\text{ mA}$
		3	Ω max	
LEAKAGE CURRENT				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = 13.2\text{ V}$ $V_D = 12.2\text{ V}/1\text{ V}, V_S = 1\text{ V}/12.2\text{ V}$
	± 0.5	± 3	nA max	See Figure 15
Drain OFF Leakage I_D (OFF)	± 0.01		nA typ	$V_D = 12.2\text{ V}/1\text{ V}, V_S = 1\text{ V}/12.2\text{ V}$
	± 0.5	± 3	nA max	See Figure 15
Channel ON Leakage I_D, I_S (ON)	± 0.08		nA typ	$V_S = V_D = 12.2\text{ V}/1\text{ V}$
	± 0.5	± 3	nA max	Figure 16
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}		± 0.00001	μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.5	μA max	
DYNAMIC CHARACTERISTICS²				
t_{ON}	105		ns typ	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$
	150	220	ns max	$V_S = 8\text{ V}$; Figure 17
t_{OFF}	40		ns typ	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$
	60	100	ns max	$V_S = 8\text{ V}$; Figure 17
t_{OPEN}	50		ns typ	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$
Charge Injection	2		pC typ	$V_S = 6\text{ V}, R_S = 0\ \Omega, C_L = 1\text{ nF}$
	6		pC max	$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$; see Figure 18
OFF Isolation	60		dB typ	$R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$; see Figure 19
Channel-to-Channel Crosstalk	100		dB typ	$R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$; see Figure 20
C_S (OFF)	7		pF typ	$f = 1\text{ MHz}$
C_D (OFF)	10		pF typ	$f = 1\text{ MHz}$
C_D, C_S (ON)	16		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}				$V_{DD} = 13.2\text{ V}$ Digital Inputs = 0 V or 5 V
ADG441/ADG442		80	μA max	
ADG444	0.001		μA typ	
	1	2.5	μA max	
I_L (ADG444 Only)	0.001		μA typ	$V_L = 5.5\text{ V}$
	1	2.5	μA max	

¹ Temperature range is: B Version: -40°C to $+85^\circ\text{C}$.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	44 V
V_{DD} to GND	-0.3 V to +25 V
V_{SS} to GND	+0.3 V to -25 V
V_L to GND	-0.3 V to $V_{DD} + 0.3$ V
Analog, Digital Inputs	$V_{SS} - 2$ V to $V_{DD} + 2$ V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	100 mA
Operating Temperature Range Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature, Soldering (10 sec)	300°C
Plastic Package, Power Dissipation	470 mW
θ_{JA} , Thermal Impedance	177°C/W
Lead Temperature, Soldering (10 sec)	260°C
SOIC Package, Power Dissipation	600 mW
θ_{JA} , Thermal Impedance	77°C/W
Lead Temperature, Soldering Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Truth Table

ADG441/ADG444 IN	ADG442 IN	Switch Condition
0	1	ON
1	0	OFF

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

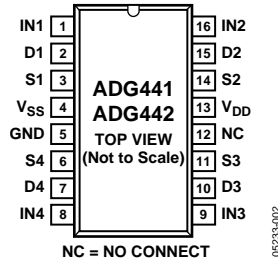


Figure 2. ADG441/ADG442 (DIP/SOIC)

Table 5. ADG441/ADG442 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16	IN1 to IN4	Logic Control Input.
2, 7, 10, 15	D1 to D4	Drain Terminal. May be an input or output.
3, 6, 11, 14	S1 to S4	Source Terminal. May be an input or output.
4	V _{SS}	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it may be connected to ground.
5	GND	Ground (0 V) Reference.
12	NC	No Connect.
13	V _{DD}	Most Positive Power Supply Potential.

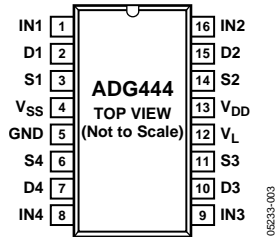


Figure 3. ADG444 (DIP/SOIC)

Table 6. ADG444 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16	IN1 to IN4	Logic Control Input.
2, 7, 10, 15	D1 to D4	Drain Terminal. May be an input or output.
3, 6, 11, 14	S1 to S4	Source Terminal. May be an input or output.
4	V _{SS}	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it may be connected to ground.
5	GND	Ground (0 V) Reference.
12	V _L	Logic Power Supply (5 V).
13	V _{DD}	Most Positive Power Supply Potential.

TYPICAL PERFORMANCE CHARACTERISTICS

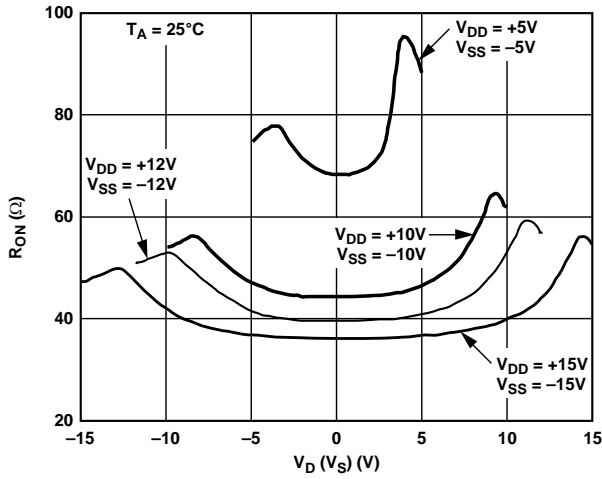


Figure 4. R_{ON} as a Function of V_D (V_S): Dual Supply

06233-005

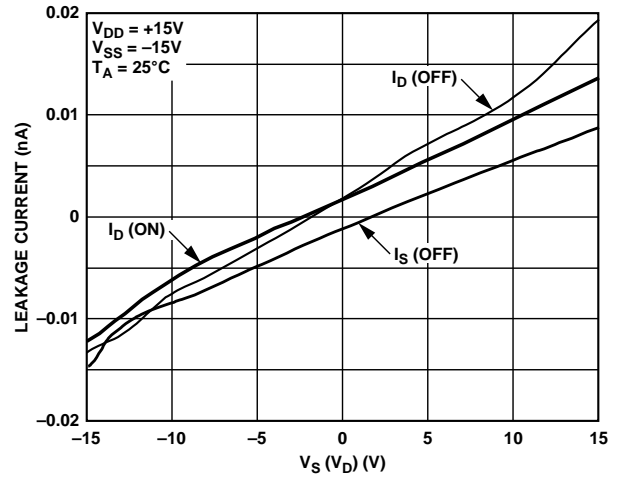


Figure 7. Leakage Currents as a Function of V_S (V_D)

06233-006

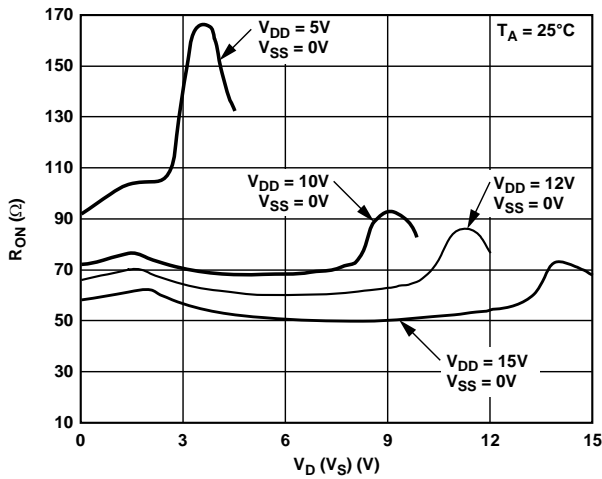


Figure 5. R_{ON} as a Function of V_D (V_S): Single Supply

06233-006

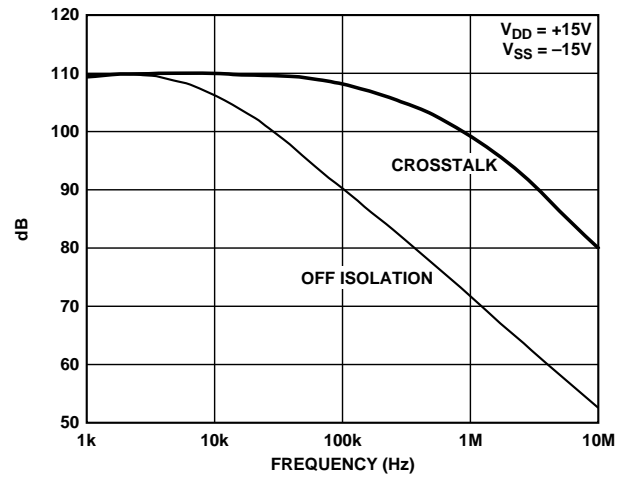


Figure 8. Crosstalk and Off Isolation vs. Frequency

06233-009

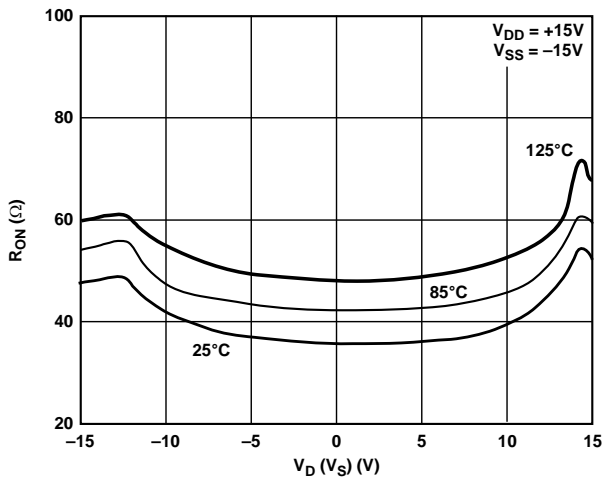


Figure 6. R_{ON} as a Function of V_D (V_S) for Different Temperatures

06233-007

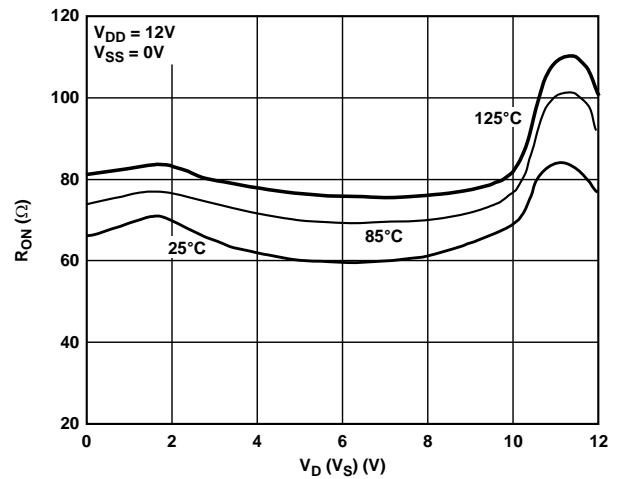


Figure 9. R_{ON} as a Function of V_D (V_S) for Different Temperatures

06233-010

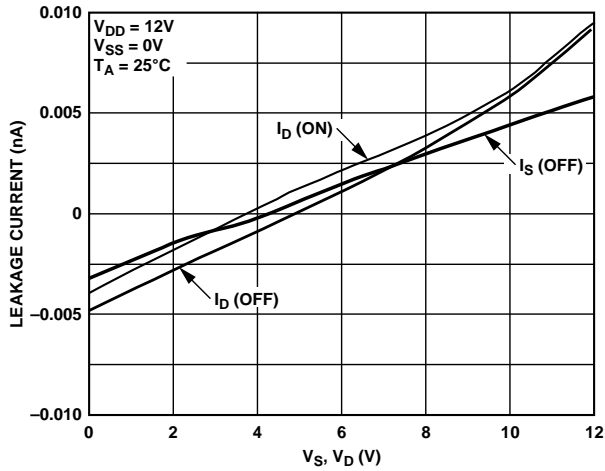


Figure 10. Leakage Currents as a Function of V_S (V_D)

05233-011

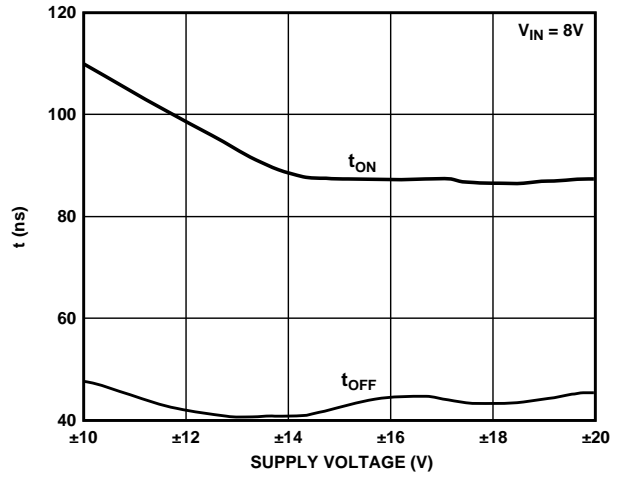


Figure 12. Switching Time vs. Bipolar Supply

05233-013

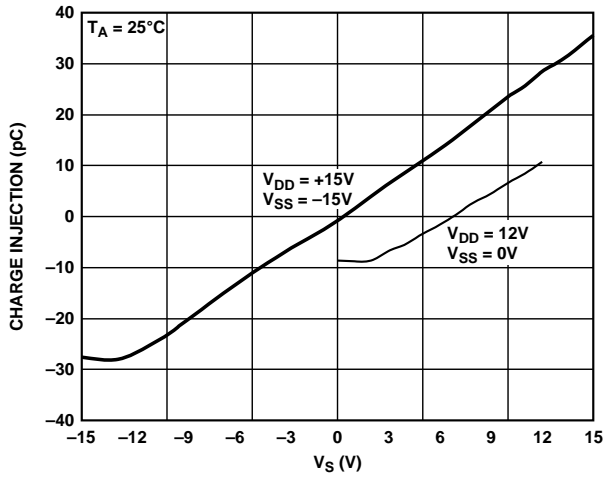


Figure 11. Charge Injection vs. Source Voltage

05233-012

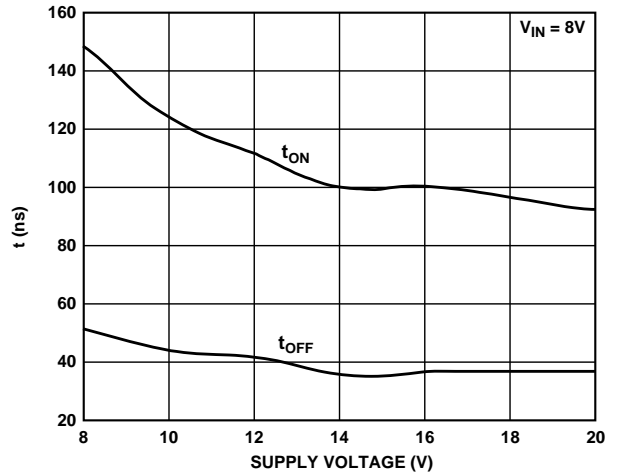


Figure 13. Switching Time vs. Single Supply

05233-014

TEST CIRCUITS

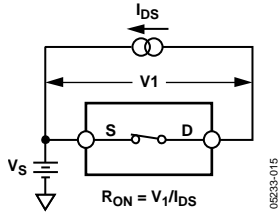


Figure 14. On Resistance

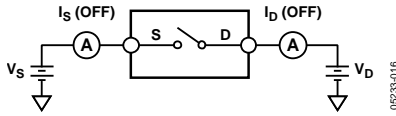


Figure 15. Off Leakage

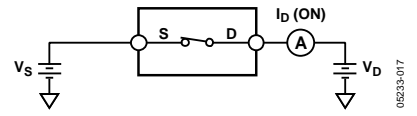


Figure 16. On Leakage

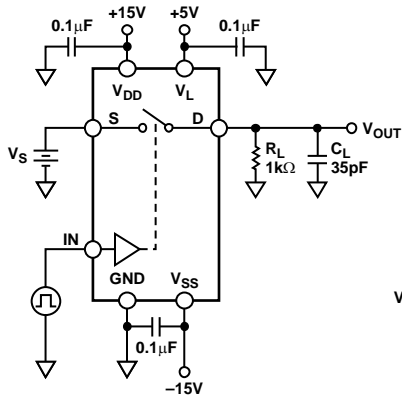


Figure 17. Switching Times

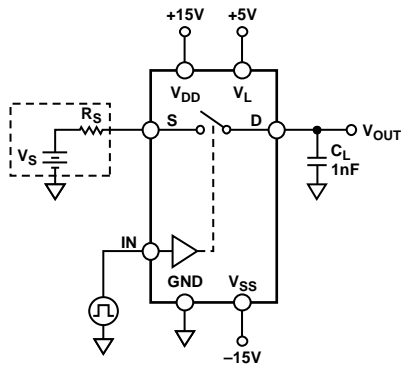
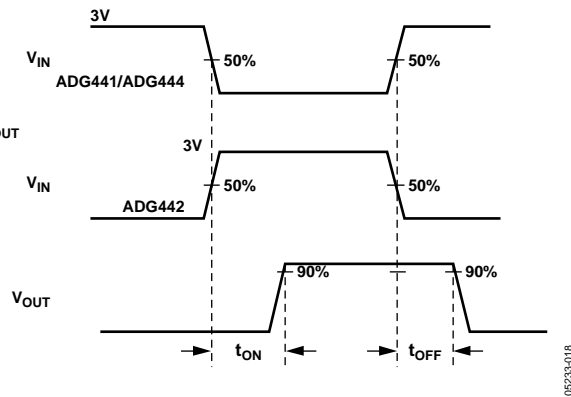
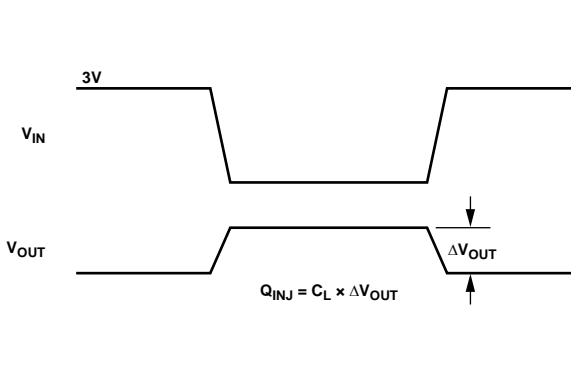
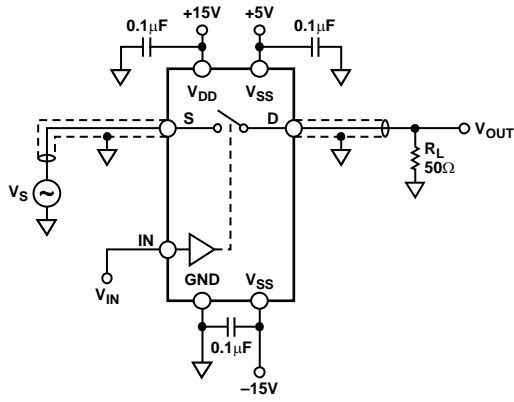


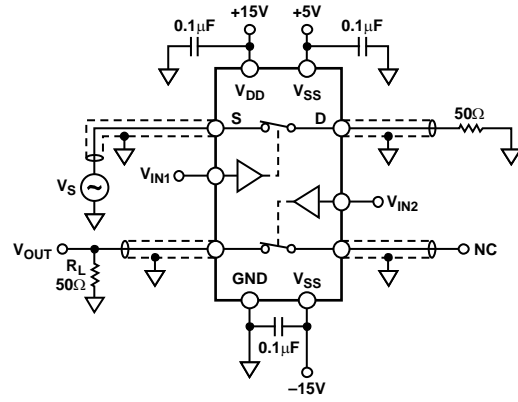
Figure 18. Charge Injection





05233-021

Figure 19. Off Isolation



05233-022

CHANNEL-TO-CHANNEL CROSSTALK = $20 \times \text{LOG} |V_S/V_{OUT}|$

Figure 20. Channel-to-Channel Crosstalk

TERMINOLOGY

R_{ON}

Ohmic resistance between D and S.

R_{ON Match}

Difference between the R_{ON} of any two channels.

I_S (OFF)

Source leakage current with the switch OFF.

I_D (OFF)

Drain leakage current with the switch OFF.

I_D, I_S (ON)

Channel leakage current with the switch ON.

V_D (V_S)

Analog voltage on Terminals D, S.

C_S (OFF)

OFF switch source capacitance.

C_D (OFF)

OFF switch drain capacitance.

C_D, C_S (ON)

ON switch capacitance.

t_{ON}

Delay between applying the digital control input and the output switching on.

t_{OFF}

Delay between applying the digital control input and the output switching off.

t_{OPEN}

Break-before-make delay when switches are configured as a multiplexer.

Crosstalk

A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an OFF switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

TRENCH ISOLATION

In the [ADG441A](#), [ADG442A](#), and [ADG444A](#), an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward-biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

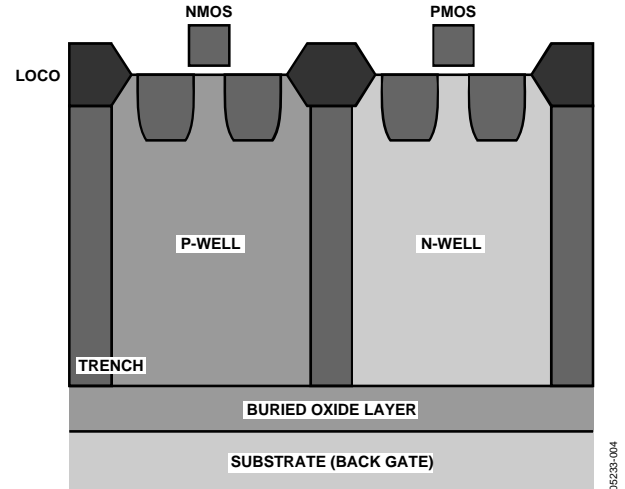
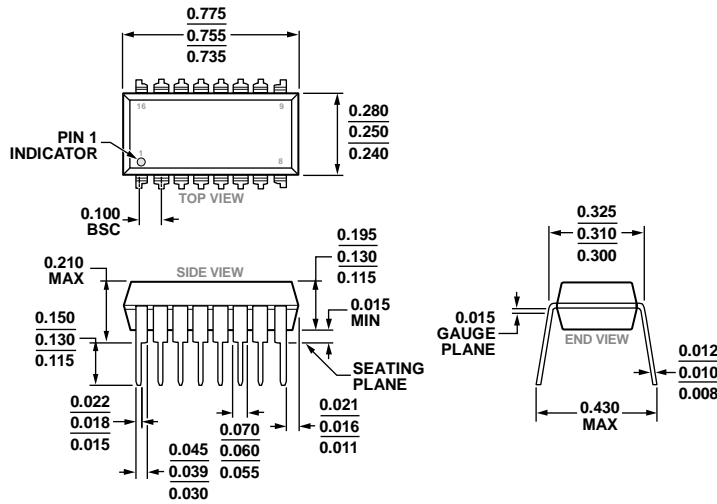


Figure 21. Trench Isolation

OUTLINE DIMENSIONS

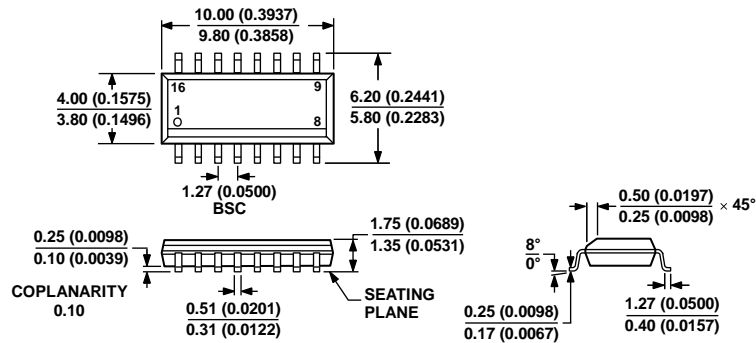


COMPLIANT TO JEDEC STANDARDS MS-001-BB

Figure 22. 16-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-16)

Dimensions shown in inches

03-07-2014-D



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 23. 16-Lead Standard Small Outline Package [SOIC_N] (R-16)

Dimensions shown in millimeters and (inches)

060606-A

ORDERING GUIDE

Model ^{1,2}	Temperature Range	Package Description	Package Option
ADG441BNZ	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG441BR	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG441BR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG441BRZ	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG441BRZ-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG441ABCHIPS		DIE	
ADG441ABR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG441ABRZ-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG442BNZ	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG442BRZ	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG442BRZ-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG444BNZ	-40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG444BR	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG444BR-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG444BRZ	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG444BRZ-REEL	-40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16

¹ Z = RoHS Compliant Part.

² A = Trench isolated.

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