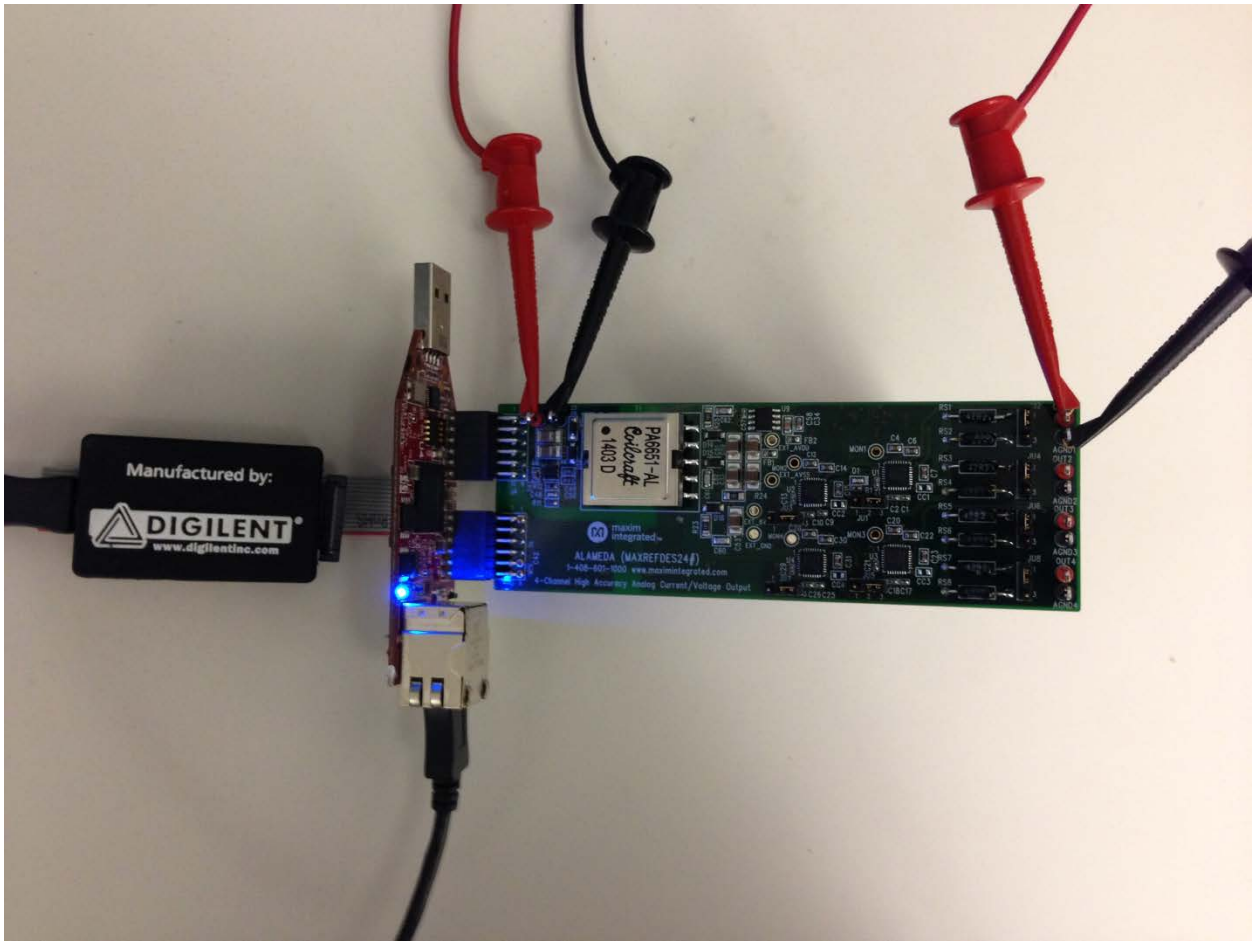
Alameda (MAXREFDES24#) LX9 MicroBoard Quick Start Guide

Rev 0; 3/14



Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000

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1. Required Equipment

- PC with Windows® OS with Xilinx® ISE®/SDK version 14.2 or later and two USB ports (Refer to Xilinx AR# 51895 if you installed ISE WebPACK™ design software on your PC.)
- License for Xilinx EDK/SDK version 14.2 or later (free WebPACK license is OK)
- Alameda (MAXREFDES24#) board
- Avnet Spartan®-6 LX9 MicroBoard
- One +24V 1A DC power supply
- One 750Ω 0.25W resistor

2. Overview

Below is a high-level overview of the steps required to quickly get the Alameda design running by downloading and running the FPGA project. Detailed instructions for each step are provided in the following pages. **The Alameda (MAXREFDES24#) subsystem reference design will be referred to as Alameda throughout this document.**

1) Connect the Alameda board to the J4 and J5 ports of an LX9 MicroBoard as shown in Figure 1. Ensure the connector is aligned as shown in Figure 2. The communication between the Alameda board and the LX9 MicroBoard is through the pins on the J4 connector. The J5 connector is for the board physical support only.
2) Download the latest **RD24V01_00.ZIP** file located at the Alameda page.
3) Extract the **RD24V01_00.ZIP** file to a directory on your PC.
4) Open the Xilinx SDK.
5) Download the bitstream (.BIT) file to the board. This bitstream contains the FPGA hardware design and software bootloader.
6) Open a terminal program to communicate with FPGA board.
7) Use Xilinx SDK to download and run the executable file (.ELF) on the MicroBlaze™.

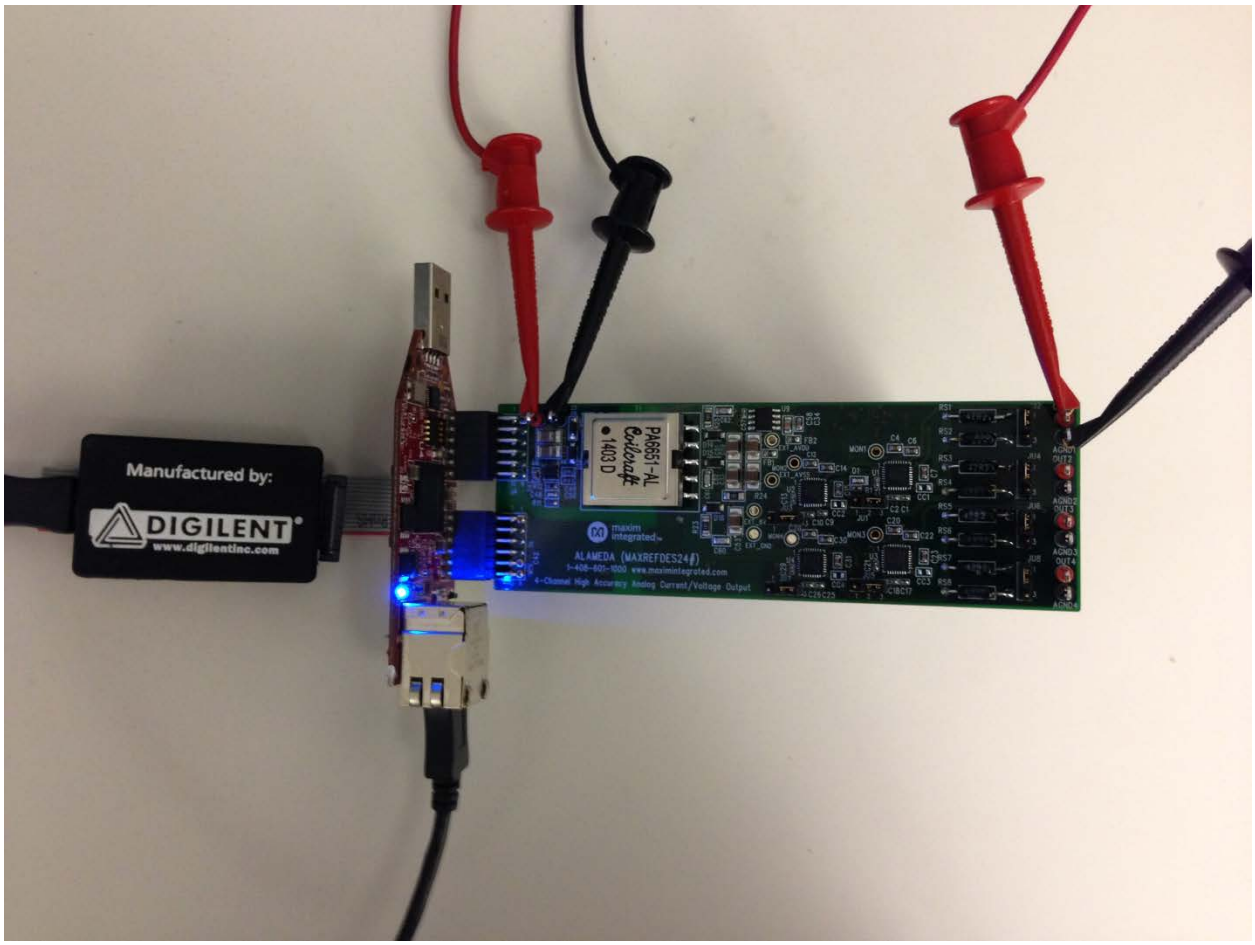


Figure 1. Alameda Board Connected to LX9 Kit

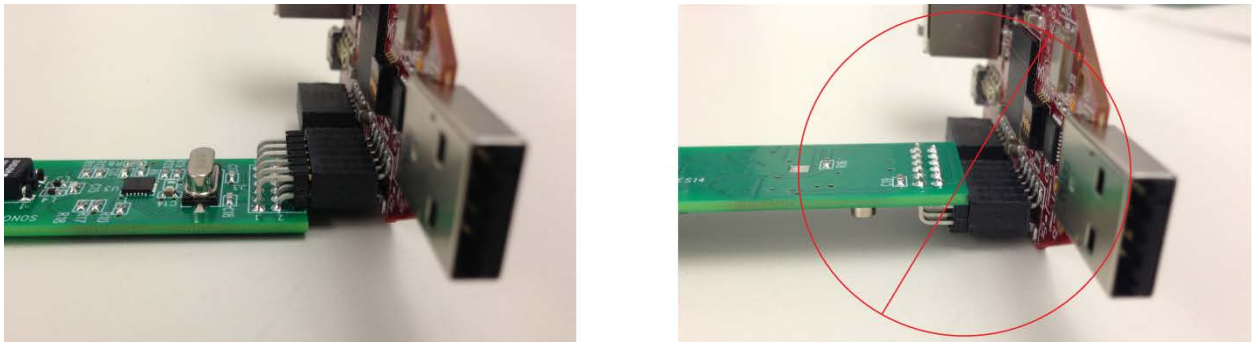


Figure 2. Pmod™ Connector Alignment

3. Included Files

The top level of the hardware design is a Xilinx ISE Project Navigator Project (.XISE) for Xilinx ISE version 14.2. The Verilog-based HDL design instantiates the MicroBlaze core, the support hardware required to run the MicroBlaze, and the peripherals that interface to the Pmod ports. Software is supplied as a Xilinx software development kit (SDK) project that includes a demonstration software application to evaluate the Alameda subsystem reference design. The lower level c-code driver routines are portable to the user's own software project.

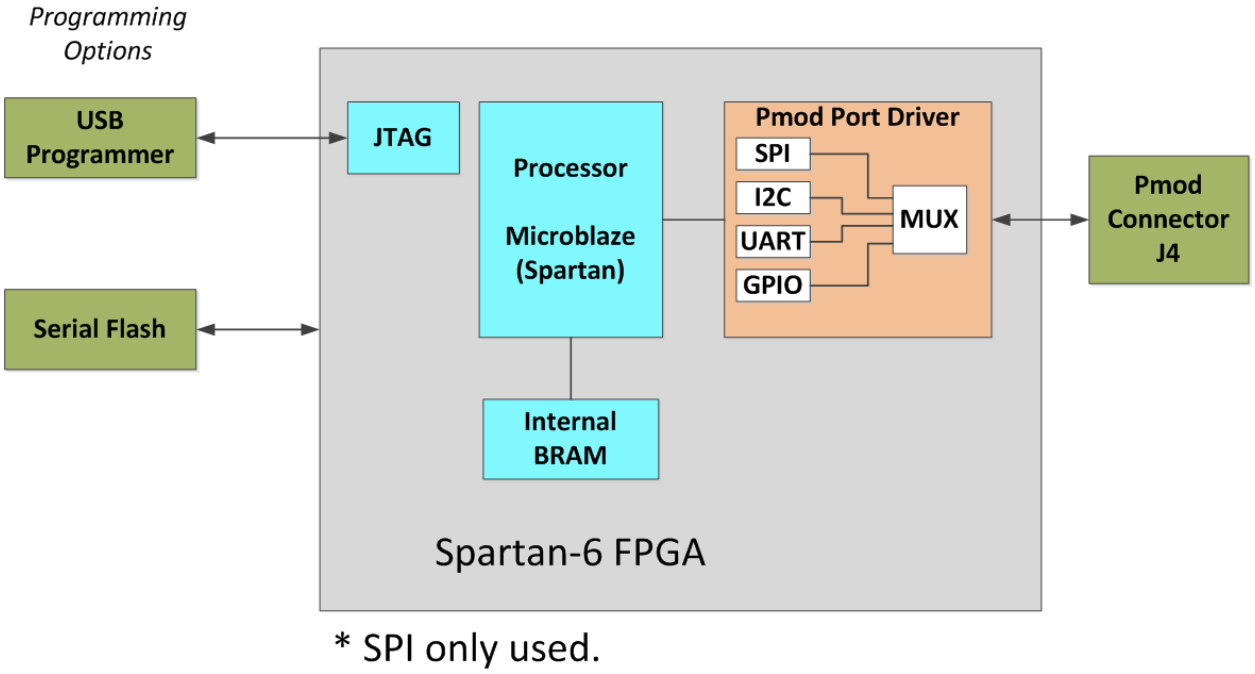


Figure 3. Block Diagram of FPGA Hardware Design

4. Procedure

1. Connect the Alameda board to the J4 and J5 ports of an LX9 MicroBoard as shown in Figure 1.

2. Connect the +24V power supply positive terminal and the ground terminal to the +24V and the PGND connectors on the Alameda board, respectively.

3. Connect one end of the 750Ω load resistor to the OUT1 connector on the Alameda board. Connect the other end of the 750Ω load resistor to the AGND1 connector on the Alameda board.

4. Verify that the JU1, JU3, JU5, and JU7 jumpers are on the 2-3 position.

5. Verify that the JU2, JU4, JU6, and JU8 jumpers are on the 1-2 position.

6. Connect the J3 USB connector of the LX9 MicroBoard to a PC. This connection is used to communicate with a PC through a terminal program. See step 16 for USB driver installation.

7. Connect the J6 JTAG connector of the LX9 MicroBoard to a PC through a Xilinx programming cable. This connection is used to program and debug the FPGA.

8. Download the latest **RD24V01_00.ZIP** file at **www.maximintegrated.com/Alameda**. All files available for download are available at the bottom of the page.

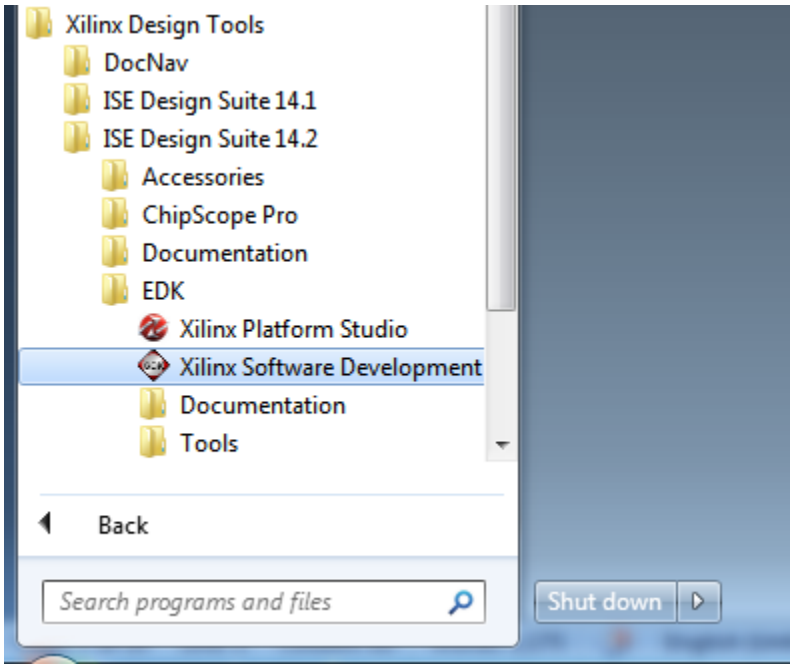
9. Extract the **RD24V01_00.ZIP** file to a directory on your PC. The location is arbitrary but the maximum path length limitation in Windows (260 characters) should not be exceeded.

   In addition, the Xilinx tools require the path to not contain any spaces.

   C:\Do Not Use Spaces In The Path\RD24V01_00.ZIP
   (This path has spaces.)

   For the purposes of this document, it will be **C:\designs\maxim\RD24V01_00**. See **Appendix A: Project Structure and Key Filenames** in this document for the project structure and key filenames.

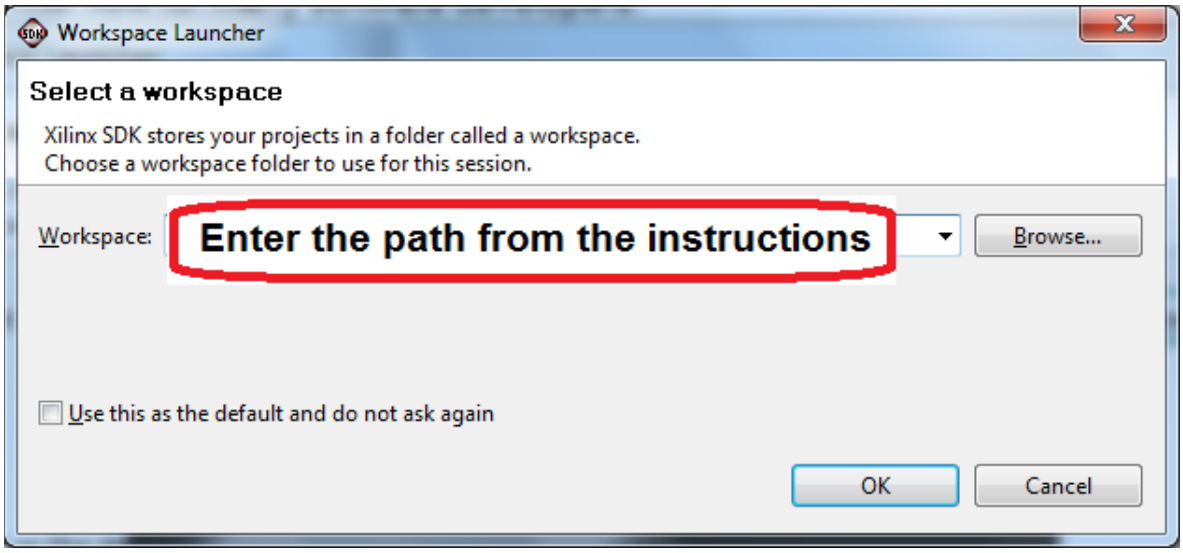
10. Open the **Xilinx Software Development Kit (SDK)** from the Windows **Start** menu.



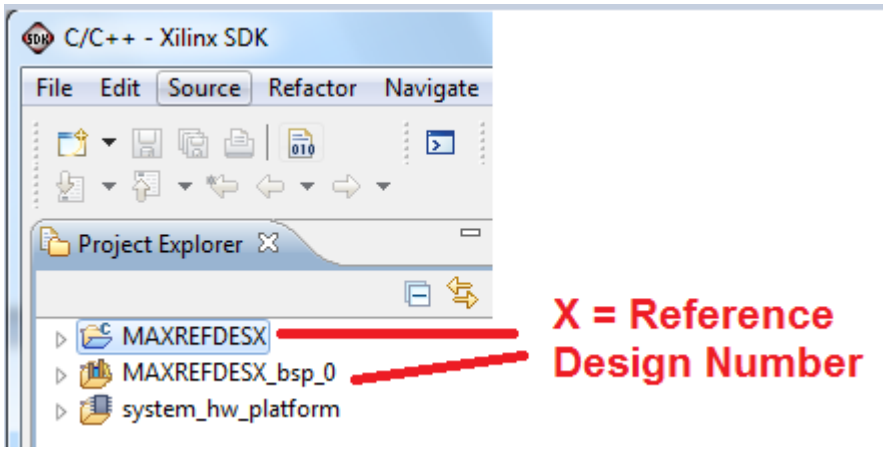
11. SDK will prompt for a workspace directory, which is the location where the software project is located. For this example, it is:

C:\designs\maxim\RD24V01_00\RD24_LX9_V01_00\Design_Files\sdkWorkspace

Click **OK** and SDK will open. The Xilinx SDK is based on an Eclipse™-based IDE, so it will be a familiar flow for many software developers.



12. Review the SDK IDE. The **Project Explorer** in the upper left tab should have three components as shown in the image below. If all three subfolders are present, you can skip the next step.

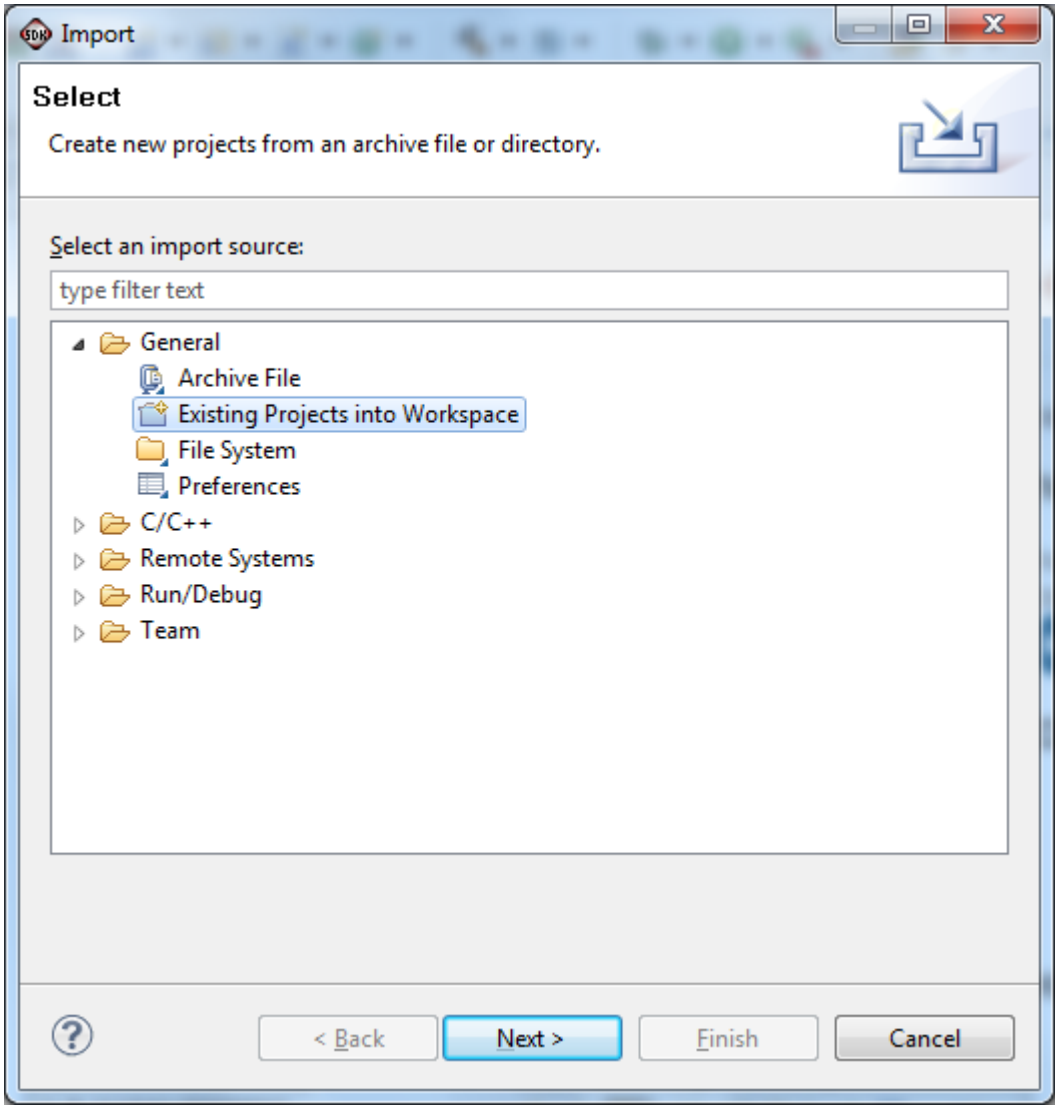


13. If the **Project Explorer** does not contain these three subfolders, launch the **File | Import** menu, expand the **General** folder, and select **Existing Projects into Workspace**. Click **Next**. Set the root directory to:

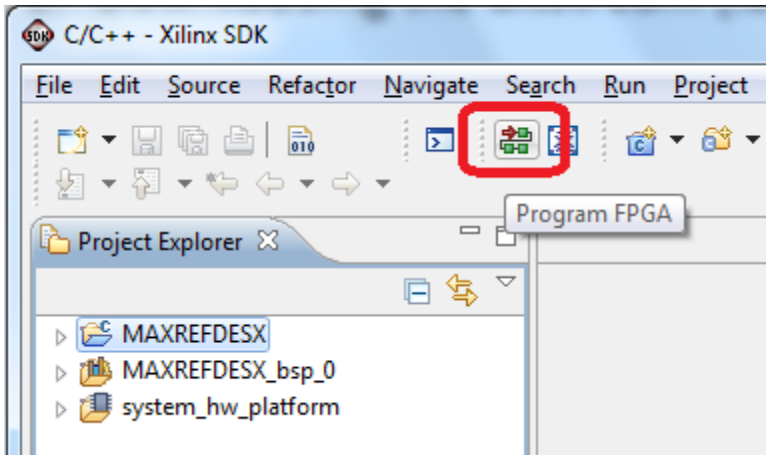
    C:\designs\maxim\RD24V01_00\RD24_LX9_V01_00\Design_Files\sdkWorkspace

    and the missing projects should appear in SDK **Project Explorer** with their checkboxes checked.

    Click **Finish** to import the projects.



14. To download the bitstream (.BIT) file to the board, click on the **Program FPGA** icon (which looks like a green chain of devices).

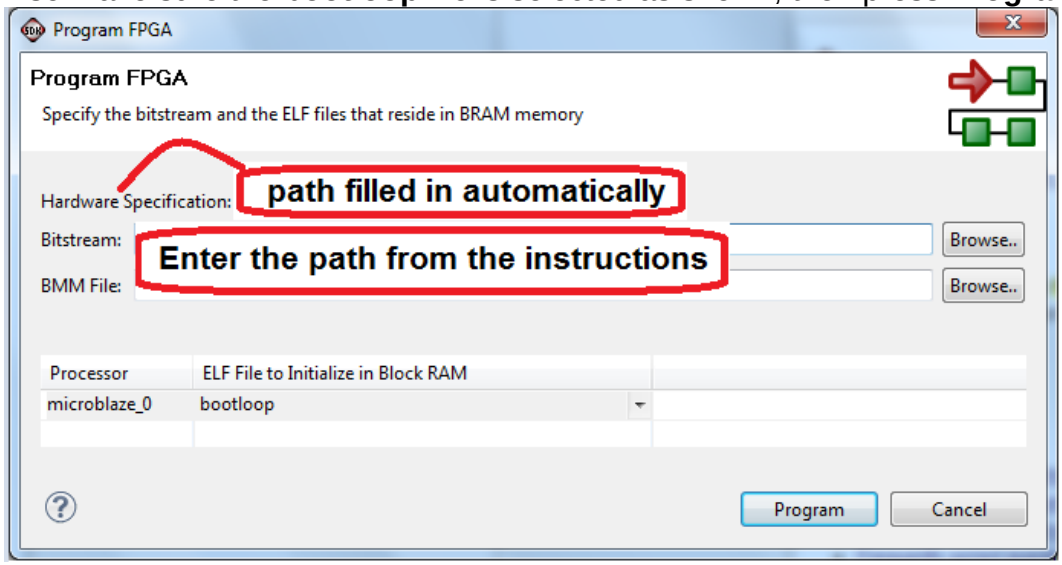


The **Program FPGA** dialog box appears. From here, an FPGA Bitstream (.bit) file is selected as well as an FPGA BMM (.bmm) file. Be sure to select the .bit file and the .bmm file by using the paths below.

Bitstream:
C:\designs\maxim\RD24V01_00\RD24_LX9_V01_00\Design_Files\top.bit

BMM File:
C:\designs\maxim\RD24V01_00\RD24_LX9_V01_00\Design_Files\edkBmmFile_bd.bmm

Also make sure the **bootloop** file is selected as shown, then press **Program**.



It takes approximately 10 seconds to download the FPGA, then a message box indicating **FPGA configuration complete** appears.

15. Set up the terminal program to run on the PC using the following steps. Before loading the executable firmware file on the FPGA, the terminal program on the PC should be running. The example firmware running on the FPGA communicates with the PC via a USB port set up to emulate a serial port (UART). To establish this communication link, the PC must be configured with the appropriate Windows drivers. A suitable terminal program such as Tera Term or HyperTerminal should be invoked.

    The micro USB (J3) on the LX9 is the communication port. The LX9 utilizes the Silicon Labs CP2102 USB-UART bridge IC, so you need to install Silicon Labs' virtual COM port (VCP) driver for their CP210x device family. These may be obtained from the Silicon Labs website (www.silabs.com).

    Once installed, Windows will assign a previously unused COM port. Use the Windows **Control Panel | System | Device Manager** to determine the COM port number. (It will be named **Silicon Labs CP210x USB to UART Bridge**.) Make a note of which COM port this is. That information is needed in the next step.

    Next, a terminal emulation program needs to be installed and launched. For Windows XP® and earlier systems, the HyperTerminal program is the usual choice. However, since HyperTerminal was eliminated from Windows 7, it may be necessary to locate an alternative. Several are available; one good choice is called Tera Term (http://ttssh2.sourceforge.jp/). Whatever terminal program you choose, the communication should be set up by opening the COM port number previously described above and the port configured as:

    bits per second: **115,200**;

    data bits: **8**;

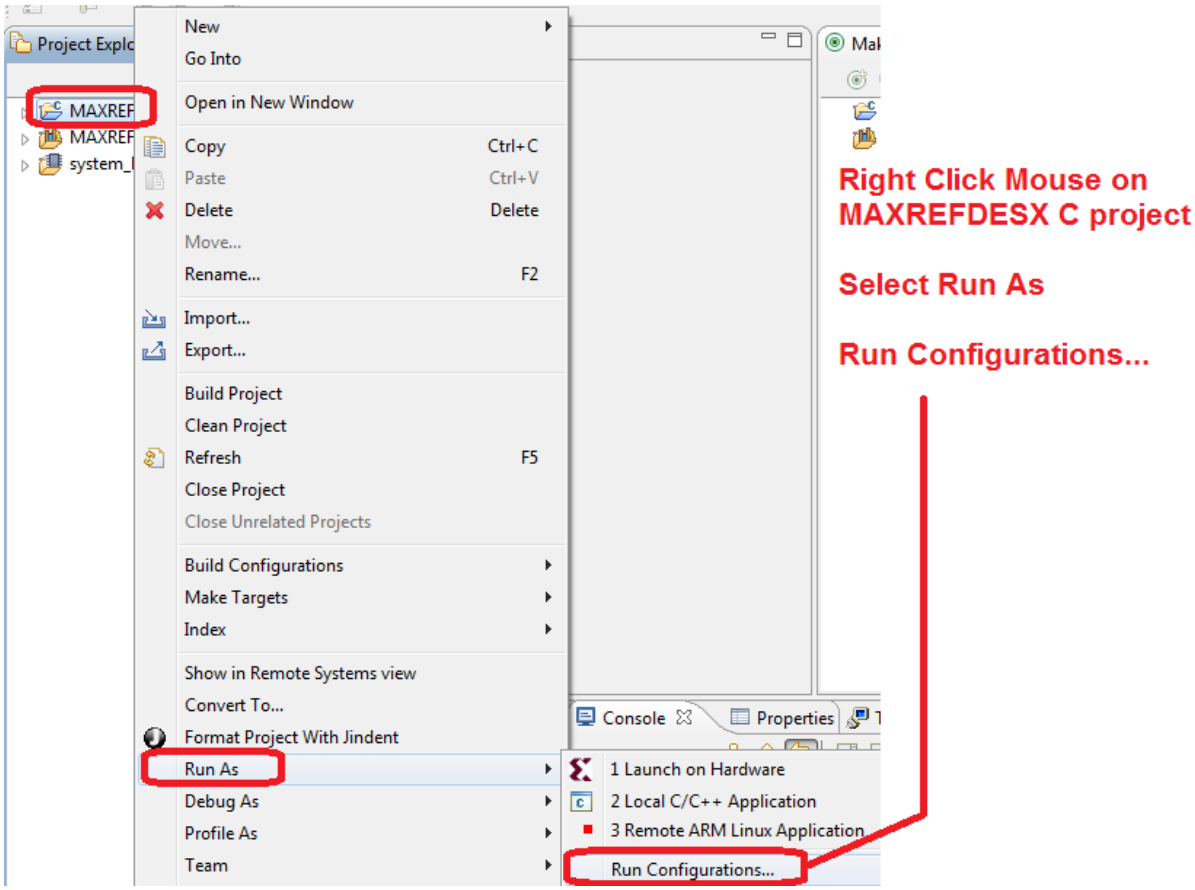
    parity: **none**;

    stop bits: **1**;

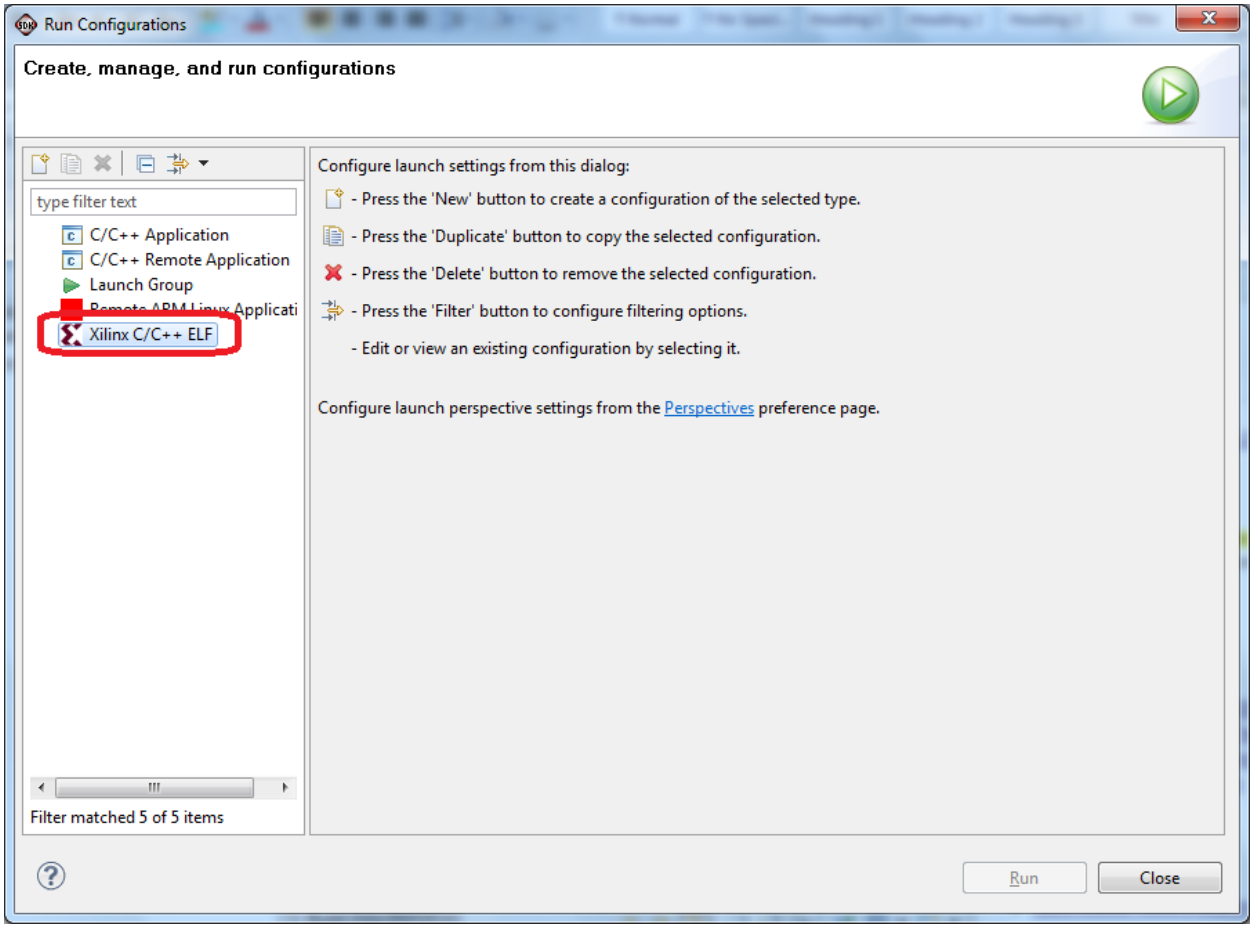
    flow control: **none**.

16. Use the Xilinx SDK to download and run the executable ELF (.ELF) file on the MicroBlaze using the following steps.

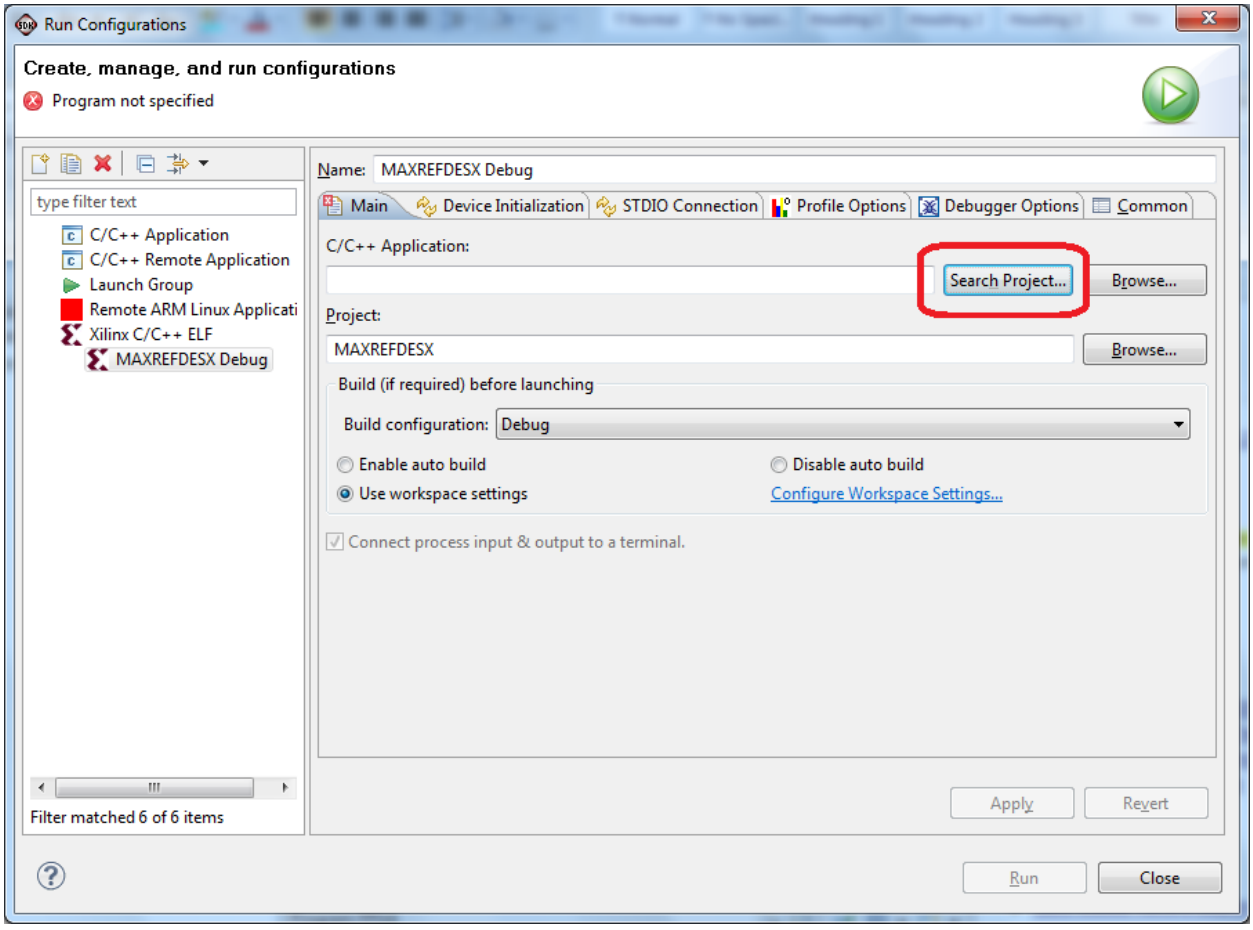
    Right-click the mouse while the **MAXREFDES24 C** project is selected, choose the **Run As** menu, and then **Run Configurations…** menu as shown below.



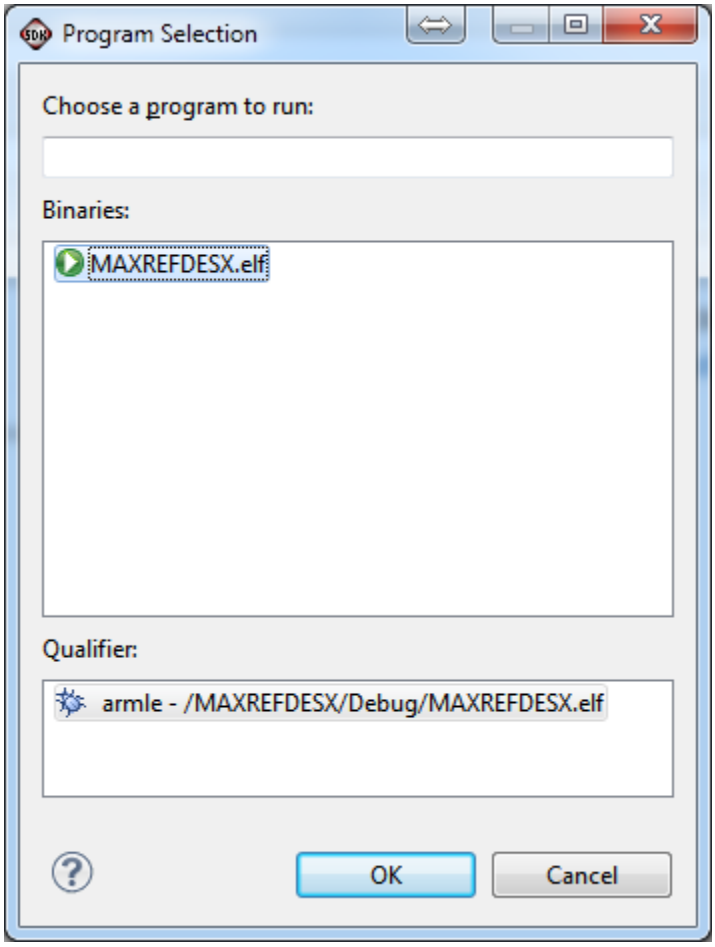
Next, double-click the mouse on the **Xilinx C/C++ ELF** menu.



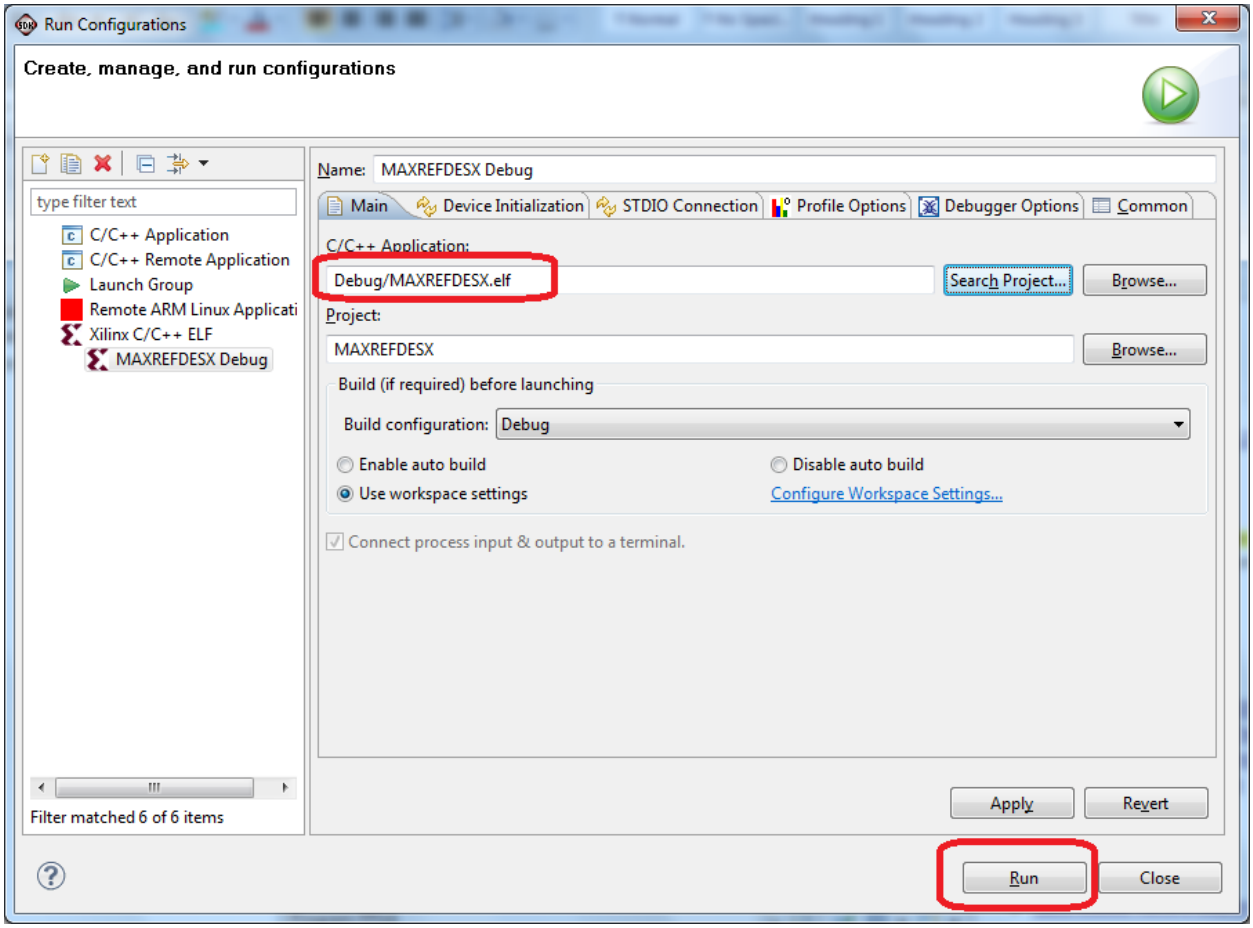
Next, press the **Search Project** button.



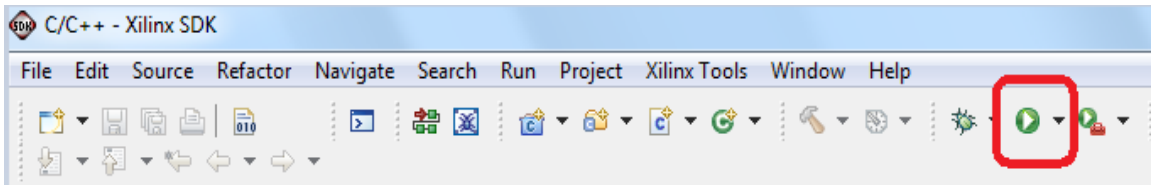
Double-click on the **MAXREFDES24.elf** binary.



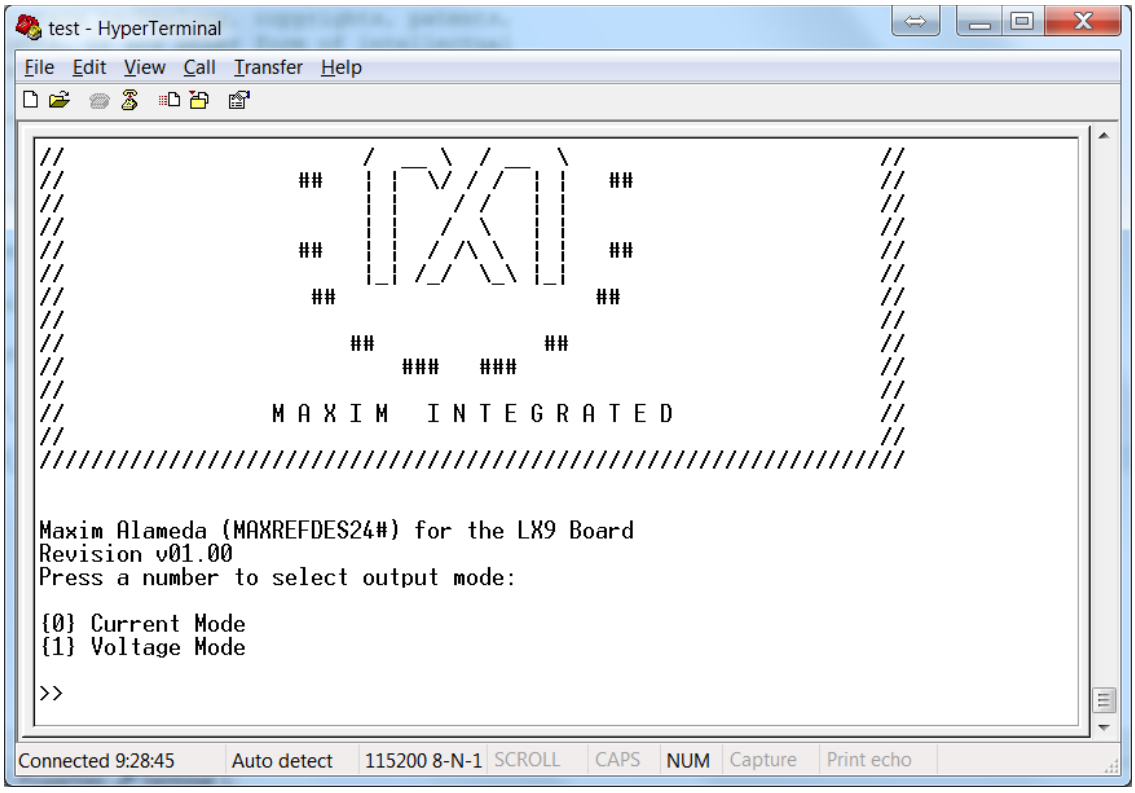
Verify the application is selected on the **Main** tab and press the **Run** button.



Once the Debug/MAXREFDES24 configuration is set up once, you just need to press the **Run** button if you ever want to run the program again.

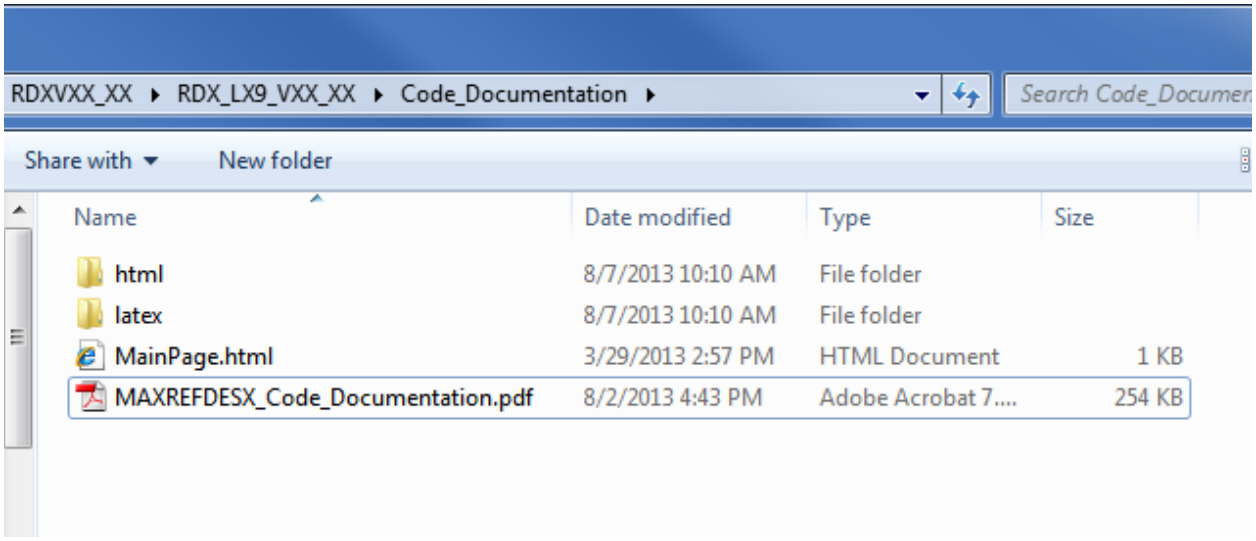


At this point, the application will be running on the MicroBlaze and the terminal program should show the menu below. Make the desired selections by pressing the appropriate keys on the keyboard. For example, to select current output, press **0**.



5. Code Documentation

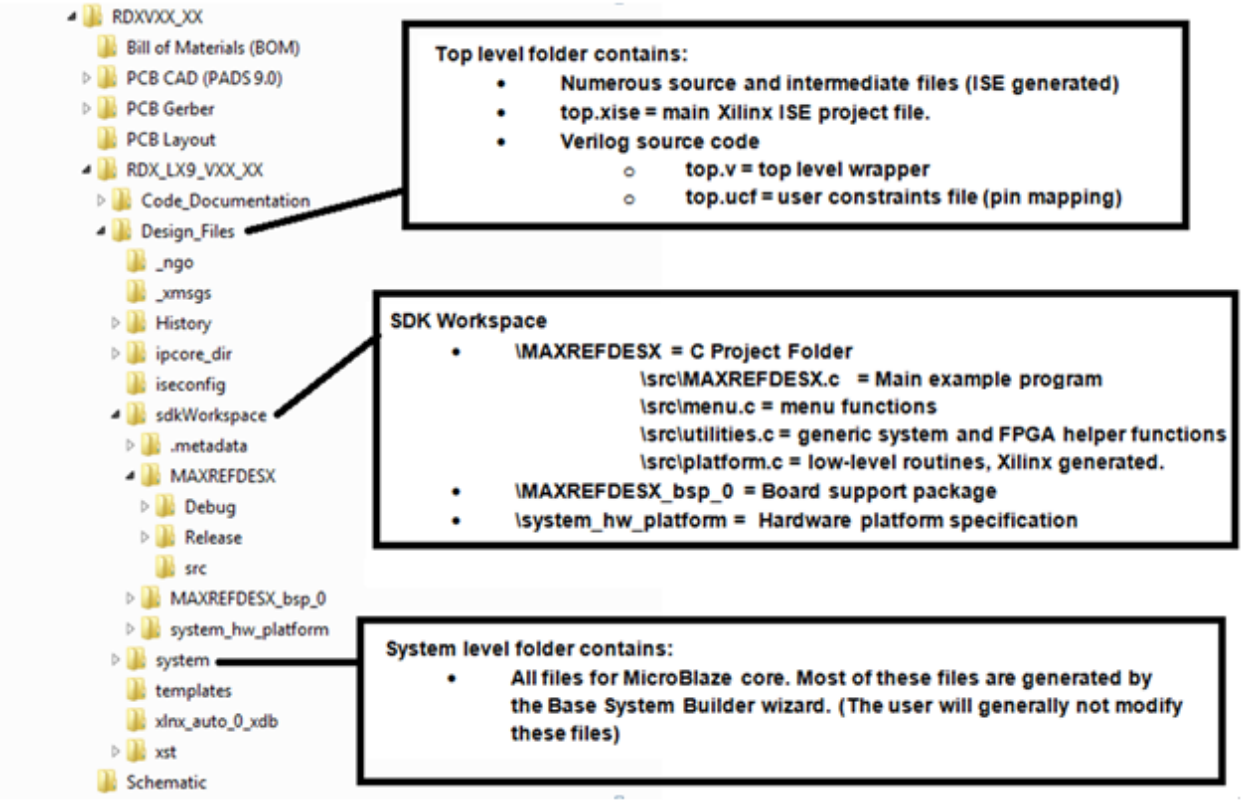
Code documentation can be found at:
C:\...\RD24V01_00\RD24_LX9_V01_00\Code_Documentation



To view the code documentation in HTML format with a browser, open the **MainPage.html** file.

To view the code documentation in .PDF format with a PDF reader, open the **MAXREFDES24_Code_Documentation.pdf** file.

6. Appendix A: Project Structure and Key Filenames



7. Trademarks

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8. Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/14	Initial release	—

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