

## **General Description**

The MAX9947 evaluation kit (EV kit) provides a proven design to evaluate the MAX9947 AISG-compliant integrated transceiver. The EV kit has two MAX9947 devices installed on the board. When one MAX9947 works as a transmitter, the other works as a receiver.



### System Diagram

### Features

- Two MAX9947 Devices (One Works as a Transmitter and the Other as a Receiver)
- Proven PCB Layout
- Fully Assembled and Tested

### **Ordering Information**

PART	TYPE	
MAX9947EVKIT+	EV Kit	
+Denotes lead(Pb)-free an	d RoHS compliant.	

## Component List

DESIGNATION	QTY	DESCRIPTION	
C1, C2, C10, C11	4	10µF ±10%, 10V X5R ceramic capacitors (0805) Murata GRM21BR61A106K	
C3, C4, C12, C13	4	0.1µF ±10%, 16V X7R ceramic capacitors (0603) Murata GRM188R71C104K	
C5, C14	2	1μF ±10%, 16V X7R ceramic capacitors (0603) Murata GRM188R71C105K	
C6, C7, C15, C16	0	Not installed, ceramic capacitors (0603)	
C8, C9, C17, C18	4	39pF ±5%, 50V C0G ceramic capacitors (0603) Murata GRM1885C1H390J	

DESIGNATION	QTY	DESCRIPTION	
J1, J3	2	SMA connectors, edge mount	
J2, J4	2	SMA connectors, vertical mount	
JU1, JU6, JU7, JU12–JU16	8	2-pin headers	
JU2–JU5, JU8–JU11	8	3-pin headers	
L1, L2	2	$0\Omega \pm 5\%$ resistors (0805)	
R1, R7	2	1kΩ ±5% resistors (0603)     4.12kΩ ±1% resistors (0603)     10kΩ ±1% resistors (0603)	
R2, R8	2		
R3, R9	2		
R4, R10	2	49.9 $\Omega$ ±1% resistors (0603)	
R5, R11	0	Not installed, resistors (0603)   10kΩ ±5% resistors (0603)   Red multipurpose test points	
R6, R12	2		
TP1, TP9	2		

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# **MAX9947 Evaluation Kit**

Evaluates: MAX9947

DESIGNATION	QTY	DESCRIPTION	
TP2, TP4, TP10, TP12	4	Black multipurpose test points	
TP3, TP11	2	Yellow multipurpose test points	
TP5–TP8, TP13–TP18	10	Red miniature test points	
U1, U2	2	AISG integrated transceivers (16 TQFN-EP*) Maxim MAX9947ETE+	

## **Component List (continued)**

DESIGNATION	QTY	DESCRIPTION
VR1, VR2	2	50k $\Omega$ top-adjust 12-turn trimmers (2mm)
Y1, Y2	2	8.704MHz crystals Hong Kong X'tals SSL87040N1HS188F0-0
—	16	Shunts
_	1	PCB: MAX9947 EVALUATION KIT+

\*EP = Exposed pad.

### **Component Suppliers**

SUPPLIER	PHONE	WEBSITE	
Hong Kong X'tals Ltd.	852-35112388	www.hongkongcrystal.com	
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com	

Note: Indicate that you are using the MAX9947 when contacting these component suppliers.

## \_Quick Start

### **Required Equipment**

- MAX9947 EV kit
- 3.3V 100mA DC power supply
- Waveform generator
- 2-channel oscilloscope

#### Procedure

The following procedure demonstrates one MAX9947 (as a transmitter) modulating a 38.4kbps OOK signal and transmitting the modulated signal to the second MAX9947 (as a receiver). The receiver demodulates the modulated signal and reconstructs the digital signal.

- 1) Verify that all jumpers (JU1–JU16) are in their default positions, as shown in Table 1.
- Connect the 3.3V DC power supply between TP1 (U1\_VCC) and TP2 (GND).

- Connect the 3.3V DC power supply between TP9 (U2\_VCC) and TP10 (GND).
- 4) Set the waveform generator to output a square wave. Set the amplitude to 3.3V, frequency to 38.4kHz, duty cycle to 50%, and offset to 1.65V.
- 5) Connect the waveform-generator output between TP6 (TXIN) and TP2 (GND).
- 6) Unused TXIN pin must be tied to VL to avoid data collision. Tie TP14 to VL when using U2 as a receiver.
- 7) Connect the oscilloscope channel 1 to TP6 (TXIN).
- 8) Connect the oscilloscope channel 2 to TP15 (RXOUT).
- 9) Verify that the waveforms of channels 1 and 2 are similar.
- 10) Verify that TP16 (DIR) is asserted high, indicating data is flowing from U1 to U2.

# **MAX9947 Evaluation Kit**

JUMPER	SHUNT POSITION	DESCRIPTION
11.14	1-2*	U1 VL pin connected to U1 VCC pin
JUI	Open	U1 VL pin disconnected from U1 VCC pin
JU2		DESCRIPTION     U1 VL pin connected to U1 VCC pin     U1 VL pin disconnected from U1 VCC pin     See Table 2     U1 output level at TXOUT is set at +3dBm     U1 output level at TXOUT is adjustable by VR1     U1 uses on-board crystal     U1 uses on-board crystal     U1 uses on-board crystal     U1 uses external clock applied on SMA J2     U2 VL pin connected to U2 VCC pin     U2 VL pin disconnected from U2 VCC pin     See Table 2     See Table 2     U2 output level at TXOUT is set at +3dBm     U2 output level at TXOUT is set at +3dBm     U2 output level at TXOUT is adjustable by VR2     U2 output level at TXOUT is adjustable by VR2     U2 uses on-board crystal     U2 uses external clock applied on SMA J4     U2 uses external clock applied on SMA J4     U3 uses external clock applied on SMA J4     U4 uses on-board crysta
JU3	_	See Table 2
11.1.4	1-2*	U1 output level at TXOUT is set at +3dBm
JU4 -	2-3	U1 output level at TXOUT is adjustable by VR1
11.15	1-2*	TIONDESCRIPTIONU1 VL pin connected to U1 VCC pinU1 VL pin disconnected from U1 VCC pinSee Table 2See Table 2U1 output level at TXOUT is set at +3dBmU1 output level at TXOUT is adjustable by VR1U1 uses on-board crystalU1 uses on-board crystalU1 uses on-board crystalU1 uses external clock applied on SMA J2U2 VL pin connected to U2 VCC pinU2 VL pin disconnected from U2 VCC pinSee Table 2See Table 2See Table 2See Table 2U2 output level at TXOUT is adjustable by VR2U2 uses on-board crystalU2 vL pin disconnected from U2 VCC pinSee Table 2See Table 2U2 output level at TXOUT is set at +3dBmU2 uses on-board crystalU2 uses on-board crystalU2 uses on-board crystalU2 uses on-board crystalU2 uses external clock applied on SMA J4U2 uses external clock applied on SM
JU5 -	2-3	<b>POSITIONDESCRIPTION</b> 1-2*U1 VL pin connected to U1 VCC pin—See Table 2—See Table 21-2*U1 output level at TXOUT is set at +3dBm2-3U1 output level at TXOUT is adjustable by VR11-2*U1 output level at TXOUT is adjustable by VR11-2*U1 uses on-board crystal2-3U1 uses external clock applied on SMA J2Dpen*U1 uses on-board crystal1-2U1 uses external clock applied on SMA J2Dpen*U1 uses external clock applied on SMA J21-2U1 uses external clock applied on SMA J21-2*U2 VL pin connected from U2 VCC pin0penU2 VL pin disconnected from U2 VCC pinSee Table 2See Table 2See Table 21-2*U2 output level at TXOUT is set at +3dBm2-3U2 output level at TXOUT is adjustable by VR21-2*U2 uses on-board crystal2-3U2 uses external clock applied on SMA J4Dpen*U2 uses on-board crystal1-2U2 uses external clock applied on SMA J4Dpen*U2 uses external clock applied on SMA J41-2*U2 uses external clock applied on SMA J41-2*U1 and U2 grounds connected1-2*U1 and U2 grounds disconnected1-2*U1 and U2 grounds disconnected1-2*U1 and U2 grounds disconnected1-2*U1 and U2 grounds disconnected1-2*U2 SYNCOUT pulled up to VCC1-2*U2 SYNCOUT not pulled up to VCC1-2*
	Open*	DSITION   DESCRIPTION     *   U1 VL pin connected to U1 VCC pin     In   U1 VL pin disconnected from U1 VCC pin     See Table 2   See Table 2     *   U1 output level at TXOUT is set at +3dBm     3   U1 output level at TXOUT is adjustable by VR1     *   U1 uses on-board crystal     3   U1 uses external clock applied on SMA J2     n*   U1 uses external clock applied on SMA J2     n*   U1 uses external clock applied on SMA J2     *   U2 VL pin connected to U2 VCC pin     an   U2 VL pin disconnected from U2 VCC pin     See Table 2   See Table 2     *   U2 output level at TXOUT is set at +3dBm     3   U2 output level at TXOUT is adjustable by VR2     *   U2 output level at TXOUT is adjustable by VR2     *   U2 uses on-board crystal     3   U2 uses on-board crystal     4   U2 uses on-board crystal     5   U2 uses external clock applied on SMA J4     n*   U2 uses on-board crystal     2   U2 uses external clock applied on SMA J4     *   SMA J1 and J3 signals connecte
JU6	1-2	ITION   DESCRIPTION     U1 VL pin connected to U1 VCC pin   U1 VL pin disconnected from U1 VCC pin     See Table 2   See Table 2     U1 output level at TXOUT is set at +3dBm   U1 output level at TXOUT is adjustable by VR1     U1 uses on-board crystal   U1 uses on-board crystal     U1 uses on-board crystal   U1 uses external clock applied on SMA J2     U1 uses external clock applied on SMA J2   U2 uses external clock applied on SMA J2     U2 VL pin connected to U2 VCC pin   U2 VL pin disconnected from U2 VCC pin     See Table 2   See Table 2     U2 output level at TXOUT is set at +3dBm   U2 output level at TXOUT is adjustable by VR2     U2 uses on-board crystal   U2 uses on-board crystal     U2 uses on-board crystal   U2 uses on-board crystal     U2 uses on-board crystal   U2 uses on-board crystal     U2 uses on-board crystal   U2 uses external clock applied on SMA J4     U2 uses external clock applied on SMA J4   SMA J1 and J3 signals connected by a PCB trace     SMA J1 and J3 signals not connected   U1 and U2 grounds connected     U1 and U2 grounds disconnected   U1 and U2 grounds disconnected     U1 and U2 grounds disconnected   U1 and U2 grounds disconnected
11.17	1-2*	NDESCRIPTIONU1 VL pin connected to U1 VCC pinU1 VL pin disconnected from U1 VCC pinSee Table 2See Table 2U1 output level at TXOUT is set at +3dBmU1 output level at TXOUT is adjustable by VR1U1 uses on-board crystalU1 uses on-board crystalU1 uses on-board crystalU1 uses on-board crystalU1 uses external clock applied on SMA J2U2 VL pin connected to U2 VCC pinU2 VL pin disconnected from U2 VCC pinSee Table 2See Table 2See Table 2U2 output level at TXOUT is set at +3dBmU2 output level at TXOUT is set at +3dBmU2 output level at TXOUT is adjustable by VR2U2 uses on-board crystalU2 uses external clock applied on SMA J4U2 uses on-board crystalU2 uses external clock applied on SMA J4U2 uses external clock applied on SMA J4<
JU7	Open	U2 VL pin disconnected from U2 VCC pin
JU8		See Table 2
JU9		See Table 2
	1-2*	U2 output level at TXOUT is set at +3dBm
JU 10	2-3	U2 output level at TXOUT is adjustable by VR2
11.14.4	1-2*	U2 uses on-board crystal
JUTI	2-3	U2 uses external clock applied on SMA J4
11.140	Open*	U2 uses on-board crystal
JU12	1-2	U2 uses external clock applied on SMA J4
11.140	1-2*	SMA J1 and J3 signals connected by a PCB trace
JU13	Open	SMA J1 and J3 signals not connected
11.14.4	1-2*	U1 and U2 grounds connected
JU14	Open	U1 and U2 grounds disconnected
11.14.5	1-2*	U1 SYNCOUT pulled up to VCC through a $1k\Omega$ resistor
JU15	Open	U1 SYNCOUT not pulled up to VCC
1110	1-2*	U2 SYNCOUT pulled up to VCC through a 1k $\Omega$ resistor
JUID	Open	U2 SYNCOUT not pulled up to VCC

## Table 1. Jumper Descriptions (JU1–JU16)

\*Default position.

## **MAX9947 Evaluation Kit**

## \_Detailed Description of Hardware

The MAX9947 IC is an AISG-compliant, fully integrated transceiver.

The EV kit has two MAX9947 devices on the board. When one MAX9947 is configured as a transmitter, the other can be configured as a receiver. A user can connect the transmitter and the receiver though a usersupplied coaxial cable, or by simply shorting a jumper on the board for quick testing.

#### **Transmission Output Power**

The IC output level at TXOUT can be set by using two external resistors that connect at the RES and BIAS pins.

The EV kit defaults to the nominal power level of +3dBm at the feeder cable as the AISG standard requires. Using the U1 transceiver as an example, with R2 =  $4.12k\Omega$  and R3 =  $10k\Omega$ , provides  $1.78V_{P-P}$  at TXOUT.

By placing a shunt on jumper JU4 (JU10 in the case of U2 transceiver) across pins 2-3, the TXOUT voltage level can be varied by using the on-board variable resistor VR1 (VR2 in the case of U2). TXOUT is varied according to the following equations:

For U1:  $V_{TXOUT}$  (V<sub>P-P</sub>) = 2.52V<sub>P-P</sub> x R3/(R3 + VR1) For U2:  $V_{TXOUT}$  (V<sub>P-P</sub>) = 2.52V<sub>P-P</sub> x R9/(R9 + VR2)

### **External Clock for AISG Transceiver**

By default, nominal 8.704MHz crystals are connected to each MAX9947 AISG transceiver. Alternatively, a user can apply an external clock on SMA connector J2 (J4 in the case of U2) and place shunts across pins 2-3 of jumper JU5 and pins 1-2 of jumper JU6 (JU11 and JU12 in the case of U2) to disable the on-board crystals.

#### **Bit-Time Duration Selector**

Jumpers JU2 and JU3 (JU8 and JU9 in the case of U2) define the duration of the bit time, as shown in Table 2.

DIRMD2 (JU2, JU8 SHUNT POSITION)	DIRMD1 (JU3, JU9 SHUNT POSITION)	AISG DATA RATE (kbps)	UNITY BIT TIME (µs)
0 (2-3)	0 (2-3)	9.6	104.16
0 (2-3*)	1 (1-2*)	38.4	26.04
1 (1-2)	0 (2-3)	115.2	8.68
1 (1-2)	1 (1-2)	—	—

### Table 2. Bit-Time Duration Selector (JU2, JU3, JU8, JU9)

\*Default position.

**MAX9947 Evaluation Kit** 



Figure 1. MAX9947 EV Kit Schematic







Figure 2. MAX9947 EV Kit Component Placement Guide—Component Side



Figure 3. MAX9947 EV Kit PCB Layout—Component Side

### 0 8 **ооц**) 0 0 8 0 0 0 °00 В 5 0 Ū Ο e e Ξ 8 0 0 0 Ο 0 00 6 0 000 0 - 1.0"

Figure 4. MAX9947 EV Kit PCB Layout—Solder Side

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**MAX9947 Evaluation Kit** 

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