

## FEATURES

- Low offset voltage:** 120  $\mu\text{V}$  maximum at 25°C
- Low input bias current:** 1 nA maximum at 25°C
- Low voltage noise density:** 8 nV/ $\sqrt{\text{Hz}}$  typical at 1 kHz
- Large signal voltage gain ( $A_{v0}$ ):** 108 dB minimum over full supply voltage and operating temperature
- Input overvoltage protection to 32 V above and below the supply voltage rail**
- Integrated EMI filter**
  - 70 dB typical rejection at 1000 MHz
  - 90 dB typical rejection at 2400 MHz
- Rail-to-rail output swing**
- Low supply current:** 500  $\mu\text{A}$  typical per amplifier
- Wide bandwidth**
  - Gain bandwidth product ( $A_v = 100$ ): 3.5 MHz typical
  - Unity-gain crossover ( $A_v = 1$ ): 3.5 MHz typical
  - 3 dB bandwidth ( $A_v = 1$ ): 6 MHz typical
- Dual-supply operation**
  - Specified at  $\pm 5\text{ V}$  to  $\pm 15\text{ V}$ , operates over  $\pm 2.5\text{ V}$  to  $\pm 18\text{ V}$
- Unity-gain stable**
- No phase reversal**

## APPLICATIONS

- Wireless base station control circuits
- Optical network control circuits
- Instrumentation
- Sensors and controls
  - Thermocouples, RTDs, strain gages, shunt current measurements

## GENERAL DESCRIPTION

The ADA4177-2CHIPS is a dual-channel amplifier that features low offset voltage (3  $\mu\text{V}$  typical), low input bias current, low noise, and low current consumption (500  $\mu\text{A}$  typical). Outputs are stable with capacitive loads of more than 1000 pF with no external compensation.

The inputs of the ADA4177-2CHIPS feature outstanding precision amplifier robustness, providing input protection against

## FUNCTIONAL BLOCK DIAGRAM

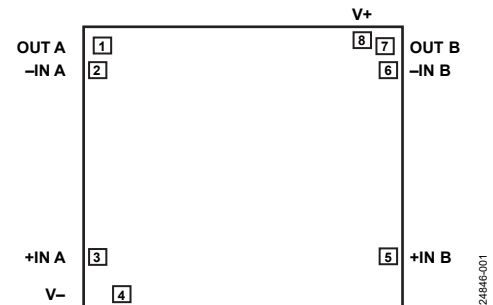


Figure 1.

signal excursions 32 V beyond either supply, as well as 70 dB of rejection for electromagnetic interference (EMI) at 1000 MHz.

Additional application and technical information can be found in the [ADA4177-2](#) data sheet.

The ADA4177-2CHIPS is specified for +25°C only, and is functional over the -40°C to +125°C temperature range. The ADA4177-2CHIPS is guaranteed only on the specifications of this data sheet.

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**REVISION HISTORY**

10/2020—Revision 0: Initial Version

## SPECIFICATIONS

ELECTRICAL CHARACTERISTICS,  $\pm 5$  V

Power supply voltage ( $V_{SY}$ ) =  $\pm 5.0$  V, common-mode voltage ( $V_{CM}$ ) = 0 V,  $T_A$  = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$			3	120	$\mu$ V
Offset Voltage Matching					110	$\mu$ V
Input Bias Current	$I_B$		-1	-0.4	+1	nA
Input Offset Current	$I_{OS}$		-0.75	+0.1	+0.75	nA
Input Voltage Range	IVR		-3.5		+3.5	V
Overvoltage Current Limit <sup>1</sup>	$I_{OVP}$	$5\text{ V} < V_{CM} < 37\text{ V}$		12		mA
		$-37\text{ V} < V_{CM} < -5\text{ V}$		10		mA
Common-Mode Rejection Ratio	CMRR	$-3.5\text{ V} \leq V_{CM} \leq +3.5\text{ V}$	122	130		dB
Large Signal (Open-Loop) Voltage Gain	$A_{VO}$	Load resistance ( $R_L$ ) = 2 k $\Omega$ , output voltage ( $V_{OUT}$ ) = -4.5 V to +4.5 V	108	110		dB
		$R_L = 10\text{ k}\Omega$ , $V_{OUT} = -4.5\text{ V}$ to +4.5 V	115	120		dB
Input Capacitance	$C_{INDM}$	Differential mode		1		pF
	$C_{INCM}$	Common mode		8		pF
Input Resistance	$R_{DIFF}$	Differential mode		4		M $\Omega$
	$R_{CM}$	Common mode		100		G $\Omega$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage						
High	$V_{OH}$	Load current ( $I_{LOAD}$ ) = 1 mA	4.95			V
Low	$V_{OL}$	$I_{LOAD} = 7\text{ mA}$	4.80			V
		$I_{LOAD} = 1\text{ mA}$			-4.95	V
		$I_{LOAD} = 7\text{ mA}$			-4.80	V
Output Current	$I_{OUT}$	Dropout voltage ( $V_{DROPOUT}$ ) < 1 V		25		mA
Short-Circuit Current	$I_{SC}$	$T_A = 25^\circ\text{C}$				
Sourcing				36		mA
Sinking				48		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ kHz}$ , closed-loop gain ( $A_V$ ) = 1		0.11		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 2.5\text{ V}$ to $\pm 18\text{ V}$	125	145		dB
Supply Current per Amplifier	$I_{SY}$	$V_{OUT} = 0\text{ V}$		500	560	$\mu$ A
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		1.5		V/ $\mu$ s
Settling Time	$t_s$					
To 0.1%		Input voltage ( $V_{IN}$ ) = 1 V step, $R_L = 2\text{ k}\Omega$ , $A_V = -1$		1.8		$\mu$ s
To 0.01%		$V_{IN} = 1\text{ V}$ step, $R_L = 2\text{ k}\Omega$ , $A_V = -1$		3.5		$\mu$ s
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV}$ p-p, $R_L = 2\text{ k}\Omega$ , $A_V = 100$		3.5		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV}$ p-p, $R_L = 2\text{ k}\Omega$ , $A_V = 1$		3.5		MHz
-3 dB Closed-Loop Bandwidth	$f_{-3\text{ dB}}$	$V_{IN} = 10\text{ mV}$ p-p, $R_L = 2\text{ k}\Omega$ , $A_V = 1$		6		MHz
Total Harmonic Distortion Plus Noise	THD + N	$V_{IN} = 1\text{ V}$ rms, $R_L = 2\text{ k}\Omega$ , $A_V = 1$ , $f = 1\text{ kHz}$		0.003		%
EMI Rejection of +IN x	EMIR	$V_{IN} = 200\text{ mV}$ p-p				
$f = 1000\text{ MHz}$				70		dB
$f = 2400\text{ MHz}$				90		dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n$ p-p	0.1 Hz to 10 Hz		175		nV p-p
Voltage Noise Density	$e_n$	$f = 10\text{ Hz}$		10		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		8		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.2		pA/ $\sqrt{\text{Hz}}$

<sup>1</sup> All inputs are stressed to 32 V beyond supplies for 500 ms.

**ELECTRICAL CHARACTERISTICS, ±15 V**

$V_{SY} = \pm 15\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$			3	120	$\mu\text{V}$
Offset Voltage Matching					110	$\mu\text{V}$
Input Bias Current	$I_B$		-1	-0.3	+1	nA
Input Offset Current	$I_{OS}$		-0.75	+0.1	+0.75	nA
Input Voltage Range	IVR		-13.5		+13.5	V
Overvoltage Current Limit <sup>1</sup>	$I_{OVP}$	$15\text{ V} < V_{CM} < 47\text{ V}$		12		mA
		$-47\text{ V} < V_{CM} < -15\text{ V}$		10		mA
Common-Mode Rejection Ratio	CMRR	$-13.5\text{ V} \leq V_{CM} \leq +13.5\text{ V}$	128	130		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_{OUT} = -14.2\text{ V to }+14.2\text{ V}$	110	114		dB
		$R_L = 10\text{ k}\Omega$ , $V_{OUT} = -14.5\text{ V to }+14.5\text{ V}$	118	120		dB
Input Capacitance	$C_{INDM}$	Differential mode		1		pF
	$C_{INCM}$	Common mode		8		pF
Input Resistance	$R_{DIFF}$	Differential mode		4		M $\Omega$
	$R_{CM}$	Common mode		130		G $\Omega$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_{LOAD} = 1\text{ mA}$	14.95			V
		$I_{LOAD} = 7\text{ mA}$	14.80			V
Low	$V_{OL}$	$I_{LOAD} = 1\text{ mA}$			-14.95	V
		$I_{LOAD} = 7\text{ mA}$			-14.80	V
Output Current	$I_{OUT}$	$V_{DROPOUT} < 1\text{ V}$		25		mA
Short-Circuit Current	$I_{SC}$	$T_A = 25^\circ\text{C}$		53		mA
				65		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ kHz}$ , $A_V = 1$		0.08		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 2.5\text{ V to } \pm 18\text{ V}$	125	145		dB
Supply Current per Amplifier	$I_{SY}$	$V_{OUT} = 0\text{ V}$		500	580	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		1.5		V/ $\mu\text{s}$
Settling Time	$t_s$	$V_{IN} = 10\text{ V p-p}$ , $R_L = 2\text{ k}\Omega$ , $A_V = -1$		5.5		$\mu\text{s}$
		$V_{IN} = 10\text{ V p-p}$ , $R_L = 2\text{ k}\Omega$ , $A_V = -1$		7.5		$\mu\text{s}$
		$V_{IN} = 10\text{ mV p-p}$ , $R_L = 2\text{ k}\Omega$ , $A_V = 100$		3.5		MHz
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 2\text{ k}\Omega$ , $A_V = 100$		3.5		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 2\text{ k}\Omega$ , $A_V = 1$		3.5		MHz
-3 dB Closed-Loop Bandwidth	$f_{-3\text{ dB}}$	$V_{IN} = 10\text{ mV p-p}$ , $R_L = 2\text{ k}\Omega$ , $A_V = 1$		6		MHz
Total Harmonic Distortion Plus Noise	THD + N	$V_{IN} = 1\text{ V rms}$ , $A_V = 1$ , $R_L = 2\text{ k}\Omega$ , $f = 1\text{ kHz}$		0.002		%
EMI Rejection of +IN x	EMIR	$V_{IN} = 200\text{ mV p-p}$		70		dB
				90		dB
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n\text{ p-p}$	0.1 Hz to 10 Hz		175		nV p-p
Voltage Noise Density	$e_n$	$f = 10\text{ Hz}$		10		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		8		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.2		pA/ $\sqrt{\text{Hz}}$
MULTIPLE AMPLIFIERS, CHANNEL SEPARATION	$C_S$	$f = 1\text{ kHz}$		127		dB

<sup>1</sup> All inputs are stressed to 32 V beyond supplies for 500 ms.

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	$V_{SY} \pm 32$ V
Differential Input Voltage	$\pm V_{SY}$
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.  
Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

### ESD Ratings for ADA4177-2CHIPS

Table 4. ADA4177-2CHIPS, 8-Pad CHIP

ESD Model	Withstand Threshold (V)	Class
HBM	4000	3A
FICDM	1250	IV
MM	200	Not applicable

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTION

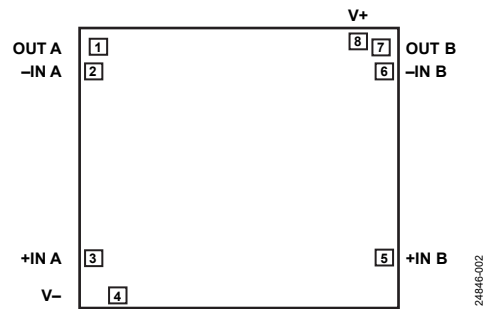


Figure 2. Pad Configuration

Table 5. Pad Configuration Descriptions<sup>1</sup>

Pad No.	Mnemonic	X Coordinate	Y Coordinate	Description
1	OUT A	-600	+522	Output, Channel A
2	-IN A	-625	+421	Inverting Input, Channel A
3	+IN A	-625	-389	Noninverting Input, Channel A
4	V-	-520	-550	Negative Supply Voltage
5	+IN B	+625	-389	Noninverting Input, Channel B
6	-IN B	+625	+421	Inverting Input, Channel B
7	OUT B	+600	+522	Output, Channel B
8	V+	+510	+550	Positive Supply Voltage

<sup>1</sup> All dimensions are referenced from the center of the die to the center of each bond pad.

### OUTLINE DIMENSIONS

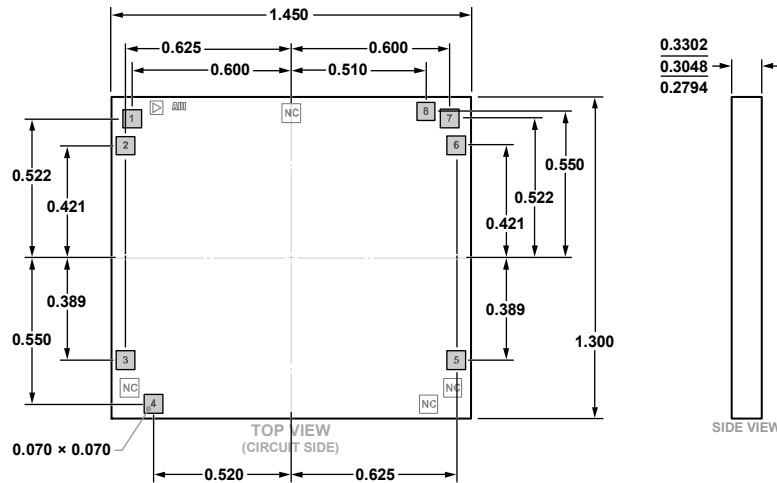


Figure 3. 8-Pad Bare Die [CHIP] (C-8-24)  
Dimensions shown in millimeters

### DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Die Specifications

Parameter	Value	Unit
Chip Size	1360 × 1210	μm
Scribe Line Width	90	μm
Die Size (Maximum)	1450 × 1300	μm
Thickness	12	mils
Backside	Connect to V-	Not applicable
Passivation	Undoped oxide/silicon nitride (SiN)	Not applicable
Bond Pads (Minimum)	70 × 70	μm
Bond Pad Composition	Aluminum silicon (AlSi) (1.0%), copper (Cu) (0.5%)	%
Polyimide Thickness	18	μm
Die Marker ID	ada4177_2z	Not applicable

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Hitachi EN 4900GC
Bonding Method	Forward bond
Bonding Sequence	Lead to bond first = 1

### ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4177-2CHIPS	-40°C to +125°C	8-Pad Bare Die [CHIP]	C-8-24	400

<sup>1</sup> ADA4177-2CHIPS is RoHS compliant.

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