

SN74LVC1G80 Single Positive-Edge-Triggered D-Type Flip-Flop

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to V_{CC}
- Maximum t_{pd} of 4.2 ns at 3.3 V
- Low Power Consumption, 10- μ A Maximum I_{CC}
- \pm 24-mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Test and Measurement
- Enterprise Switching
- Telecom Infrastructure
- Motor Drives

3 Description

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the \bar{Q} output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

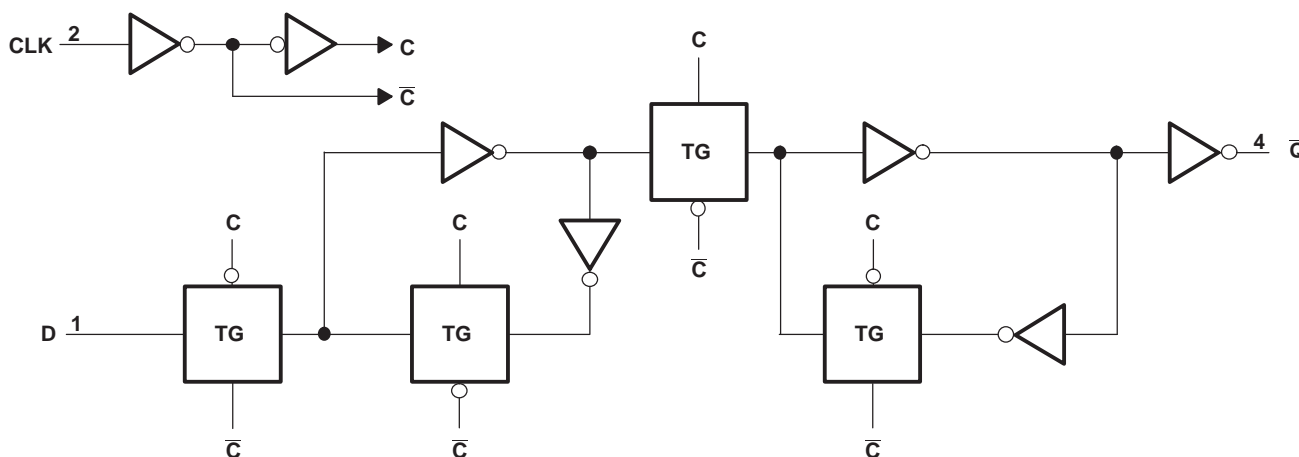
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G80DBV	SOT-23 (5)	2.90 mm x 1.60 mm
SN74LVC1G80DCK	SC70 (5)	2.00 mm x 1.25 mm
SN74LVC1G80YZP	DSBGA (5)	1.41 mm x 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



(1) TG - Transmission Gate



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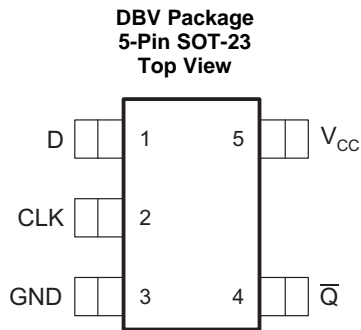
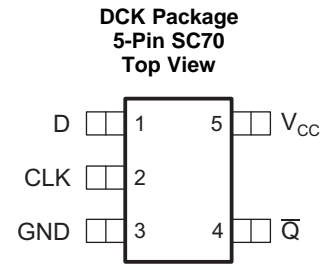
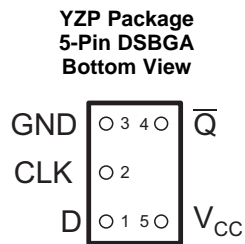
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (December 2013) to Revision S	Page
• Added <i>Applications</i> section, <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.	1
• Added max junction temperature to the <i>Recommended Operating Conditions</i> table	5
• Added operating free-air temperature for YZP package to the <i>Recommended Operating Conditions</i> table	5
• Changed $R_{\theta JA}$ value for DBV package from: $206^\circ\text{C}/\text{W}$ to: $243.4^\circ\text{C}/\text{W}$	5
• Changed $R_{\theta JA}$ value for DCK package from: $252^\circ\text{C}/\text{W}$ to: $278.9^\circ\text{C}/\text{W}$	5
• Changed $R_{\theta JA}$ value for YZP package from: $132^\circ\text{C}/\text{W}$ to: $136.9^\circ\text{C}/\text{W}$	5

Changes from Revision Q (January 2007) to Revision R	Page
• Updated document to new TI data sheet format.	1
• Removed <i>Ordering Information</i> table.	1
• Updated I_{off} in <i>Features</i>	1
• Updated operating temperature range.	4
• Added ESD warning	15

5 Pin Configuration and Functions



Pin Functions⁽¹⁾

PIN		I/O	DESCRIPTION
NO.	NAME		
1	D	I	Data input
2	CLK	I	Clocking input
3	GND	—	Ground pin
4	\bar{Q}	O	Flip-flop output
5	V _{CC}	—	Power pin

(1) See [Mechanical, Packaging, and Orderable Information](#) for dimensions

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	6.5	V
V _I	Input voltage ⁽²⁾	-0.5	6.5	V
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-50	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in *Recommended Operating Conditions*.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
		Machine model (MM)	±200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5
		Data retention only	1.5	
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 3 V to 3.6 V	2	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 3 V to 3.6 V	0.8	
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	-4	mA
		V _{CC} = 2.3 V	-8	
		V _{CC} = 3 V	-16	
		V _{CC} = 4.5 V	-24	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$	4	mA	
		$V_{CC} = 2.3\text{ V}$	8		
		$V_{CC} = 3\text{ V}$	16		
			24		
		$V_{CC} = 4.5\text{ V}$	32		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$	20	ns/V	
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	10		
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	5		
T_J	Junction temperature		150	°C	
T_A	Operating free-air temperature	DBV and DCK packages	-40	125	°C
		YZP package	-40	85	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G80			UNIT	
	DBV (SOT-23)	DCK (SC70)	YZP (DSBGA)		
	5 PINS	5 PINS	5 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	243.4	278.9	136.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	179	121.3	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	65.6	32.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	58.4	7.5	6.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77	64.9	32.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	1.65 V to 5.5 V	$V_{CC} - 0.1$		V	
	$I_{OH} = -4\text{ mA}$	1.65 V	1.2			
	$I_{OH} = -8\text{ mA}$	2.3 V	1.9			
	$I_{OH} = -16\text{ mA}$	3 V	2.4			
			2.3			
	$I_{OH} = -32\text{ mA}$	4.5 V	3.8			
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	1.65 V to 5.5 V	0.1		V	
	$I_{OL} = 4\text{ mA}$	1.65 V	0.45			
	$I_{OL} = 8\text{ mA}$	2.3 V	0.3			
	$I_{OL} = 16\text{ mA}$	3 V	0.4			
			0.55			
	$I_{OL} = 32\text{ mA}$	4.5 V	0.55			
I_I	CLK or D inputs $V_I = 5.5\text{ V}$ or GND	0 to 5.5 V	± 10		μA	
I_{off}	V_I or $V_O = 5.5\text{ V}$	0	± 10		μA	
I_{CC}	$V_I = 5.5\text{ V}$ or GND, $I_O = 0$	1.65 V to 5.5 V	10		μA	
ΔI_{CC}	One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND	3 V to 5.5 V	500		μA	
C_i	$V_I = V_{CC}$ or GND $T_A = -40^\circ\text{C}$ to 85°C	3.3 V	3.5		pF	

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

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6.6 Timing Requirements: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

 over recommended operating free-air temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (unless otherwise noted) (see [Figure 2](#))

		V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		160	MHz
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$			
t_w	Pulse duration, CLK high or low	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.5		ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$			
t_{su}	Data high	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.3		ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	1.5		
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.3		
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$	1.1		
	Data low	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.5		
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	1.5		
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.3		
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$	1.1		
t_h	Hold time, data after CLK \uparrow	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	0		ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	0.2		
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0.9		
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$	0.4		

6.7 Timing Requirements: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$

 over recommended operating free-air temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (unless otherwise noted) (see [Figure 2](#))

		V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		160	MHz
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$			
t_w	Pulse duration, CLK high or low	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.5		ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$			
t_{su}	Data high	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.3		ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	1.5		
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.3		
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$	1.1		
	Data low	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.5		
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	1.5		
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.3		
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$	1.1		
t_h	Hold time, data after CLK \uparrow	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	0		ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	0.2		
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0.9		
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$	0.4		

6.8 Switching Characteristics: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 15\text{ pF}$

over recommended operating free-air temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 15\text{ pF}$ (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	160		MHz
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			
t_{pd}	CLK	\bar{Q}	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	3	9.1	ns
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	1.5	6	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.3	4.2	
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	1.1	3.8	

6.9 Switching Characteristics: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 30\text{ pF}$ or 50 pF

over recommended operating free-air temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 30\text{ pF}$ or 50 pF (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	160		MHz
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			
t_{pd}	CLK	\bar{Q}	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	4.4	9.9	ns
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	2.3	7	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	2	5.2	
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	1.3	4.5	

6.10 Switching Characteristics: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $C_L = 30\text{ pF}$ or 50 pF

over recommended operating free-air temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $C_L = 30\text{ pF}$ or 50 pF (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	160		MHz
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			
t_{pd}	CLK	\bar{Q}	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	4.4	12.5	ns
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	2.3	8.5	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	2	6	
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	1.3	5.5	

6.11 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT	
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	$V_{CC} = 1.8\text{ V}$	24	pF
			$V_{CC} = 2.5\text{ V}$	24	
			$V_{CC} = 3.3\text{ V}$	25	
			$V_{CC} = 5\text{ V}$	27	

6.12 Typical Characteristics

This plot shows the different I_{CC} values for various voltages on the data input (D). Voltage sweep on the input is from 0 V to 7 V. $V_{CC} = 5$ V.

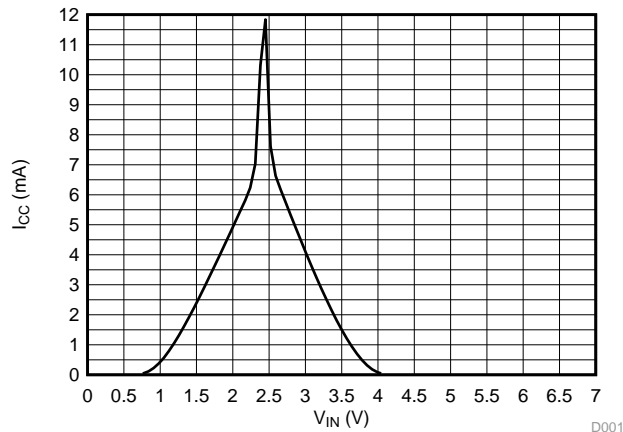


Figure 1. I_{CC} vs V_{IN}

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7 Parameter Measurement Information



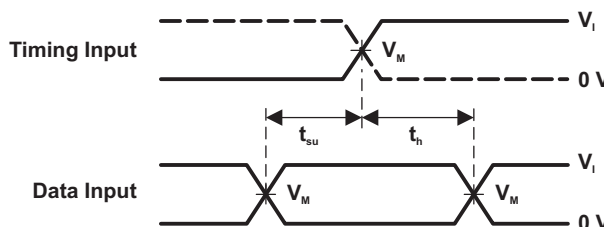
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_i	t_i/t_r					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



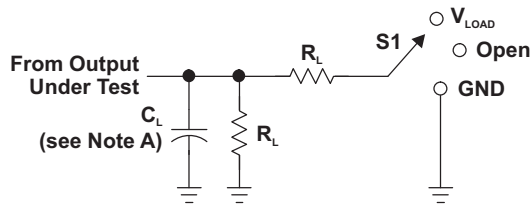
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

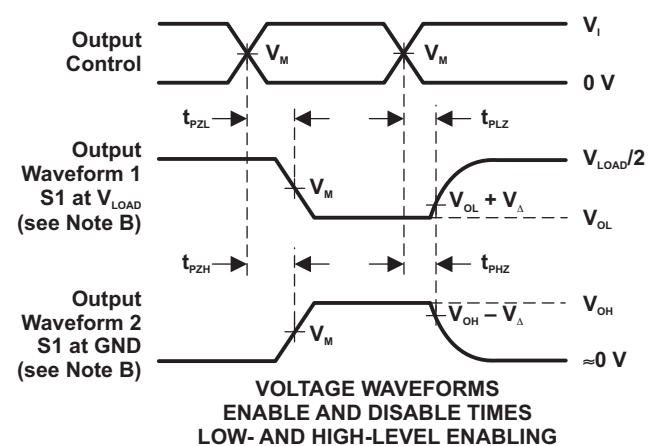
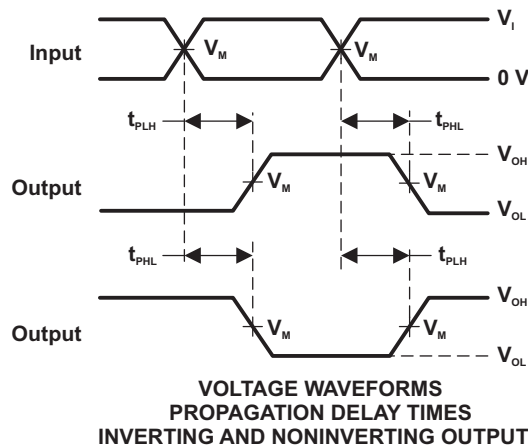
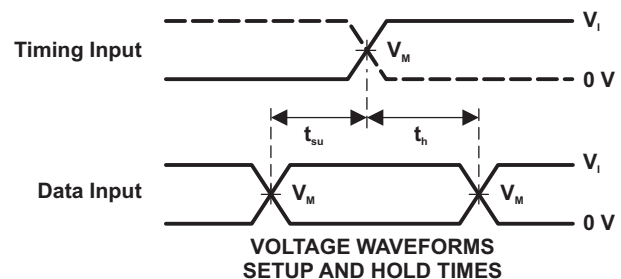
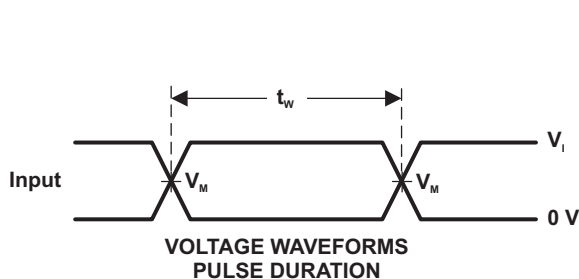
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{on} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G80 is a single positive-edge-trigger D-type flip-flop. Data at the input (D) is transferred to the output (\bar{Q}) on the positive-going edge of the clock pulse when the setup time requirement is met. Because the clock triggering occurs at a voltage level, it is not directly related to the rise time of the clock pulse. This allows for data at the input to be changed without affecting the level at the output, following the hold-time interval.

8.2 Functional Block Diagram

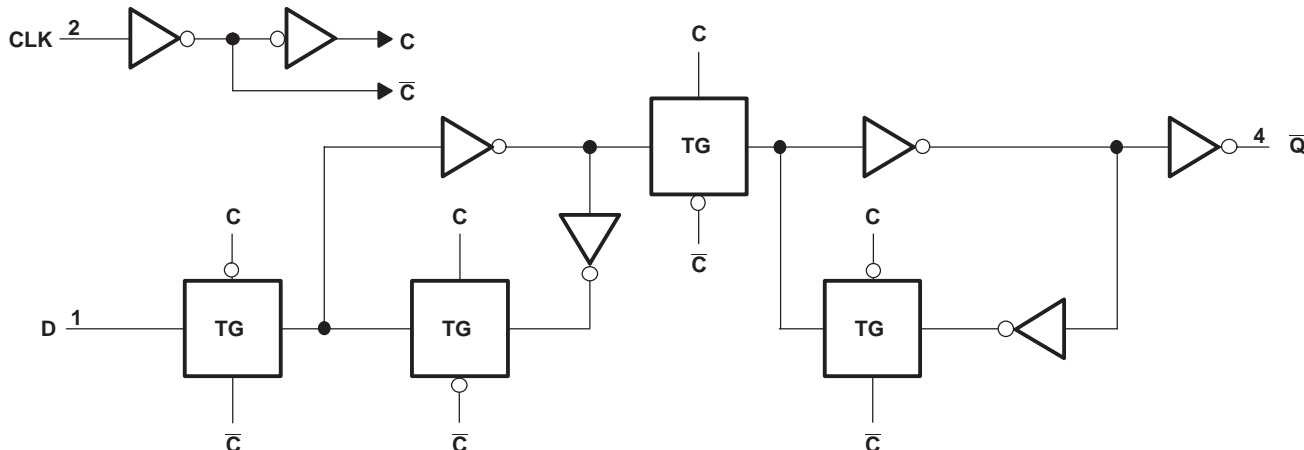


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

This device has a wide operating VCC range of 1.65 V to 5.5 V. The wide operating range allows for a broad range of systems the device can be used in. The output can handle This device is full specified for partial-power-down applications. When $V_{CC} = 0$, the I_{off} circuitry disables the outputs, preventing damaging current backflow through the device.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1G80.

Table 1. Function Table

INPUTS		OUTPUT
CLK	D	\bar{Q}
↑	H	L
↑	L	H
L	X	Q_0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A useful application for the SN74LVC1G80 is using it as a frequency divider. By feeding back the output (\bar{Q}) to the input (D), the output will toggle on every rising edge of the clock waveform. In other words, the output goes HIGH once every two clock cycles so essentially the frequency of the clock signal is divided by a factor of two. The SN74LVC1G80 does not have preset or clear functions so the initial state of the output is unknown. This application implements the use of a microcontroller GPIO pin to initially set the input HIGH, so the output LOW. Initialization is not needed, but should be kept in mind. Post initialization, the GPIO pin is set to a high impedance mode. Depending on the microcontroller, the GPIO pin could be set to an input and used to monitor the clock division.

9.2 Typical Application

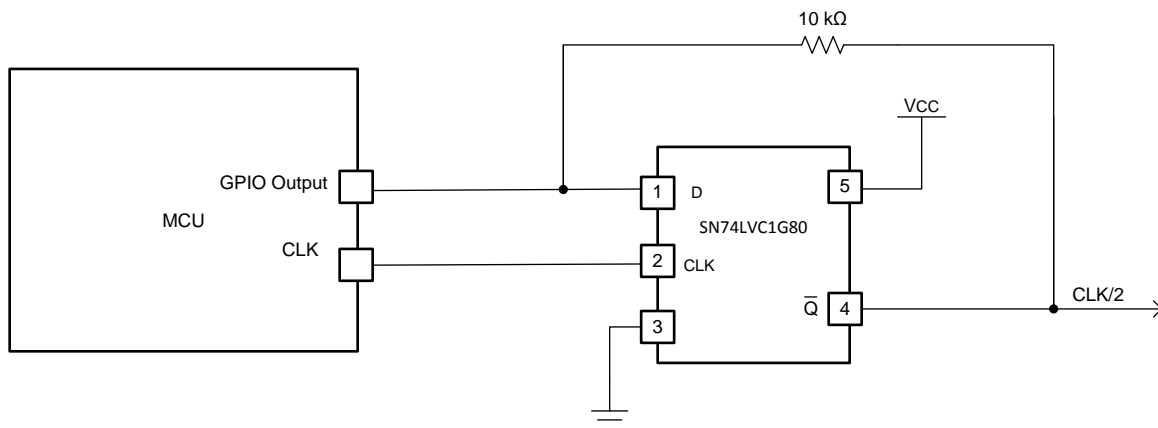


Figure 5. Clock Frequency Division

9.2.1 Design Requirements

For this application a resistor needs to be placed on the feedback line in order for the initialization voltage from the microcontroller to overpower the signal coming from the output (\bar{Q}). Without it the state at the input would be challenged by the GPIO from the microcontroller and from the output of the SN74LVC1G80.

The SN74LVC1G80 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in [Recommended Operating Conditions](#).
 - For specified high and low levels, see V_{IH} and V_{IL} in [Recommended Operating Conditions](#).
 - Input voltages are recommended to not go below 0 V and not exceed 5.5 V for any V_{CC} . See [Recommended Operating Conditions](#).
2. Recommended output conditions:
 - Load currents should not exceed ± 50 mA. See [Absolute Maximum Ratings](#).
 - Output voltages are recommended to not go below 0 V and not exceed the V_{CC} voltage. See [Recommended Operating Conditions](#).

Typical Application (continued)

3. Feedback resistor:

- A 10-k Ω resistor is chosen here to bias the input so the microcontroller GPIO output can initialize the input and output. The resistor value is important because a resistance too high, say at 1 M Ω , would cause too much of a voltage drop, causing the output to no longer be able to drive the input. On the other hand, a resistor too low, such as a 1 Ω , would not bias enough and might cause current to flow into the microcontroller, possibly damaging the device.

9.2.3 Application Curve

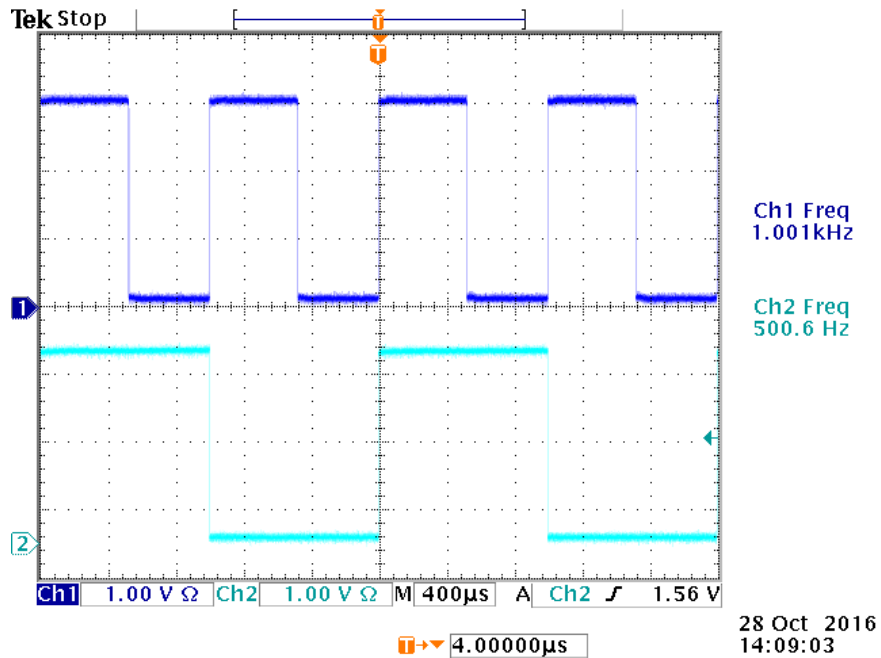


Figure 6. Frequency Division

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in [Absolute Maximum Ratings](#). Each VCC terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μF bypass capacitor is recommended. If multiple pins are labeled VCC, then a 0.01- μF or 0.022- μF capacitor is recommended for each VCC because the VCC pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example VCC and VDD, a 0.1- μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 7](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

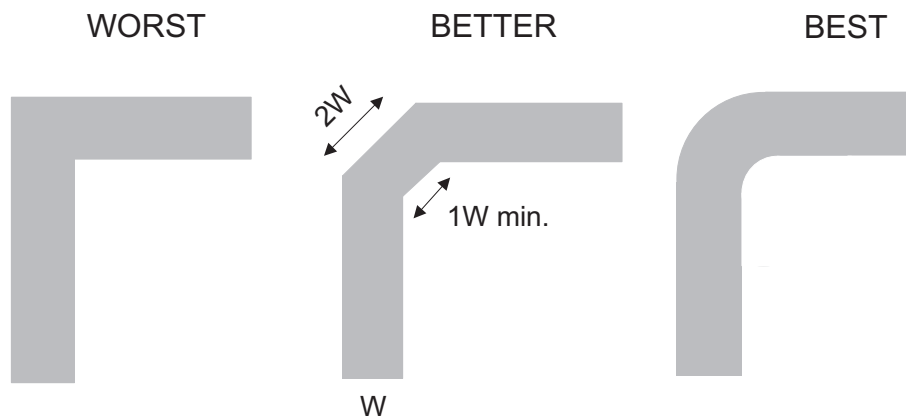


Figure 7. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G80DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C805, C80F, C80J, C80R)	Samples
SN74LVC1G80DBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F	Samples
SN74LVC1G80DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F	Samples
SN74LVC1G80DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C805, C80F, C80J, C80R)	Samples
SN74LVC1G80DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F	Samples
SN74LVC1G80DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CX5, CXF, CXJ, CXK, CXR)	Samples
SN74LVC1G80DCKRE4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX5	Samples
SN74LVC1G80DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX5	Samples
SN74LVC1G80DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CX5, CXF, CXJ, CXK, CXR)	Samples
SN74LVC1G80YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CX7, CXN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G80 :

- Automotive: [SN74LVC1G80-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

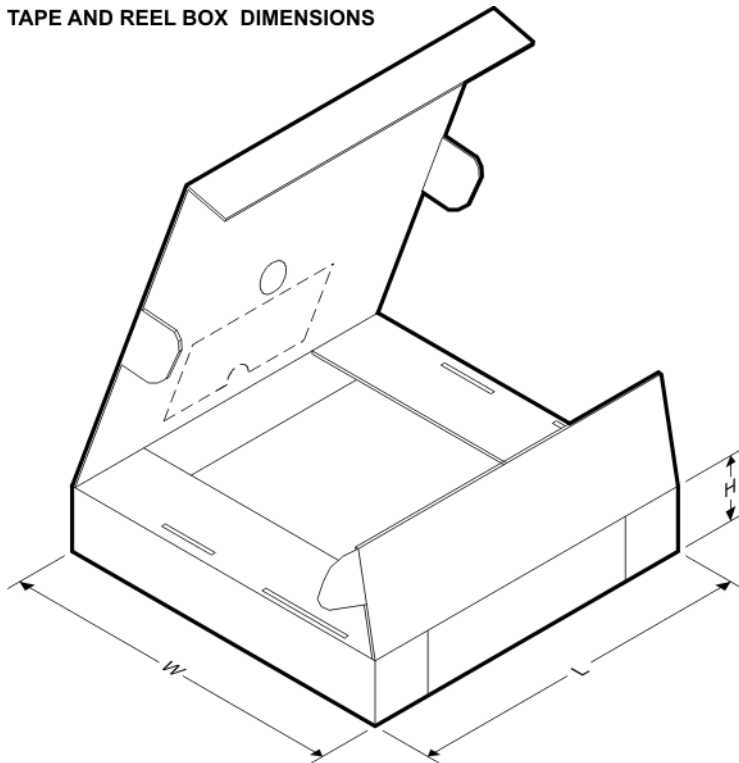


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G80DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G80DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G80DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G80DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G80DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G80DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G80DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G80YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

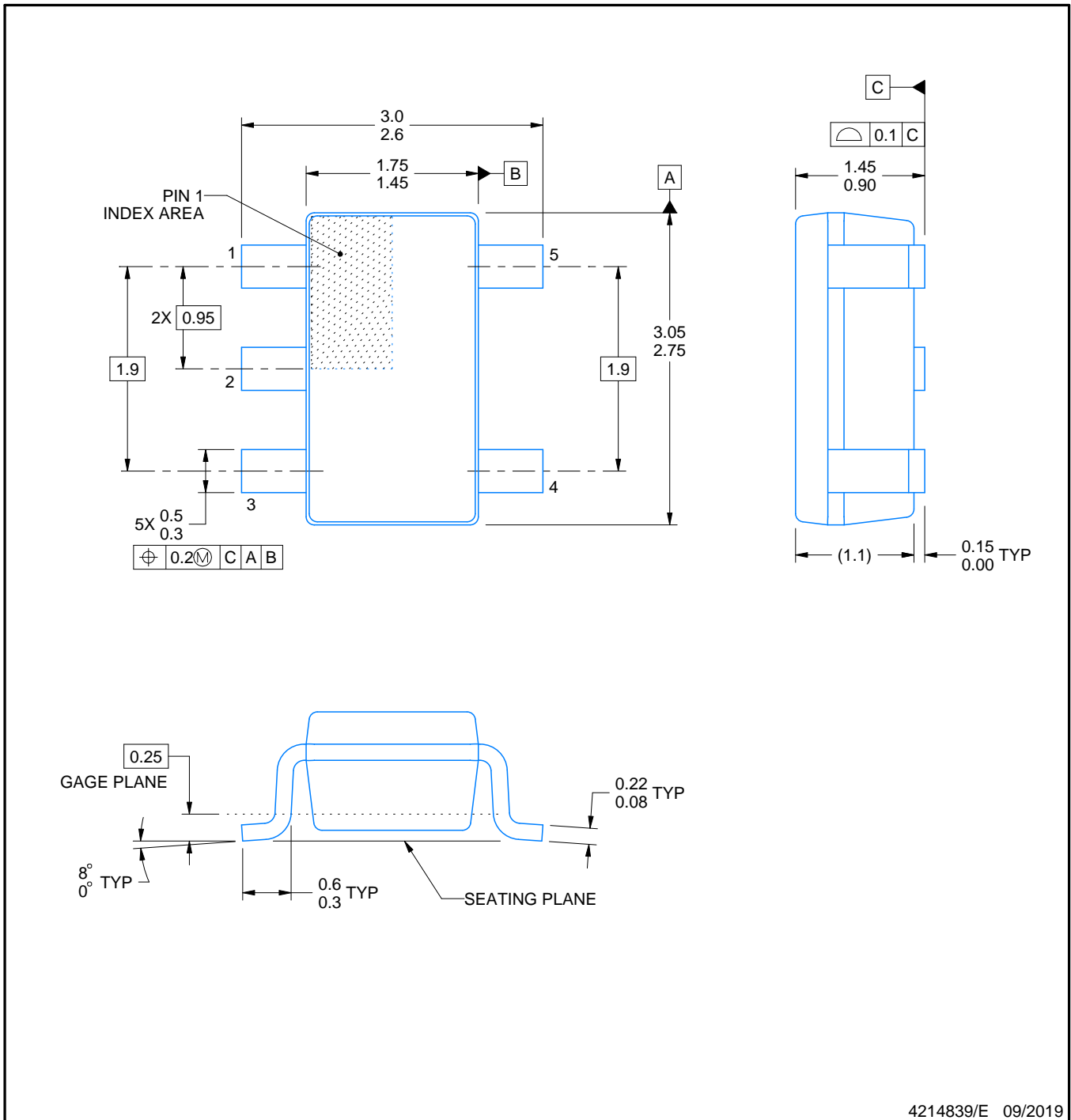
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Reference JEDEC MO-178.
- Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

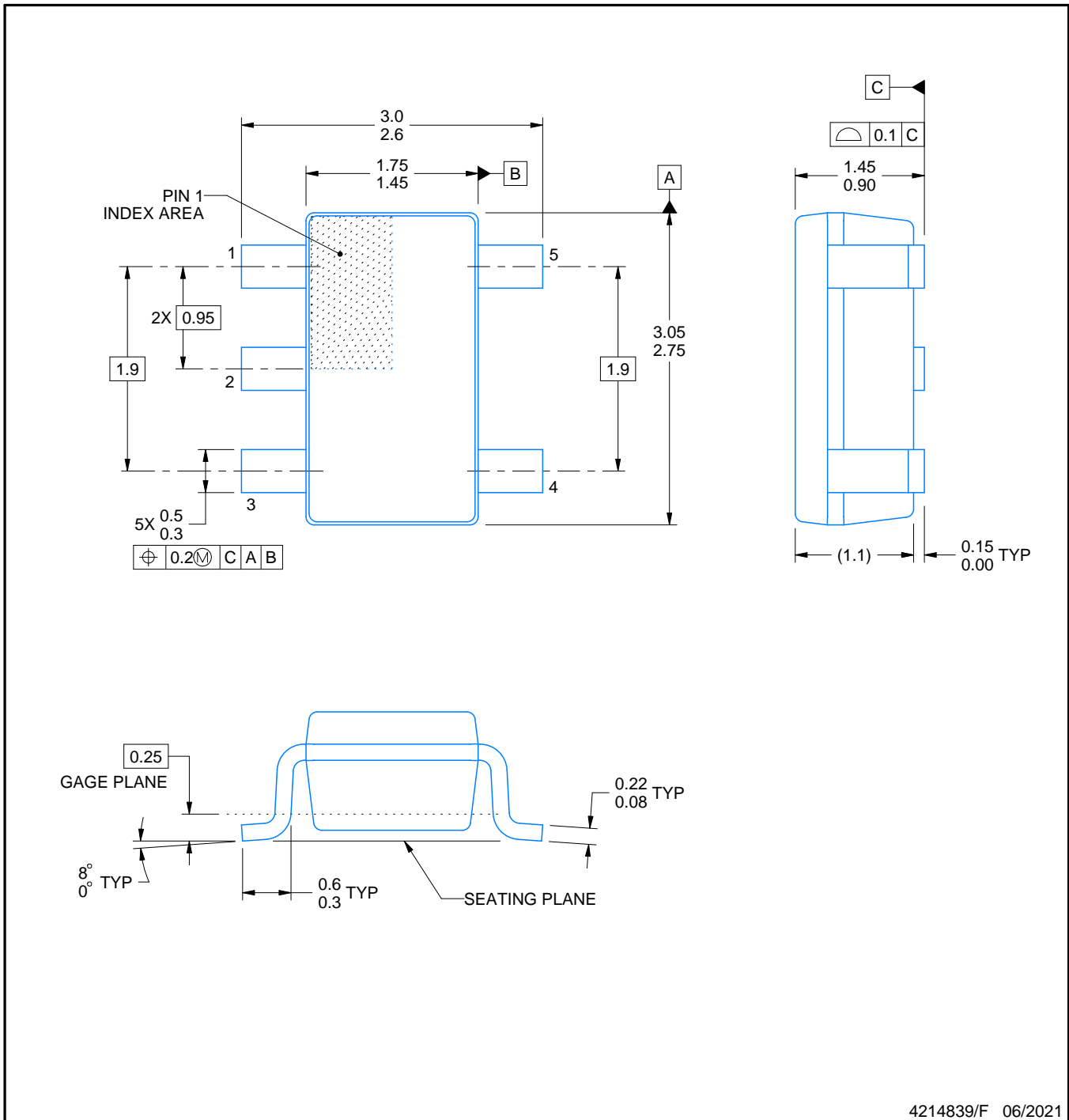


PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

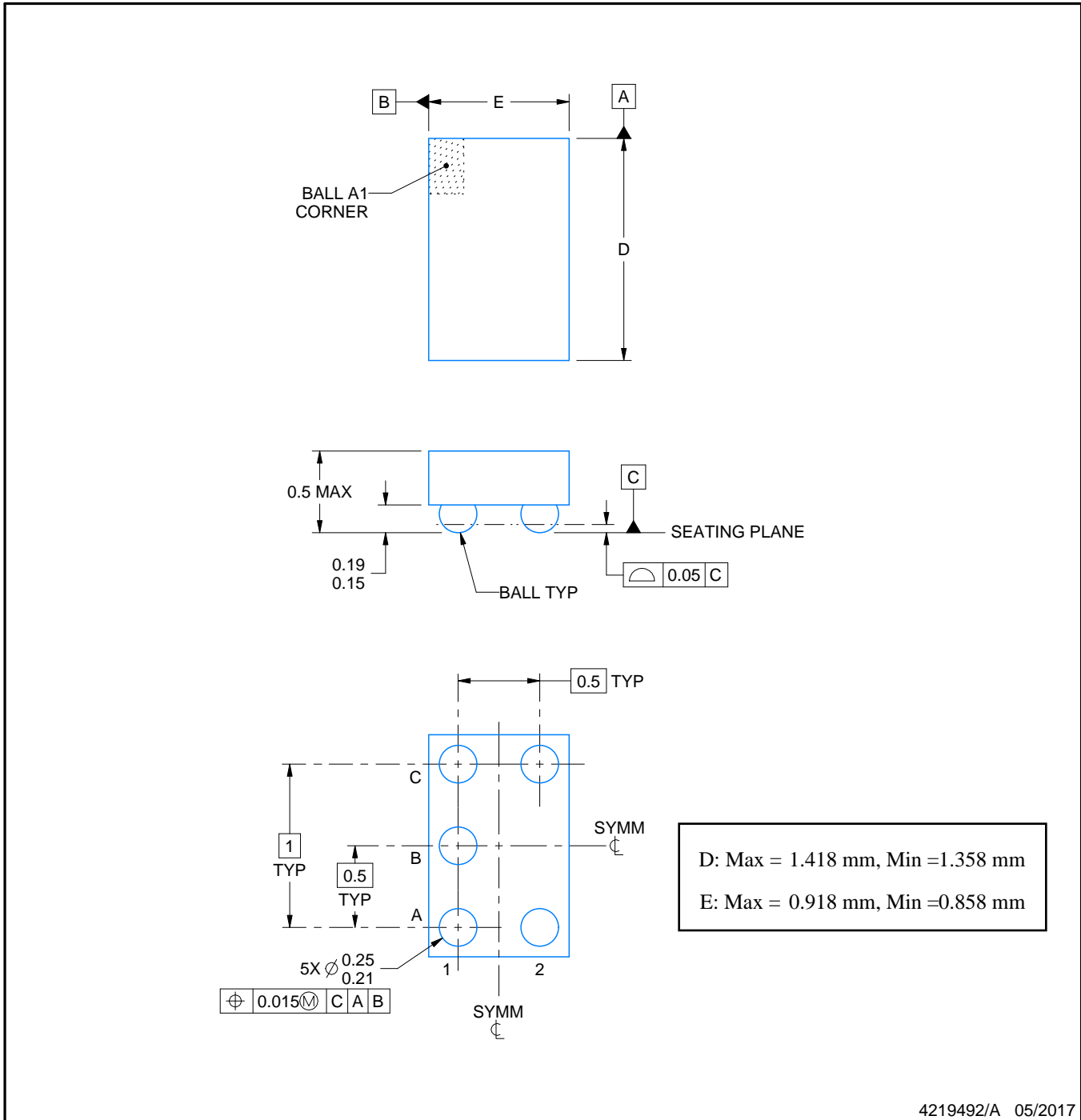
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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