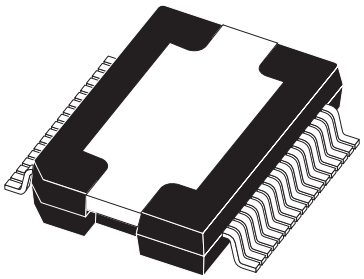
STA516B

65 V, 7.5 A quad power half bridge

Datasheet - production data



PowerSO-36 package with exposed pad up

Features

- Low input/output pulse width distortion
- 200 mΩ R_{dsON} complementary DMOS output stage
- CMOS compatible logic inputs
- Thermal protection
- Thermal warning output
- Undervoltage protection

Description

STA516B is a monolithic quad half-bridge stage in multipower BCD technology. The device can be used as dual bridge or reconfigured, by connecting pin CONFIG to pins VDD, as a single bridge with double-current capability or as a half bridge (binary mode) with half current capability.

The device is designed, particularly, to be the output stage of a stereo all digital high efficiency amplifier. It is capable of delivering 200 W + 200 W into 6 Ω loads with THD = 10% at V_{CC} = 51 V or, in single BTL configuration, 400 W into a 3 Ω load with THD = 10% at V_{CC} = 52 V.

The input pins have a threshold proportional to the voltage on pin VL.

The STA516B is aimed at audio amplifiers in hi-fi applications, such as home theatre systems, active speakers and docking stations.

It comes in a 36 pin PowerSO package with exposed pad up (EPU).

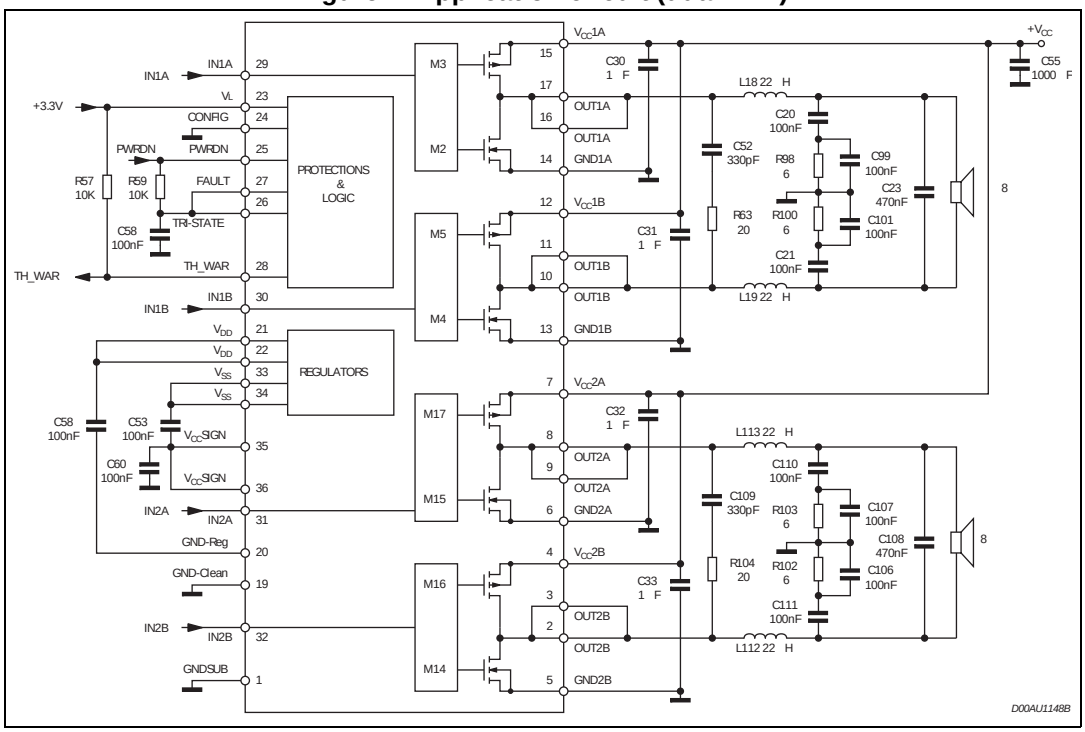
Table 1. Device summary

Order code	Temperature range	Package	Packing
STA516B13TR	0 to 90 °C	PowerSO-36 (EPU)	Tape and reel

Contents

1 Introduction

Figure 1. Application circuit (dual BTL)



2 Pin description

Figure 2. Pin out (top view)

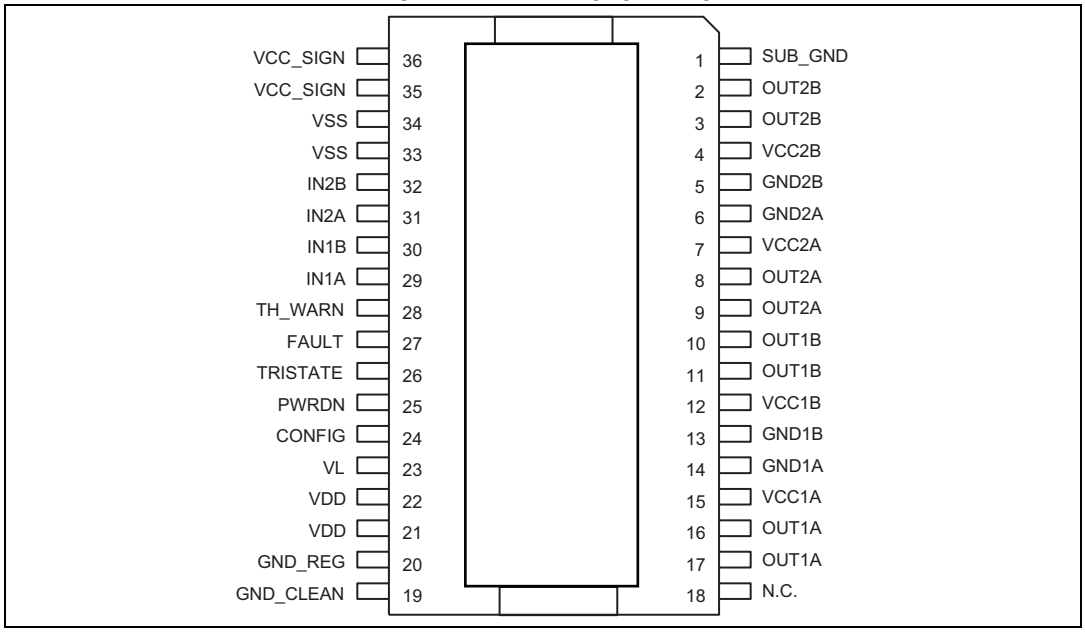


Table 2. Pin function

Pin	Name	Type	Description
1	GND_SUB	PWR	Substrate ground
2, 3	OUT2B	O	Output half bridge 2B
4	VCC2B	PWR	Positive supply
5	GND2B	PWR	Negative supply
6	GND2A	PWR	Negative supply
7	VCC2A	PWR	Positive supply
8, 9	OUT2A	O	Output half bridge 2A
10, 11	OUT1B	O	Output half bridge 1B
12	VCC1B	PWR	Positive supply
13	GND1B	PWR	Negative supply
14	GND1A	PWR	Negative supply
15	VCC1A	PWR	Positive supply
16, 17	OUT1A	O	Output half bridge 1A
18	N.C.	-	No internal connection
19	GND_CLEAN	PWR	Logical ground
20	GND_REG	PWR	Ground for regulator V_{DD}
21, 22	VDD	PWR	5-V regulator referred to ground

Table 2. Pin function (continued)

Pin	Name	Type	Description
23	VL	PWR	High logical state setting voltage, V_L
24	CONFIG	I	Configuration pin: 0: normal operation 1: bridges in parallel (OUT1A = OUT1B, OUT2A = OUT2B (If IN1A = IN1B, IN2A = IN2B))
25	PWRDN	I	Standby pin: 0: low-power mode 1: normal operation
26	TRISTATE	I	Hi-Z pin: 0: all power amplifier outputs in high impedance state 1: normal operation
27	FAULT	O	Fault pin advisor (open-drain device, needs pull-up resistor): 0: fault detected (short circuit or thermal, for example) 1: normal operation
28	TH_WARN	O	Thermal warning advisor (open-drain device, needs pull-up resistor): 0: temperature of the IC >130 °C 1: normal operation
29	IN1A	I	Input of half bridge 1A
30	IN1B	I	Input of half bridge 1B
31	IN2A	I	Input of half bridge 2A
32	IN2B	I	Input of half bridge 2B
33, 34	VSS	PWR	5-V regulator referred to $+V_{CC}$
35, 36	VCC_SIGN	PWR	Signal positive supply

3 Electrical characteristics

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC_MAX}	DC supply voltage (pins 4, 7, 12, 15)	65	V
V_{max}	Maximum voltage on pins 23 to 32	5.5	V
T_{j_MAX}	Operating junction temperature	0 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

Warning: **Stresses beyond those listed under "Absolute maximum ratings" make cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating condition" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supply with nominal value rated inside recommended operating conditions, may experience some rising beyond the maximum operating condition for short time when no or very low current is sinked (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum rating is not exceeded.**

Table 4. Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{j\text{-}case}$	Thermal resistance junction to case (thermal pad)	-	1	2.5	°C/W
T_{warn}	Thermal warning temperature	-	130	-	°C
T_{jSD}	Thermal shut-down junction temperature	-	150	-	°C
t_{hSD}	Thermal shut-down hysteresis	-	25	-	°C

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage for pins PVCCA, PVCCB	10	-	58	V
T_{amb}	Ambient operating temperature	0	-	90	°C

Unless otherwise stated, the test conditions for *Table 6* below are V_L = 3.3 V, V_{CC} = 50 V and T_{amb} = 25 °C

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{dsON}	Power P-channel/N-channel MOSFET R_{dsON}	I_{dd} = 1 A	-	200	240	mΩ
I_{dss}	Power P-channel/N-channel leakage Idss	-	-	-	50	µA
g_N	Power P-channel R_{dsON} matching	I_{dd} = 1 A	95	-	-	%
g_P	Power N-channel R_{dsON} matching	I_{dd} = 1 A	95	-	-	%
Dt_s	Low current dead time (static)	see *Figure 3*	-	10	20	ns
Dt_d	High current dead time (dynamic)	L = 22 µH, C = 470 nF R_L = 8 Ω, I_{dd} = 4.5 A see *Figure 4*	-	-	50	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load	-	-	100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load	-	-	100	ns
t_r	Rise time	Resistive load see *Figure 3*	-	-	25	ns
t_f	Fall time	Resistive load see *Figure 3*	-	-	25	ns
$V_{IN\text{-}High}$	High level input voltage	-	-	-	V_L / 2 + 300 mV	V
$V_{IN\text{-}Low}$	Low level input voltage	-	V_L / 2 - 300 mV	-	-	V
$I_{IN\text{-}H}$	High level input current	V_{IN} = V_L	-	1	-	µA
$I_{IN\text{-}L}$	Low level input current	V_{IN} = 0.3 V	-	1	-	µA
$I_{PWRDN\text{-}H}$	High level PWRDN pin input current	V_L = 3.3 V	-	35	-	µA
V_{Low}	Low logical state voltage (pins PWRDN, TRISTATE) (see*Table 7*)	V_L = 3.3 V	0.8	-		V
V_{High}	High logical state voltage (pins PWRDN, TRISTATE) (see*Table 7*)	V_L = 3.3 V		-	1.7	V
$I_{VCC\text{-}PWRDN}$	Supply current from V_{CC} in power down	V_{PWRDN} = 0 V	-	-	2.4	mA
I_{FAULT}	Output current on pins FAULT, TH_WARN with fault condition	V_{pin} = 3.3 V	-	1	-	mA
$I_{VCC\text{-}HiZ}$	Supply current from V_{CC} in tristate	$V_{TRISTATE}$ = 0 V	-	22	-	mA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{VCC}	Supply current from V_{CC} in operation, both channels switching)	Input pulse width = 50% duty, switching frequency = 384 kHz, no LC filters	-	70	-	mA
I_{OCP}	Overcurrent protection threshold I_{sc} (short-circuit current limit) (1)	-	7.5	8.5	10	A
V_{UVP}	Undervoltage protection threshold	-	-	7	-	V
V_{OVP}	Overvoltage protection threshold	-	61	62.5		V
t_{pw_min}	Output minimum pulse width	No load	50	-	110	ns

1. See specific application note number: AN1994

Table 7. Threshold switching voltage variation with voltage on pin VL

Voltage on pin VL, V_L	V_{LOW} max.	V_{HIGH} min.	Unit
2.7	1.05	1.65	V
3.3	1.4	1.95	V
5.0	2.2	2.8	V

Table 8. Logic truth table

Pin TRISTATE	Inputs as per *Figure 4*		Transistors as per *Figure 4*				Output mode
	INxA	INxB	Q1	Q2	Q3	Q4	
0	x	x	Off	Off	Off	Off	Hi Z
1	0	0	Off	Off	On	On	Dump
1	0	1	Off	On	On	Off	Negative
1	1	0	On	Off	Off	On	Positive
1	1	1	On	On	Off	Off	Not used

3.1 Test circuits

Figure 3. Test circuit

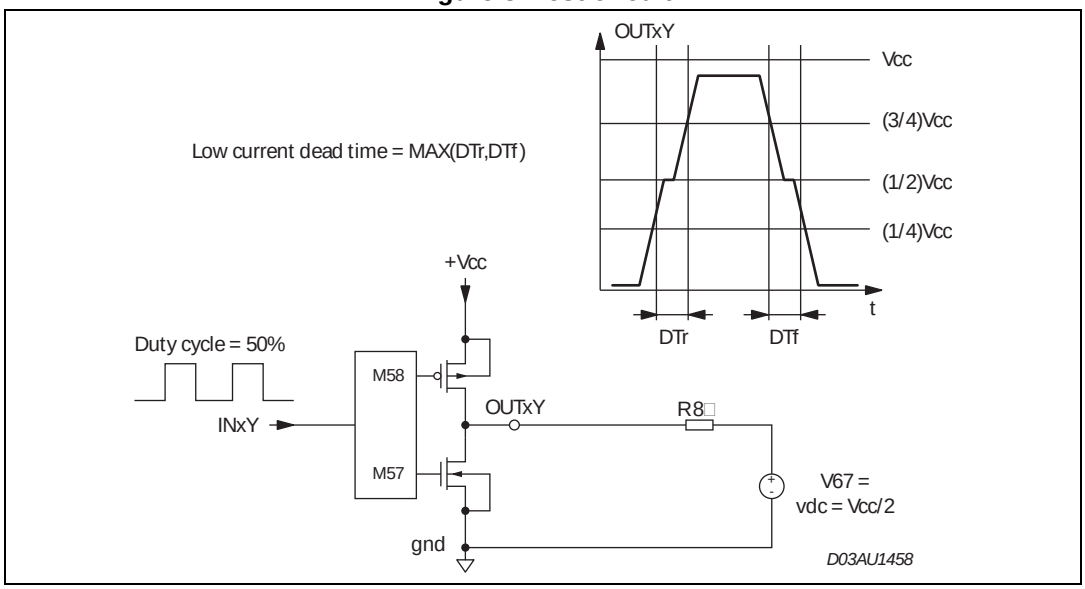
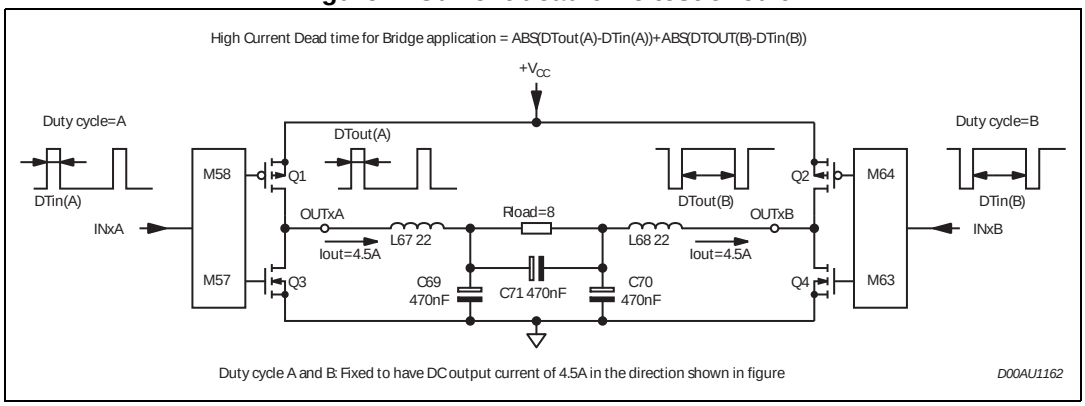


Figure 4. Current dead-time test circuit



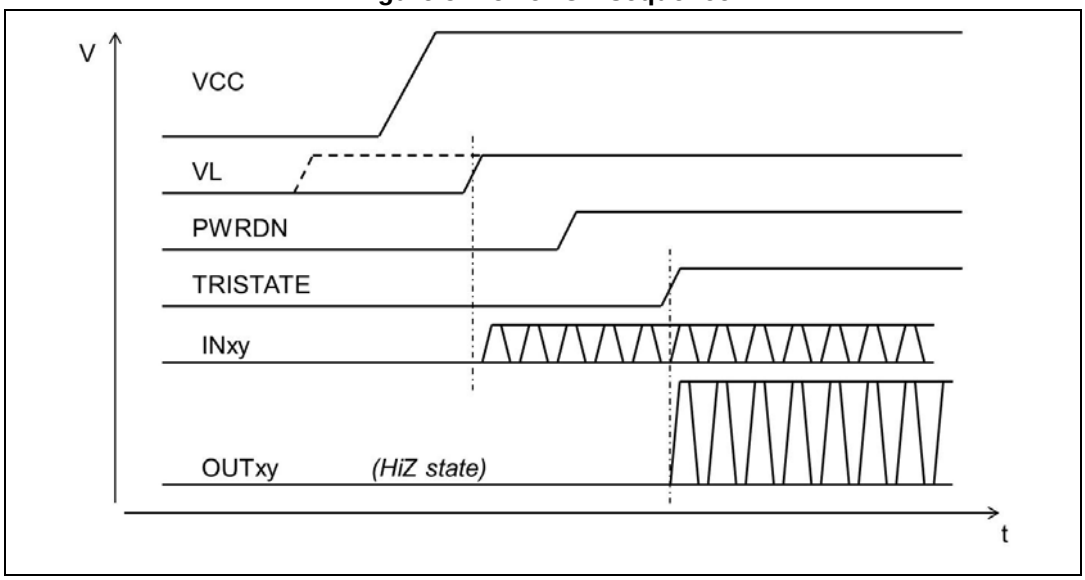
4 Power supply and control sequencing

To guarantee correct operation and reliability, the recommended power-on sequence as given below should be followed:

- Apply V_{CC} and V_L, in any order, keeping PWRDN low in this phase
- Release PWRDN from low to high, keeping TRISTATE low (until V_{DD} and V_{SS} are stable)
- Release TRISTATE from low to high

Always maintain PWM inputs INxy < V_L.

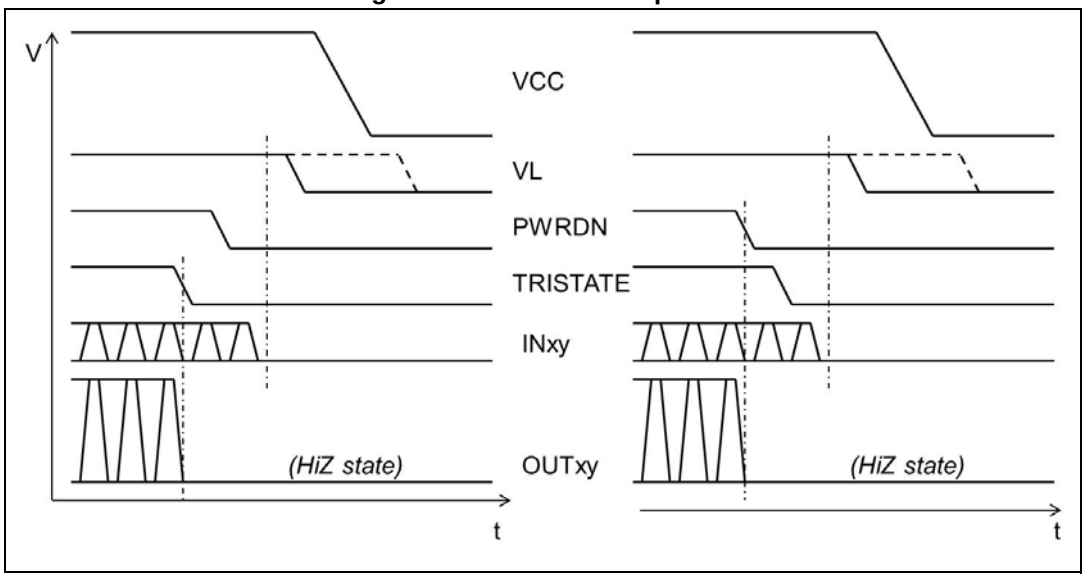
Figure 5. Power-ON sequence



Power-OFF sequence:

– When TRISTATE or PWRDN go low, the outputs go into HiZ state
– Inputs INxy are removed before VL is removed
– VL can be removed before or after VCC

Figure 6. Power-OFF sequence



5 Technical information

The STA516B is a dual channel H-bridge that is able to deliver 200 W per channel (into R_L = 6 Ω with THD = 10% and V_{CC} = 51 V) of audio output power very efficiently. It operates in conjunction with a pulse-width modulator driver such as the STA321 or STA309A.

The STA516B converts ternary, phase-shift or binary-controlled PWM signals into audio power at the load. It includes a logic interface, integrated bridge drivers, high efficiency MOSFET outputs and thermal and short-circuit protection circuitry.

In differential mode (ternary, phase-shift or binary differential), two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a bridge configuration, according to the damped ternary modulation operation.

In binary mode, both full bridge and half bridge modes are supported. The STA516B includes overcurrent and thermal protection as well as an undervoltage lockout with automatic recovery. A thermal warning status is also provided.

Figure 7. Block diagram of full-bridge DDX® or binary mode

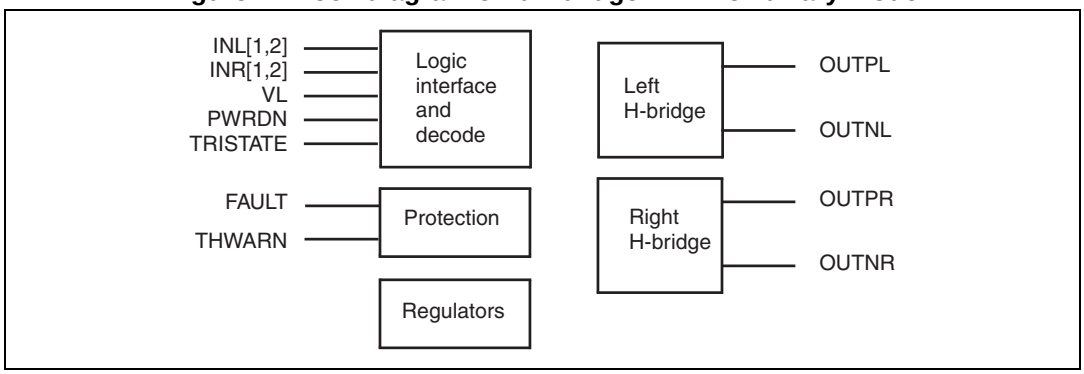
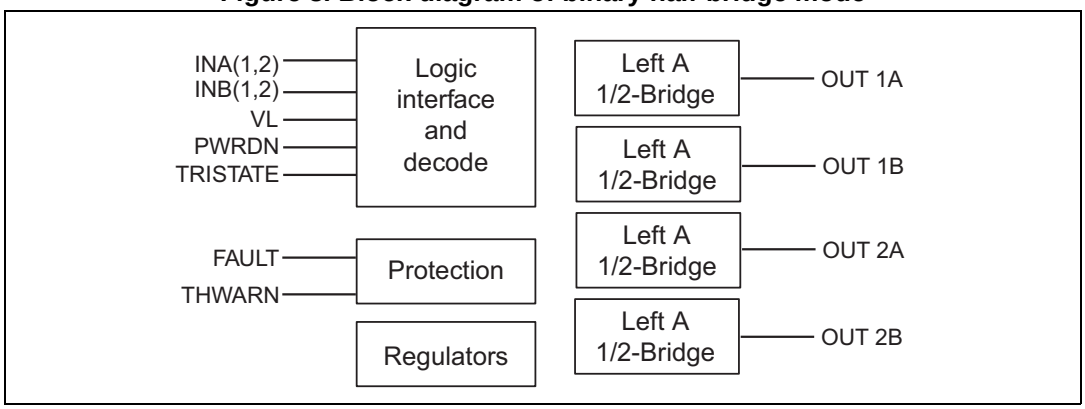


Figure 8. Block diagram of binary half-bridge mode



5.1 Logic interface and decode

The STA516B power outputs are controlled using one or two logic-level timing signals. In order to provide a proper logic interface, the V_L input must operate at the same voltage as the DDX control logic supply.

5.2 Protection circuitry

The STA516B includes protection circuitry for overcurrent and thermal overload conditions. A thermal warning pin (THWARN, pin 28, open drain MOSFET) is activated low when the IC temperature exceeds 130 °C, just in advance of thermal shutdown. When a fault condition is detected an internal fault signal immediately disables the output power MOSFETs, placing both H-bridges in a high-impedance state. At the same time the open-drain MOSFET of pin FAULT (pin 27) is switched on.

There are two possible modes subsequent to activating a fault.

- **Shutdown mode**: with pins FAULT (with pull-up resistor) and TRISTATE separate, an activated fault disables the device, signaling a low at pin FAULT output.
  The device may subsequently be reset to normal operation by toggling pin TRISTATE from high to low to high using an external logic signal.
- **Automatic recovery mode:** This is shown in the applications circuits below where pins FAULT and TRISTATE are connected together to a time-constant circuit (R59 and C58).
  An activated fault forces a reset on pin TRISTATE causing normal operation to resume following a delay determined by the time constant of the circuit.
  If the fault condition persists, the circuit operation repeats until the fault condition is cleared.
  An increase in the time constant of the circuit produces a longer recovery interval. Care must be taken in the overall system design not to exceed the protection threshold under normal operation.

5.3 Power outputs

The STA516B power and output pins are duplicated to provide a low-impedance path for the device bridged outputs. All duplicate power, ground and output pins must be connected for proper operation.

The PWRDN or TRISTATE pin should be used to set all power MOSFETs to the high-impedance state during power-up until the logic power supply, V_L, has settled.

5.4 Parallel output / high current operation

When using the DDX mode output, the STA516B outputs can be connected in parallel in order to increase the output current capability to a load. In this configuration the STA516B can provide up to 240 W into a 3 Ω load.

This mode of operation is enabled with the pin CONFIG (pin 24) connected to pin VDD. The inputs are joined so that IN1A = IN1B, IN2A = IN2B and similarly the outputs OUT1A = OUT1B, OUT2A = OUT2B as shown in *Figure 9 on page 14*

5.5 Output filtering

A passive 2nd order filter is used on the STA516B power outputs to reconstruct the analog audio signal. System performance can be significantly affected by the output filter design and choice of passive components. A filter design for 6 or 8 Ω loads is shown in the application circuit of *Figure 8*, and for 3 or 4 Ω loads in *Figure 9* and *Figure 10*.

6 Applications

Figure 9 below shows a single-BLT configuration capable of giving 400 W into a 3 Ω load at 10% THD with V_{CC} = 52 V. This result was obtained using the STA30X+STA50X demo board. Note that a PWM modulator as driver is required.

Figure 9. Typical single-BTL configuration for 400 W

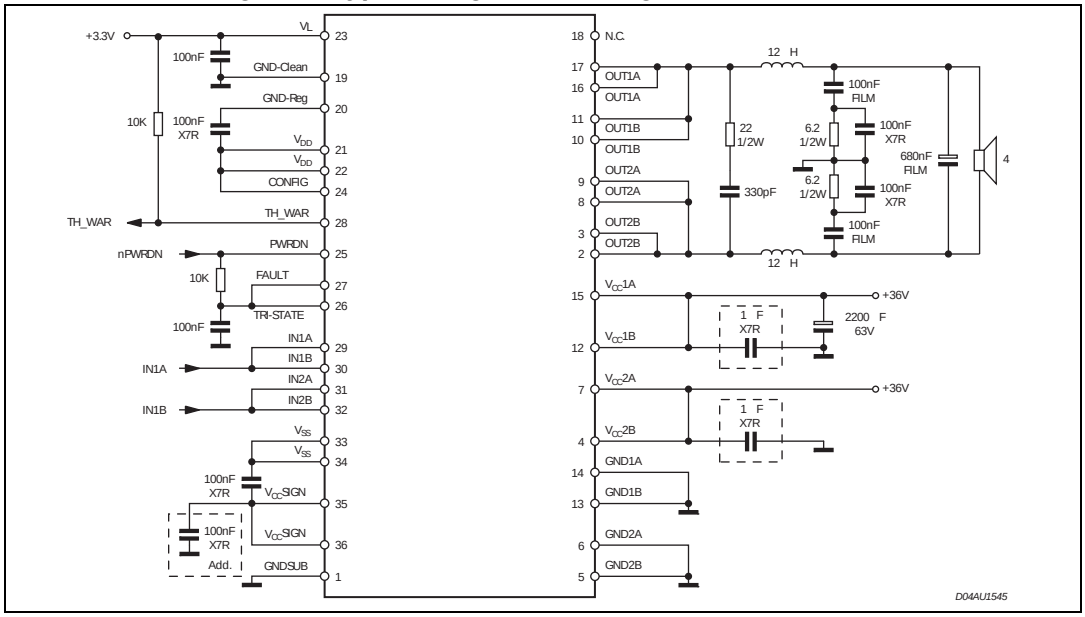
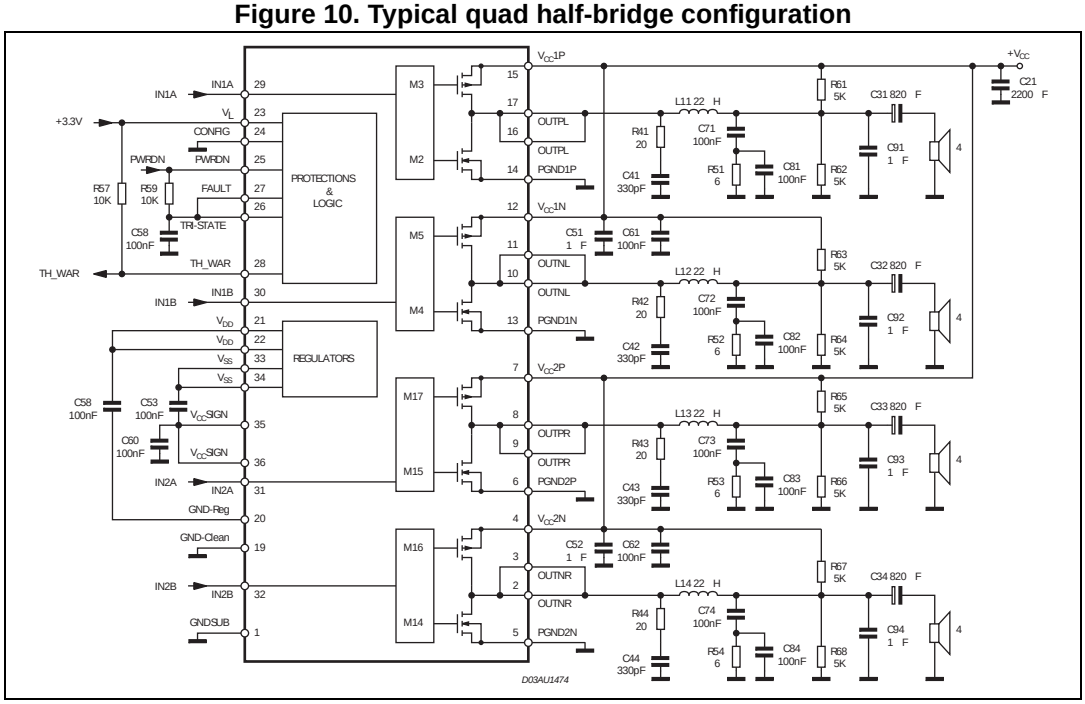


Figure 10. Typical quad half-bridge configuration



For more information, refer to the application note AN1994.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK is an ST trademark

7.1 PowerSO-36 exposed pad up package information

Figure 11. PowerSO-36 exposed pad up package outline

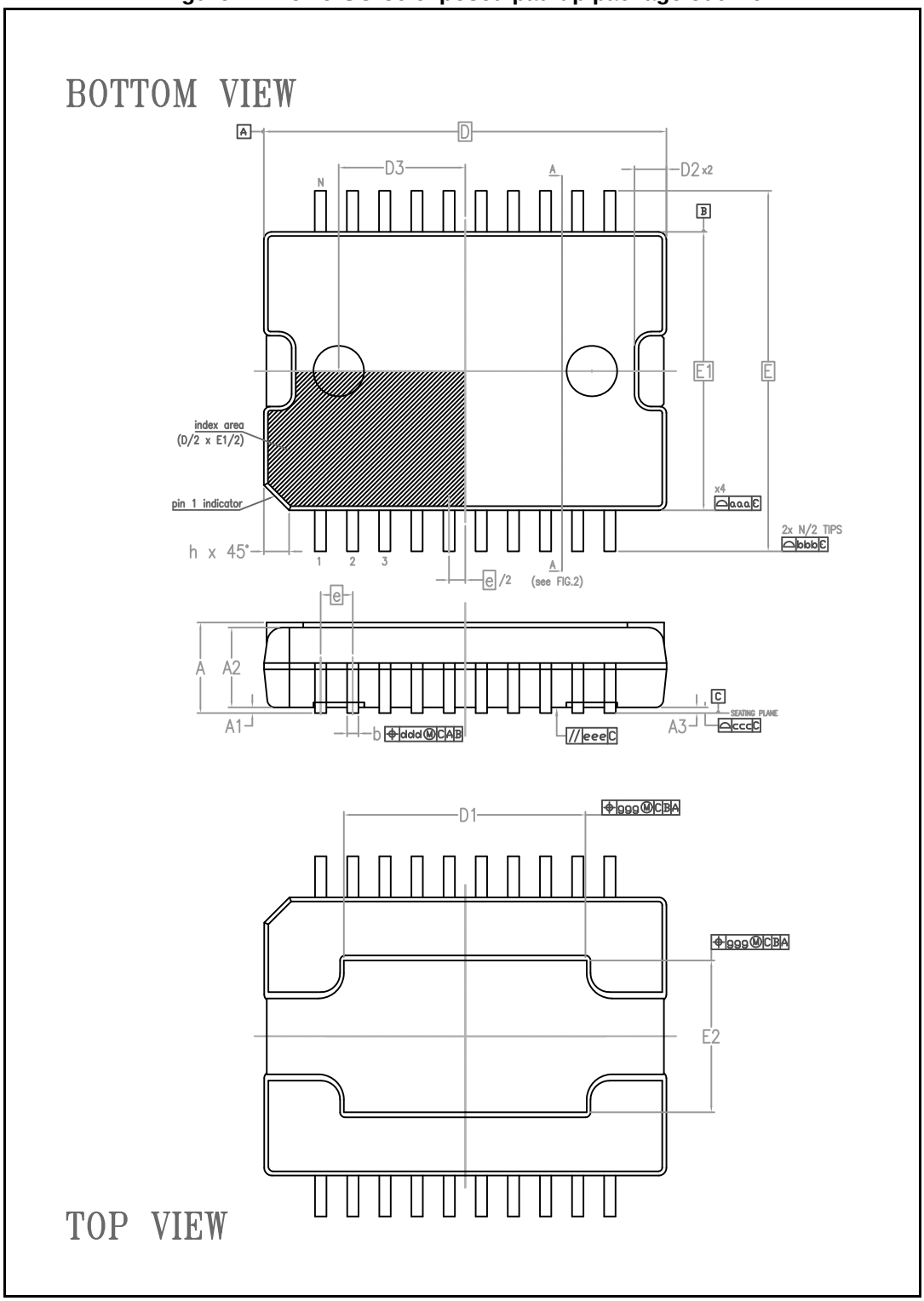


Figure 12. PowerSO-36 section A-A and B-B package outline

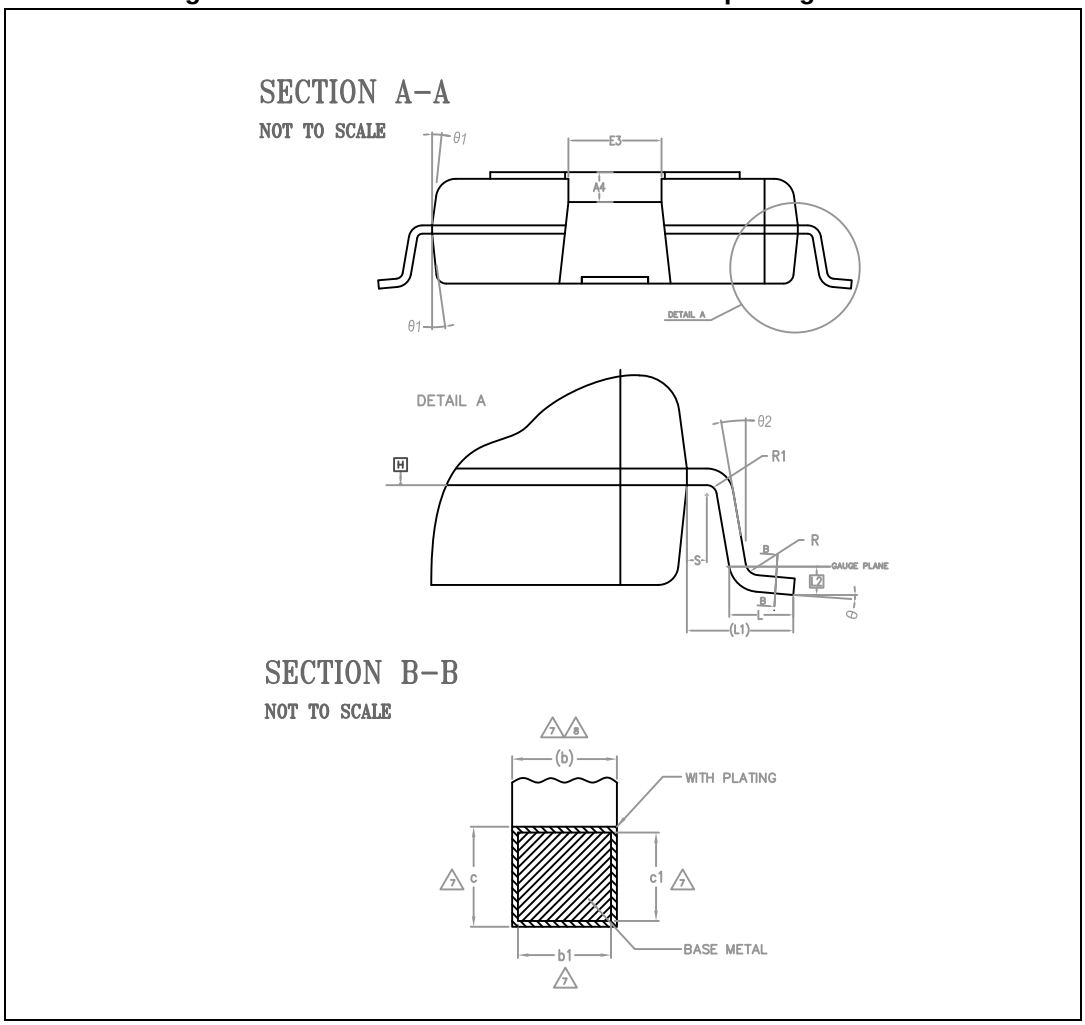


Table 9. PowerSO-36 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
Θ	0°	-	8°
Θ1	5°	-	10°
Θ2	0°	-	-
A	-	-	3.41
A1	0.30	-	-0.40
A2	3.10	3.14	3.18
A3	-	0.2	-
A4	0.80	-	1.00
b	0.22	-	0.41
b1	0.22	-	0.38
c	0.23	-	0.32
c1	0.23	0.25	0.29
D	15.90 BSC		
D1	VARIATION		
D2		-	1.00
D3	-	5.00	-
e	0.65 BSC		
E	14.20 BSC		
E1	11.00 BSC		
E2	VARIATION		
E3	-	-	2.90
h	-	-	1.10
L	0.80	-	1.10
L1	1.60 REF		
L2	0.35 BSC		
N	36		
R	0.20	-	-
R1	0.20	-	-
s	0.25	-	-

Table 10. Tolerance of form and position

Symbol	Databook
aaa	0.10
bbb	0.30
ccc	0.075
ddd	0.25
eee	0.10
ggg	0.25
Note	1.2

Table 11. Variations

Symbol	Databook			Opt.
	Min.	Typ.	Max.	
D1	9.40	-	9.80	A
E2	5.80	-	6.20	

8 Revision history

Table 12. Document revision history

Date	Revision	Changes
01-Feb-2007	1	Initial release.
19-Mar-2007	2	Updated to reflect product maturity.
11-Aug-2009	3	Updated section Description on cover page.
16-Nov-2010	4	Modified presentation Updated Chapter 3: Electrical specifications on page 5 Added Chapter 5: Applications information on page 10
15-Jan-2014	5	Modified *Section 4: Power supply and control sequencing on page 9*
11-Feb-2014	6	Updated order code *Table 1 on page 1*
16-Nov-2020	7	Updated *Section 7.1: PowerSO-36 exposed pad up package information*.

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