TL431A, B Series, NCV431A, B Series, SCV431A

Programmable Precision References

The TL431A, B integrated circuits are three−terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

Features

- Programmable Output Voltage to 36 V
- Voltage Reference Tolerance: ±0.4%, Typ @ 25°C (TL431B)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 mA to 100 mA
- Equivalent Full−Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- NCV/SCV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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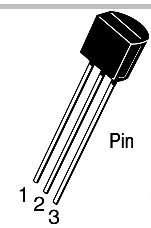
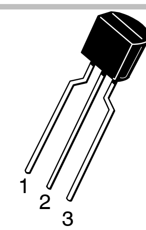


Pin 1. Reference
2. Anode
3. Cathode

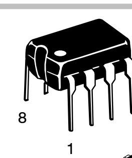


STRAIGHT LEAD
BULK PACK

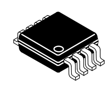
BENT LEAD
TAPE & REEL
AMMO PACK

TO−92
LP SUFFIX
CASE 29−11

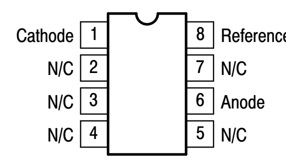
TO−92
LPRA, LPRE, LPRM, LPRP SUFFIX
CASE 29−11



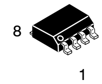
PDIP−8
P SUFFIX
CASE 626



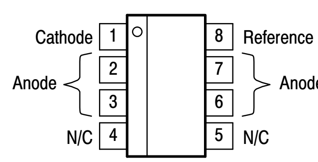
Micro8™
DM SUFFIX
CASE 846A



(Top View)



SOIC−8
D SUFFIX
CASE 751



(Top View)

This is an internally modified SOIC−8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification increases power dissipation capability when appropriately mounted on a printed circuit board. This modified package conforms to all external dimensions of the standard SOIC−8 package.

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 14 of this data sheet.

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January, 2019 − Rev. 40
Publication Order Number:
TL431/D

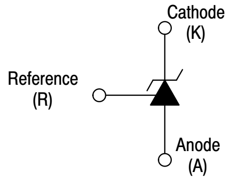


Figure 1. Symbol

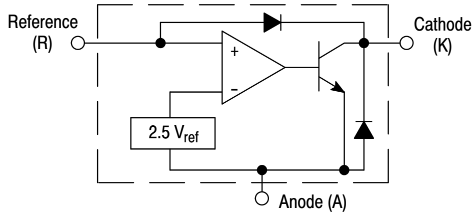


Figure 2. Representative Block Diagram

This device contains 12 active transistors.

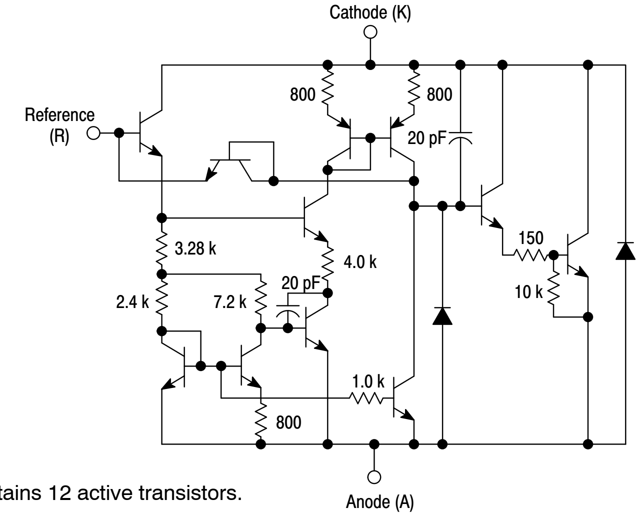


Figure 3. Representative Schematic Diagram

Component values are nominal

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	−100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	−0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A		°C
TL431I, TL431AI, TL431BI		−40 to +85	
TL431C, TL431AC, TL431BC		0 to +70	
NCV431AI, NCV431B, TL431BV, SCV431AI		−40 to +125	
Storage Temperature Range	T_{stg}	−65 to +150	°C
Total Power Dissipation @ T_A = 25°C	P_D		W
Derate above 25°C Ambient Temperature			
D, LP Suffix Plastic Package		0.70	
P Suffix Plastic Package		1.10	
DM Suffix Plastic Package		0.52	
Total Power Dissipation @ T_C = 25°C	P_D		W
Derate above 25°C Case Temperature			
D, LP Suffix Plastic Package		1.5	
P Suffix Plastic Package		3.0	
ESD Rating (Note 1)			V
Human Body Model per JEDEC JESD22−A114F	HBM	>2000	
Machine Model per JEDEC JESD22−A115C	MM	>200	
Charged Device Model per JEDEC JESD22−C101E	CDM	>500	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch−up protection and exceeds ±100 mA per JEDEC standard JESD78.

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL CHARACTERISTICS

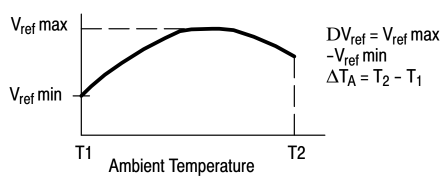
Characteristic	Symbol	D, LP Suffix Package	P Suffix Package	DM Suffix Package	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	178	114	240	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83	41	–	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 2)	V_{ref}	 2.44 2.41	 2.495 –	 2.55 2.58	 2.44 2.423	 2.495 –	 2.55 2.567	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 3, 4) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	–	7.0	30	–	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	 – –	 −1.4 −1.0	 −2.7 −2.0	 – –	 −1.4 −1.0	 −2.7 −2.0	mV/V
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞ T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 2)	I_{ref}	 – –	 1.8 –	 4.0 6.5	 – –	 1.8 –	 4.0 5.2	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 3) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	–	0.8	2.5	–	0.4	1.2	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	–	0.5	1.0	–	0.5	1.0	mA
Off−State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	–	20	1000	–	20	1000	nA
Dynamic Impedance (Figure 1, Note 5) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA, f ≤ 1.0 kHz	$\|Z_{KA}\|$	–	0.22	0.5	–	0.22	0.5	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. T_{low} = −40°C for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM;
   = 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
   T_{high} = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM
   = +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
3. Guaranteed by design.
4. The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$V_{ref}\ \frac{ppm}{°C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref}\ @\ 25°C}\right) X\ 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref}\ @\ 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,
V_{ref} @ 25°C = 2.495 V, ΔT_A = 70°C

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70\ (2.495)} = 45.8\ ppm/°C$$

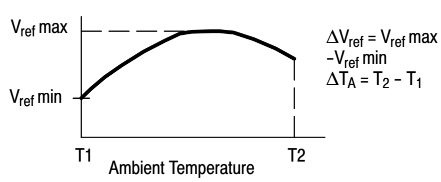
5. The dynamic impedance Z_{KA} is defined as: $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$. When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as: $|Z_{KA}'| \approx |Z_{KA}| \left(1 + \frac{R1}{R2}\right)$

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431AI / NCV431AI/ SCV431AI			TL431AC			TL431BC / TL431BI / TL431BV / NCV431BV			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 6)	V_{ref}	2.47 2.44	2.495 –	2.52 2.55	2.47 2.453	2.495 –	2.52 2.537	2.485 2.475	2.495 2.495	2.505 2.515	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 7, 8) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	–	7.0	30	–	3.0	17	–	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	– –	−1.4 −1.0	−2.7 −2.0	– –	−1.4 −1.0	−2.7 −2.0	– –	−1.4 −1.0	−2.7 −2.0	mV/V
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞ T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 6)	I_{ref}	– –	1.8 –	4.0 6.5	– –	1.8 –	4.0 5.2	– –	1.1 –	2.0 4.0	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 7) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	–	0.8	2.5	–	0.4	1.2	–	0.8	2.5	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	–	0.5	1.0	–	0.5	1.0	–	0.5	1.0	mA
Off−State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	–	20	1000	–	20	1000	–	0.23	500	nA
Dynamic Impedance (Figure 1, Note 9) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{KA} \rvert$	–	0.22	0.5	–	0.22	0.5	–	0.14	0.3	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. T_{low} = −40°C for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431BV, TL431AIDM, TL431IDM, TL431BIDM, NCV431AIDMR2G, NCV431AIDR2G, NCV431BVDR2G, SCV431AIDMR2G
   = 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM, SCV431AIDMR2G
   T_{high} = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM
   = +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
   = +125°C TL431BV, NCV431AIDMR2G, NCV431AIDR2G, NCV431BVDMR2G, NCV431BVDR2G, SCV431AIDMR2G
7. Guaranteed by design.
8. The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$V_{ref}\ \frac{ppm}{°C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref}\ @\ 25°C}\right) X\ 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref}\ @\ 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,

V_{ref} @ 25°C = 2.495 V, ΔT_A = 70°C

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70\ (2.495)} = 45.8\ ppm/°C$$

9. The dynamic impedance Z_{KA} is defined as $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$ When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as: $|Z_{KA}'| \approx |Z_{KA}| \left(1 + \frac{R1}{R2}\right)$
10. NCV431AIDMR2G, NCV431AIDR2G, NCV431BVDMR2G, NCV431BVDR2G, SCV431AIDMR2G T_{low} = −40°C, T_{high} = +125°C. NCV prefix is for automotive and other applications requiring unique site and control change requirements.

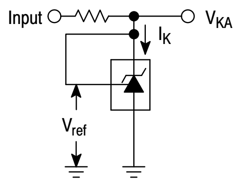


Figure 1. Test Circuit for $V_{KA} = V_{ref}$

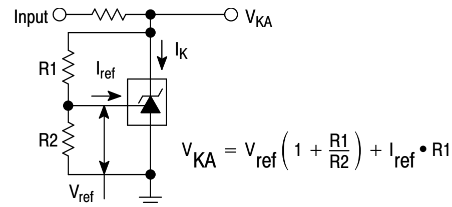


Figure 2. Test Circuit for $V_{KA} > V_{ref}$

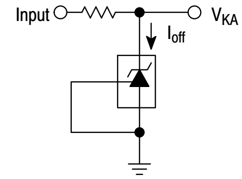


Figure 3. Test Circuit for I_{off}

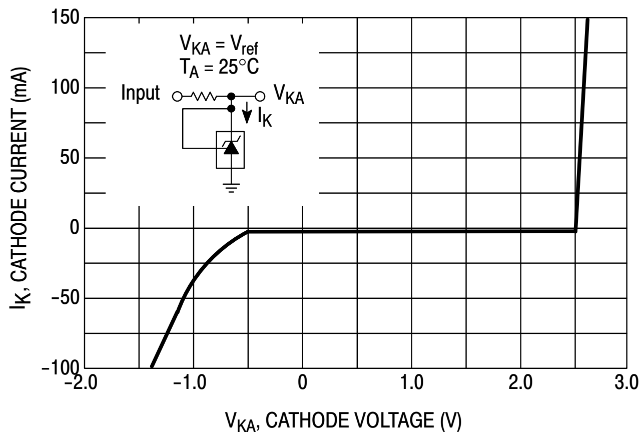


Figure 4. Cathode Current versus Cathode Voltage

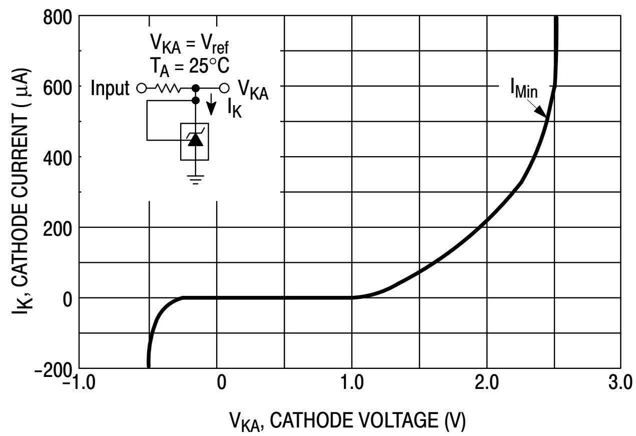


Figure 5. Cathode Current versus Cathode Voltage

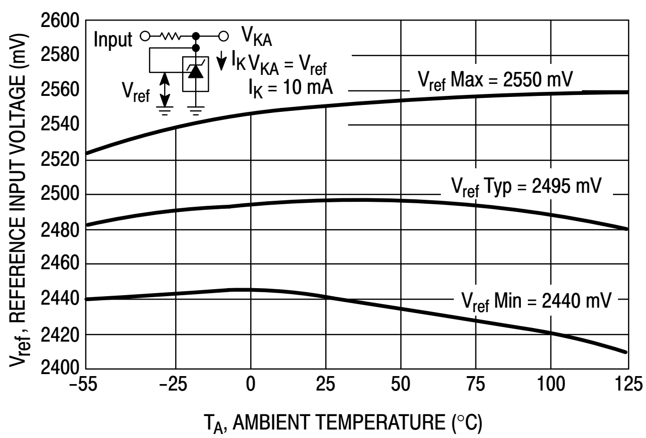


Figure 6. Reference Input Voltage versus Ambient Temperature

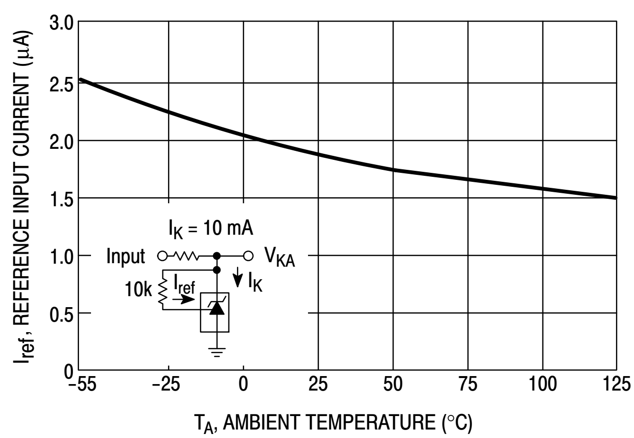


Figure 7. Reference Input Current versus Ambient Temperature

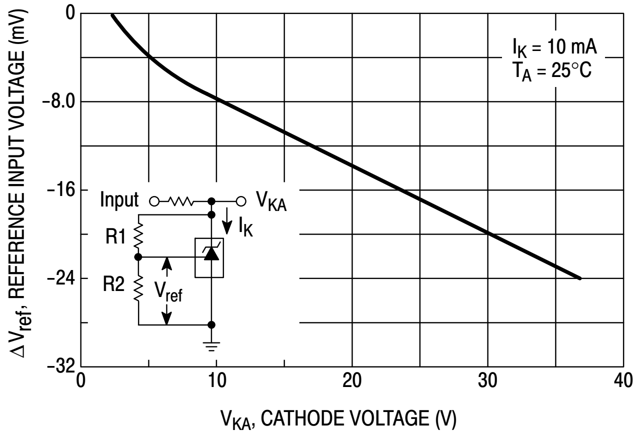


Figure 8. Change in Reference Input Voltage versus Cathode Voltage

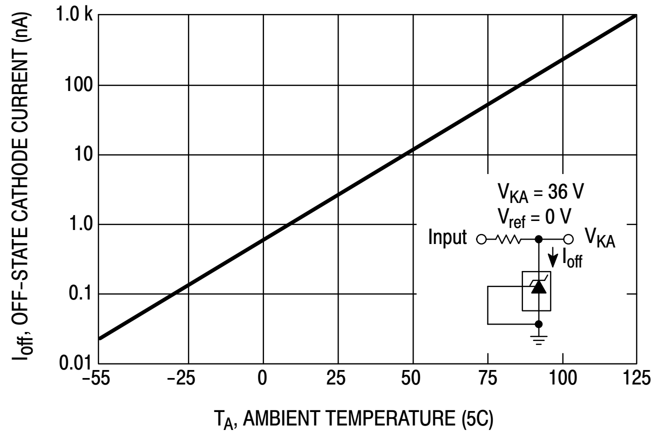


Figure 9. Off−State Cathode Current versus Ambient Temperature

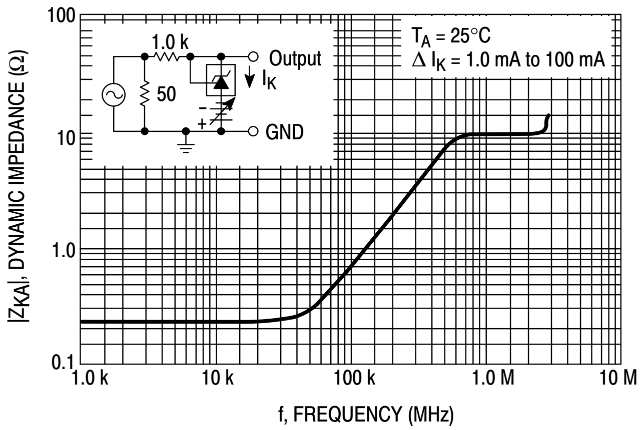


Figure 10. Dynamic Impedance versus Frequency

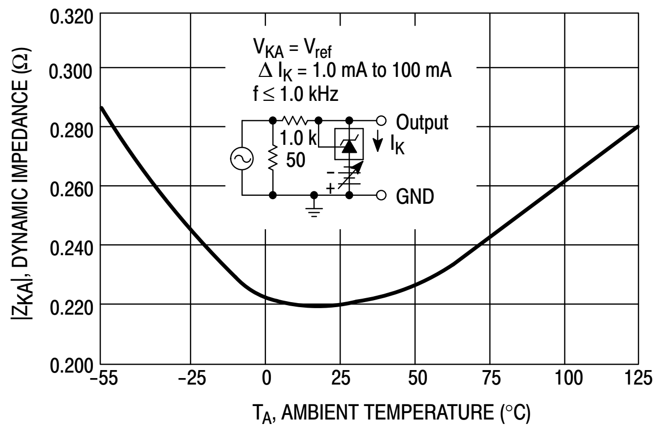


Figure 11. Dynamic Impedance versus Ambient Temperature

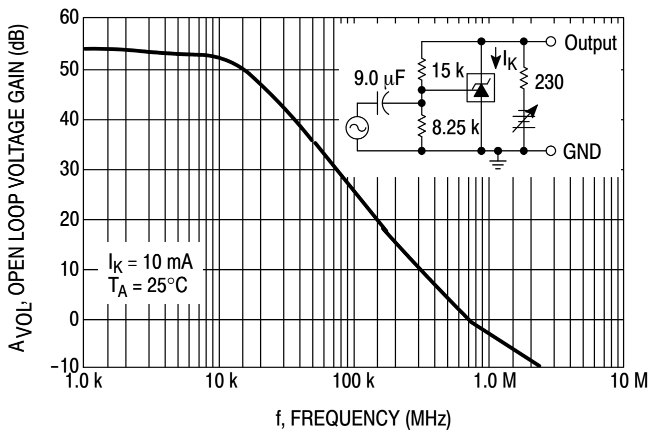


Figure 12. Open−Loop Voltage Gain versus Frequency

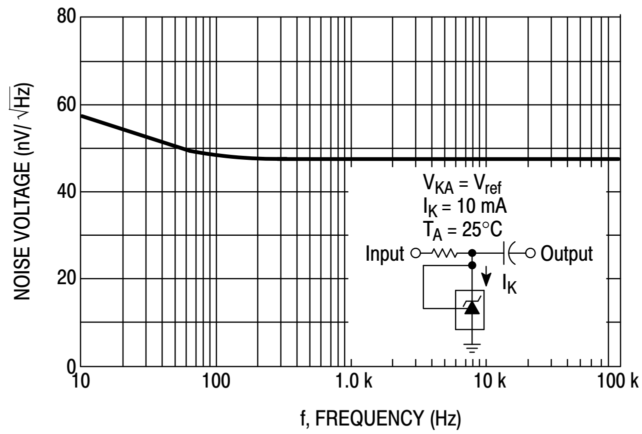


Figure 13. Spectral Noise Density

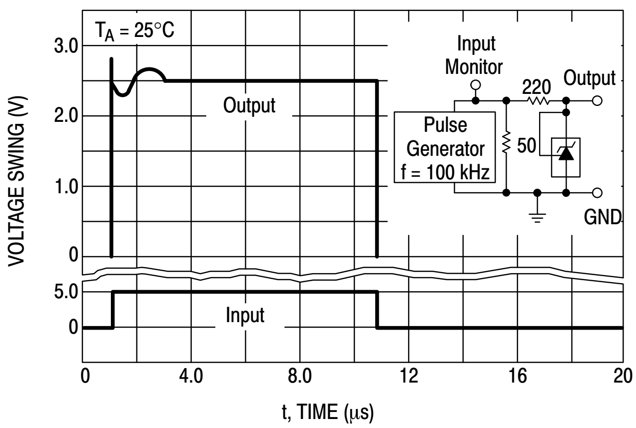


Figure 14. Pulse Response

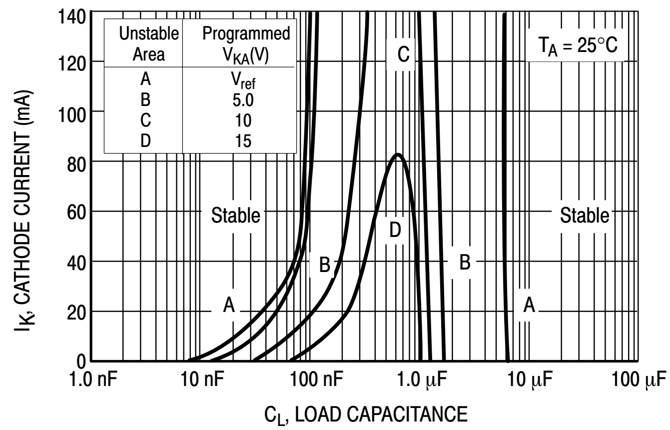


Figure 15. Stability Boundary Conditions

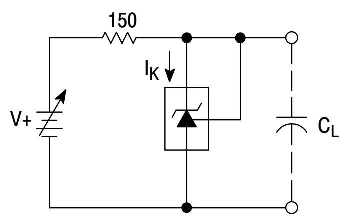


Figure 16. Test Circuit For Curve A of Stability Boundary Conditions

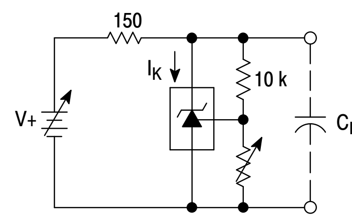


Figure 17. Test Circuit For Curves B, C, And D of Stability Boundary Conditions

TYPICAL APPLICATIONS

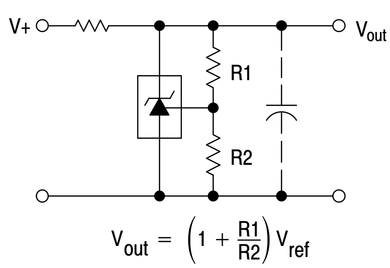


Figure 18. Shunt Regulator

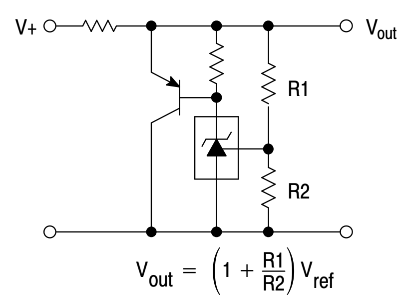
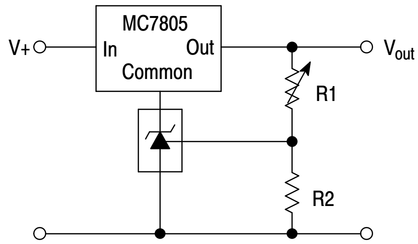


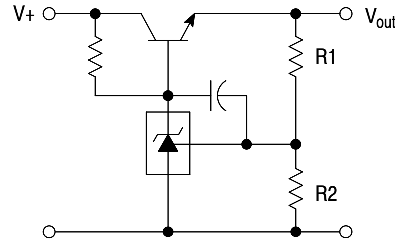
Figure 19. High Current Shunt Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$V_{out(min)} = V_{ref} + 5.0\ V$$

Figure 20. Output Control for a Three−Terminal Fixed Regulator

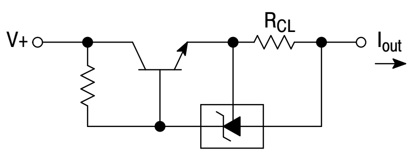


$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$V_{in(min)} = V_{out} + V_{be}$$

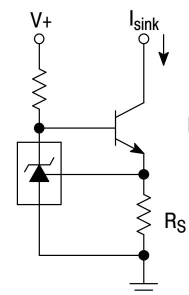
$$V_{out(min)} = V_{ref}$$

Figure 21. Series Pass Regulator



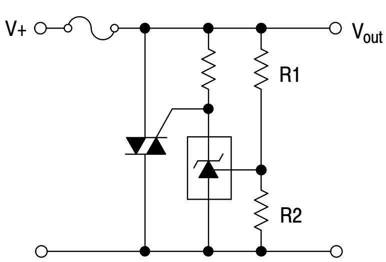
$$I_{out} = \frac{V_{ref}}{R_{CL}}$$

Figure 22. Constant Current Source



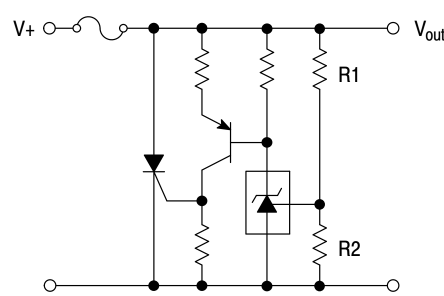
$$I_{Sink} = \frac{V_{ref}}{R_S}$$

Figure 23. Constant Current Sink



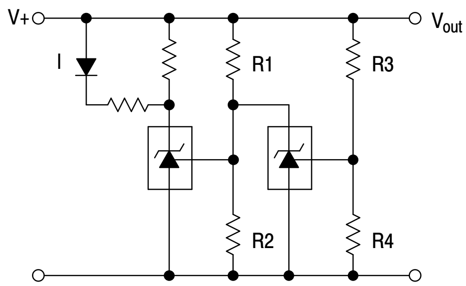
$$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 24. TRIAC Crowbar



$$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 25. SRC Crowbar

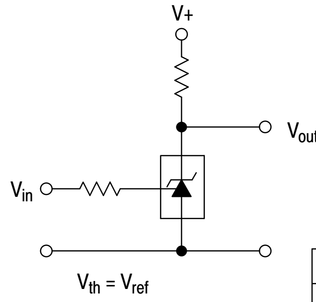


L.E.D. indicator is 'on' when V+ is between the upper and lower limits.

$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$$

Figure 26. Voltage Monitor



V_{in}	V_{out}
< V_{ref}	V+
> V_{ref}	≈ 2.0 V

Figure 27. Single−Supply Comparator with Temperature−Compensated Threshold

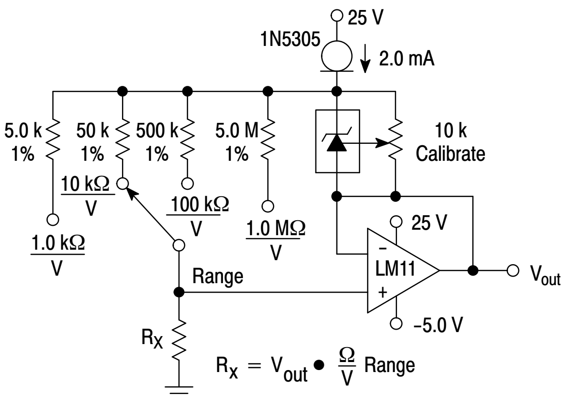


Figure 28. Linear Ohmmeter

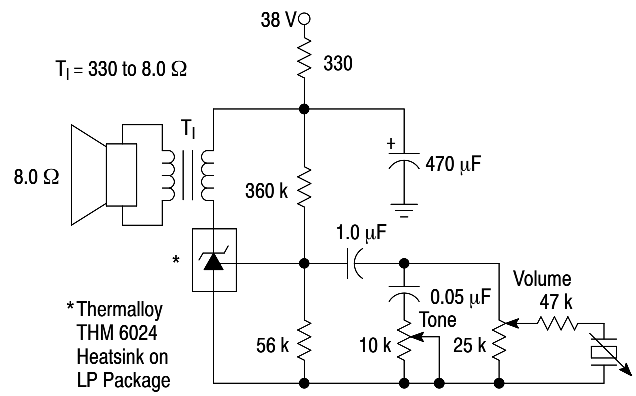


Figure 29. Simple 400 mW Phono Amplifier

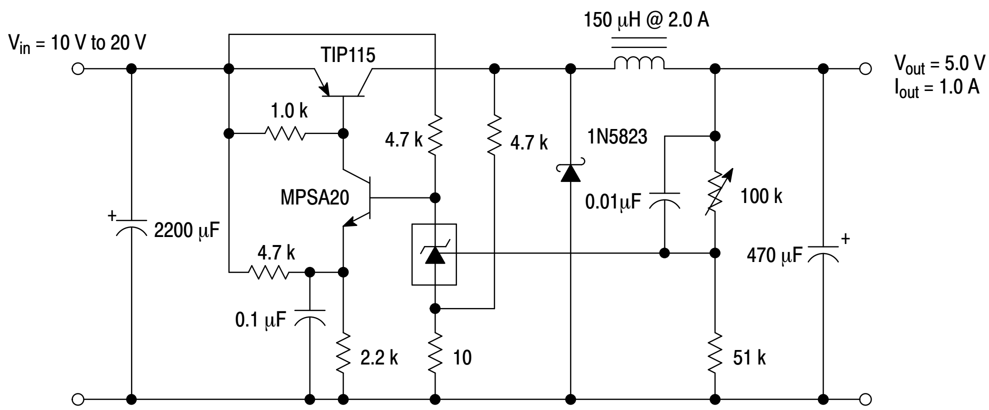


Figure 30. High Efficiency Step−Down Switching Converter

Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 20 V, I_o = 1.0 A	53 mV (1.1%)
Load Regulation	V_{in} = 15 V, I_o = 0 A to 1.0 A	25 mV (0.5%)
Output Ripple	V_{in} = 10 V, I_o = 1.0 A	50 mVpp P.A.R.D.
Output Ripple	V_{in} = 20 V, I_o = 1.0 A	100 mVpp P.A.R.D.
Efficiency	V_{in} = 15 V, I_o = 1.0 A	82%

APPLICATIONS INFORMATION

The TL431 is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non−standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 15. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition. Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation.

A simplified model of the TL431 is shown in Figure 31. When tested for stability boundaries, the load resistance is 150 Ω. The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, Gm, develops a current whose amplitude is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of Gm flows through compensation capacitance, C_{P2}. The voltage across C_{P2} drives the output dependent current source, Go, which is connected across the device cathode and anode.

Model component values are:
$V_{ref} = 1.78$ V
$Gm = 0.3 + 2.7 \exp(-I_C/26\ mA)$
where I_C is the device cathode current and Gm is in mhos

$Go = 1.25\ (V_{cp}2)$ μmhos.

Resistor and capacitor typical values are shown on the model. Process tolerances are ±20% for resistors, ±10% for capacitors, and ±40% for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

$$P1 = \frac{1}{2\pi R_{GM} C_{P1}} = \frac{1}{2\pi * 1.0\ M * 20\ pF} = 7.96\ kHz$$

$$P2 = \frac{1}{2\pi R_{P2} C_{P2}} = \frac{1}{2\pi * 10\ M * 0.265\ pF} = 60\ kHz$$

$$Z1 = \frac{1}{2\pi R_{Z1} C_{P1}} = \frac{1}{2\pi * 15.9\ k * 20\ pF} = 500\ kHz$$

In addition, there is an external circuit pole defined by the load:

$$P_L = \frac{1}{2\pi R_L C_L}$$

Also, the transfer dc voltage gain of the TL431 is:

$$G = G_M R_{GM} Go R_L$$

Example 1:

$I_C = 10\ mA, R_L = 230\ \Omega, C_L = 0$. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} Go R_L = (2.138)(1.0\ M)(1.25\ \mu)(230) = 615 = 56\ dB$$

$$\text{Loop gain} = G \frac{8.25\ k}{8.25\ k + 15\ k} = 218 = 47\ dB$$

The resulting transfer function Bode plot is shown in Figure 32. The asymptotic plot may be expressed as the following equation:

$$Av = 615 \frac{\left(1 + \frac{jf}{500\ kHz}\right)}{\left(1 + \frac{jf}{8.0\ kHz}\right)\left(1 + \frac{jf}{60\ kHz}\right)}$$

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz. The phase margin, calculated from the equation, would be 55.9 degrees. This model matches the Open−Loop Bode Plot of Figure 12. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44 degrees.

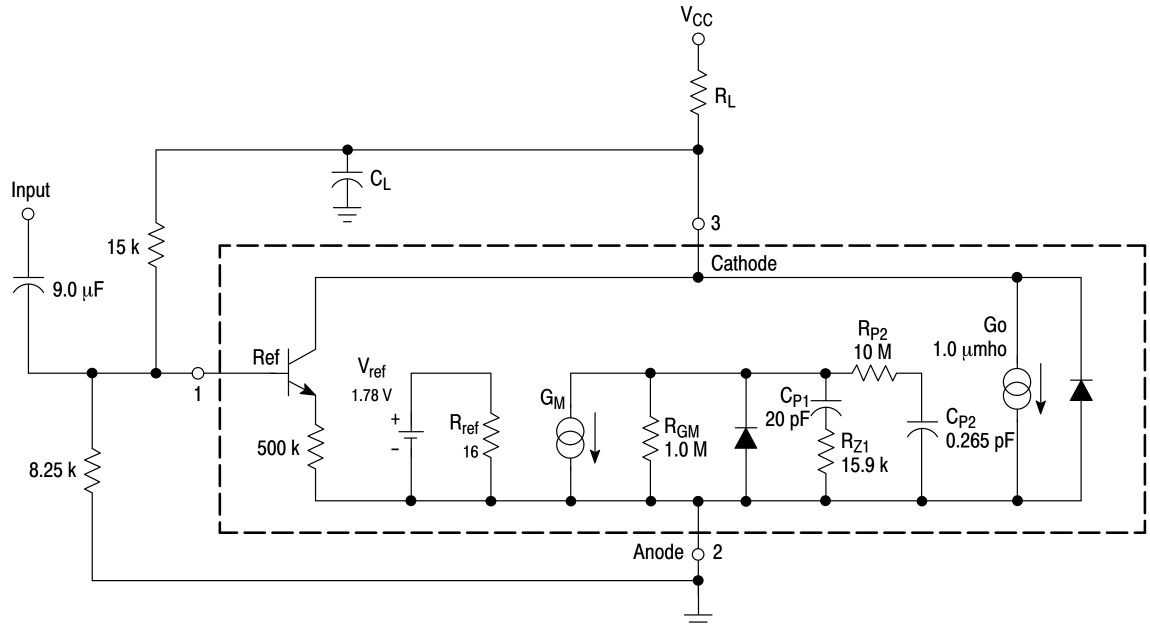


Figure 31. Simplified TL431 Device Model

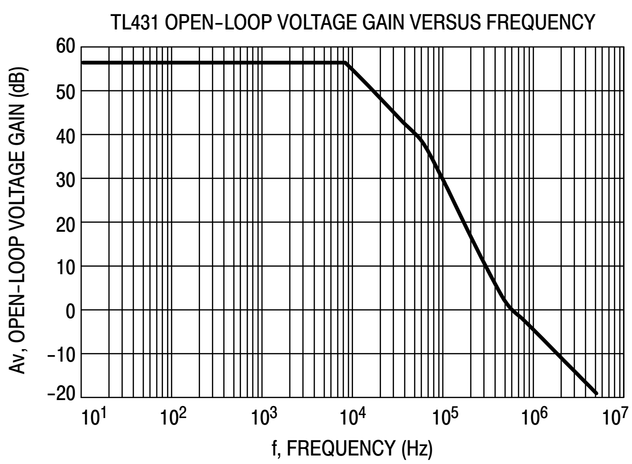


Figure 32. Example 1 Circuit Open Loop Gain Plot

Example 2.

I_C = 7.5 mA, R_L = 2.2 kΩ, C_L = 0.01 μF. Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 15) shows that this value of load capacitance and cathode current is on the boundary. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} Go R_L =$$

$$(2.323)(1.0\ M)(1.25\ \mu)(2200) = 6389 = 76\ dB$$

The resulting open loop Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

$$Av = 615 \frac{\left(1 + \frac{jf}{500\ kHz}\right)}{\left(1 + \frac{jf}{8.0\ kHz}\right)\left(1 + \frac{jf}{60\ kHz}\right)\left(1 + \frac{jf}{7.2\ kHz}\right)}$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.

Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about −46 degrees. Therefore, instability of this circuit is likely.

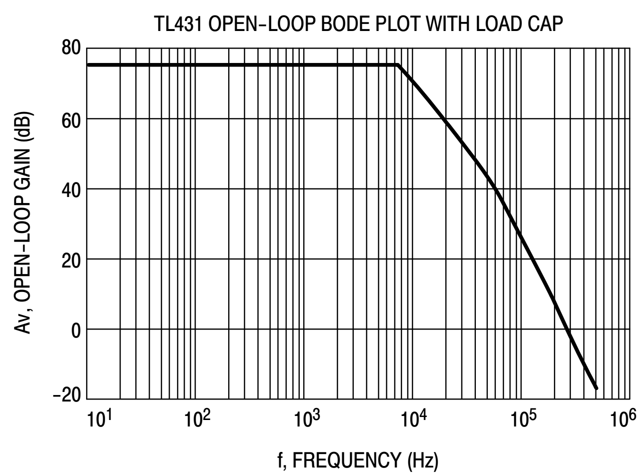


Figure 33. Example 2 Circuit Open Loop Gain Plot

With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

ORDERING INFORMATION

Device	Marking Code	Operating Temperature Range	Package Code	Shipping Information†	Tolerance
TL431ACDG	AC	0°C to 70°C	SOIC−8 (Pb−Free)	98 Units / Rail	1.0%
TL431BCDG	BC				0.4%
TL431CDG	C				2.2%
TL431ACDR2G	AC			2500 / Tape & Reel	1.0%
TL431BCDR2G	BC				0.4%
TL431CDR2G	C				2.2%
TL431ACDMR2G	TAC		Micro8 (Pb−Free)	4000 / Tape & Reel	1.0%
TL431BCDMR2G	TBC				0.4%
TL431CDMR2G	T−C				2.2%
TL431ACPG	ACP		PDIP−8 (Pb−Free)	50 Units / Rail	1.0%
TL431BCPG	BCP				0.4%
TL431CPG	CP				2.2%
TL431ACLPG	ACLP		TO−92 (Pb−Free)	2000 Units / Bag	1.0%
TL431BCLPG	BCLP				0.4%
TL431CLPG	CLP				2.2%
TL431ACLPRAG	ACLP			2000 / Tape & Reel	1.0%
TL431BCLPRAG	BCLP				0.4%
TL431CLPRAG	CLP				2.2%
TL431ACLPREG	ACLP				1.0%
TL431BCLPREG	BCLP				0.4%
TL431CLPREG	CLP				2.2%
TL431ACLPRPG	ACLP			2000 / Tape & Ammo Box	1.0%
TL431BCLPRMG	BCLP			2000 / Fan−Fold	0.4%
TL431CLPRMG	CLP				2.2%
TL431CLPRPG	CLP				
TL431AIDG	AI	−40°C to 85°C	SOIC−8 (Pb−Free)	98 Units / Rail	1.0%
TL431BIDG	BI				0.4%
TL431IDG	I				2.2%
TL431AIDR2G	AI			2500s / Tape & Reel	1.0%
TL431BIDR2G	BI				0.4%
TL431IDR2G	I				2.2%
TL431AIDMR2G	TAI		Micro8 (Pb−Free)	4000 / Tape & Reel	1.0%
TL431BIDMR2G	TBI				0.4%
TL431IDMR2G	T−I				2.2%
TL431AIPG	AIP		PDIP−8 (Pb−Free)	50 Units / Rail	1.0%
TL431BIPG	BIP				0.4%
TL431IPG	IP				2.2%
TL431AILPG	AILP		TO−92 (Pb−Free)	2000 Units / Bag	1.0%
TL431BILPG	BILP				0.4%
TL431ILPG	ILP				2.2%
TL431AILPRAG	AILP			2000 / Tape & Reel	1.0%
TL431BILPRAG	BILP				0.4%
SC431ILPRAG	ILP				2.2%
TL431ILPRAG	ILP				
TL431AILPRMG	AILP			2000 / Tape & Ammo Box	1.0%
TL431AILPRPG					
TL431ILPRPG	ILP				2.2%

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV/SCV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ORDERING INFORMATION

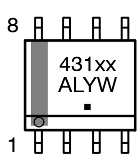
Device	Marking Code	Operating Temperature Range	Package Code	Shipping Information†	Tolerance
TL431BVDG	BV	−40°C to 125°C	SOIC−8 (Pb−Free)	98 Units / Rail	0.4%
TL431BVDR2G				2500 / Tape & Reel	
TL431BVDMR2G	TBV		Micro8 (Pb−Free)	4000 / Tape & Reel	
TL431BVLPG	BVLP		TO−92 (Pb−Free)	2000 Units / Bag	
TL431BVLPRAG				2000 / Tape & Reel	
TL431BVPG	BVP		PDIP−8 (Pb−Free)	50 Units / Rail	0.4%
NCV431AIDMR2G*	RAN		Micro8 (Pb−Free)	4000 / Tape & Reel	1%
SCV431AIDMR2G*	RAP				
NCV431AIDR2G*	AV		SOIC−8 (Pb−Free)	2500 / Tape & Reel	
NCV431BVDMR2G*	NVB		Micro8 (Pb−Free)	4000 / Tape & Reel	0.4%
NCV431BVDR2G*	BV		SOIC−8 (Pb−Free)	2500 / Tape & Reel	

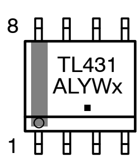
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV/SCV Prefixes for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MARKING DIAGRAMS

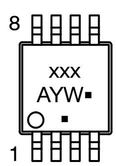
SOIC−8
D SUFFIX
CASE 751



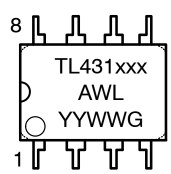


(Exception for the TL431CD and TL431ID only)

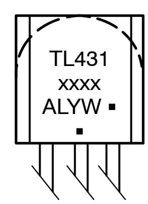
Micro8
CASE 846A



PDIP−8
CASE 626



TO−92 (TO−226)
CASE 29

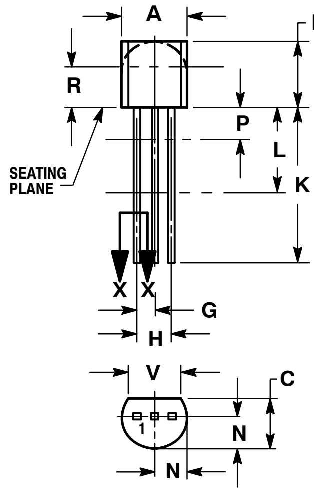


xxxx	= See Specific Marking Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
▪ or G	= Pb−Free Package

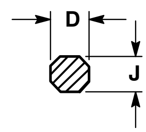
(Note: Microdot may be in either location)

PACKAGE DIMENSIONS

TO−92 (TO−226)
CASE 29−11
ISSUE AN



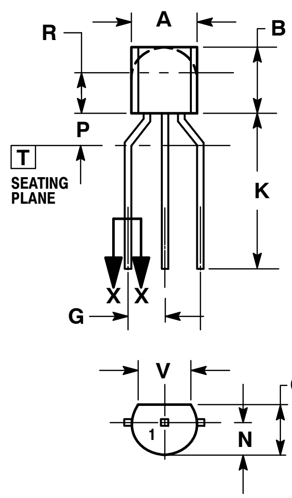
STRAIGHT LEAD
BULK PACK



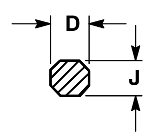
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD
TAPE & REEL
AMMO PACK



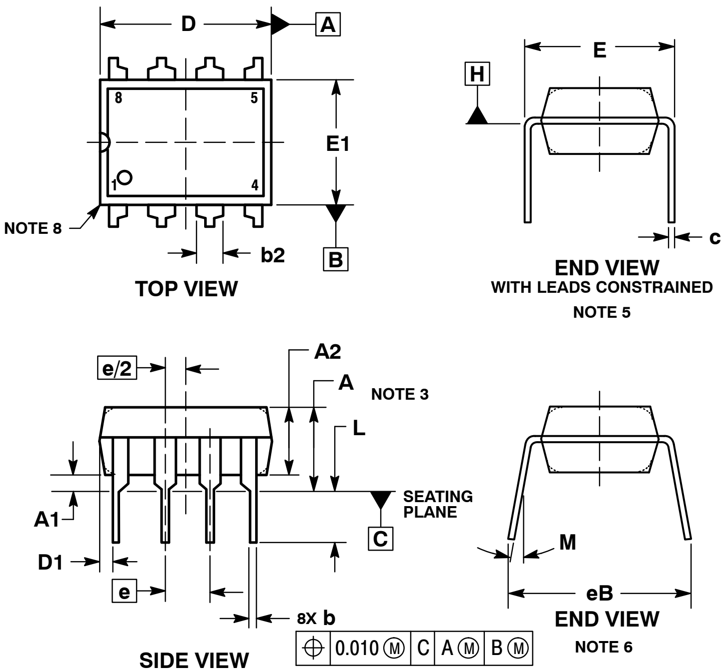
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

PACKAGE DIMENSIONS

PDIP−8
CASE 626−05
ISSUE P

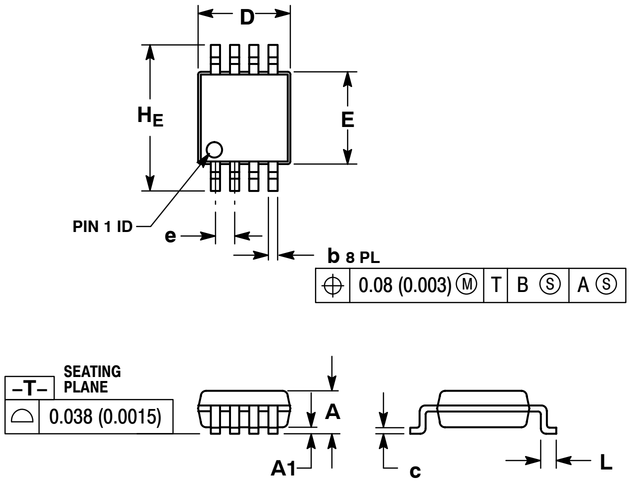


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

PACKAGE DIMENSIONS

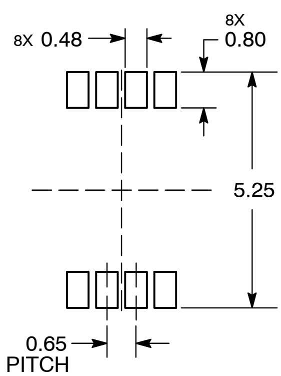
Micro8™
CASE 846A−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

RECOMMENDED SOLDERING FOOTPRINT*

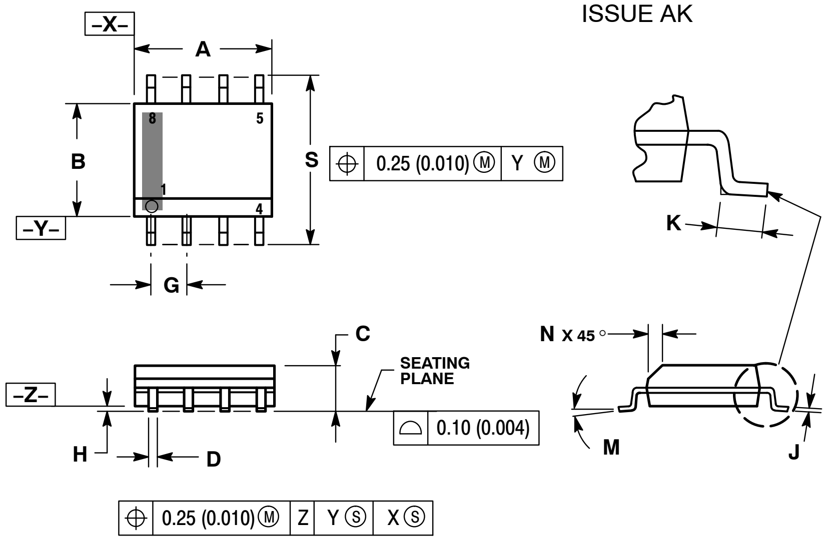


DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

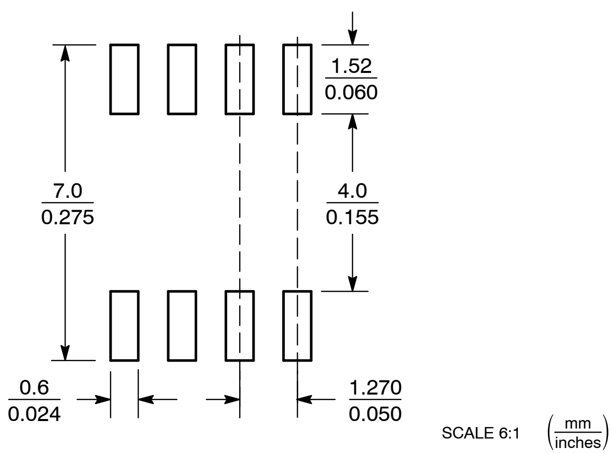
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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