STB15N65M5, STD15N65M5

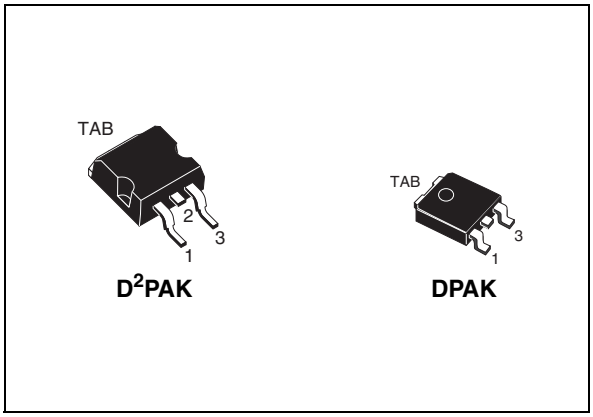
N-channel 650 V, 0.308 Ω typ., 11 A MDmesh™ V Power MOSFET in D²PAK and DPAK packages

Datasheet — production data

Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STB15N65M5	710 V	< 0.34 Ω	11 A
STD15N65M5			

- Worldwide best $R_{DS(on)}$ * area
- Higher V_{DSS} rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested



Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

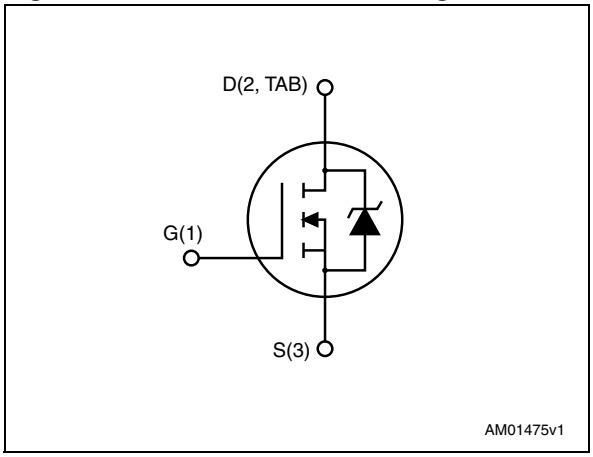


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB15N65M5	15N65M5	D²PAK	Tape and reel
STD15N65M5		DPAK	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	11	A
I_D	Drain current (continuous) at T_C = 100 °C	6.9	A
I_{DM} (1)	Drain current (pulsed)	44	A
P_{TOT}	Total dissipation at T_C = 25 °C	85	W
dv/dt (1)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. $I_{SD} \leq 11$ A, di/dt ≤400 A/µs; V_{DD} = 400 V, $V_{DS(peak)} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D^2PAK	DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.47		°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	30	50	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D= I_{AR}; V_{DD}=50 V)	160	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V V_{DS} = 650 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5.5 A		0.308	0.34	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	816 23 2.6	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0	-	70	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	21	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 5.5 A, V_{GS} = 10 V (see *Figure 18*)	-	22 5.5 11	-	nC nC nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	V_{DD} = 400 V, I_D = 7 A,	-	30	-	ns
$t_{r\ (V)}$	Voltage rise time	R_G = 4.7 Ω, V_{GS} = 10 V		8		ns
$t_{f\ (i)}$	Current fall time	(see *Figure 19* and		11		ns
$t_{c(off)}$	Crossing time	*Figure 22*)		12.5		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
I_{SDM} (1)	Source-drain current (pulsed)				44	A
V_{SD} (2)	Forward on voltage	I_{SD} = 11 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs	-	247		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V (see *Figure 22*)		2.4		µC
I_{RRM}	Reverse recovery current			19.5		A
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs	-	312		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_j = 150 °C		3		µC
I_{RRM}	Reverse recovery current	(see *Figure 22*)		19		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK

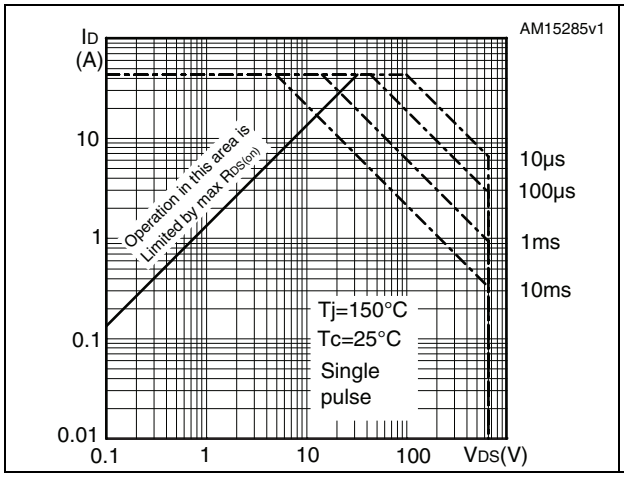


Figure 3. Thermal impedance for D²PAK

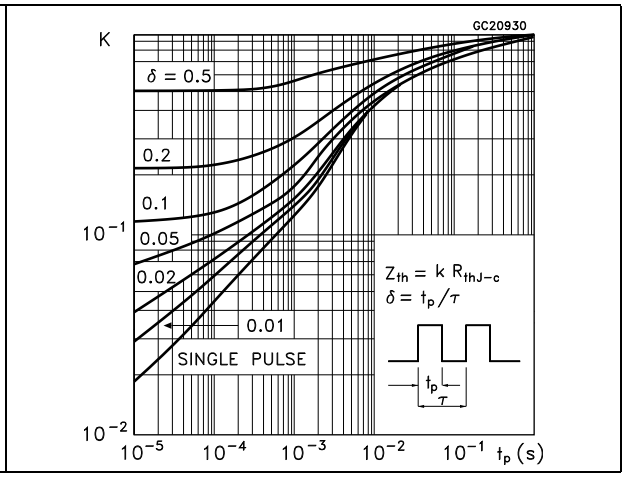


Figure 4. Safe operating area for DPAK

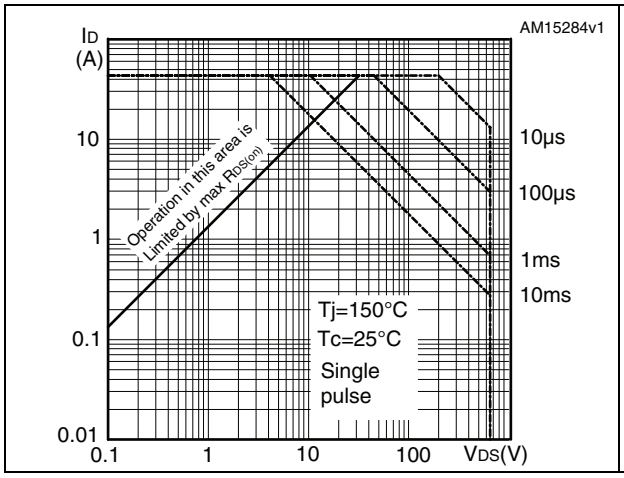


Figure 5. Thermal impedance for DPAK

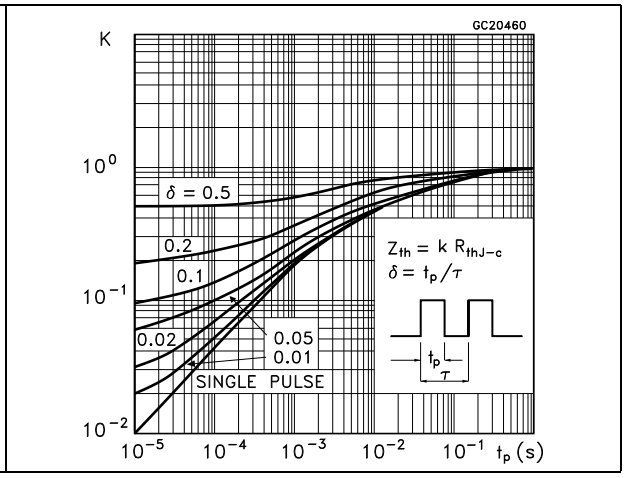


Figure 6. Output characteristics

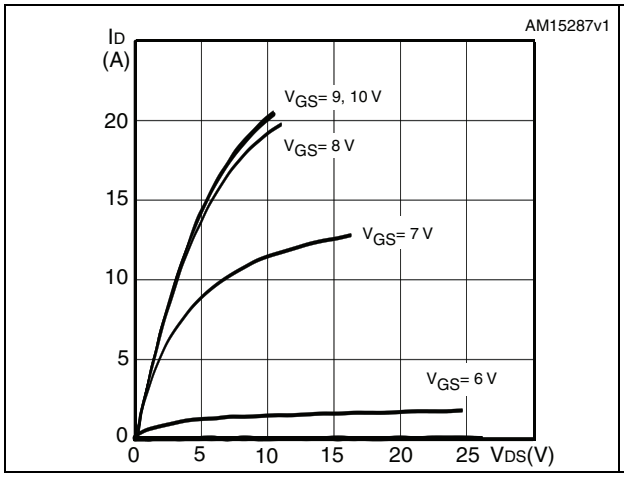


Figure 7. Transfer characteristics

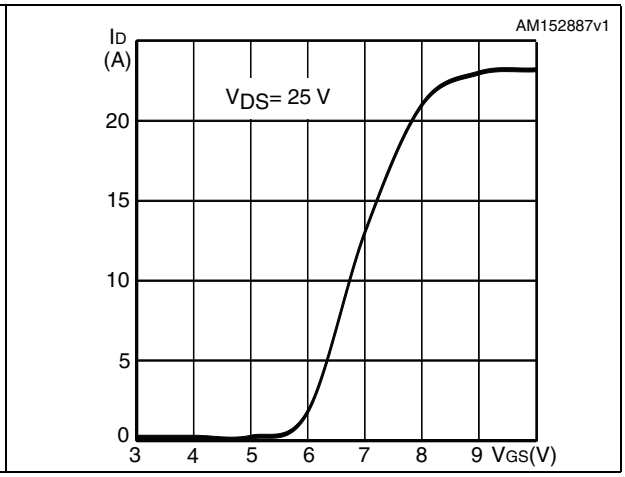


Figure 8. Gate charge vs gate-source voltage

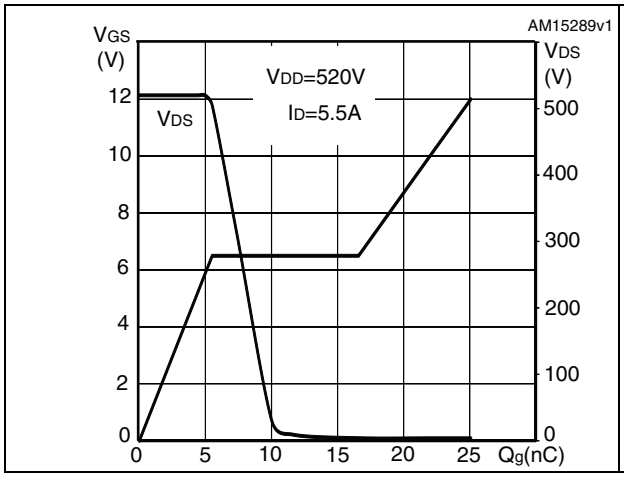


Figure 9. Static drain-source on-resistance

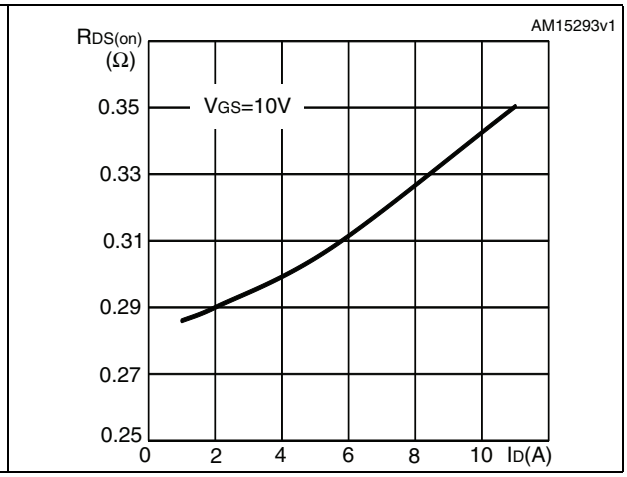


Figure 10. Capacitance variations

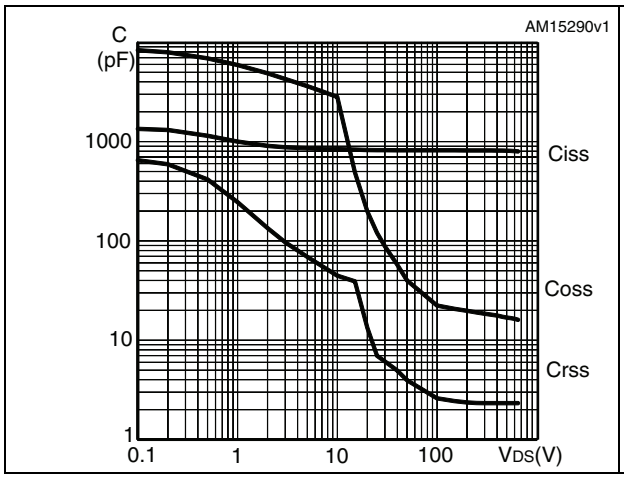


Figure 11. Output capacitance stored energy

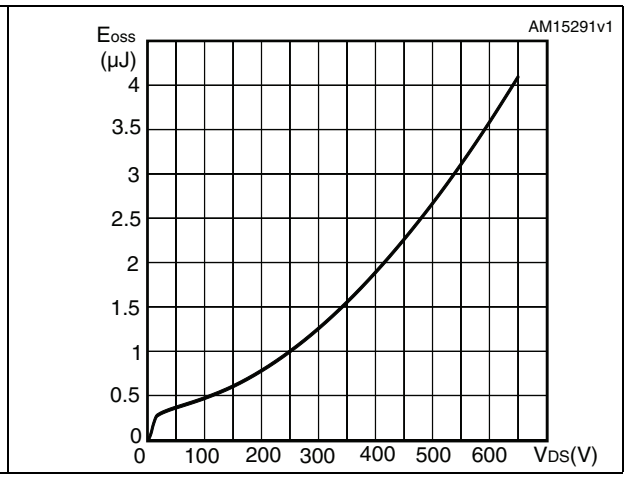


Figure 12. Normalized gate threshold voltage vs temperature

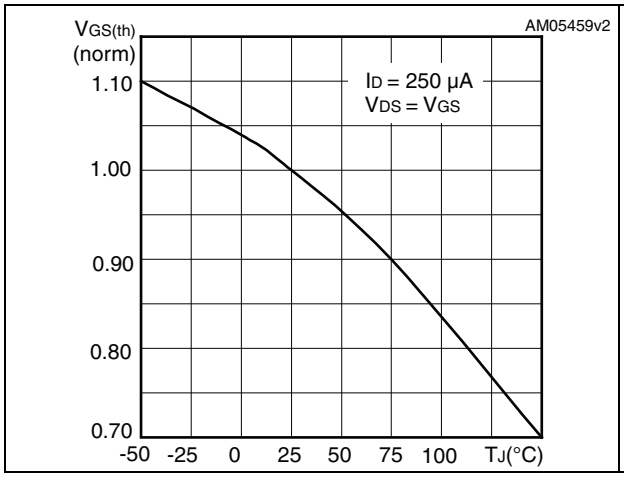


Figure 13. Normalized on-resistance vs temperature

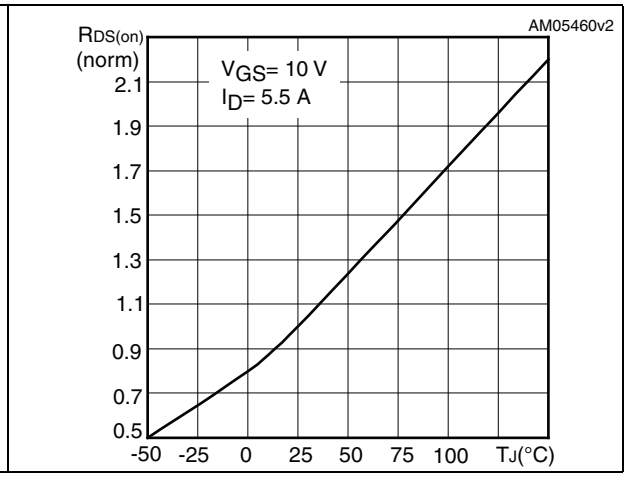


Figure 14. Source-drain diode forward characteristics

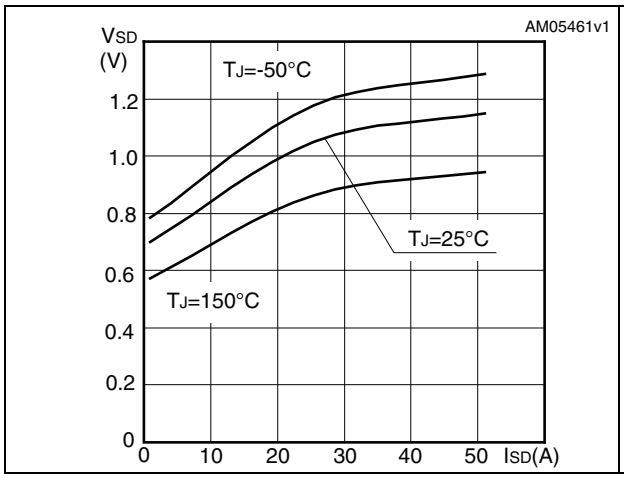


Figure 15. Normalized B_{VDSS} vs temperature

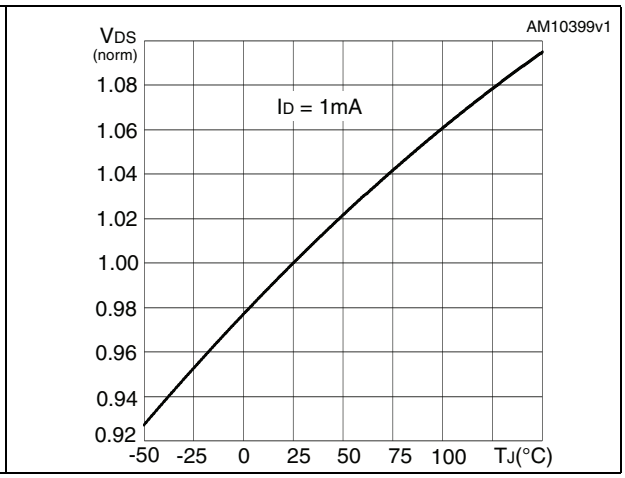
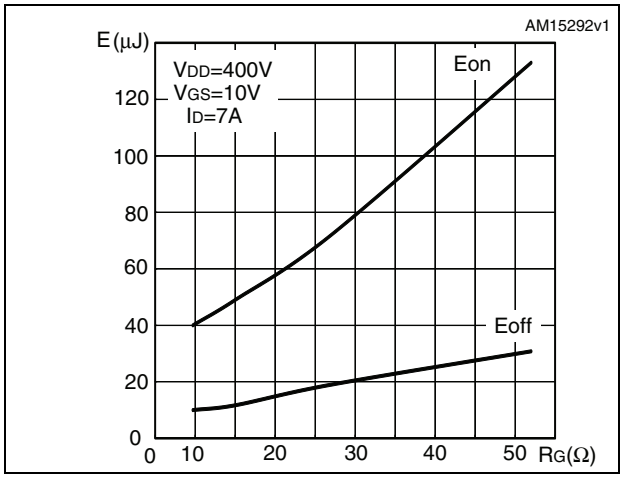


Figure 16. Switching losses vs gate resistance (1)



1. Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 17. Switching times test circuit for resistive load

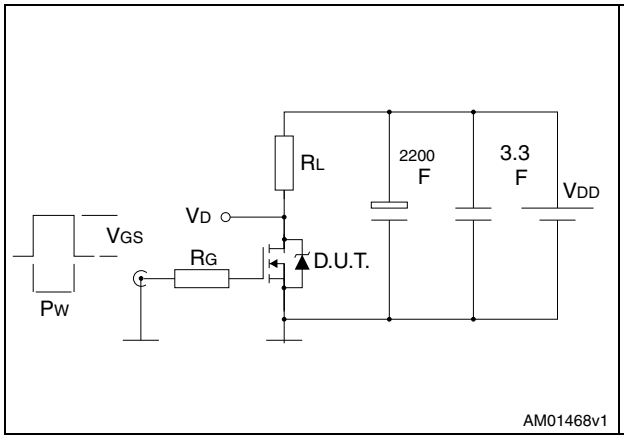


Figure 18. Gate charge test circuit

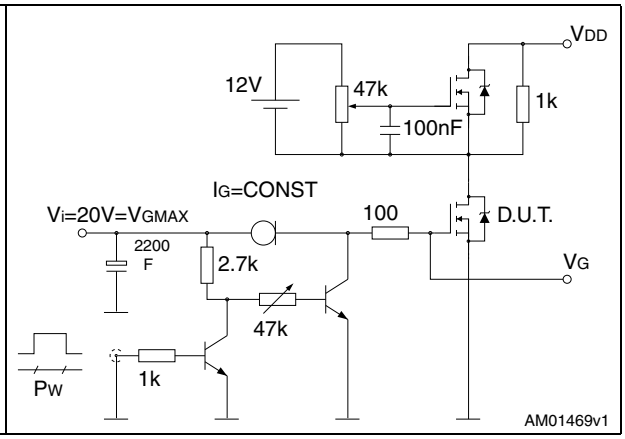


Figure 19. Test circuit for inductive load switching and diode recovery times

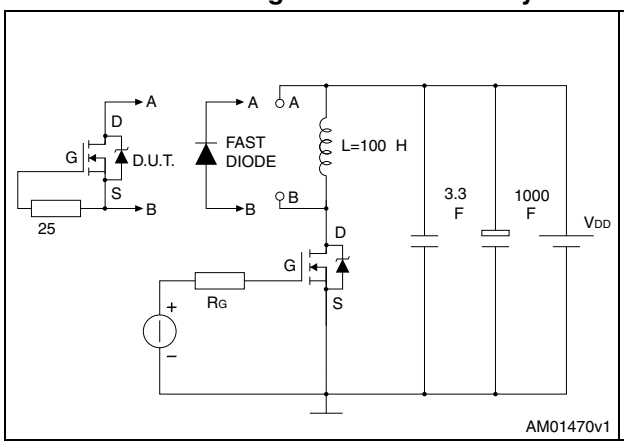


Figure 20. Unclamped inductive load test circuit

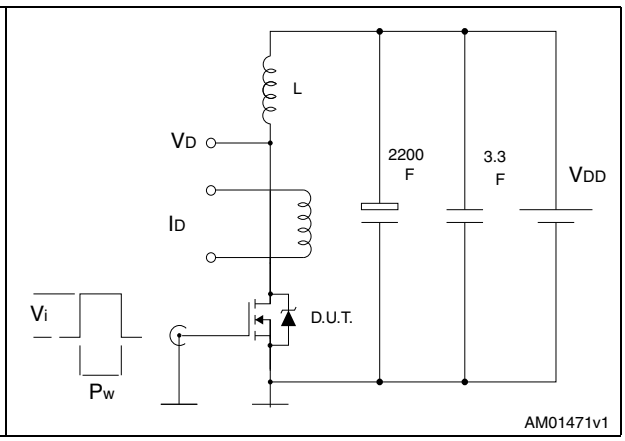


Figure 21. Unclamped inductive waveform

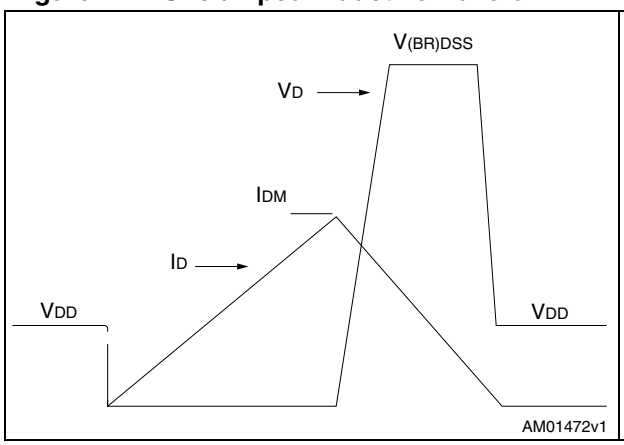
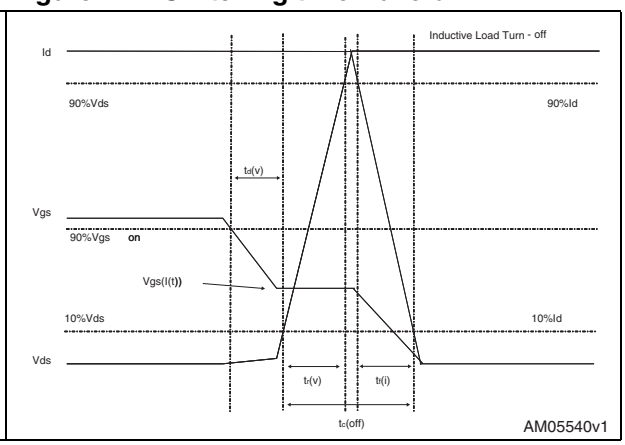


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D²PAK (TO-263) drawing

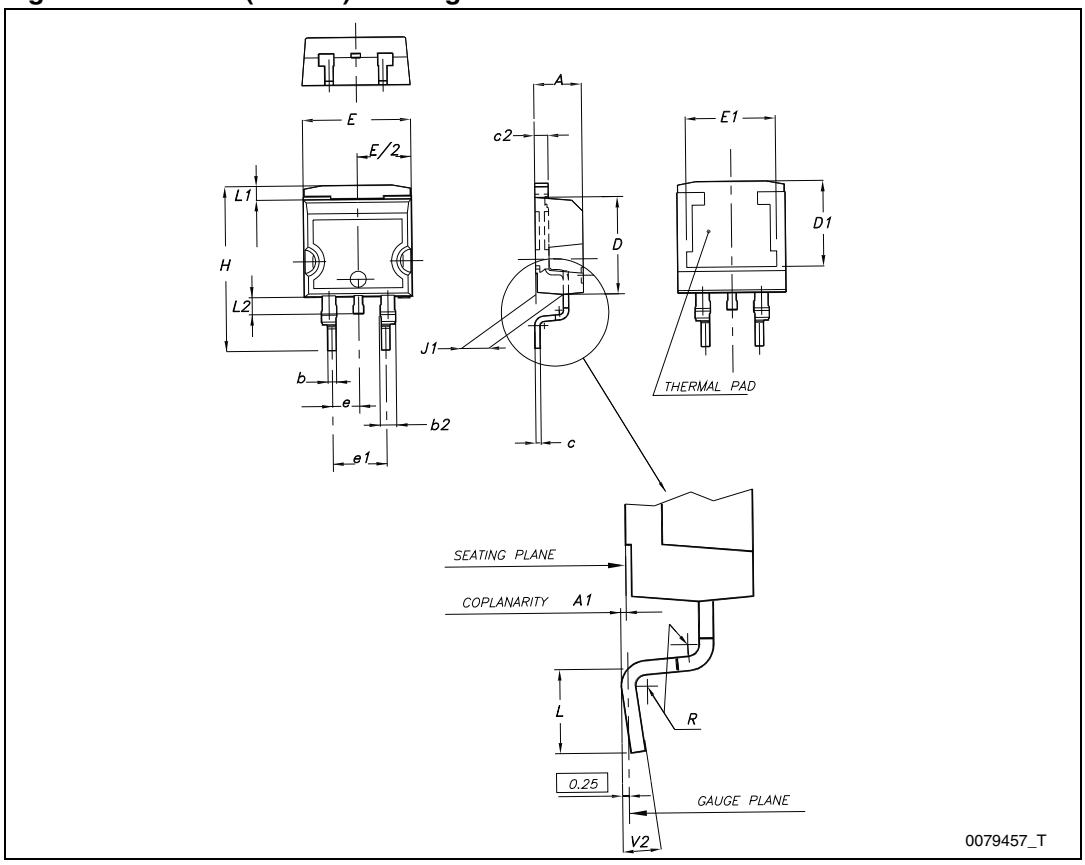
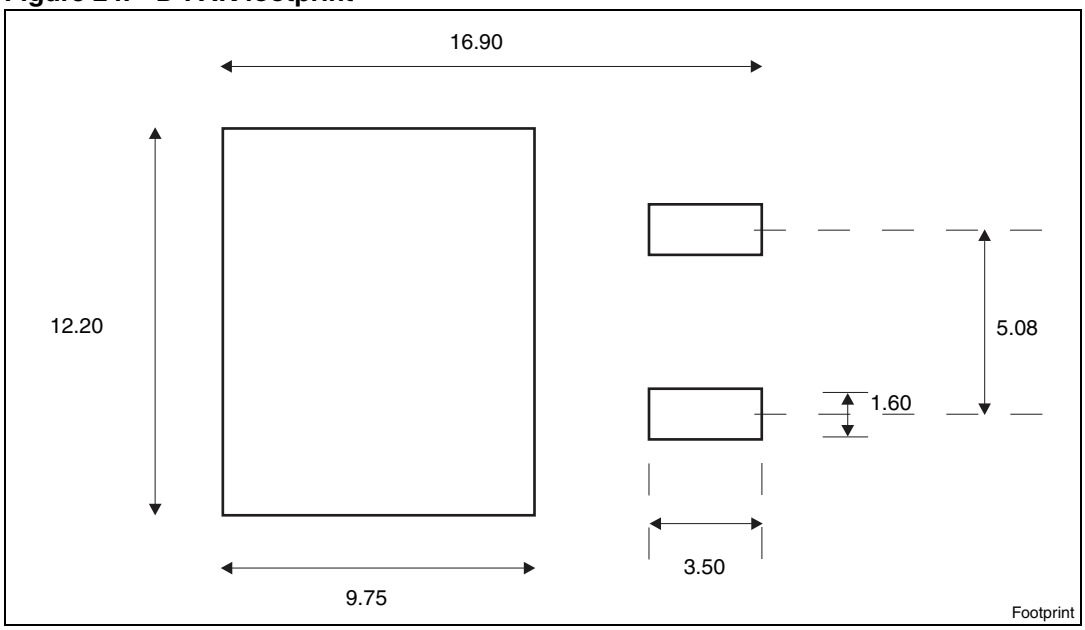


Figure 24. D²PAK footprint[a]



a. All dimensions are in millimeters

Table 10. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) drawing

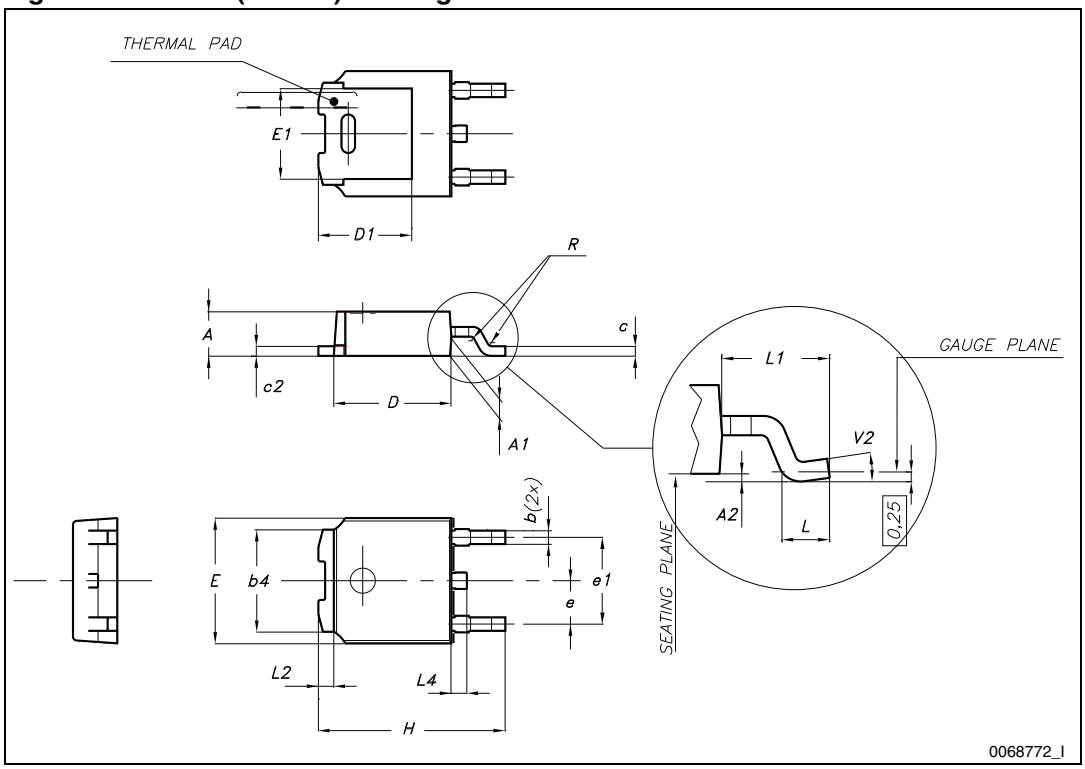
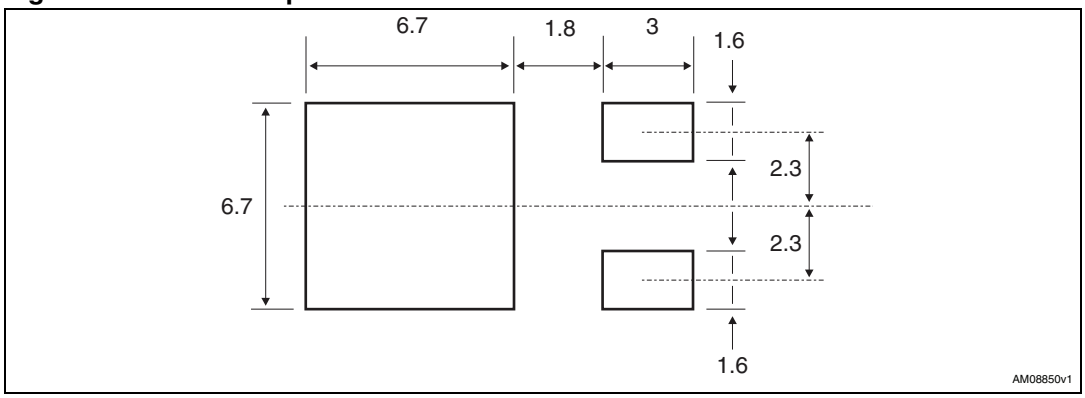


Figure 26. DPAK footprint[b]



b. All dimensions are in millimeters

5 Packaging mechanical data

Table 11. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 27. Tape for D²PAK (TO-263) and DPAK (TO-252)

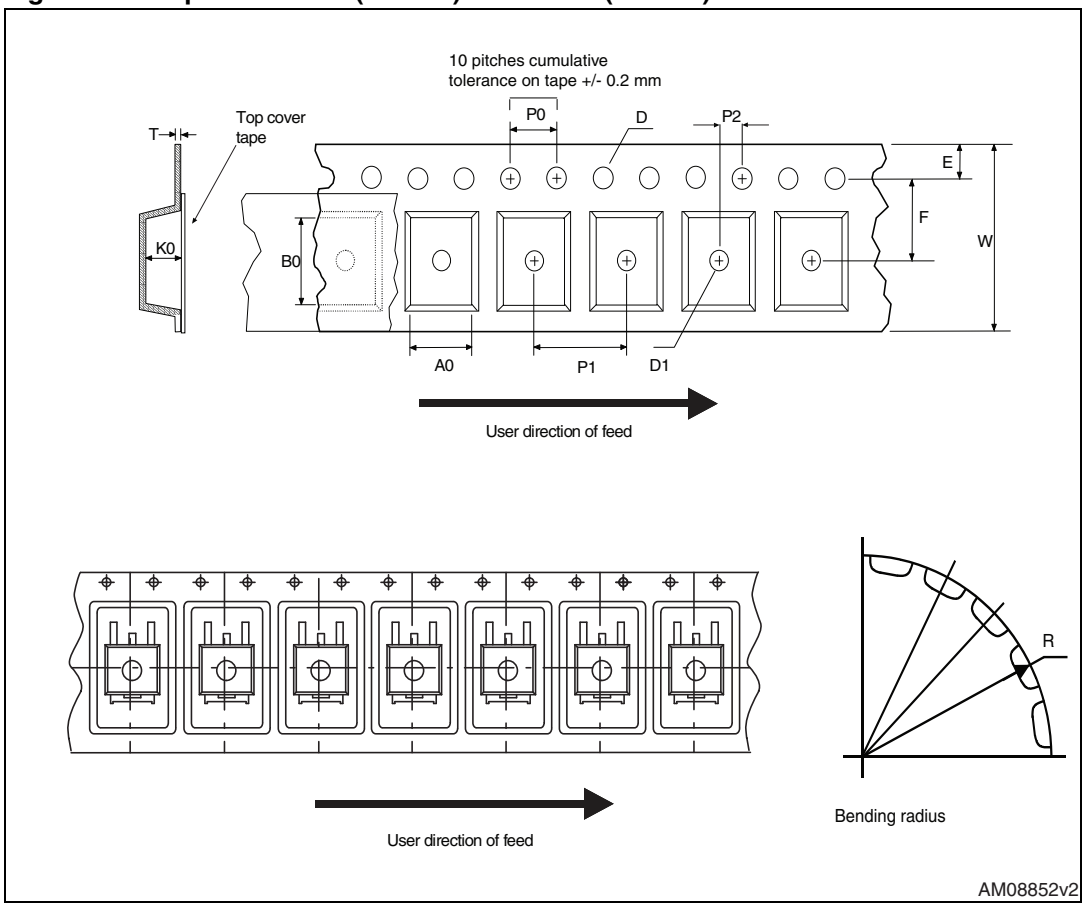
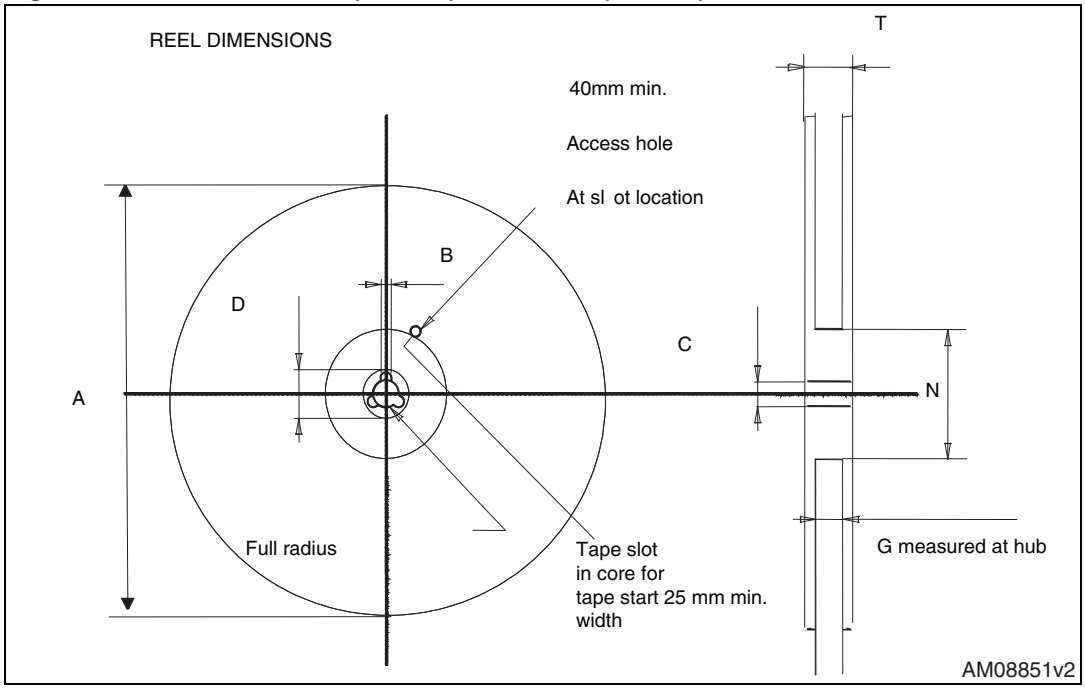


Figure 28. Reel for D²PAK (TO-263) and DPAK (TO-252)



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
09-Nov-2012	1	First release.

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