

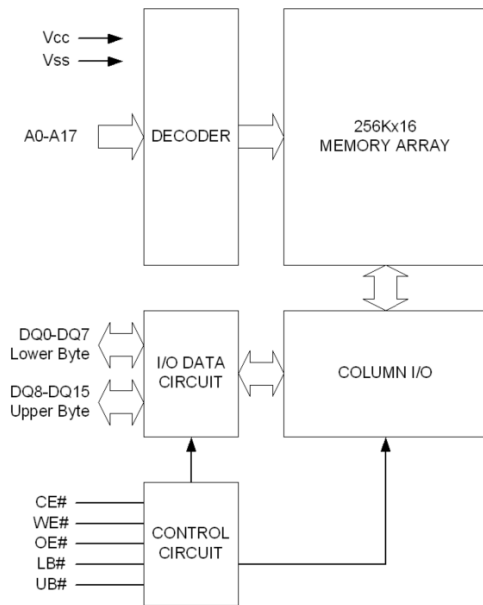
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**Revision History**  
**256K X 16 BIT LOW POWER CMOS SRAM**

Revision	Details	Date
Rev 1.0	Initial Release	Feb 2023



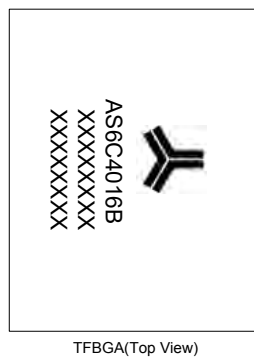
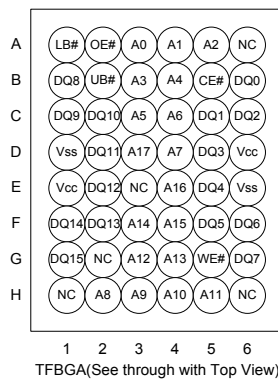
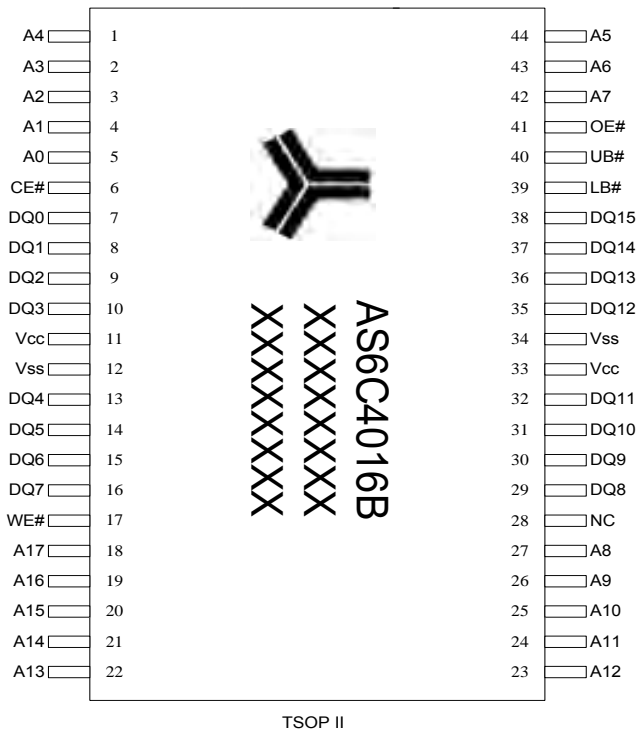
## FUNCTIONAL BLOCK DIAGRAM



## PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V <sub>CC</sub> relative to V <sub>SS</sub>	V <sub>T1</sub>	-0.5 to 4.6	V
Voltage on any other pin relative to V <sub>SS</sub>	V <sub>T2</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Operating Temperature	T <sub>A</sub>	-40 to 85	°C
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

## TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	High – Z	High – Z	I <sub>SB1</sub>
	X	X	X	H	H	High – Z	High – Z	
Output Disable	L	H	H	L	X	High – Z	High – Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	H	H	X	L	High – Z	High – Z	
Read	L	L	H	L	H	D <sub>OUT</sub>	High – Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	L	H	H	L	High – Z	D <sub>OUT</sub>	
	L	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	
Write	L	X	L	L	H	D <sub>IN</sub>	High – Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	X	L	H	L	High – Z	D <sub>IN</sub>	
	L	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>4</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		2.7	3.0	3.6	V	
Input High Voltage	V <sub>IH</sub> <sup>1</sup>		2.2	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub> <sup>2</sup>		- 0.2	-	0.6	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	- 1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	- 1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.2	2.7	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# ≤ 0.2V, I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> -0.2V	-	12	20	mA	
	I <sub>CC1</sub>	Cycle time = 1μs CE# = 0.2V, I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> - 0.2V	-	2	4	mA	
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> - 0.2V Others at 0.2V or V <sub>CC</sub> - 0.2V	40°C	-	2	4.5	μA <sup>5</sup>
				-	1.8	12	μA

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C
- This parameter is measured at V<sub>CC</sub> = 3.0V

## CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

## AC TEST CONDITIONS

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -1mA/2mA

## AC ELECTRICAL CHARACTERISTICS

### (1) READ CYCLE

PARAMETER	SYM.	AS6C4016B-45		UNIT
		MIN.	MAX.	
Read Cycle Time	$t_{RC}$	45	-	ns
Address Access Time	$t_{AA}$	-	45	ns
Chip Enable Access Time	$t_{ACE}$	-	45	ns
Output Enable Access Time	$t_{OE}$	-	25	ns
Chip Enable to Output in Low-Z	$t_{CLZ}^*$	10	-	ns
Output Enable to Output in Low-Z	$t_{OLZ}^*$	5	-	ns
Chip Disable to Output in High-Z	$t_{CHZ}^*$	-	15	ns
Output Disable to Output in High-Z	$t_{OHZ}^*$	-	15	ns
Output Hold from Address Change	$t_{OH}$	10	-	ns
LB#, UB# Access Time	$t_{BA}$	-	45	ns
LB#, UB# to High-Z Output	$t_{BHZ}^*$	-	20	ns
LB#, UB# to Low-Z Output	$t_{BLZ}^*$	10	-	ns

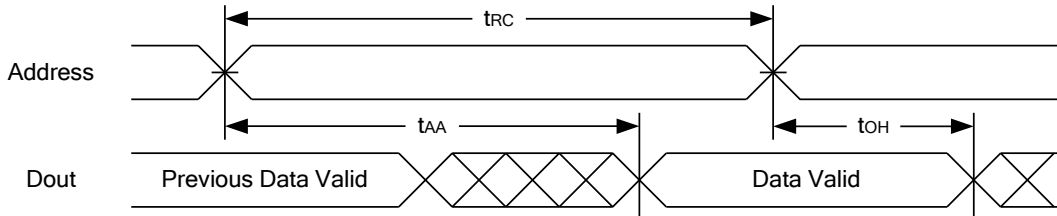
### (2) WRITE CYCLE

PARAMETER	SYM.	AS6C4016B-45		UNIT
		MIN.	MAX.	
Write Cycle Time	$t_{WC}$	45	-	ns
Address Valid to End of Write	$t_{AW}$	40	-	ns
Chip Enable to End of Write	$t_{CW}$	40	-	ns
Address Set-up Time	$t_{AS}$	0	-	ns
Write Pulse Width	$t_{WP}$	35	-	ns
Write Recovery Time	$t_{WR}$	0	-	ns
Data to Write Time Overlap	$t_{DW}$	20	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	ns
Output Active from End of Write	$t_{OW}^*$	5	-	ns
Write to Output in High-Z	$t_{WHZ}^*$	-	15	ns
LB#, UB# Valid to End of Write	$t_{BW}$	35	-	ns

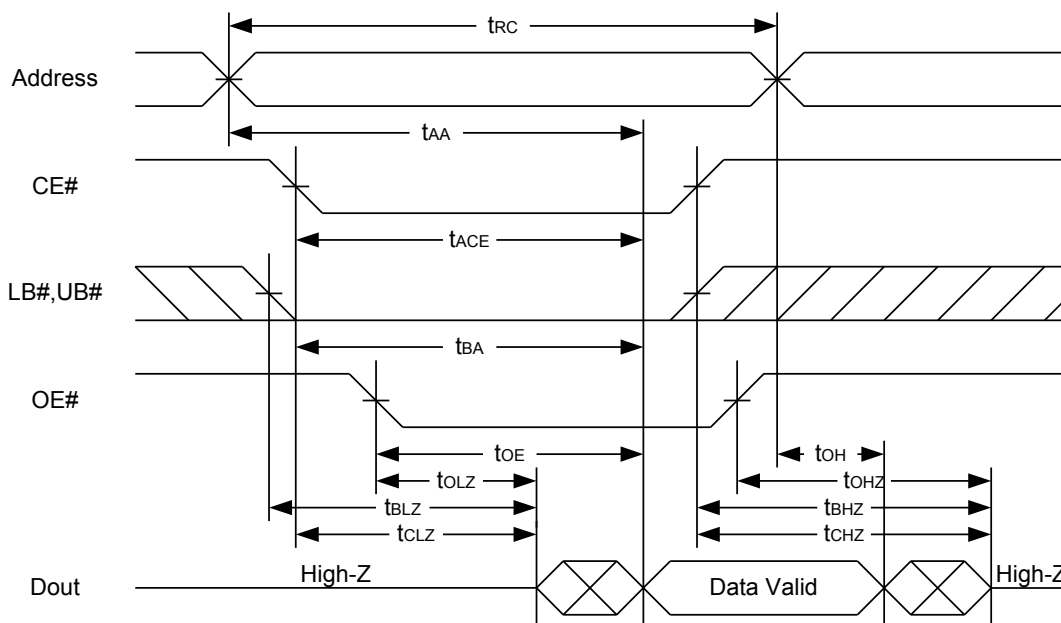
\*These parameters are guaranteed by device characterization, but not production tested.

## TIMING WAVEFORMS

### READ CYCLE 1 (Address Controlled) (1,2)



### READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

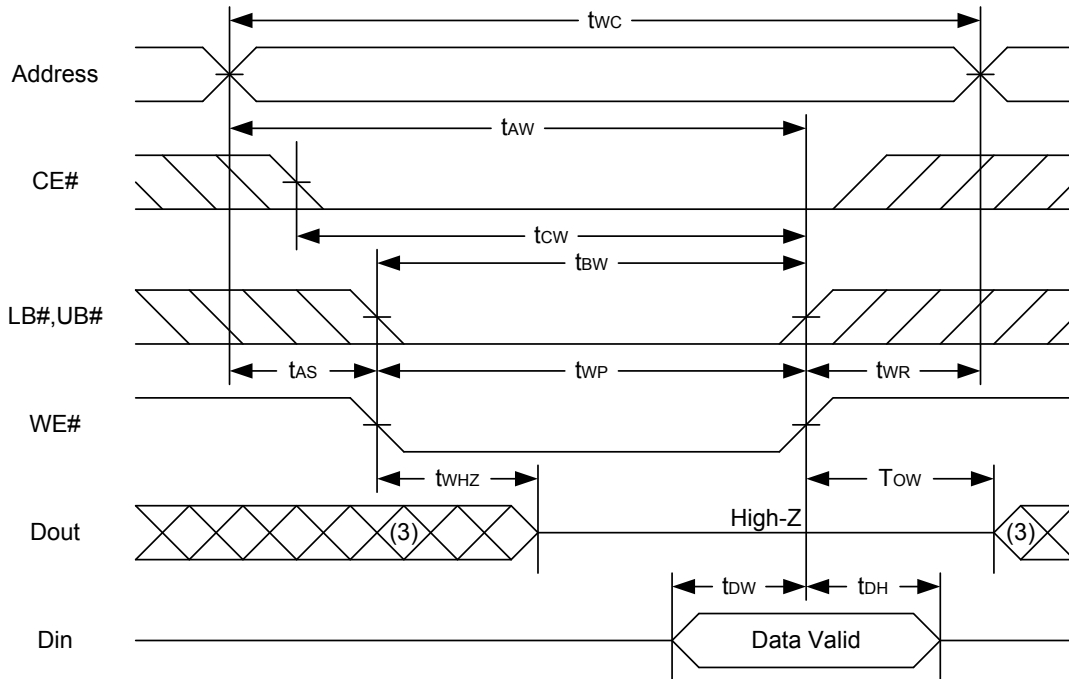


#### Notes :

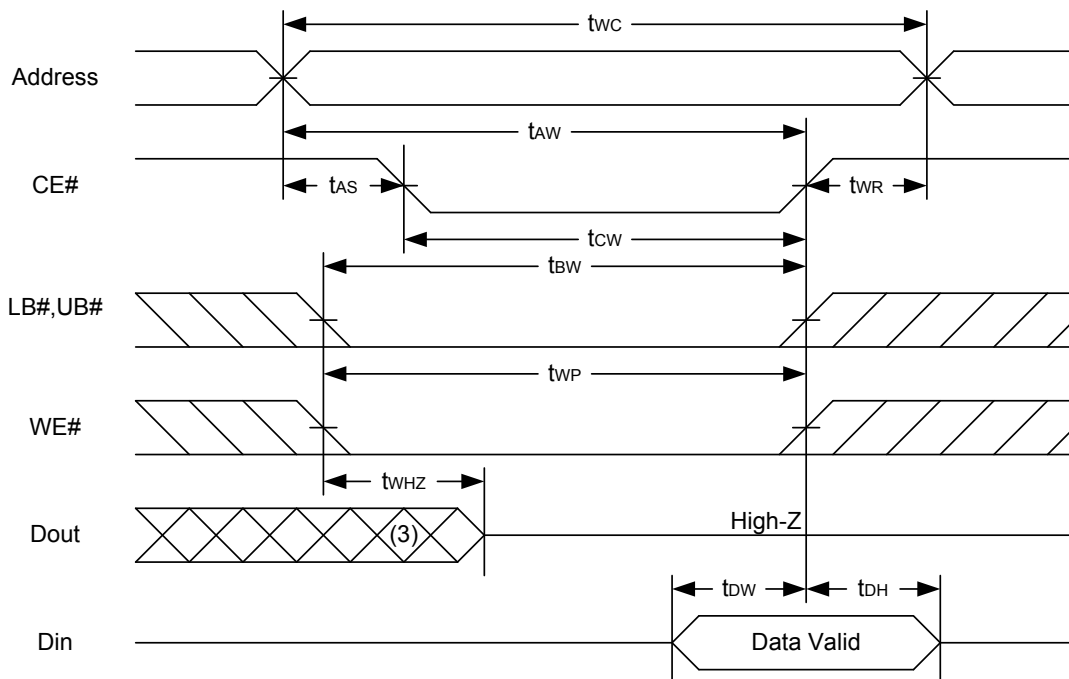
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5\text{pF}$ . Transition is measured  $\pm 500\text{mV}$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BHZ}$  is less than  $t_{BLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .



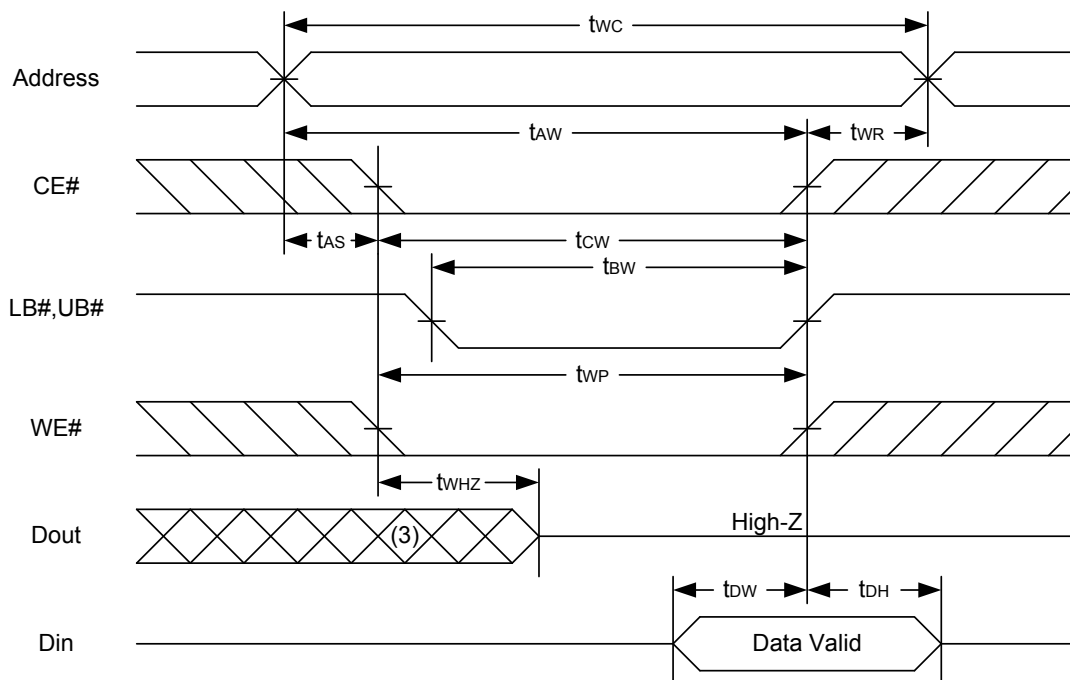
### WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



### WRITE CYCLE 2 (CE# Controlled) (1,4,5)



## WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



### Notes :

1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.  $t_{ow}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.

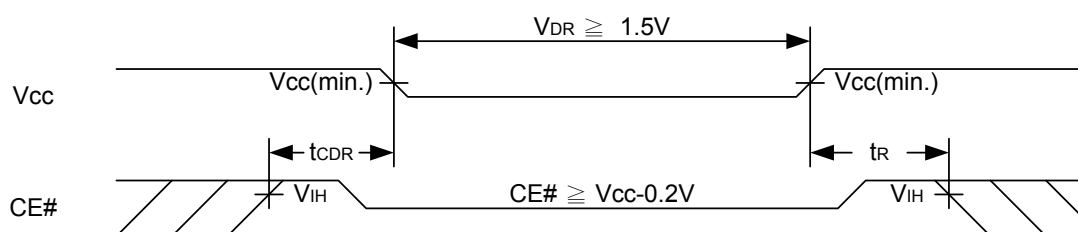
## DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V	1.5	-	3.6	V	
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 1.5V	40°C	-	2	4.5	μA
		CE# ≥ V <sub>CC</sub> - 0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V		-	1.8	12	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns	

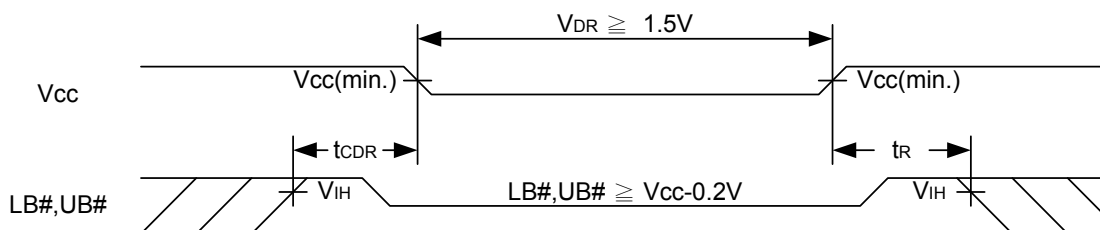
t<sub>RC</sub>\* = Read Cycle Time

## DATA RETENTION WAVEFORM

**Low V<sub>CC</sub> Data Retention Waveform (1)** (CE# controlled)

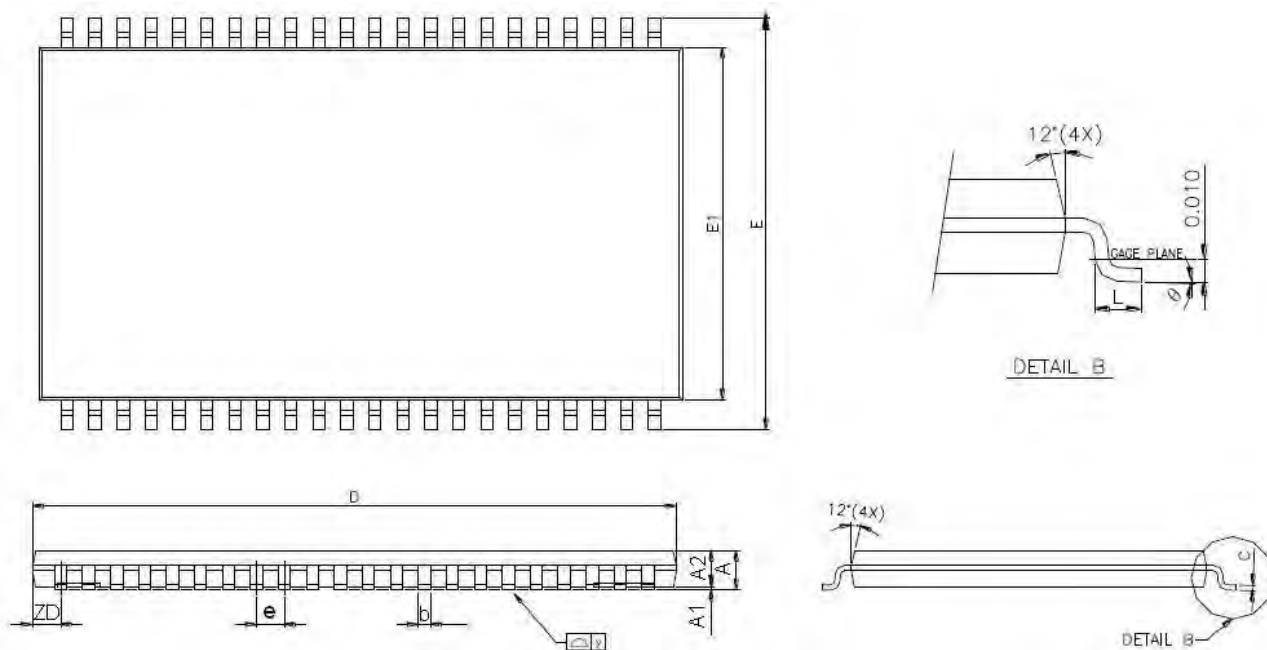


**Low V<sub>CC</sub> Data Retention Waveform (2)** (LB#, UB# controlled)



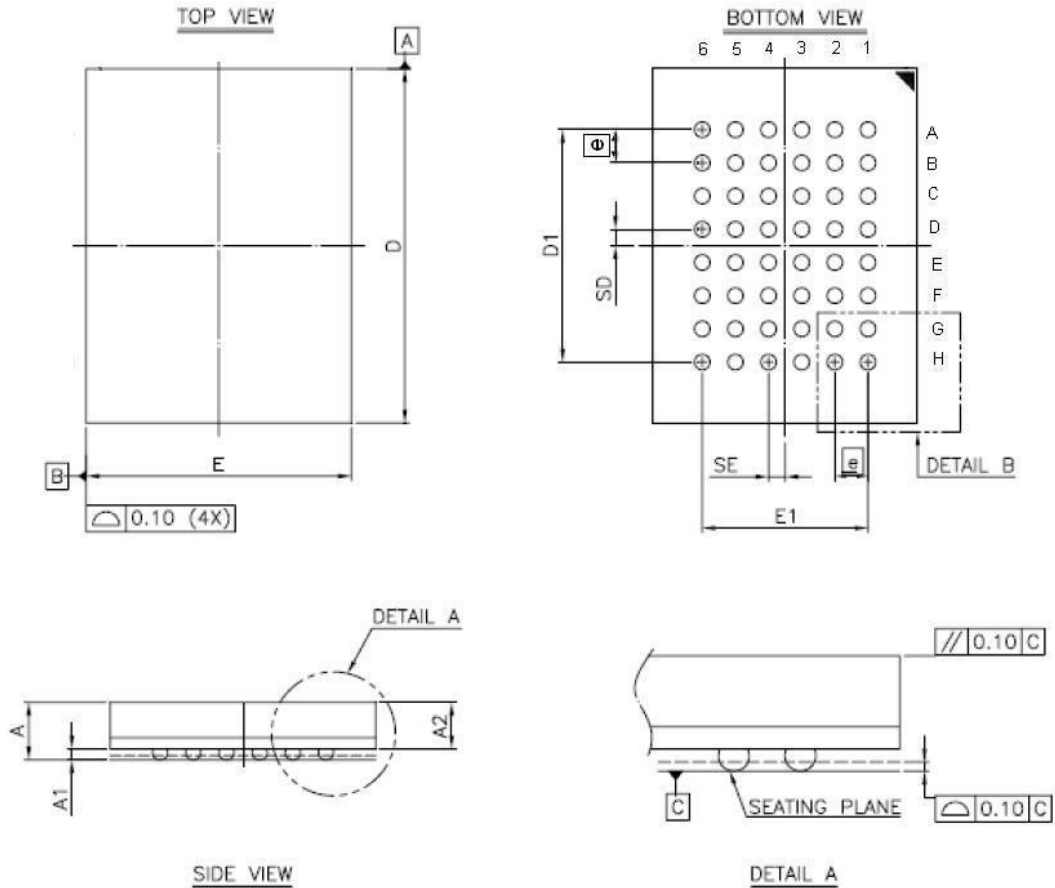
## PACKAGE OUTLINE DIMENSION

### 44-pin 400mil TSOP II Package Outline Dimension

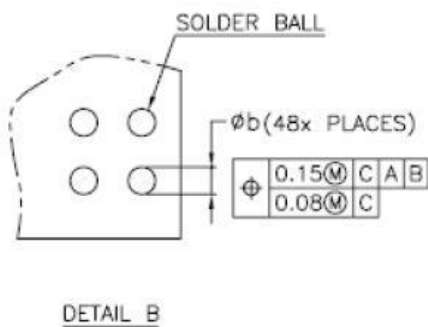


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

## 48-ball 6mm × 8mm TFBGA Package Outline Dimension



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.40	—	—	0.055
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	—	—	1.05	—	—	0.041
b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.25 BSC			0.207 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.75 BSC			0.148 BSC		
SE	0.375 TYP			0.015 TYP		
SD	0.375 TYP			0.015 TYP		
Ⓜ	0.75 BSC			0.030 BSC		



**NOTE:**

1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

## ORDERING INFORMATION

Alliance Part Number	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C4016B-45ZIN	256K x 16	2.7 ~ 3.6V	44-pin 400 mil TSOP II	Industrial -40°C ~ 85°C	45
AS6C4016B-45BIN	256K x 16	2.7 ~ 3.6V	48-ball 6mm x 8mm FBGA	Industrial -40°C ~ 85°C	45

## PART NUMBERING SYSTEM

AS6C	4016B	-45	Z/B	I	N	XX
<b>AS6C</b> = Low Power SRAM	Device Number <b>40</b> = 4Meg <b>16</b> = x 16 bit <b>B</b> = B die version	Access Time <b>45</b> = 45ns	<b>Z</b> =TSOPII <b>B</b> =FBGA	<b>I</b> = Industrial Temp -40°C~ 85°C	Indicates Pb and Halogen Free	Packing Type <b>None</b> : Tray <b>TR</b> : Reel



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