



# 74VHC573 Octal D-Type Latch with 3-STATE Outputs

#### **Features**

- High Speed: t<sub>PD</sub> = 5.0ns (Typ.) at V<sub>CC</sub> = 5V
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Power Down Protection is provided on all inputs
- Low Noise:  $V_{OLP} = 0.6V$  (Typ.)
- Low Power Dissipation:  $I_{CC} = 4\mu A \text{ (Max.)} \oslash T_A = 25^{\circ}C$
- Pin and function compatible with 74HC573

## **General Description**

The VHC573 is an advanced high speed CMOS octal latch with 3-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type latch is controlled by a latch enable input (LE) and an Output Enable input ( $\overline{OE}$ ). When the  $\overline{OE}$  input is HIGH, the eight outputs are in a high impedance state.

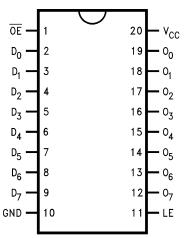
An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## **Ordering Information**

Order Number	Package Number	Package Description
74VHC573M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC573SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC573MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number. Pb-Free package per JEDEC J-STD-020B.

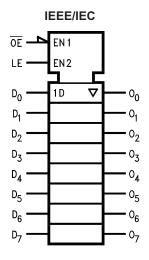
# **Connection Diagram**



## **Pin Description**

Pin Names	Description
D <sub>0</sub> –D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
ŌĒ	3-STATE Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	3-STATE Outputs

## **Logic Symbol**



## **Functional Description**

The VHC573 contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs, a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable  $(\overline{OE})$  input. When  $\overline{OE}$  is LOW, the buffers are enabled. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode, but, this does not interfere with entering new data into the latches.

#### **Truth Table**

	Inputs	Outputs	
ŌĒ	LE	D	O <sub>n</sub>
L	Н	Н	Н
L	Н	L	L
L	L	Х	O <sub>0</sub>
Н	Х	Х	Z

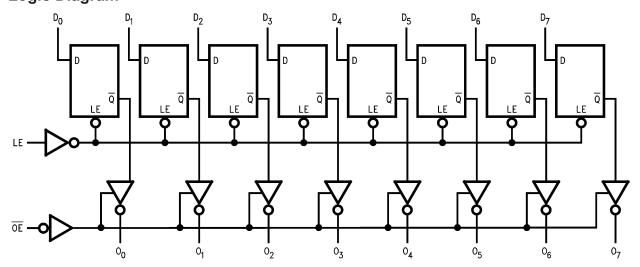
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V <sub>CC</sub>	Supply Voltage	-0.5V to +7.0V
V <sub>IN</sub>	DC Input Voltage	-0.5V to +7.0V
V <sub>OUT</sub>	DC Output Voltage	–0.5V to V <sub>CC</sub> + 0.5V
I <sub>IK</sub>	Input Diode Current	–20mA
I <sub>OK</sub>	Output Diode Current	±20mA
I <sub>OUT</sub>	DC Output Current	±25mA
I <sub>CC</sub>	DC V <sub>CC</sub> /GND Current	±75mA
T <sub>STG</sub>	Storage Temperature	–65°C to +150°C
T <sub>L</sub>	Lead Temperature (Soldering, 10 seconds)	260°C

# Recommended Operating Conditions<sup>(1)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V <sub>CC</sub>	Supply Voltage	2.0V to +5.5V
V <sub>IN</sub>	Input Voltage	0V to +5.5V
V <sub>OUT</sub>	Output Voltage	0V to V <sub>CC</sub>
T <sub>OPR</sub>	Operating Temperature	-40°C to +85°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time,	
	$V_{CC} = 3.3V \pm 0.3V$	0ns/V ~ 100ns/V
	$V_{CC} = 5.0V \pm 0.5V$	0ns/V ~ 20ns/V

#### Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

# **DC Electrical Characteristics**

					Т	A = 25°	С	T <sub>A</sub> = -40°0	C to +85°C	
Symbol	Parameter	V <sub>CC</sub> (V)	Con	ditions	Min.	Тур.	Max.	Min.	Max.	Units
V <sub>IH</sub>	HIGH Level Input	2.0			1.50			1.50		V
	Voltage	3.0-5.5			0.7 x V <sub>CC</sub>			0.7 x V <sub>CC</sub>		
V <sub>IL</sub>	LOW Level Input	2.0					0.50		0.50	V
	Voltage	3.0-5.5					0.3 x V <sub>CC</sub>		0.3 x V <sub>CC</sub>	
V <sub>OH</sub>	HIGH Level	2.0		$I_{OH} = -50\mu A$	1.9	2.0		1.9		V
	Output Voltage	3.0	or V <sub>IL</sub>		2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		$I_{OH} = -4mA$	2.58			2.48		
		4.5		$I_{OH} = -8mA$	3.94			3.80		
V <sub>OL</sub>	LOW Level	2.0	$V_{IN} = V_{IH}$	$I_{OL} = 50\mu A$		0.0	0.1		0.1	V
	Output Voltage	3.0	or V <sub>IL</sub>			0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		I <sub>OL</sub> = 4mA			0.36		0.44	
		4.5		I <sub>OL</sub> = 8mA			0.36		0.44	
I <sub>OZ</sub>	3-STATE Output Off-State Current	5.5	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $V_{OUT} = V_{CC} \text{ or GND}$				±0.25		±2.5	μA
I <sub>IN</sub>	Input Leakage Current	0–5.5	$V_{IN} = 5.5V$ or GND				±0.1		±1.0	μА
I <sub>CC</sub>	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$	or GND			4.0		40.0	μA

# **Noise Characteristics**

				<b>T</b> <sub>A</sub> = 25°C		
Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	Тур.	Limits	Units
V <sub>OLP</sub> <sup>(2)</sup>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	C <sub>L</sub> = 50pF	0.9	1.2	V
V <sub>OLV</sub> <sup>(2)</sup>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	C <sub>L</sub> = 50pF	-0.8	-1.0	V
V <sub>IHD</sub> <sup>(2)</sup>	Minimum HIGH Level Dynamic Input Voltage	5.0	C <sub>L</sub> = 50pF		3.5	V
V <sub>ILD</sub> <sup>(2)</sup>	Maximum LOW Level Dynamic Input Voltage	5.0	C <sub>L</sub> = 50pF		1.5	V

#### Note:

2. Parameter guaranteed by design.

#### **AC Electrical Characteristics**

					Т	' <sub>A</sub> = 25°	С	T <sub>A</sub> = -	-40°C 85°C	
Symbol	Parameter	V <sub>CC</sub> (V)	Cond	ditions	Min.	Тур.	Max.	Min.	Max.	Units
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay	3.3 ± 0.3		C <sub>L</sub> = 15pF		7.6	11.9	1.0	14.0	ns
	Time (LE to O <sub>n</sub> )			C <sub>L</sub> = 50pF		10.1	15.4	1.0	17.5	
		5.0 ± 0.5		C <sub>L</sub> = 15pF		5.0	7.7	1.0	9.0	
				C <sub>L</sub> = 50pF		6.5	9.7	1.0	11.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay	$3.3 \pm 0.3$		C <sub>L</sub> = 15pF		7.0	11.0	1.0	13.0	ns
	Time (D–O <sub>n</sub> )			C <sub>L</sub> = 50pF		9.5	14.5	1.0	16.5	
		5.0 ± 0.5		C <sub>L</sub> = 15pF		4.5	6.8	1.0	8.0	
				C <sub>L</sub> = 50pF		6.0	8.8	1.0	10.0	
t <sub>PZL</sub> , t <sub>PZH</sub>	3-STATE Output	3.3 ± 0.3	$R_L = 1k\Omega$	C <sub>L</sub> = 15pF		7.3	11.5	1.0	13.5	ns
	Enable Time			C <sub>L</sub> = 50pF		9.8	15.0	1.0	17.0	
		5.0 ± 0.5		$C_L = 15pF$		5.2	7.7	1.0	9.0	
				$C_L = 50pF$		6.7	9.7	1.0	11.0	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	3-STATE Output	3.3 ± 0.3	$R_L = 1k\Omega$	$C_L = 50pF$		10.7	14.5	1.0	16.5	ns
	Disable Time	5.0 ± 0.5		C <sub>L</sub> = 50pF		6.7	9.7	1.0	11.0	
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output	3.3 ± 0.3	(3)	C <sub>L</sub> = 50pF			1.5		1.5	ns
	Skew	5.0 ± 0.5		$C_L = 50pF$			1.0		1.0	
C <sub>IN</sub>	Input Capacitance		V <sub>CC</sub> = Ope	en		4	10		10	pF
C <sub>OUT</sub>	Output Capacitance		V <sub>CC</sub> = 5.0\	/		6				pF
C <sub>PD</sub>	Power Dissipation Capacitance		(4)			29				pF

#### Notes:

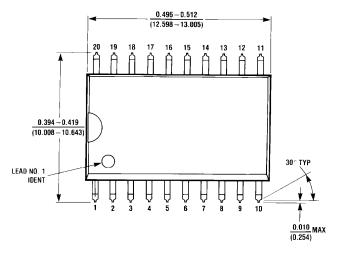
- 3. Parameter guaranteed by design.  $t_{OSLH} = |t_{PLH\;max} t_{PLH\;min}|; \ t_{OSHL} = |t_{PHL\;max} t_{PHL\;min}|$
- 4. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:
  I<sub>CC</sub> (Opr.) = C<sub>PD</sub> V<sub>CC</sub> f<sub>IN</sub> + I<sub>CC</sub> / 8 (per Latch). The total C<sub>PD</sub> when n pcs. of the Latch operates can be calculated by the equation: C<sub>PD</sub>(total) = 21 + 8n.

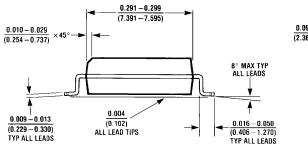
# **AC Operating Requirements**

		V <sub>CC</sub>	1	Γ <sub>A</sub> = 25°0		T <sub>A</sub> = -4	10°C to 5°C	
Symbol	Parameter	V <sub>CC</sub> (V)	Min.	Тур.	Max.	Min.	Max.	Units
$t_w(H), t_w(L)$	Minimum Pulse Width (LE)	3.3 ± 0.3	5.0			5.0		ns
		5.0 ± 0.5	5.0			5.0		
t <sub>S</sub>	Minimum Setup Time	3.3 ± 0.3	3.5			3.5		ns
		5.0 ± 0.5	3.5			3.5		
t <sub>H</sub>	Minimum Hold Time	3.3 ± 0.3	1.5			1.5		ns
		5.0 ± 0.5	1.5			1.5		

# **Physical Dimensions**

Dimensions are in inches (millimeters) unless otherwise noted.





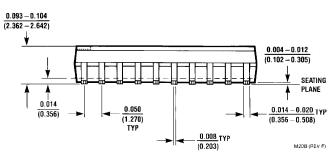
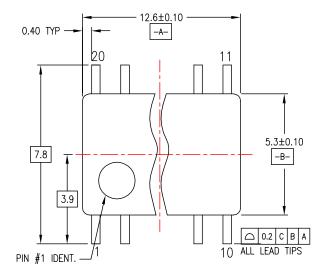
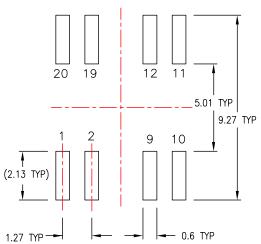


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B

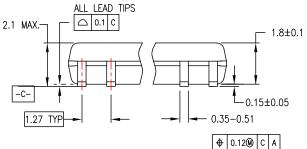
# Physical Dimensions (Continued)

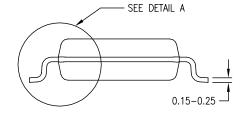
Dimensions are in millimeters unless otherwise noted.





LAND PATTERN RECOMMENDATION





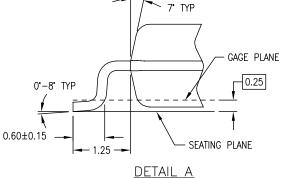
DIMENSIONS ARE IN MILLIMETERS

### NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

  B. DIMENSIONS ARE IN MILLIMETERS.

  C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

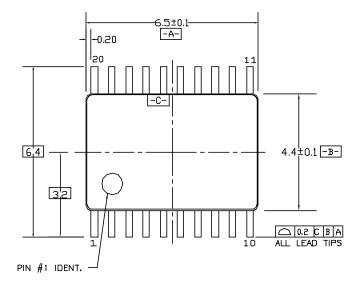


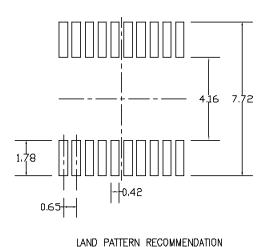
M20DREVC

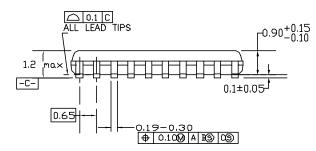
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

# Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



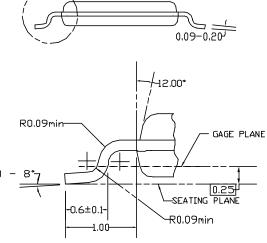






#### NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



SEE DETAIL A

DETAIL A

MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20





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