CDCE(L)925: Flexible Low Power LVCMOS Clock Generator With SSC Support for EMI Reduction

1 Features

- Member of Programmable Clock Generator Family
  - CDCEx913: 1-PLL, 3 Outputs
  - *CDCEx925: 2-PLL, 5 Outputs*
  - CDCEx925: 3-PLL, 7 Outputs
  - CDCEx949: 4-PLL, 9 Outputs
- In-System Programmability and EEPROM
  - Serial Programmable Volatile Register
  - Nonvolatile EEPROM to Store Customer Settings
- Flexible Input Clocking Concept
  - External Crystal: 8 MHz to 32 MHz
  - On-Chip VCXO: Pull Range ±150 ppm
  - Single-Ended LVCMOS Up to 160 MHz
- Free Selectable Output Frequency Up to 230 MHz
- Low-Noise PLL Core
  - PLL Loop Filter Components Integrated
  - Low Period Jitter (Typical 60 ps)
- Separate Output Supply Pins
  - CDCE925: 3.3 V and 2.5 V
  - CDCEL925: 1.8 V
- Flexible Clock Driver
  - Three User-Definable Control Inputs [S0/S1/S2], for Example, SSC Selection, Frequency Switching, Output Enable, or Power Down
  - Generates Highly Accurate Clocks for Video, Audio, USB, IEEE1394, RFID, Bluetooth®, WLAN, Ethernet™, and GPS
  - Generates Common Clock Frequencies Used With TI-DaVinci™, OMAP™, DSPs
  - Programmable SSC Modulation
  - Enables 0-PPM Clock Generation
- 1.8-V Device Power Supply
- Wide Temperature Range: –40°C to 85°C
- Packaged in TSSOP
- Development and Programming Kit for Easy PLL Design and Programming (TI Pro-Clock™)

2 Applications

D-TVs, STBs, IP-STBs, DVD Players, DVD Recorders, and Printers

3 Description

The CDCE925 and CDCEL925 are modular PLL-based low-cost, high-performance, programmable clock synthesizers, multipliers, and dividers. They generate up to five output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using up to two independent configurable PLLs.

The CDCEx925 has a separate output supply pin, V_{DDOUT}, which is 1.8 V for CDCEL925 and 2.5 V to 3.3 V for CDCE925.

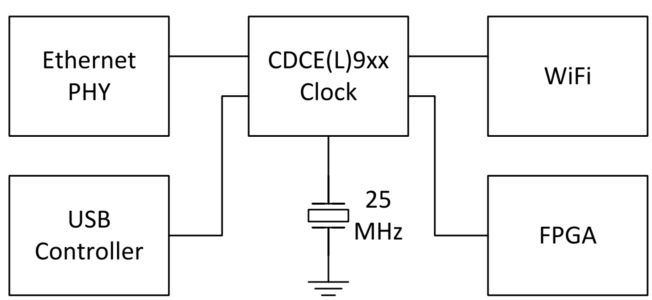
The input accepts an external crystal or LVCMOS clock signal. In case of a crystal input, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20 pF. Additionally, an on-chip VCXO is selectable which allows synchronization of the output frequency to an external control signal, that is, PWM signal.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCEx925	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (August 2016) to Revision I **Page**

- Changed data sheet title from: *CDCEx925 Programmable 2-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V, 3.3-V LVCMOS Outputs* to: *CDCE(L)925: Flexible Low Power LVCMOS Clock Generator With SSC Support for EMI Reduction* 1

Changes from Revision G (November 2011) to Revision H **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed $R_{\theta JB}$ from 64°C/W : to 63.63°C/W 6
- Changed ψ_{JT} from 1.0°C/W : to 1.01°C/W 6
- Added ψ_{JB} parameter to *Thermal Information* table 6
- Deleted figure 20

Changes from Revision F (March 2010) to Revision G **Page**

- Changed in Figure 9, second S to Sr 18
- Changed under second where page 21 from N′ = N × 2^PN ≥ M100 MHz ≤ f_{VCO} ≤ 200 MHz; TO 3 lines with last line being changed to 80 MHz ≤ f_{VCO} ≤ 230 MHz and 0 ≤ p ≤ 7 changed to 0 ≤ p ≤ 4 26

Copyright © 2007–2016, Texas Instruments Incorporated

Changes from Revision E (October 2009) to Revision F	Page
• Added PLL settings limits: 16 ≤ q ≤ 63, 0 ≤ p ≤ 7, 0 ≤ r ≤ 511, 0 < N < 4096 to PLL1 and PLL2 Configure Register tables	21
• Added PLL settings limits: 16 ≤ q ≤ 63, 0 ≤ p ≤ 7, 0 ≤ r ≤ 511, 0 < N < 511 to PLL Multiplier/Divder Definition Section	25

Changes from Revision D (September 2009) to Revision E	Page
• Deleted sentence - A different default setting can be programmed on customer request. Contact Texas Instruments sales or marketing representative for more information.	15

Changes from Revision C (December 2007) to Revision D	Page
• Added Note 3: SDA and SCL can go up to 3.6 V as stated in the *Recommended Operating Conditions* table	5

Changes from Revision B (August 2007) to Revision C	Page
• Changed all values except in add rows: Original - 108, 102, 100, 96, 34	6
• Changed *Generic Configuration Register* table RID From: 0h To: Xb	19
• Added note to the PWDN description in *Generic Configuration Register* table	19

Changes from Revision A (August 2007) to Revision B	Page
• Changed I_{DDPD} Power-down current Typ value from 20 to 30	6
• Changed I_I LVCMOS Input current Typ value from ±5 to ±5 Max	6
• Changed I_{IH} LVCMOS Input current for S0/S1/S2 value from 5 Typ to 5 Max	6
• Changed I_{IL} LVCMOS Input current for S0/S1/S2 value from –4 Typ to –4 Max	6
• Changed text of Note 4 in the DEVICE CHARACTERISTIC table	8
• Changed Test Load for 50-Ω Board Environment	11
• Changed *PLL Setting* table header From: OUTPUT SELECTION (Y2 ... Y9) To: OUTPUT SELECTION (Y2 ... Y5)	14
• Changed *Generic Configuration Register* table 01h Bit 7 From: For interla use – always write To: Reserved – always write	19
• Changed *PLL2 Configuration Register* table PLL2_1N [11:4] description From: f_{VCO1_1} To: f_{VCO2_1}	23

Changes from Original (July 2007) to Revision A	Page
• Changed the data sheet status From: Product Preview To: Production data	1

5 Description (continued)

The deep M/N divider ratio allows the generation of zero-ppm audio/video, networking (WLAN, Bluetooth, Ethernet, GPS), or interface (USB, IEEE1394, memory stick) clocks from a 27-MHz reference input frequency, for example.

All PLLs support SSC (spread-spectrum clocking). SSC can be center-spread or down-spread clocking, which is a common technique to reduce electromagnetic interference (EMI).

Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristic of each PLL.

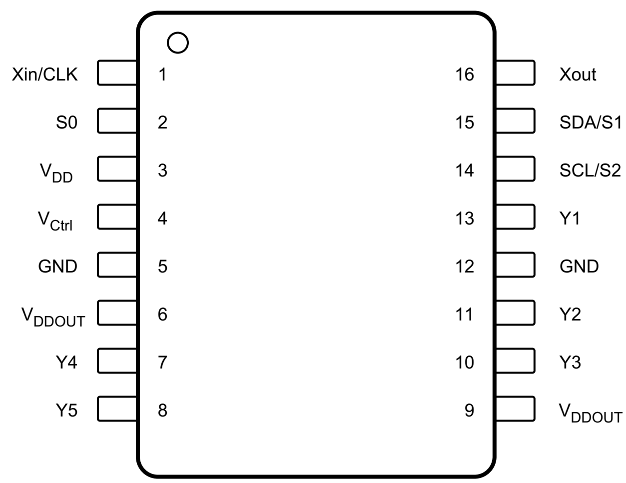
The device supports nonvolatile EEPROM programming for easy customization of the device in the application. It is preset to a factory default configuration and can be reprogrammed to a different application configuration before it goes onto the PCB or reprogrammed by in-system programming. All device settings are programmable through the SDA/SCL bus, a 2-wire serial interface.

Three, free programmable control inputs, S0, S1, and S2, can be used to select different frequencies, or change the SSC setting for lowering EMI, or other control features like outputs disable to low, outputs in high-impedance state, power down, PLL bypass, and so forth.

The CDCx925 operates in a 1.8-V environment and in a temperature range of –40°C to 85°C.

6 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
GND	5, 12	G	Ground
SCL/S2	14	I	**SCL:** Serial clock input (default configuration), LVCMOS; internal pullup **S2:** User-programmable control input; LVCMOS inputs; internal pullup
SDA/S1	15	I/O	**SDA:** Bidirectional serial data input/output (default configuration), LVCMOS; internal pullup **S1:** User-programmable control input; LVCMOS inputs; internal pullup
S0	2	I	User-programmable control input S0; LVCMOS inputs; internal pullup
V_{Ctrl}	4	I	VCXO control voltage (leave open or pull up when not used)
V_{DD}	3	P	1.8-V power supply for the device
V_{DDOUT}	6, 9	P	**CDCEL925**: 1.8-V supply for all outputs
			CDCE925: 3.3-V or 2.5-V supply for all outputs

(1) G = Ground, I = Input, O = Output, P = Power

Copyright © 2007–2016, Texas Instruments Incorporated

Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
Xin/CLK	1	I	Crystal oscillator input or LVCMOS clock Input (selectable through SDA/SCL bus)
Xout	16	O	Crystal oscillator output (leave open or pull up when not used)
Y1	13	O	LVCMOS output
Y2	11		
Y3	10		
Y4	7		
Y5	8		

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage, V_{DD}	–0.5	2.5	V
Input voltage, V_I [2][3]	–0.5	V_{DD} + 0.5	V
Output voltage, V_O [2]	–0.5	V_{DD} + 0.5	V
Input current, I_I ($V_I < 0$, $V_I > V_{DD}$)		20	mA
Continuous output current, I_O		50	mA
Maximum junction temperature, T_J		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) SDA and SCL can go up to 3.6 V as stated in the *Recommended Operating Conditions* table.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage		1.7	1.8	1.9	V
V_{DDOUT}	Output Yx supply voltage	CDCE925	2.3		3.6	V
		CDCEL925	1.7		1.9	
V_{IL}	Low-level input voltage LVCMOS				0.3 × V_{DD}	V
V_{IH}	High-level input voltage LVCMOS		0.7 × V_{DD}			V
$V_{I(thresh)}$	Input voltage threshold LVCMOS			0.5 × V_{DD}		V
$V_{I(S)}$	Input voltage	S0	0		1.9	V
		S1, S2, SDA, SCL; $V_{(Ithresh)}$ = 0.5 V_{DD}	0		3.6	
$V_{I(CLK)}$	Input voltage, CLK		0		1.9	V
I_{OH} / I_{OL}	Output current	V_{DDOUT} = 3.3 V			±12	mA
		V_{DDOUT} = 2.5 V			±10	
		V_{DDOUT} = 1.8 V			±8	
C_L	Output load LVCMOS				15	pF

Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	–40		85	°C
CRYSTAL AND VCXO (1)					
f_{Xtal}	Crystal input frequency (fundamental mode)	8	27	32	MHz
ESR	Effective series resistance			100	Ω
f_{PR}	Pulling (0 V ≤ V_{Ctrl} ≤ 1.8 V) (2)	±120	±150		ppm
V_{Ctrl}	Frequency control voltage	0		V_{DD}	V
C_0/C_1	Pullability ratio			220	
C_L	On-chip load capacitance at Xin and Xout	0		20	pF

(1) For more information about VCXO configuration, and crystal recommendation, see *VCXO Application Guideline for CDCE(L)9xx Family* (SCAA085).
(2) Pulling range depends on crystal-type, on-chip crystal load capacitance and PCB stray capacitance; pulling range of minimum ±120 ppm applies for crystal listed in *VCXO Application Guideline for CDCE(L)9xx Family* (SCAA085).

7.4 Thermal Information

THERMAL METRIC (1)			CDCEx925 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Airflow 0 (LFM)	101	°C/W
		Airflow 150 (LFM)	85	
		Airflow 200 (LFM)	84	
		Airflow 250 (LFM)	82	
		Airflow 500 (LFM)	74	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		63.63	°C/W
ψ_{JT}	Junction-to-top characterization parameter		1.01	°C/W
ψ_{JB}	Junction-to-board characterization parameter		58.12	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		58	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
I_{DD}	Supply current (see Figure 1)	All outputs off, f_{CLK} = 27 MHz, f_{VCO} = 135 MHz, f_{OUT} = 27 MHz	All PLLS on		20		mA
			Per PLL		9		
I_{DDOUT}	Supply current (see Figure 2 and Figure 3)	No load, all outputs on, f_{OUT} = 27 MHz	CDCE925, V_{DDOUT} = 3.3 V		2		mA
			CDCEL925, V_{DDOUT} = 1.8 V		1		
I_{DDPD}	Power-down current. Every circuit powered down except SDA/SCL	f_{IN} = 0 MHz, V_{DD} = 1.9 V			30		µA
V_{PUC}	Supply voltage V_{DD} threshold for power-up control circuit			0.85		1.45	V
f_{VCO}	VCO frequency range of PLL			80		230	MHz
f_{OUT}	LVCMOS output frequency	CDCEx925 V_{DDOUT} = 1.8 V		230			MHz
LVCMOS							
V_{IK}	LVCMOS input voltage	V_{DD} = 1.7 V, I_S = –18 mA				–1.2	V
I_I	LVCMOS input current	V_I = 0 V or V_{DD}, V_{DD} = 1.9 V				±5	µA
I_{IH}	LVCMOS input current for S0/S1/S2	V_I = V_{DD}, V_{DD} = 1.9 V				5	µA
I_{IL}	LVCMOS Input current for S0/S1/S2	V_I = 0 V, V_{DD} = 1.9 V				–4	µA

(1) All typical values are at respective nominal V_{DD}.

Copyright © 2007–2016, Texas Instruments Incorporated

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
C_I	Input capacitance at Xin/Clk	V_{IClk} = 0 V or V_{DD}		6		pF
	Input capacitance at Xout	V_{IXout} = 0 V or V_{DD}		2		
	Input capacitance at S0/S1/S2	V_{IS} = 0 V or V_{DD}		3		
CDCE925 – LVCMOS FOR V_{DDOUT} = 3.3 V						
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 3 V, I_{OH} = –0.1 mA	2.9			V
		V_{DDOUT} = 3 V, I_{OH} = –8 mA	2.4			
		V_{DDOUT} = 3 V, I_{OH} = –12 mA	2.2			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 3 V, I_{OL} = 0.1 mA			0.1	V
		V_{DDOUT} = 3 V, I_{OL} = 8 mA			0.5	
		V_{DDOUT} = 3 V, I_{OL} = 12 mA			0.8	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass		3.2		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 3.3 V (20%–80%)		0.6		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter[2][3]	1 PLL switching, Y2-to-Y3		50	70	ps
		2 PLL switching, Y2-to-Y5		90	130	
$t_{jit(per)}$	Peak-to-peak period jitter[3]	1 PLL switching, Y2-to-Y3		60	100	ps
		2 PLL switching, Y2-to-Y5		100	160	
$t_{sk(o)}$	Output skew[4]	f_{OUT} = 50 MHz, Y1-to-Y3			70	ps
		f_{OUT} = 50 MHz, Y2-to-Y5			150	
odc	Output duty cycle[5]	f_{VCO} = 100 MHz, Pdiv = 1	45%		55%	
CDCE925 – LVCMOS FOR V_{DDOUT} = 2.5 V						
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 2.3 V, I_{OH} = –0.1 mA	2.2			V
		V_{DDOUT} = 2.3 V, I_{OH} = –6 mA	1.7			
		V_{DDOUT} = 2.3 V, I_{OH} = –10 mA	1.6			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 2.3 V, I_{OL} = 0.1 mA			0.1	V
		V_{DDOUT} = 2.3 V, I_{OL} = 6 mA			0.5	
		V_{DDOUT} = 2.3 V, I_{OL} = 10 mA			0.7	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass		3.6		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 2.5 V (20%–80%)		0.8		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter[2][3]	1 PLL switching, Y2-to-Y3		50	70	ps
		2 PLL switching, Y2-to-Y5		90	130	
$t_{jit(per)}$	Peak-to-peak period jitter[3]	1 PLL switching, Y2-to-Y3		60	100	ps
		2 PLL switching, Y2-to-Y5		100	160	
$t_{sk(o)}$	Output skew[4]	f_{OUT} = 50 MHz, Y1-to-Y3			70	ps
		f_{OUT} = 50 MHz, Y2-to-Y5			150	
odc	Output duty cycle[5]	f_{VCO} = 100 MHz, Pdiv = 1	45%		55%	
CDCEL925 – LVCMOS FOR V_{DDOUT} = 1.8 V						
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 1.7 V, I_{OH} = –0.1 mA	1.6			V
		V_{DDOUT} = 1.7 V, I_{OH} = –4 mA	1.4			
		V_{DDOUT} = 1.7 V, I_{OH} = –8 mA	1.1			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 1.7 V, I_{OL} = 0.1 mA			0.1	V
		V_{DDOUT} = 1.7 V, I_{OL} = 4 mA			0.3	
		V_{DDOUT} = 1.7 V, I_{OL} = 8 mA			0.6	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass		2.6		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 1.8 V (20%–80%)		0.7		ns

(2) 10,000 cycles
(3) Jitter depends on configuration. Jitter data is for input frequency = 27 MHz, f_{VCO} = 135 MHz, f_{OUT} = 27 MHz. f_{OUT} = 3.072 MHz or input frequency = 27 MHz, f_{VCO} = 108 MHz, f_{OUT} = 27 MHz. f_{OUT} = 16.384 MHz, f_{OUT} = 25 MHz, f_{OUT} = 74.25 MHz, f_{OUT} = 48 MHz
(4) The tsk(o) specification is only valid for equal loading of each bank of outputs, and the outputs are generated from the same divider, data sampled on rising edge (t_r).
(5) odc depends on output rise- and fall-time (t_r/t_f);

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{jit(cc)}$	Cycle-to-cycle jitter (2) (3)	1 PLL switching, Y2-to-Y3		80	110	ps
		2 PLL switching, Y2-to-Y5		130	200	
$t_{jit(per)}$	Peak-to-peak period jitter (3)	1 PLL switching, Y2-to-Y3		100	130	ps
		2 PLL switching, Y2-to-Y5		150	220	
$t_{sk(o)}$	Output skew (4)	f_{OUT} = 50 MHz, Y1-to-Y3			50	ps
		f_{OUT} = 50 MHz, Y2-to-Y5			110	
odc	Output duty cycle (5)	f_{VCO} = 100 MHz, Pdiv = 1	45%		55%	
SDA AND SCL						
V_{IK}	SCL and SDA input clamp voltage	V_{DD} = 1.7 V, I_I = –18 mA			–1.2	V
I_{IH}	SCL and SDA input current	$V_I = V_{DD}$, V_{DD} = 1.9 V			±10	µA
V_{IH}	SDA/SCL input high voltage (6)		0.7 × V_{DD}			V
V_{IL}	SDA/SCL input low voltage (6)				0.3 × V_{DD}	V
V_{OL}	SDA low-level output voltage	I_{OL} = 3 mA, V_{DD} = 1.7 V			0.2 × V_{DD}	V
C_I	SCL/SDA Input capacitance	V_I = 0 V or V_{DD}		3	10	pF

(6) SDA and SCL pins are 3.3-V tolerant.

7.6 EEPROM Specification

		MIN	TYP	MAX	UNIT
EEcyc	Programming cycles of EEPROM	100	1000		cycles
EEret	Data retention	10			years

7.7 Timing Requirements: CLK_IN

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{CLK}	LVCMOS clock input frequency	PLL bypass mode	0		160	MHz
		PLL mode	8		160	
t_r / t_f	Rise and fall time CLK signal (20% to 80%)				3	ns
$duty_{CLK}$	Duty cycle CLK at V_{DD} / 2		40%		60%	

7.8 Timing Requirements: SDA/SCL

over operating free-air temperature range (unless otherwise noted; see Figure 8)

			MIN	NOM	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
$t_{su(START)}$	START setup time (SCL high before SDA low)	Standard mode	4.7			µs
		Fast mode	0.6			
$t_{h(START)}$	START hold time (SCL low after SDA low)	Standard mode	4			µs
		Fast mode	0.6			
$t_{w(SCLL)}$	SCL low-pulse duration	Standard mode	4.7			µs
		Fast mode	1.3			
$t_{w(SCLH)}$	SCL high-pulse duration	Standard mode	4			µs
		Fast mode	0.6			
$t_{h(SDA)}$	SDA hold time (SDA valid after SCL low)	Standard mode	0		3.45	µs
		Fast mode	0		0.9	
$t_{su(SDA)}$	SDA setup time	Standard mode	250			ns
		Fast mode	100			

 Copyright © 2007–2016, Texas Instruments Incorporated

Timing Requirements: SDA/SCL (continued)

over operating free-air temperature range (unless otherwise noted; see Figure 8)

			MIN	NOM	MAX	UNIT
t_r	SCL/SDA input rise time	Standard mode			1000	ns
		Fast mode			300	
t_f	SCL/SDA input fall time, standard and fast mode				300	ns
$t_{su(STOP)}$	STOP setup time	Standard mode	4			µs
		Fast mode	0.6			
t_{BUS}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			

7.9 Typical Characteristics

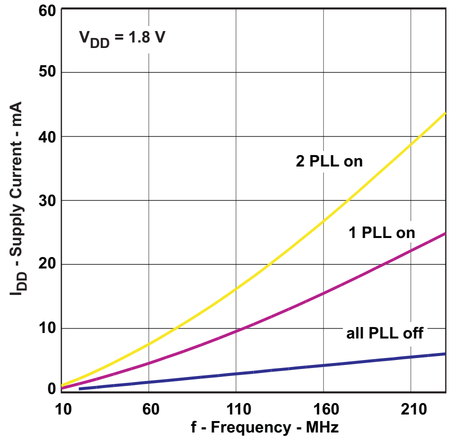


Figure 1. CDCEx925 Supply Current vs PLL Frequency

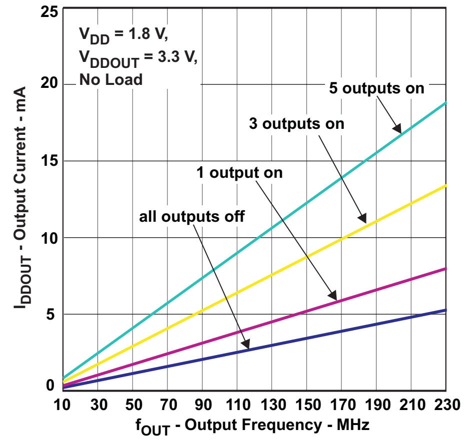


Figure 2. CDCE925 Output Current vs Output Frequency

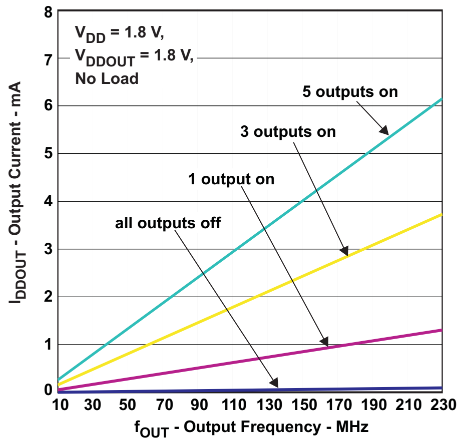
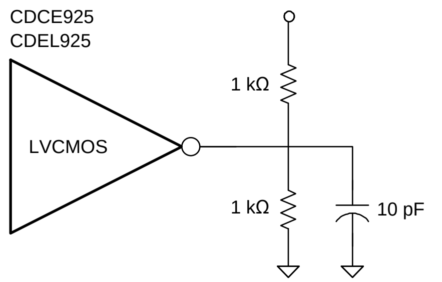


Figure 3. CDCEL925 Output Current vs Output Frequency

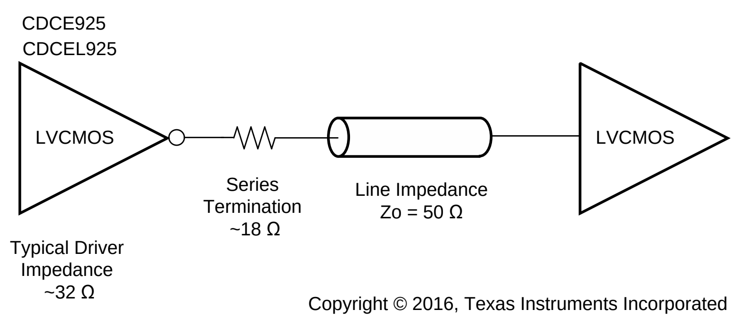
Copyright © 2007–2016, Texas Instruments Incorporated

8 Parameter Measurement Information



Copyright © 2016, Texas Instruments Incorporated

Figure 4. Test Load



Copyright © 2016, Texas Instruments Incorporated

Figure 5. Test Load for 50-Ω Board Environment

9 Detailed Description

9.1 Overview

The CDCE925 and CDCEL925 devices are modular PLL-based, low-cost, high-performance, programmable clock synthesizers, multipliers, and dividers. They generate up to five output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using one of the two integrated configurable PLLs.

The CDCx925 has separate output supply pins, V_{DDOUT}, which is 1.8 V for CDCEL925 and 2.5 V to 3.3 V for CDCE925.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 pF to 20 pF. Additionally, a selectable on-chip VCXO allows synchronization of the output frequency to an external control signal, that is, the PWM signal.

The deep M/N divider ratio allows the generation of 0-ppm audio and video, networking (WLAN, Bluetooth, Ethernet, GPS), or interface (USB, IEEE1394, memory stick) clocks from a reference input frequency such as 27 MHz.

All PLLs support spread-spectrum clocking (SSC). SSC can be center-spread or down-spread clocking. This is a common technique to reduce electro-magnetic interference (EMI).

Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability, and to optimize the jitter-transfer characteristic of each PLL.

The device supports non-volatile EEPROM programming for easy customization of the device in the application. It is preset to a factory default configuration (see *Default Device Setting*). It can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through the SDA and SCL bus, a 2-wire serial interface.

Three free programmable control inputs, S0, S1, and S2, can be used to control various aspects of operation including frequency selection, changing the SSC parameters to lower EMI, PLL bypass, power down, or other control features like outputs disable to low, outputs in high-impedance state, and so forth.

The CDCx925 operates in a 1.8-V environment. It operates within a temperature range of –40°C to 85°C.

Copyright © 2007–2016, Texas Instruments Incorporated

9.2 Functional Block Diagram

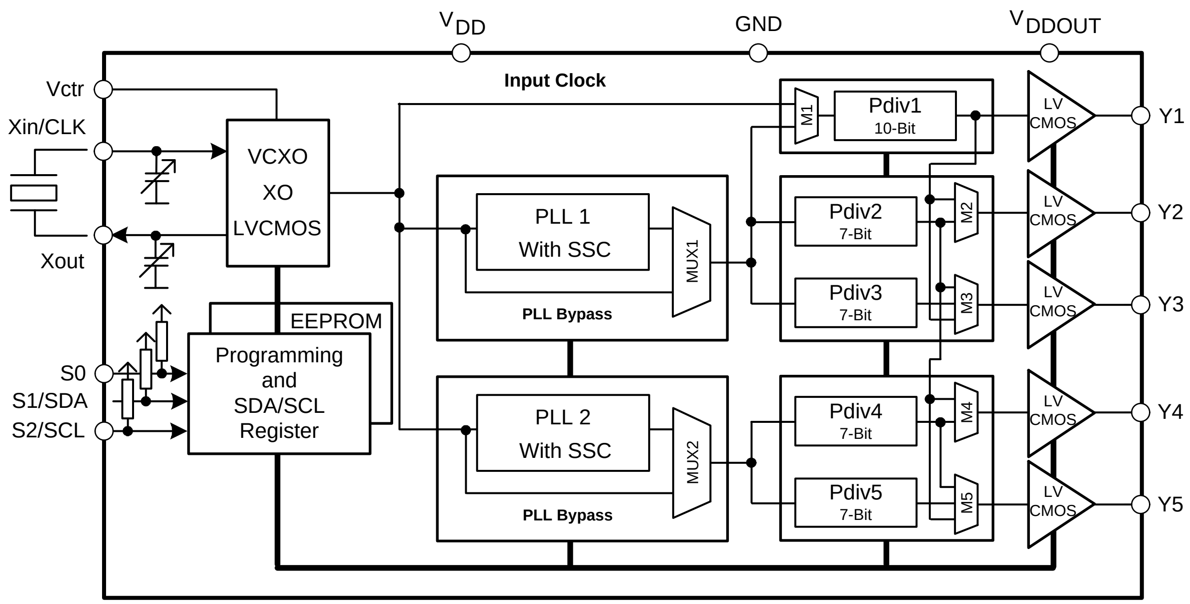


Figure 6. Functional Block Diagram for CDCEx925

9.3 Feature Description

9.3.1 Control Terminal Setting

The CDCEx925 has three user-definable control terminals (S0, S1, and S2) which allow external control of device settings. They can be programmed to any of the following settings:

- Spread spectrum clocking selection → spread type and spread amount selection
- Frequency selection → switching between any of two user-defined frequencies
- Output state selection → output configuration and power-down control

The user can predefine up to eight different control settings. Table 1 and Table 2 explain these settings.

Table 1. Control Terminal Definition

EXTERNAL CONTROL BITS	PLL1 SETTING			PLL2 SETTING			Y1 SETTING
Control function	PLL frequency selection	SSC selection	Output Y2/Y3 selection	PLL frequency selection	SSC selection	Output Y4/Y5 selection	Output Y1 and power-down selection

Table 2. PLL Setting (Can Be Selected for Each PLL Individual)(1)

SSC SELECTION (CENTER/DOWN)				
SSCx [3-Bits]			CENTER	DOWN
0	0	0	0% (off)	0% (off)
0	0	1	±0.25%	–0.25%
0	1	0	±0.5%	–0.5%
0	1	1	±0.75%	–0.75%
1	0	0	±1%	–1.0%
1	0	1	±1.25%	–1.25%

(1) Center/down-spread, Frequency0/1 and State0/1 are user-definable in the PLLx configuration register.

Table 2. PLL Setting (Can Be Selected for Each PLL Individual)(1) (continued)

SSC SELECTION (CENTER/DOWN)				
SSCx [3-Bits]			CENTER	DOWN
1	1	0	±1.5%	–1.5%
1	1	1	±2%	–2%
FREQUENCY SELECTION (2)				
FSx		FUNCTION		
0		Frequency0		
1		Frequency1		
OUTPUT SELECTION (3) (Y2 ... Y5)				
YxYx		FUNCTION		
0		State0		
1		State1		

(2) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range.
(3) State0/1 selection is valid for both outputs of the corresponding PLL module and can be power down, high-impedance state, low, or active

Table 3. Y1 Setting (1)

Y1 SELECTION	
Y1	FUNCTION
0	State 0
1	State 1

(1) State0 and State1 are user definable in the generic configuration register and can be power down, high-impedance state, low, or active.

SDA/S1 and SCL/S2 pins of the CDCEx925 are dual-function pins. In the default configuration, they are predefined as the SDA/SCL serial programming interface. They can be programmed to control pins (S1/S2) by setting the relevant bits in the EEPROM. Note that the changes of the bits in the control register (bit [6] of byte 02h) have no effect until they are written into the EEPROM.

Once they are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA/SCL).

S0 is not a multi-use pin; it is a control pin only.

9.3.2 Default Device Setting

The internal EEPROM of CDCEx925 is preconfigured as shown in Figure 7. The input frequency is passed through the output as a default. This allows the device to operate in default mode without the extra production step of programming it. The default setting appears after power is supplied or after a power-down/up sequence until it is reprogrammed by the user to a different application configuration. A new register setting is programmed through the serial SDA/SCL interface.

 Copyright © 2007–2016, Texas Instruments Incorporated

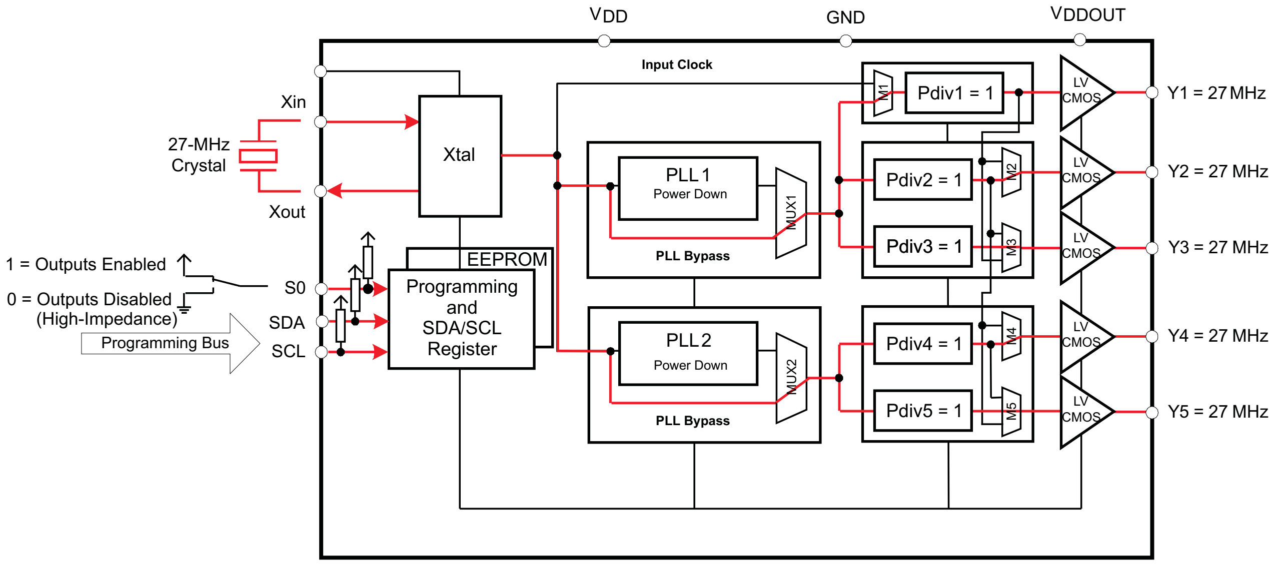


Figure 7. Preconfiguration of CDCEx925 Internal EEPROM

Table 4 shows the factory default setting for the control terminal register (external control pins). Note that even though eight different register settings are possible, in default configuration, only the first two settings (0 and 1) can be selected with S0, as S1 and S2 are configured as programming pins in the default mode.

Table 4. Factory Default Settings for Control Terminal Register(1)

			Y1	PLL1 SETTINGS			PLL2 SETTINGS		
EXTERNAL CONTROL PINS			OUTPUT SELECTION	FREQUENCY SELECTION	SSC SELECTION	OUTPUT SELECTION	FREQUENCY SELECTION	SSC SELECTION	OUTPUT SELECTION
S2	*S1*	**S0**	**Y1**	*FS1*	*SSC1*	**Y2Y3**	*FS2*	*SSC2*	**Y4Y5**
SCL (I2C)	SDA (I2C)	**0**	**High-impedance state**	f_{VCO1_0}	Off	**High-impedance state**	f_{VCO2_0}	Off	**High-impedance state**
SCL (I2C)	SDA (I2C)	**1**	**Enabled**	f_{VCO1_0}	Off	**Enabled**	f_{VCO2_0}	Off	**Enabled**

(1) S1 is SDA and S2 is SCL in default mode or when programmed (SPICON bit 6 of register 2 set to 0). They do not have any control-pin function but they are internally interpreted as if S1 = 0 and S2 = 0. S0, however, is a control pin which in the default mode switches all outputs ON or OFF (as previously predefined).

9.3.3 SDA/SCL Serial Interface

This section describes the SDA/SCL interface of the CDCEx925 device. The CDCEx925 operates as a slave device of the 2-wire serial SDA/SCL bus, compatible with the popular SMBus or I²C specification. It operates in the standard-mode transfer (up to 100 kbps) and fast-mode transfer (up to 400 kbps) and supports 7-bit addressing.

The SDA/S1 and SCL/S2 pins of the CDCEx925 are dual-function pins. In the default configuration they are used as SDA/SCL serial programming interface. They can be reprogrammed as general-purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, byte 02h, bit [6].

Copyright © 2007–2016, Texas Instruments Incorporated

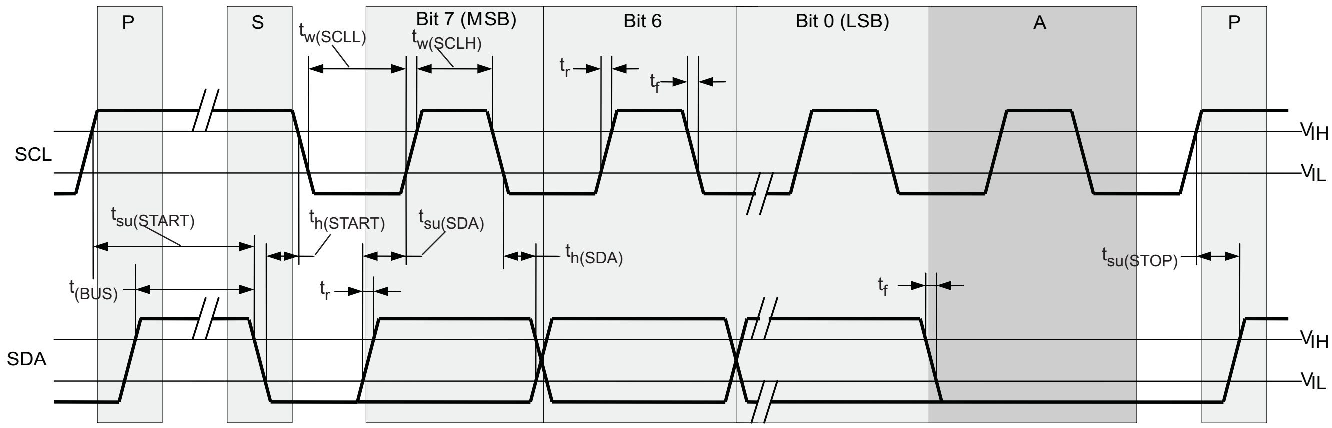


Figure 8. Timing Diagram for SDA/SCL Serial Control Interface

9.3.4 Data Protocol

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most-significant bit first) with the ability to stop after any complete byte has been transferred. The numbers of bytes read out are defined by byte count in the generic configuration register. At the *Block Read* instruction, all bytes defined in the byte count must be read out to finish the read cycle correctly.

Once a byte has been sent, it is written into the internal register and is effective immediately. This applies to each transferred byte regardless of whether this is a *Byte Write* or a *Block Write* sequence.

If the EEPROM write cycle is initiated, the internal SDA registers are written into the EEPROM. During this write cycle, data is not accepted at the SDA/SCL bus until the write cycle is completed. However, data can be read out during the programming sequence (*Byte Read* or *Block Read*). The programming status can be monitored by *EEPIP*, byte 01h–bit 6.

The offset of the indexed byte is encoded in the command code, as described in Table 5.

Table 5. Slave Receiver Address (7 Bits)

DEVICE	A6	A5	A4	A3	A2	A1 (1)	A0 (1)	R/$\overline{W}$
CDCEx913	1	1	0	0	1	0	1	1/0
CDCEx925	*1*	*1*	*0*	*0*	*1*	*0*	*0*	*1/0*
CDCEx925	1	1	0	1	1	0	1	1/0
CDCEx949	1	1	0	1	1	0	0	1/0

(1) Address bits A0 and A1 are programmable through the SDA/SCL bus (byte 01, bit [1:0]. This allows addressing up to four devices connected to the same SDA/SCL bus. The least-significant bit of the address byte designates a write or read operation.

9.4 Device Functional Modes

9.4.1 SDA/SCL Hardware Interface

Figure 9 shows how the CDCEx925 clock synthesizer is connected to the SDA/SCL serial interface bus. Multiple devices can be connected to the bus, but the speed may need to be reduced (400 kHz is the maximum) if many devices are connected.

Note that the pullup resistors (R_P) depend on the supply voltage, bus capacitance, and number of connected devices. The recommended pullup value is 4.7 kΩ. It must meet the minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages (for more details, see SMBus or I^2C Bus specification).

Copyright © 2007–2016, Texas Instruments Incorporated

Device Functional Modes (continued)

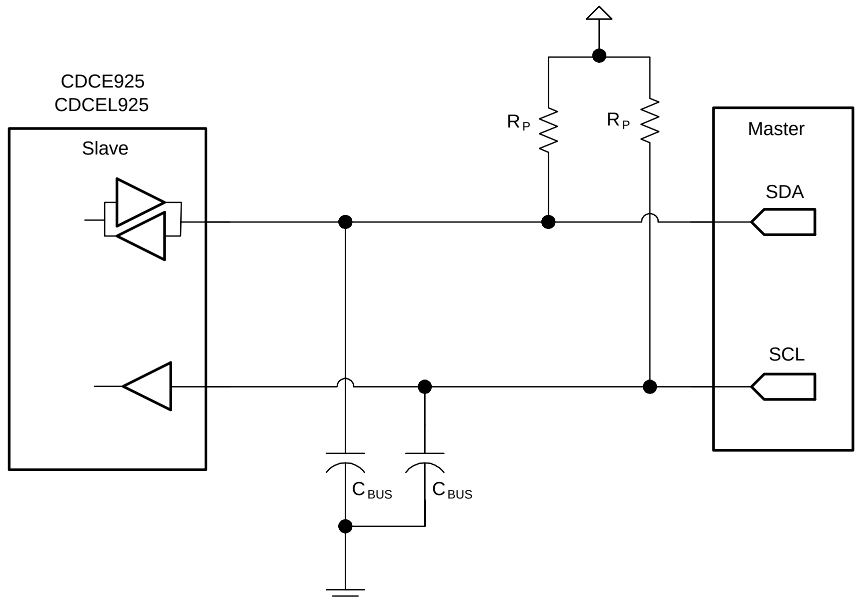


Figure 9. SDA/SCL Hardware Interface

9.5 Programming

Table 6. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Byte offset for *Byte Read*, *Block Read*, *Byte Write* and *Block Write* operations.

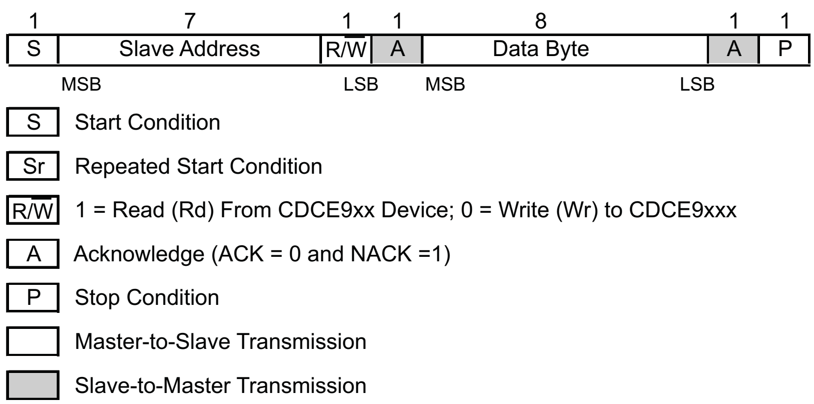


Figure 10. Generic Programming Sequence

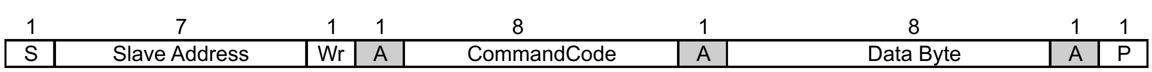


Figure 11. Byte Write Protocol

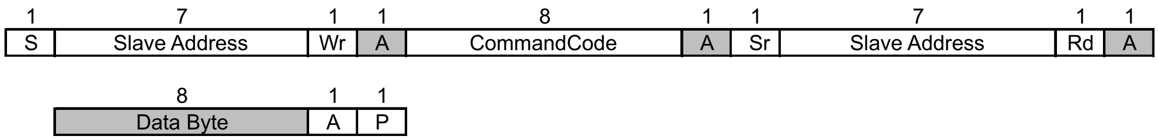
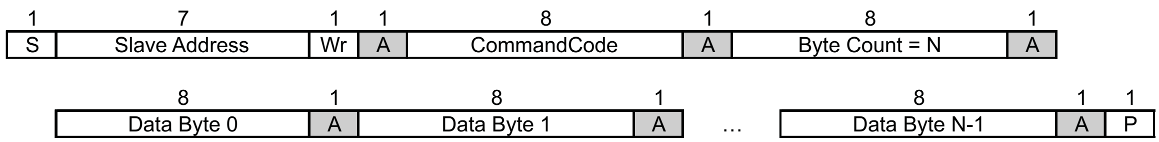


Figure 12. Byte Read Protocol



Data byte 0 bits [7:0] is reserved for Revision Code and Vendor Identification. Also, it is used for internal test purpose and must not be overwritten.

Figure 13. Block Write Protocol

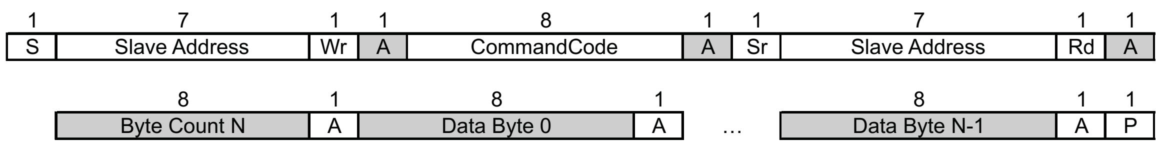


Figure 14. Block Read Protocol

9.6 Register Maps

9.6.1 SDA/SCL Configuration Registers

The clock input, control pins, PLLs, and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCEx925. All settings can be manually written into the device through the SDA/SCL bus or easily programmed by using the TI Pro-Clock™ software. TI Pro-Clock software allows the user to quickly make all settings and automatically calculates the values for optimized performance at lowest jitter.

Table 7. SDA/SCL Registers

ADDRESS OFFSET	REGISTER DESCRIPTION	TABLE
00h	Generic configuration register	Table 9
10h	PLL1 configuration register	Table 10
20h	PLL2 configuration register	Table 11

Copyright © 2007–2016, Texas Instruments Incorporated

The grey-highlighted bits, described in the Configuration Registers tables in the following pages, belong to the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2 (see Control Terminal Setting).

Table 8. Configuration Register, External Control Terminals

	EXTERNAL CONTROL PINS			Y1	PLL1 SETTINGS			PLL2 SETTINGS		
				OUTPUT SELECTION	FREQUENCY SELECTION	SSC SELECTION	OUTPUT SELECTION	FREQUENCY SELECTION	SSC SELECTION	OUTPUT SELECTION
	S2	S1	S0	Y1	FS1	SSC1	Y2Y3	FS2	SSC2	Y4Y5
0	0	0	0	Y1_0	FS1_0	SSC1_0	Y2Y3_0	FS2_0	SSC2_0	Y4Y5_0
1	0	0	1	Y1_1	FS1_1	SSC1_1	Y2Y3_1	FS2_1	SSC2_1	Y4Y5_1
2	0	1	0	Y1_2	FS1_2	SSC1_2	Y2Y3_2	FS2_2	SSC2_2	Y4Y5_2
3	0	1	1	Y1_3	FS1_3	SSC1_3	Y2Y3_3	FS2_3	SSC2_3	Y4Y5_3
4	1	0	0	Y1_4	FS1_4	SSC1_4	Y2Y3_4	FS2_4	SSC2_4	Y4Y5_4
5	1	0	1	Y1_5	FS1_5	SSC1_5	Y2Y3_5	FS2_5	SSC2_5	Y4Y5_5
6	1	1	0	Y1_6	FS1_6	SSC1_6	Y2Y3_6	FS2_6	SSC2_6	Y4Y5_6
7	1	1	1	Y1_7	FS1_7	SSC1_7	Y2Y3_7	FS2_7	SSC2_7	Y4Y5_7
	Address offset(1)			04h	13h	10h–12h	15h	23h	20h–22h	25h

(1) Address offset refers to the byte address in the configuration register in Table 9, Table 10, and Table 11.

Table 9. Generic Configuration Register

OFFSET(1)	BIT(2)	ACRONYM	DEFAULT(3)	DESCRIPTION
00h	7	E_EL	Xb	Device identification (read-only): 1 is CDCE925 (3.3 V out), 0 is CDCEL925 (1.8 V out)
	6:4	RID	Xb	Revision identification number (read-only)
	3:0	VID	1h	Vendor identification number (read-only)
01h	7	–	0b	Reserved – always write 0
	6	EEPIP	0b	EEPROM programming Status4:(4) (read-only) 0 – EEPROM programming is completed 1 – EEPROM is in programming mode
	5	EELOCK	0b	Permanently lock EEPROM data(5) 0 – EEPROM is not locked 1 – EEPROM is permanently locked
	4	PWDN	0b	Device power down (overwrites S0/S1/S2 setting; configuration register settings are unchanged) Note: PWDN cannot be set to 1 in the EEPROM. 0 – Device active (all PLLs and all outputs are enabled) 1 – Device power down (all PLLs in power down and all outputs in high-impedance state)
	3:2	INCLK	00b	Input clock selection: 00 – Xtal 01 – VCXO 10 – LVCMOS 1 – Reserved
	1:0	SLAVE_ADR	00b	Address bits A0 and A1 of the slave receiver address

(1) Writing data beyond 30h may affect device function.
(2) All data transferred with the MSB first
(3) Unless customer-specific setting
(4) During EEPROM programming, no data is allowed to be sent to the device through the SDA/SCL bus until the programming sequence is completed. Data, however, can be read out during the programming sequence (*Byte Read* or *Block Read*).
(5) If this bit is set to high in the EEPROM, the actual data in the EEPROM is permanently locked. No further programming is possible. Data, however can still be written through the SDA/SCL bus to the internal register to change device function on the fly. But new data can no longer be saved to the EEPROM. EELOCK is effective only if written into the EEPROM.

Copyright © 2007–2016, Texas Instruments Incorporated

Table 9. Generic Configuration Register (continued)

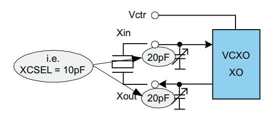
OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
02h	7	M1	1b	Clock source selection for output Y1: 0 – Input clock 1 – PLL1 clock
	6	SPICON	0b	Operation mode selection for pins 14/15[6] 0 – Serial programming interface SDA (pin 15) and SCL (pin 14) 1 – Control pins S1 (pin 15) and S2 (pin 14)
	5:4	Y1_ST1	11b	Y1-State0/1 definition00 – Device power down (all PLLs in power down and all outputs in high-impedance state) 01 – Y1 disabled to high-impedance state 10 – Y1 disabled to low 11 – Y1 enabled
	3:2	Y1_ST0	01b	
	1:0	Pdiv1 [9:8]	001h	10-bit Y1-Output-Divider Pdiv1: 0 – Divider is reset and in standby 1 to 1023 – Divider value
03h	7:0	Pdiv1 [7:0]		
04h	7	Y1_7	0b	Y1_ST0/Y1_ST1 State Selection[7] 0 – State0 (predefined by Y1_ST0) 1 – State1 (predefined by Y1_ST1)
	6	Y1_6	0b	
	5	Y1_6	0b	
	4	Y1_6	0b	
	3	Y1_6	0b	
	2	Y1_6	0b	
	1	Y1_6	0b	
	0	Y1_6	0b	
05h	7:3	XCSEL	0Ah	Crystal load-capacitor selection[8] 00h – 0 pF 01h – 1 pF 02h – 2 pF : 14h to 1Fh – 20 pF 
	2:0		0b	Reserved – do not write other than 0.
06h	7:1	BCOUNT	30h	7-bit byte count (defines the number of bytes which is sent from this device at the next *Block Read* transfer); all bytes must be read out to correctly finish the read cycle.
	0	EEWRITE	0b	Initiate EEPROM write cycle[9] 0 – No EEPROM write cycle 1 – Start EEPROM write cycle (internal registers are saved to the EEPROM)
07h-0Fh		—	0h	Reserved – do not write other than 0

Table 10. PLL1 Configuration Register

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
10h	7:5	SSC1_7 [2:0]	000b	SSC1: PLL1 SSC selection (modulation amount). [4] **Down** **Center** 000 (Off) 000 (Off) 001 – 0.25% 001 ± 0.25% 010 – 0.5% 010 ± 0.5% 011 – 0.75% 011 ± 0.75% 100 – 1.0% 100 ± 1.0% 101 – 1.25% 101 ± 1.25% 110 – 1.5% 110 ± 1.5% 111 – 2.0% 111 ± 2.0%
	4:2	SSC1_6 [2:0]	000b	
	1:0	SSC1_5 [2:1]	000b	
11h	7	SSC1_5 [0]		
	6:4	SSC1_4 [2:0]	000b	
	3:1	SSC1_3 [2:0]	000b	
	0	SSC1_2 [2]	000b	
12h	7:6	SSC1_2 [1:0]		
	5:3	SSC1_1 [2:0]	000b	
	2:0	SSC1_0 [2:0]	000b	

(6) Selection of *control pins* is effective only if written into the EEPROM. Once written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA/SCL), and the two slave receiver address bits are reset to A0 = 0 and A1 = 0.
(7) These are the bits of the control terminal register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2.
(8) The internal load capacitor (C1, C2) must be used to achieve the best clock performance. External capacitors must be used only to finely adjust C_L by a few picofarads. The value of C_L can be programmed with a resolution of 1 pF for a crystal load range of 0 pF to 20 pF. For CL > 20 pF, use additional external capacitors. Also, the value of the device input capacitance has to be considered which always adds 1.5 pF (6 pF/2 pF) to the selected C_L. For more information about VCXO configuration and crystal recommendation, see *VCXO Application Guideline for CDCE(L)9xx Family* (SCAA085).
(9) Note: The EEPROM WRITE bit must be sent last. This ensures that the content of all internal registers are stored in the EEPROM. The EEWRITE cycle is initiated with the rising edge of the EEWRITE bit. A static level-high does not trigger an EEPROM WRITE cycle. The EEWRITE bit must be reset to low after the programming is completed. The programming status can be monitored by reading out EEPIP. If EELOCK is set to high, no EEPROM programming is possible.
(1) Writing data beyond 30h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Copyright © 2007–2016, Texas Instruments Incorporated

Table 10. PLL1 Configuration Register (continued)

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
13h	7	FS1_7	0b	FS1_x: PLL1 frequency selection[4] 0 – f_{VCO1_0} (predefined by PLL1_0 – multiplier/divider value) 1 – f_{VCO1_1} (predefined by PLL1_1 – multiplier/divider value)
	6	FS1_6	0b	
	5	FS1_5	0b	
	4	FS1_4	0b	
	3	FS1_3	0b	
	2	FS1_2	0b	
	1	FS1_1	0b	
	0	FS1_0	0b	
14h	7	MUX1	1b	PLL1 multiplexer: 0 – PLL1 1 – PLL1 bypass (PLL1 is in power down)
	6	M2	1b	Output Y2 multiplexer: 0 – Pdiv1 1 – Pdiv2
	5:4	M3	10b	Output Y3 multiplexer: 00 – Pdiv1-divider 01 – Pdiv2-divider 10 – Pdiv3-divider 11 – Reserved
	3:2	Y2Y3_ST1	11b	Y2, Y3-state0/1definition: 00 – Y2/Y3 disabled to high-impedance state (PLL1 is in power down) 01 – Y2/Y3 disabled to high-impedance state (PLL1 on) 10 – Y2/Y3 disabled to low (PLL1 on) 11 – Y2/Y3 enabled (normal operation, PLL1 on)
	1:0	Y2Y3_ST0	01b	
15h	7	Y2Y3_7	0b	Y2Y3_x output state selection[4] 0 – state0 (predefined by Y2Y3_ST0) 1 – state1 (predefined by Y2Y3_ST1)
	6	Y2Y3_6	0b	
	5	Y2Y3_5	0b	
	4	Y2Y3_4	0b	
	3	Y2Y3_3	0b	
	2	Y2Y3_2	0b	
	1	Y2Y3_1	1b	
	0	Y2Y3_0	0b	
16h	7	SSC1DC	0b	PLL1 SSC down/center selection: 0 – Down 1 – Center
	6:0	Pdiv2	01h	7-bit Y2-output-divider Pdiv2: 0 – Reset and in standby 1 to 127 – Divider value
17h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv3	01h	7-bit Y3-output-divider Pdiv3: 0 – Reset and in standby 1 to 127 – Divider value
18h	7:0	PLL1_0N [11:4	004h	PLL1_0[5]: 30-bit multiplier/divider value for frequency f_{VCO1_0} (for more information, see *PLL Multiplier/Divider Definition*).
19h	7:4	PLL1_0N [3:0]		
	3:0	PLL1_0R [8:5]	000h	
1Ah	7:3	PLL1_0R[4:0]		
	2:0	PLL1_0Q [5:3]	10h	
1Bh	7:5	PLL1_0Q [2:0]		
	4:2	PLL1_0P [2:0]	010b	
	1:0	VCO1_0_RANGE	00b	f_{VCO1_0} range selection: 00 – f_{VCO1_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_0} < 175 MHz 11 – f_{VCO1_0} ≥ 175 MHz

(5) PLL settings limits: $16 \le q \le 63$, $0 \le p \le 7$, $0 \le r \le 511$, $0 < N < 4096$

Copyright © 2007–2016, Texas Instruments Incorporated

Table 10. PLL1 Configuration Register (continued)

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
1Ch	7:0	PLL1_1N [11:4]	004h	PLL1_1[5]: 30-bit multiplier/divider value for frequency f_{VCO1_1} (for more information, see *PLL Multiplier/Divider Definition*).
1Dh	7:4	PLL1_1N [3:0]		
	3:0	PLL1_1R [8:5]	000h	
1Eh	7:3	PLL1_1R[4:0]		
	2:0	PLL1_1Q [5:3]	10h	
1Fh	7:5	PLL1_1Q [2:0]		
	4:2	PLL1_1P [2:0]	010b	
	1:0	VCO1_1_RANGE	00b	f_{VCO1_1} range selection: 00 – f_{VCO1_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_1} < 175 MHz 11 – f_{VCO1_1} ≥ 175 MHz

Table 11. PLL2 Configuration Register

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
20h	7:5	SSC2_7 [2:0]	000b	SSC2: PLL2 SSC selection (modulation amount). [4] **Down** / **Center** 000 (Off) / 000 (Off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC2_6 [2:0]	000b	
	1:0	SSC2_5 [2:1]	000b	
21h	7	SSC2_5 [0]		
	6:4	SSC2_4 [2:0]	000b	
	3:1	SSC2_3 [2:0]	000b	
	0	SSC2_2 [2]	000b	
22h	7:6	SSC2_2 [1:0]		
	5:3	SSC2_1 [2:0]	000b	
	2:0	SSC2_0 [2:0]	000b	
23h	7	FS2_7	0b	FS2_x: PLL2 frequency selection[4] 0 – f_{VCO2_0} (predefined by PLL2_0 – multiplier/divider value) 1 – f_{VCO2_1} (predefined by PLL2_1 – multiplier/divider value)
	6	FS2_6	0b	
	5	FS2_5	0b	
	4	FS2_4	0b	
	3	FS2_3	0b	
	2	FS2_2	0b	
	1	FS2_1	0b	
	0	FS2_0	0b	
24h	7	MUX2	1b	PLL2 multiplexer: 0 – PLL2 1 – PLL2 bypass (PLL2 is in power down)
	6	M4	1b	Output Y4 multiplexer: 0 – Pdiv2 1 – Pdiv4
	5:4	M5	10b	Output Y5 multiplexer: 00 – Pdiv2-divider 01 – Pdiv4-divider 10 – Pdiv5-divider 11 – Reserved
	3:2	Y4Y5_ST1	11b	Y4, Y5-State0/1definition: 00 – Y4/Y5 disabled to high-impedance state (PLL2 is in power down) 01 – Y4/Y5 disabled to high-impedance state (PLL2 on) 10–Y4/Y5 disabled to low (PLL2 on) 11 – Y4/Y5 enabled (normal operation, PLL2 on)
	1:0	Y4Y5_ST0	01b	

(1) Writing data beyond 30h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

 Copyright © 2007–2016, Texas Instruments Incorporated

Table 11. PLL2 Configuration Register (continued)

OFFSET[(1)]	BIT[(2)]	ACRONYM	DEFAULT[(3)]	DESCRIPTION
25h	7	Y4Y5_7	0b	Y4Y5_x output state selection[(4)] 0 – state0 (predefined by Y4Y5_ST0) 1 – state1 (predefined by Y4Y5_ST1)
	6	Y4Y5_6	0b	
	5	Y4Y5_5	0b	
	4	Y4Y5_4	0b	
	3	Y4Y5_3	0b	
	2	Y4Y5_2	0b	
	1	Y4Y5_1	1b	
	0	Y4Y5_0	0b	
26h	7	SSC2DC	0b	PLL2 SSC down/center selection: 0 – Down 1 – Center
	6:0	Pdiv4	01h	7-Bit Y4-output-divider Pdiv4: 0 – Reset and in standby 1 to 127 – Divider value
27h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv5	01h	7-bit Y5-output-divider Pdiv5: 0 – Reset and in standby 1 to 127 – Divider value
28h	7:0	PLL2_0N [11:4	004h	PLL2_0[(5)]: 30-Bit Multiplier/Divider value for frequency f_{VCO2_0} (for more information, see *PLL Multiplier/Divider Definition*).
29h	7:4	PLL2_0N [3:0]		
	3:0	PLL2_0R [8:5]	000h	
2Ah	7:3	PLL2_0R[4:0]		
	2:0	PLL2_0Q [5:3]	10h	
2Bh	7:5	PLL2_0Q [2:0]		
	4:2	PLL2_0P [2:0]	010b	
	1:0	VCO2_0_RANGE	00b	f_{VCO2_0} range selection: 00 – f_{VCO2_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO2_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO2_0} < 175 MHz 11 – f_{VCO2_0} ≥ 175 MHz
2Ch	7:0	PLL2_1N [11:4]	004h	PLL2_1[(5)]: 30-bit multiplier/divider value for frequency f_{VCO2_1} (for more information, see *PLL Multiplier/Divider Definition*).
2Dh	7:4	PLL2_1N [3:0]		
	3:0	PLL2_1R [8:5]	000h	
2Eh	7:3	PLL2_1R[4:0]		
	2:0	PLL2_1Q [5:3]	10h	
2Fh	7:5	PLL2_1Q [2:0]		
	4:2	PLL2_1P [2:0]	010b	
	1:0	VCO2_1_RANGE	00b	f_{VCO2_1} range selection: 00 – f_{VCO2_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO2_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO2_1} < 175 MHz 11 – f_{VCO2_1} ≥ 175 MHz

(5) PLL settings limits: $16 \le q \le 63$, $0 \le p \le 7$, $0 \le r \le 511$, $0 < N < 4096$

Copyright © 2007–2016, Texas Instruments Incorporated

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The CDCEx925 device is an easy-to-use high-performance, programmable CMOS clock synthesizer. it can be used as a crystal buffer, clock synthesizer with separate output supply pin. The CDCEx925 features an on-chip loop filter and Spread-spectrum modulation. Programming can be done through SPI, pin-mode, or using on-chip EEPROM. This section shows some examples of using CDCEx925 in various applications.

10.2 Typical Application

Figure 15 shows the use of the CDCEx925 devices for replacement of crystals and crystal oscillators on a Gigabit Ethernet Switch application.

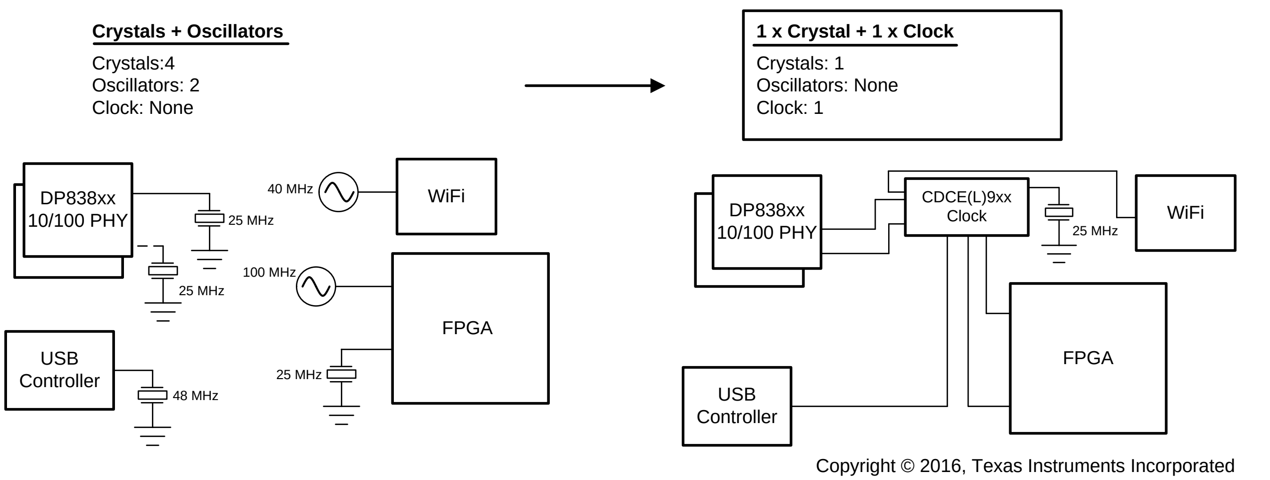


Figure 15. Crystal and Oscillator Replacement Example

10.2.1 Design Requirements

CDCEx925 supports spread spectrum clocking (SSC) with multiple control parameters:

- Modulation amount (%)
- Modulation frequency (>20 kHz)
- Modulation shape (triangular)
- Center spread / down spread (± or –)

Copyright © 2007–2016, Texas Instruments Incorporated

Typical Application (continued)

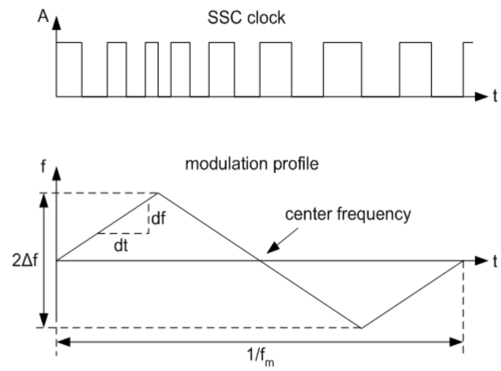
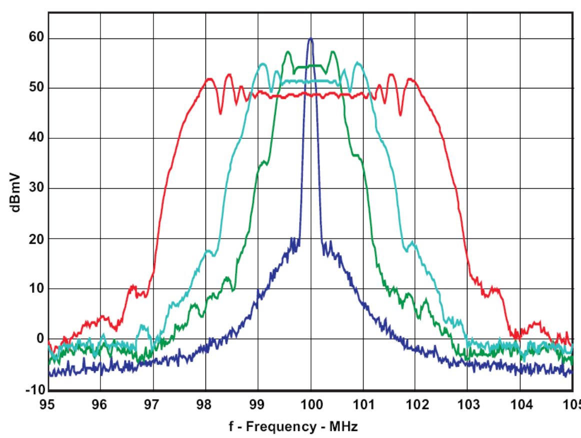


Figure 16. Modulation Frequency (fm) and Modulation Amount

10.2.2 Detailed Design Procedure

10.2.2.1 Spread Spectrum Clock (SSC)

Spread spectrum modulation is a method to spread emitted energy over a larger bandwidth. In clocking, spread spectrum can reduce Electromagnetic Interference (EMI) by reducing the level of emission from clock distribution network.



CDCS502 with a 25-MHz Crystal, FS = 1, f_{OUT} = 100 MHz, and 0%, ±0.5, ±1%, and ±2% SSC

Figure 17. Comparison Between Typical Clock Power Spectrum and Spread-Spectrum Clock

10.2.2.2 PLL Multiplier/Divider Definition

At a given input frequency (f_{IN}), the output frequency (f_{OUT}) of the CDCEx925 is calculated with Equation 1.

$$f_{OUT} = \frac{f_{IN}}{Pdiv} \times \frac{N}{M}$$

where

- M (1 to 511) and N (1 to 4095) are the multiplier/divide values of the PLL
- Pdiv (1 to 127) is the output divider (1)

The target VCO frequency (f_{VCO}) of each PLL is calculated with Equation 2.

$$f_{VCO} = f_{IN} \times \frac{N}{M} \quad (2)$$

Typical Application (continued)

The PLL internally operates as fractional divider and needs the following multiplier/divider settings:

$$NP = 4 - \text{int}\left(\log_2 \frac{N}{M}\right)\left[\textit{if } P < 0 \textit{ then } P = 0\right] \quad Q = \textit{int}\left(\frac{N'}{M}\right) \quad R = N' - M \times Q$$

where

- $N' = N \times 2^P$
- $N \geq M$
- $80\ \text{MHz} \leq f_{VCO} \leq 230\ \text{MHz}$
- $16 \leq q \leq 63$
- $0 \leq p \leq 4$
- $0 \leq r \leq 511$ (3)

Example:

for f_{IN} = 27 MHz; M = 1; N = 4; Pdiv = 2;

→ f_{OUT} = 54 MHz

→ f_{VCO} = 108 MHz

→ P = 4 – int($\log_2 4$) = 4 – 2 = 2

→ N" = 4 × 2^2 = 16

→ Q = int(16) = 16

→ R = 16 – 16 = 0

for f_{IN} = 27 MHz; M = 2; N = 11; Pdiv = 2;

→ f_{OUT} = 74.25 MHz

→ f_{VCO} = 148.50 MHz

→ P = 4 – int($\log_2 5.5$) = 4 – 2 = 2

→ N" = 11 × 2^2 = 44

→ Q = int(22) = 22

→ R = 44 – 44 = 0

The values for P, Q, R, and N' are automatically calculated when using TI Pro-Clock™ software.

10.2.2.3 Crystal Oscillator Start-Up

When the CDCEx925 is used as a crystal buffer, crystal oscillator start-up dominates the start-up time compared to the internal PLL lock time. The following diagram shows the oscillator start-up sequence for a 27-MHz crystal input with an 8-pF load. The start-up time for the crystal is in the order of approximately 250 µs compared to approximately 10 µs of lock time. In general, lock time is an order of magnitude less compared to the crystal start-up time.

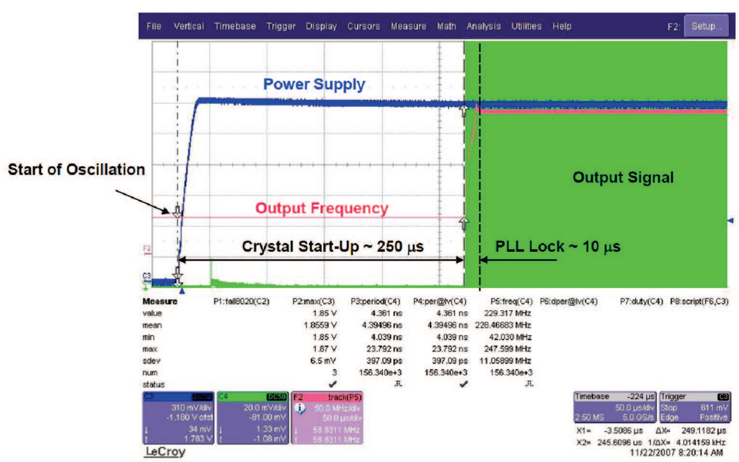


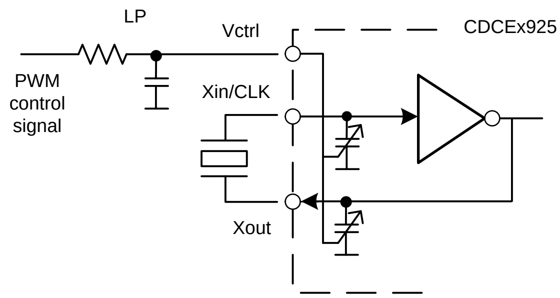
Figure 18. Crystal Oscillator Start-Up vs PLL Lock Time

10.2.2.4 Frequency Adjustment With Crystal Oscillator Pulling

The frequency for the CDCEx925 is adjusted for media and other applications with the VCXO control input V_{Ctrl}. If a PWM modulated signal is used as a control signal for the VCXO, an external filter is needed.

Copyright © 2007–2016, Texas Instruments Incorporated

Typical Application (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 19. Frequency Adjustment Using PWM Input to the VCXO Control

10.2.2.5 Unused Inputs and Outputs

If VCXO pulling functionality is not required, V_{Ctrl} should be left floating. All other unused inputs should be set to GND. Unused outputs should be left floating.

If one output block is not used, TI recommends disabling it. However, TI always recommends providing the supply for the second output block even if it is disabled.

10.2.2.6 Switching Between XO and VCXO Mode

When the CDCEx925 is in crystal oscillator or in VCXO configuration, the internal capacitors require different internal capacitance. The following steps are recommended to switch to VCXO mode when the configuration for the on-chip capacitor is still set for XO mode. To center the output frequency to 0 ppm:

1. While in XO mode, put Vctrl = Vdd/2
2. Switch from X0 mode to VCXO mode
3. Program the internal capacitors to obtain 0 ppm at the output.

10.2.3 Application Curves

Figure 20, Figure 21, Figure 22, and Figure 23 show CDCEx925 measurements with the SSC feature enabled. Device configuration: 27-MHz input, 27-MHz output.

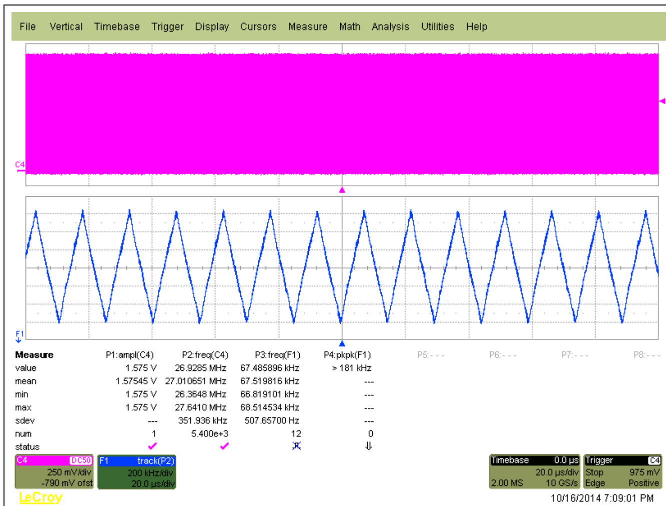


Figure 20. f_{OUT} = 27 MHz, VCO Frequency < 125 MHz, SSC (2% Center)

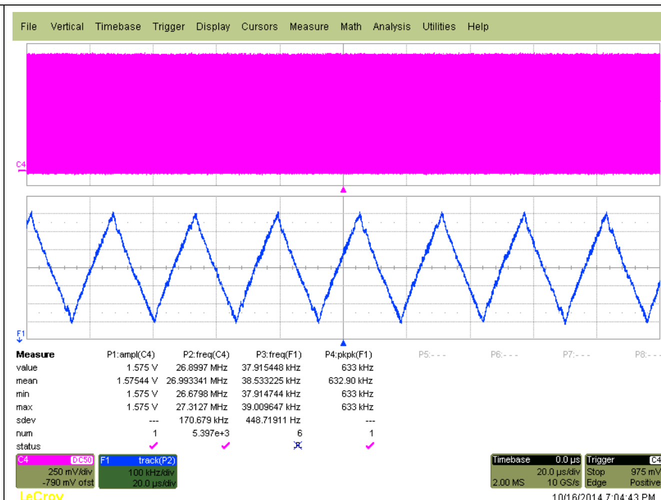


Figure 21. f_{OUT} = 27 MHz, VCO Frequency > 175 MHz, SSC (1%, Center)

Copyright © 2007–2016, Texas Instruments Incorporated

Typical Application (continued)

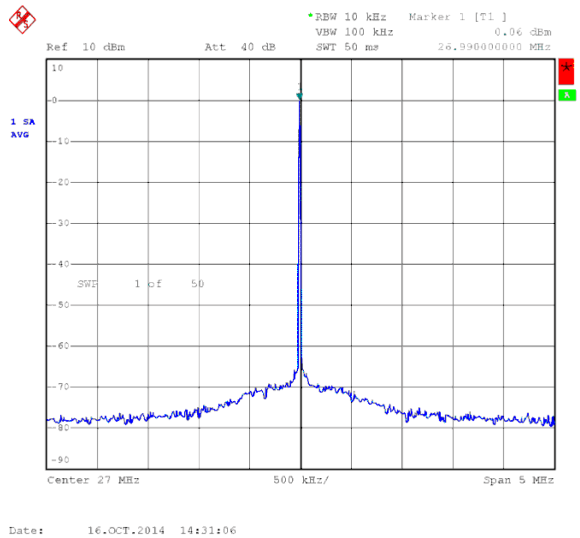


Figure 22. Output Spectrum With SSC Off

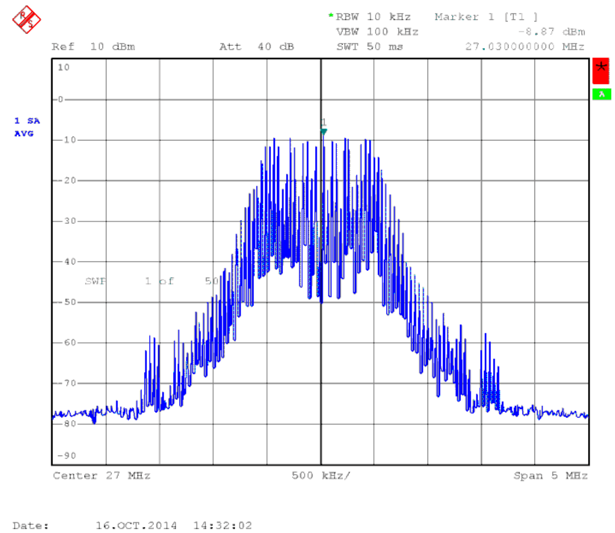


Figure 23. Output Spectrum With SSC On, 2% Center

11 Power Supply Recommendations

There is no restriction on the power-up sequence. In case the V_{DDOUT} is applied first, TI recommends grounding V_{DD}. In case the V_{DDOUT} is powered while V_{DD} is floating, there is a risk of high current flowing on the V_{DDOUT}.

The device has a power-up control that is connected to the 1.8-V supply. This keeps the whole device disabled until the 1.8-V supply reaches a sufficient voltage level. Then the device switches on all internal components, including the outputs. If there is a 3.3-V V_{DDOUT} available before the 1.8-V, the outputs stay disabled until the 1.8-V supply reaches a certain level.

12 Layout

12.1 Layout Guidelines

When the CDCEx937 is used as a crystal buffer, any parasitics across the crystal affects the pulling range of the VCXO. Therefore, take care in placing the crystal units on the board. Crystals must be placed as close to the device as possible, ensuring that the routing lines from the crystal terminals to XIN and XOUT have the same length.

If possible, cut out both ground plane and power plane under the area where the crystal and the routing to the device are placed. In this area, always avoid routing any other signal line, as it could be a source of noise coupling.

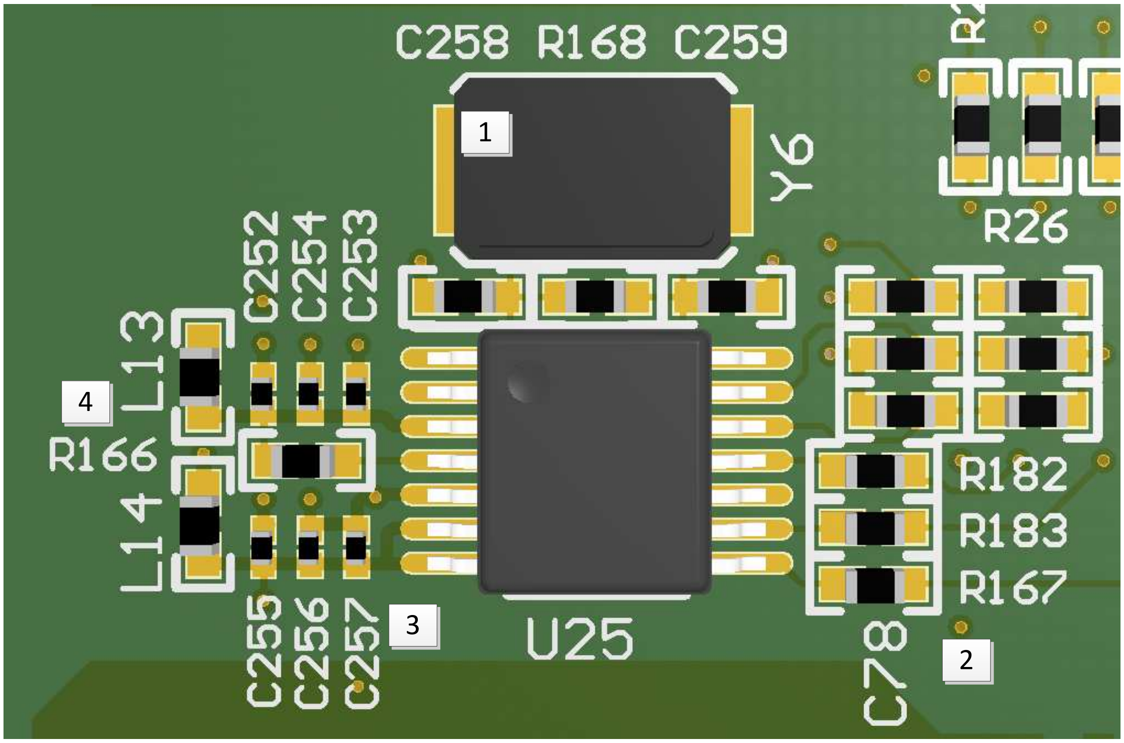
Additional discrete capacitors can be required to meet the load capacitance specification of certain crystal. For example, a 10.7-pF load capacitor is not fully programmable on the chip, because the internal capacitor can range from 0 pF to 20 pF with steps of 1 pF. The 0.7-pF capacitor therefore can be discretely added on top of an internal 10-pF capacitor.

To minimize the inductive influence of the trace, TI recommends placing this small capacitor as close to the device as possible and symmetrically with respect to XIN and XOUT.

Figure 24 shows a conceptual layout detailing recommended placement of power supply bypass capacitors on the basis of CDCEx937. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

Copyright © 2007–2016, Texas Instruments Incorporated

12.2 Layout Example



1 — Place crystal with associated load caps as close to the chip

2 — Place series termination resistors at Clock outputs to improve signal integrity

3 — Place bypass caps close to the device pins, ensure wide freq. range

4 — Use ferrite beads to isolate the device supply pins from board noise sources

Figure 24. Annotated Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.1.2 Development Support

For development support see the following:

- SMBus
- I^2C Bus

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

VCXO Application Guideline for CDCE(L)9xx Family (SCAA085)

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CDCE925	Click here	Click here	Click here	Click here	Click here
CDCEL925	Click here	Click here	Click here	Click here	Click here

13.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.6 Trademarks

TI-DaVinci, OMAP, TI Pro-Clock, Pro-Clock, E2E are trademarks of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
Ethernet is a trademark of Xerox Corporation.
All other trademarks are the property of their respective owners.

Copyright © 2007–2016, Texas Instruments Incorporated

13.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCE925PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE925	Samples
CDCE925PWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE925	Samples
CDCE925PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE925	Samples
CDCE925PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE925	Samples
CDCEL925PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL925	Samples
CDCEL925PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL925	Samples
CDCEL925PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL925	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

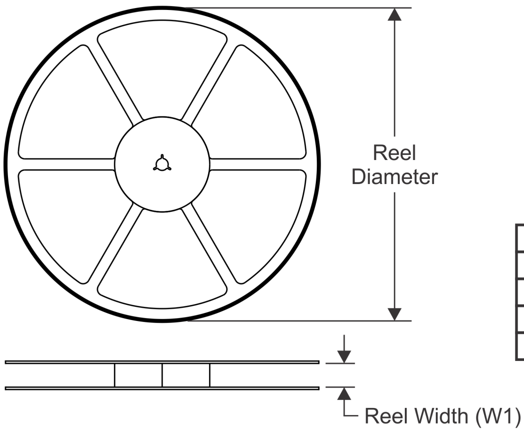
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

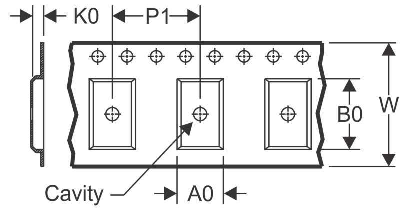
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

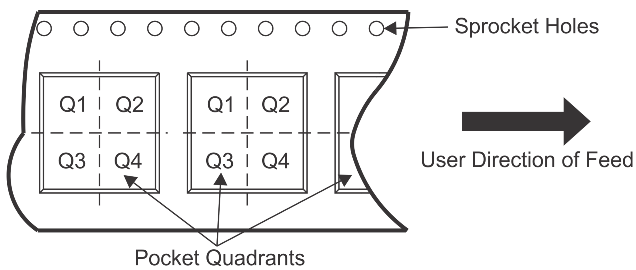


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

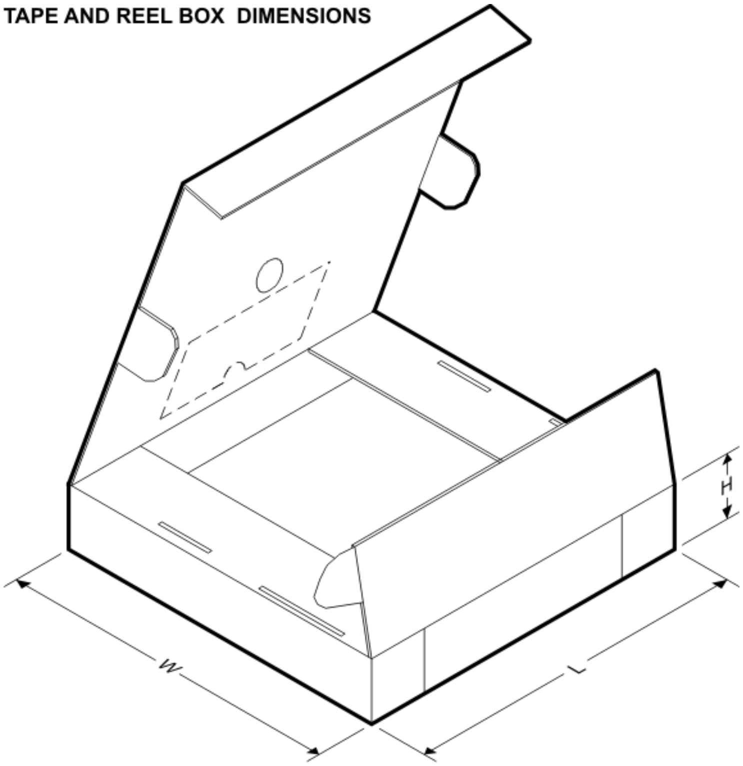
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

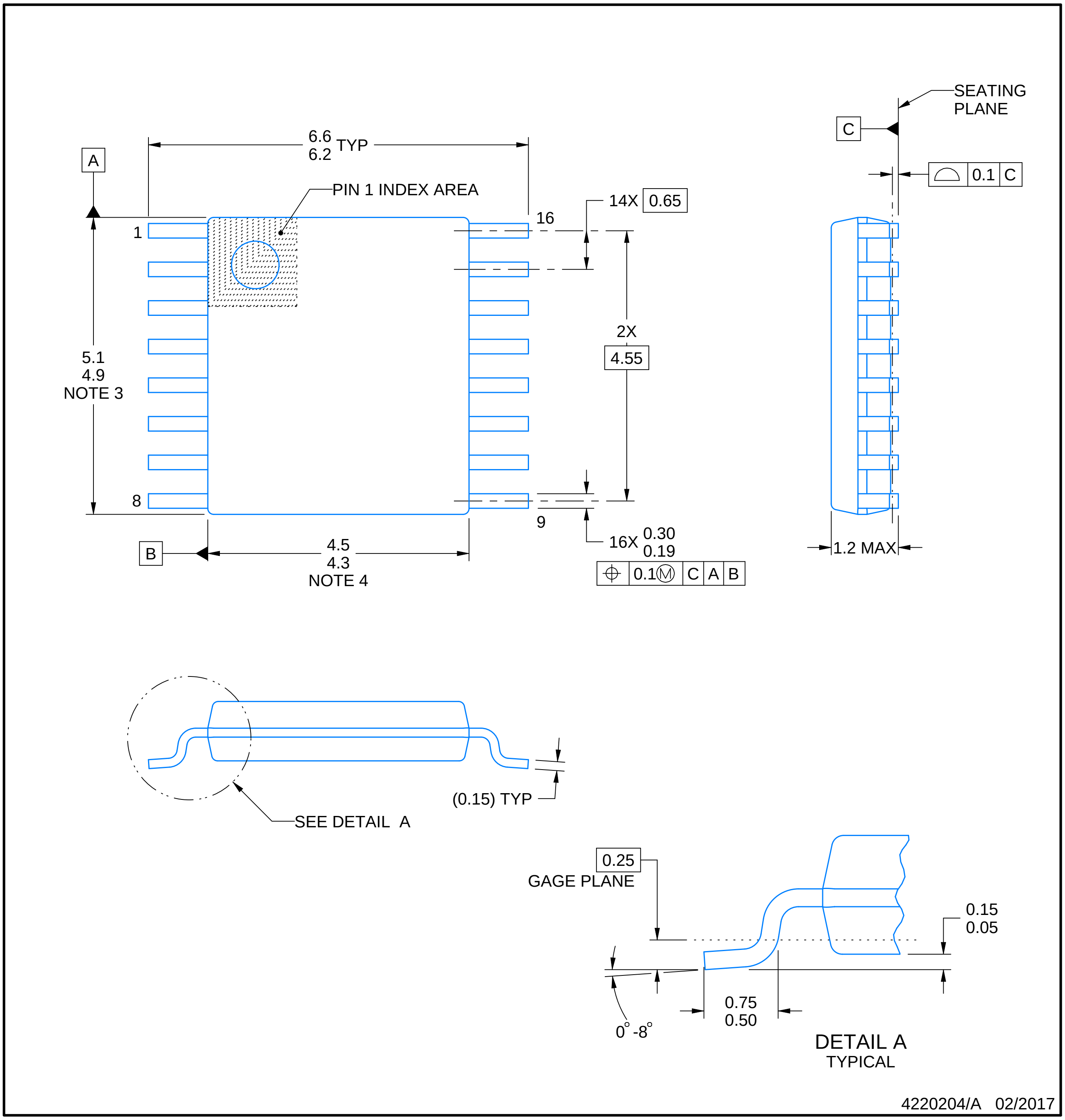
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE925PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCEL925PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



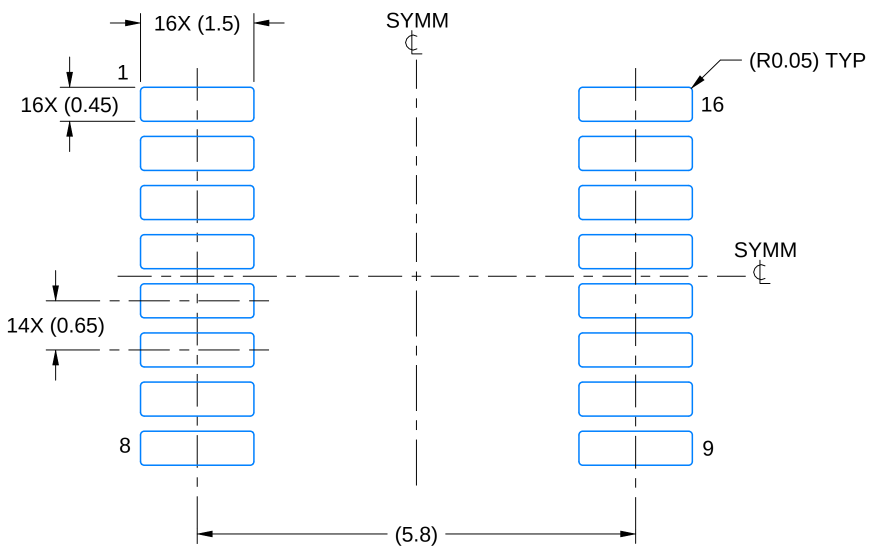
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE925PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
CDCEL925PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

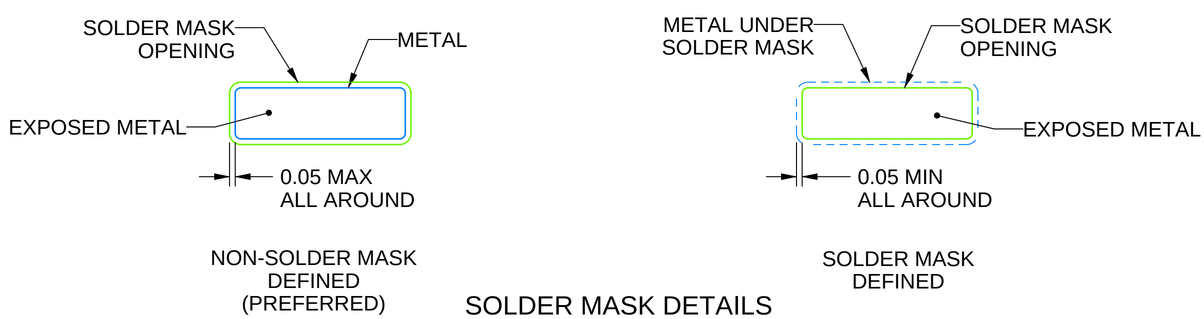


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

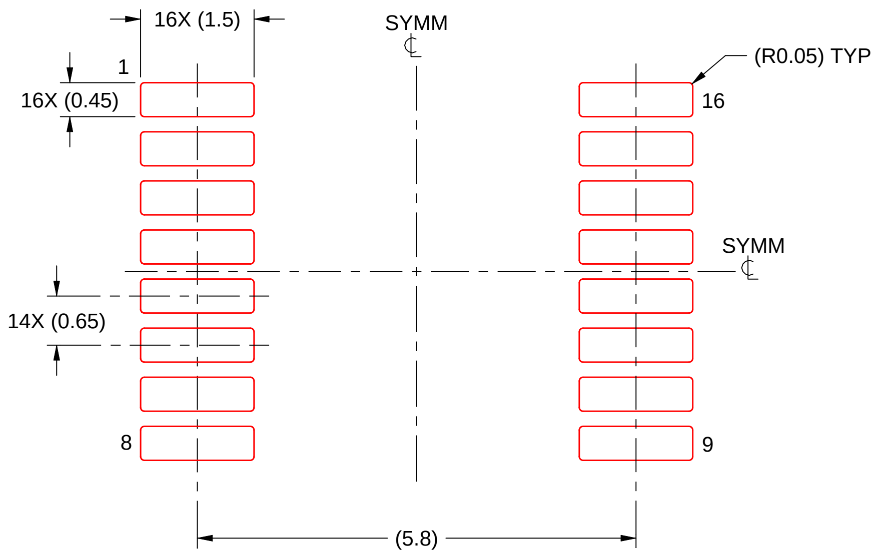


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated