Inverter for motor control

600V IGBT Intelligent Power Module (IPM)

BM64375S-VA

General Description

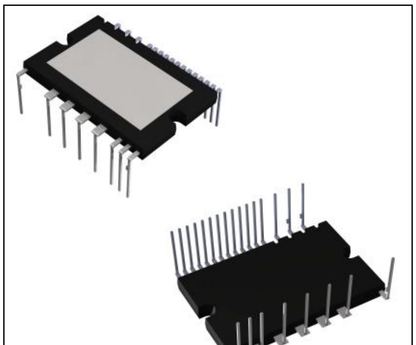
BM64375S-VA is an Intelligent Power Module composed of gate drivers, bootstrap diodes, IGBTs, fly wheel diodes.

Key Specifications

- IGBT Collector-Emitter Voltage V_{CESAT}: 1.7V(Typ)
- FWD Forward Voltage V_F: 1.65V(Typ)
- FWD Reverse Recovery Time t_{rr}: 100ns(Typ)
- Module Case Temperature T_C: -25 to +115°C
- Junction Temperature T_{jmax}: 150°C

Package

Package	W(Typ) x D(Typ) x H(Typ)
HSDIP25	38.0mm x 24.0mm x 3.5mm



HSDIP25

Features

- 3phase DC/AC Inverter
- 600V/20A
- Low Side IGBT Open Emitter
- Built -in Bootstrap Diode
- High Side IGBT Gate Driver(HVIC):
  SOI (Silicon On Insulator) Process,
  Drive Circuit, High Voltage Level Shifting,
  Current Limit for Bootstrap Diode,
  Control Supply Under-Voltage Locked Out (UVLO)
- Low Side IGBT Gate Driver(LVIC):
  Drive Circuit, Short Circuit Current Protection (SCP),
  Control Supply Under Voltage Locked Out (UVLO),
  Thermal Shutdown (TSD),
  Temperature Output by Analog Signal (VOT)
- Fault Signal(LVIC)
  Corresponding to SCP (Low Side IGBT), TSD, UVLO Fault
- Input Interface 3.3V, 5V Line
- UL Recognized: UL1557 File E468261

Application

- AC100 to 240Vrms(DC Voltage: Less Than 400V) Class Motor Control
- Compressor Motor Control for Air Conditioner, Washing Machine, Refrigerator

Typical Application Circuit

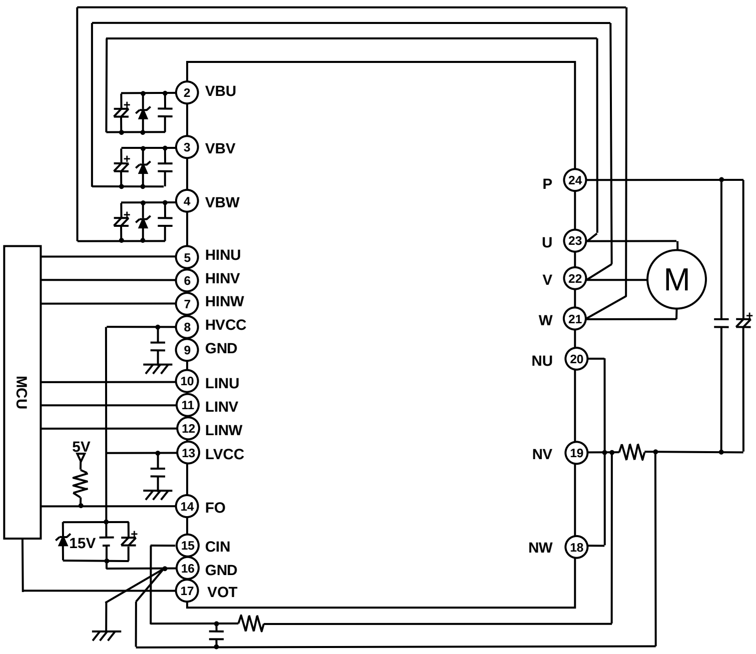


Figure 1. Example of Application Circuit

○Product structure: Semiconductor IC ○This product is not designed for protection against radioactive rays

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Pin Configuration

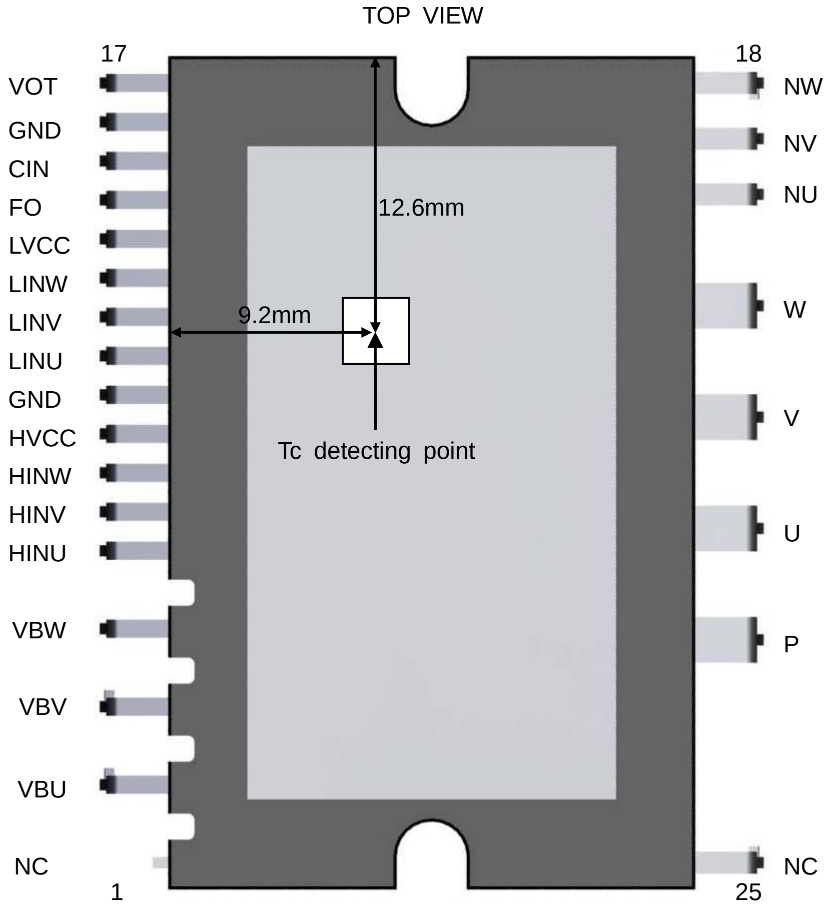

Figure 2. Pin Configuration and Tc Detecting Point

Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	NC	No connection(GND potential)	14	FO	Alarm output
2	VBU	U phase floating control supply	15	CIN	Detecting of short circuit current trip voltage
3	VBV	V phase floating control supply	16	GND	Ground (Note 1)
4	VBW	W phase floating control supply	17	VOT	Temperature output
5	HINU	U phase high side IGBT control	18	NW	W phase low side IGBT emitter
6	HINV	V phase high side IGBT control	19	NV	V phase low side IGBT emitter
7	HINW	W phase high side IGBT control	20	NU	U phase low side IGBT emitter
8	HVCC	Control supply for HVIC	21	W	W phase output
9	GND	Ground (Note 1)	22	V	V phase output
10	LINU	U phase low side IGBT control	23	U	U phase output
11	LINV	V phase low side IGBT control	24	P	Inverter supply
12	LINW	W phase low side IGBT control	25	NC	No connection (Note 2)
13	LVCC	Control supply for LVIC			

(Note 1) Two GND pins (9 & 16pin) are connected inside IPM, please connect one pin (16pin is recommended) to the 15V power supply GND outside and leave the other open.
(Note 2) NC pin (25pin) is not electrically connected to any other potential inside.

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Block Diagram

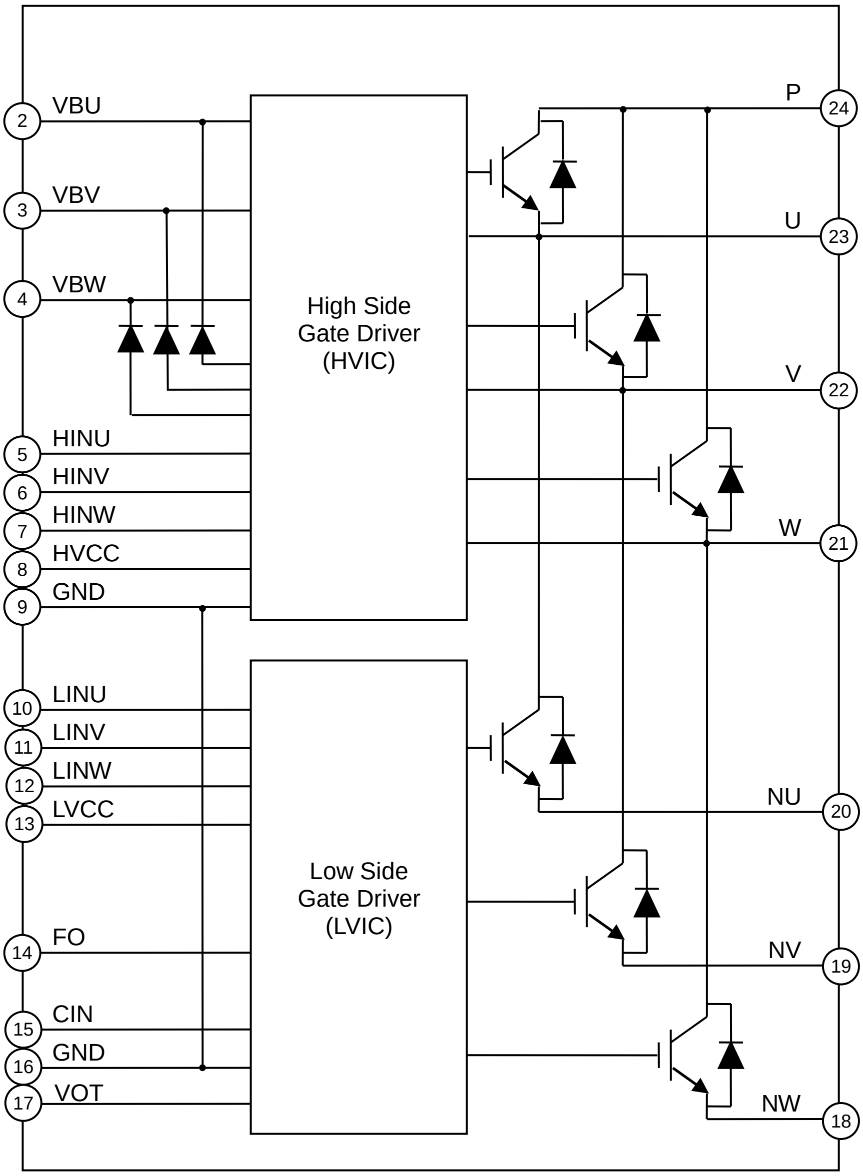

Figure 3. Block Diagram

Description of Block

1) High Side IGBT Drive (HVIC, Bootstrap Diode)
   High voltage level shifting circuit drives high side IGBT.
   Built-in bootstrap diode and current limit function for bootstrap diode enable HVIC to drive high side IGBT without external component (bootstrap diode, resistor). There is under-voltage-locked-out (UVLO) function for floating control power supply.

2) Low Side IGBT Drive (LVIC)
   LVIC drives low side IGBT.
   There is short circuit current protection (SCP), under-voltage locked out (UVLO) for control power supply LVCC, thermal shutdown (TSD) function. Alarm signal (FO) will output when these protection circuits work.
   LVIC detects temperature of itself, transform temperature into analog voltage, and output voltage to VOT pin.

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Absolute Maximum Ratings (Unless otherwise specified, Tj=25°C)

Inverter Part

Item		Symbol	Ratings	Unit	Conditions
Supply Voltage		V_P	450	V	Applied between P-NU,NV,NW
Supply Voltage(Surge)		$V_{P(surge)}$	500	V	Applied between P-NU,NV,NW
Collector-Emitter Voltage		V_{CES}	600	V	
Collector Current	DC	I_C	±20 (Note 1)	A	T_C=25°C
	PEAK	I_{CP}	±40 (Note 1)	A	T_C=25°C, less than 1ms
Collector Power Dissipation		P_C	41	W	T_C=25°C, per 1 chip
Junction Temperature		T_{jmax}	150	°C	

(Note 1) Do not, however exceed P_C, ASO.

Control part

Item	Symbol	Ratings	Unit	Conditions
Control Power Supply	V_{CC}	20	V	Applied between HVCC-GND, LVCC-GND
Floating Control Power Supply	V_{BS}	20	V	Applied between VBU-U, VBV-V, VBW-W
Control Input Voltage	V_{IN}	-0.5 to V_{CC} +0.5	V	Applied between HINX, LINX-GND (X=U,V,W)
Fault Output Supply Voltage	V_{FO}	-0.5 to V_{CC} +0.5	V	Applied between FO-GND
Fault Output Current	I_{FO}	1	mA	Sink current at FO pin
Current Sensing Input Voltage	V_{CIN}	-0.5 to +7.0	V	Applied between CIN-GND
Temperature Output Voltage	V_{OT}	-0.5 to +7.0	V	Applied between VOT-GND

Bootstrap diode part

Item	Symbol	Ratings	Unit	Conditions
Reverse Voltage	V_{RB}	600	V	
Junction Temperature	T_{jmaxD}	150	°C	

Total system

Item	Symbol	Ratings	Unit	Conditions
Self Protection Supply Voltage (SCP Capability)	$V_{P(PROT)}$	400	V	V_{CC}=13.5 to 16.5V, Inverter part T_j=125°C, non-repetitive, less than 2µs
Module Case Temperature	T_C	-25 to +115	°C	Measurement point of T_C is provided in Figure 2
Storage Temperature	T_{stg}	-40 to +125	°C	
Isolation Voltage	V_{iso}	1500	V_{rms}	Sinusoidal, 60Hz, AC 1min, between connected all pins and heat sink plate

Thermal resistance

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Junction to Case Thermal Resistance (Note 2)	$R_{th(j-c)\_IGBT}$	-	-	3.0	°C /W	Inverter IGBT(1/6 module)
	$R_{th(j-c)\_FWD}$	-	-	3.9	°C /W	Inverter FWD(1/6 module)

(Note 2) Grease with good conductivity and high reliability should be applied evenly with +100 to +200µm on the contacting surface of IPM and heat sink. Use a torque wrench to fasten up to the specified torque rating. The contacting thermal resistance between IPM case and heat sink is determined by the thickness and the thermal conductivity of the applied grease.

Caution: Operating the IPM over the absolute maximum ratings may damage the IPM. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IPM is operated over the absolute maximum ratings.

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Recommended Operating Conditions

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply Voltage	V_P	0	300	400	V	Applied between P-NU,NV,NW
Control Power Supply	V_{CC}	13.5	15.0	16.5	V	Applied between HVCC-GND, LVCC-GND
Floating Control Power Supply	V_{BS}	13.0	15.0	18.5	V	Applied between VBU-U, VBV-V, VBW-W
Control Power Supply Variation	ΔV_{CC} ΔV_{BS}	-1	-	+1	V/µs	
Control Input Voltage	V_{IN}	0	-	5.5	V	
Current Sensing Input Voltage	V_{CIN}	0	-	5.5	V	
Blanking Time for Preventing Arm-short	t_{dead}	1.0	-	-	µs	For each input signal
PWM Input Frequency	f_{PWM}	-	-	20	kHz	$T_C \leq 100°C$, $T_j \leq 125°C$
High Side IGBT Minimum Input Pulse Width(Note1)	PW_{ONH}	0.8	-	-	µs	
	PW_{OFFH}	0.8	-	-	µs	
Low Side IGBT Minimum Input Pulse Width(Note1)	PW_{ONL}	0.8	-	-	µs	
	PW_{OFFL}	0.8	-	-	µs	
Voltage Variation Between GND- NU, NV, NW	V_N	-5	-	+5	V	Between GND-NU, NV, NW (Including surge voltage)
Junction Temperature	T_j	-25	-	+125	°C	

(Note 1) IPM might not respond if the input signal pulse width is less than PW_{ON}, PW_{OFF}.

Electrical Characteristics (Unless otherwise specified, Tj=25°C, V_{CC}=V_{BS}=15V, V_P=300V)

Inverter Part

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Collector-Emitter Saturation Voltage	V_{CESAT}	-	1.70	2.15	V	I_C=20A
		-	0.90	1.20	V	I_C=2A
Collector-Emitter Cut-off Current	I_{CES}	-	-	100	µA	V_{CE}=V_{CES}
FWD Forward Voltage	V_F	-	1.65	2.15	V	I_F=20A
FWD Reverse Recovery Time	t_{rr}	-	100	-	ns	Inductive Load, I_C=20A
High Side IGBT Turn on Delay Time	t_{onH}	0.75	1.25	1.85	µs	Inductive Load, I_C=20A
High Side IGBT Turn on Switching Time	$t_{c(on)H}$	-	0.35	-	µs	Inductive Load, I_C=20A
High Side IGBT Turn off Delay Time	t_{offH}	-	1.10	1.70	µs	Inductive Load, I_C=20A
High Side IGBT Turn off Switching Time	$t_{c(off)H}$	-	0.15	-	µs	Inductive Load, I_C=20A
Low Side IGBT Turn on Delay Time	t_{onL}	0.75	1.25	1.85	µs	Inductive Load, I_C=20A
Low Side IGBT Turn on Switching Time	$t_{c(on)L}$	-	0.40	-	µs	Inductive Load, I_C=20A
Low Side IGBT Turn off Delay Time	t_{offL}	-	1.40	2.00	µs	Inductive Load, I_C=20A
Low Side IGBT Turn off Switching Time	$t_{c(off)L}$	-	0.15	-	µs	Inductive Load, I_C=20A

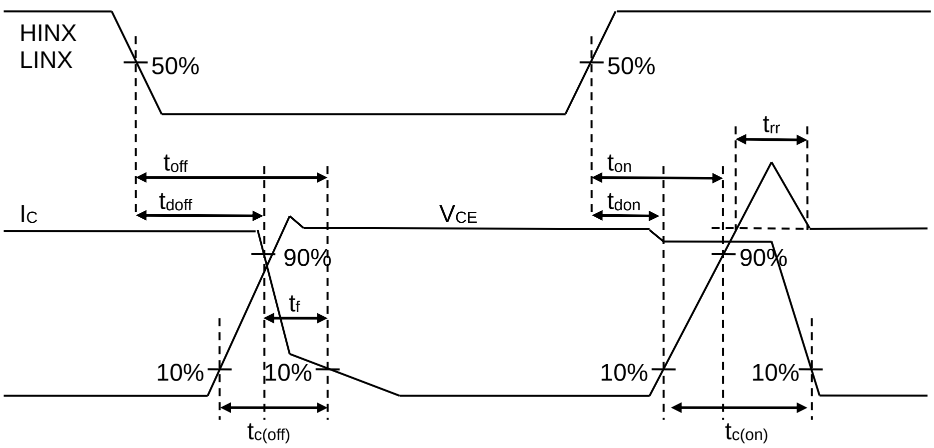

Figure 4. Switching Time Definition

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Control part

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Whole						
VCC Circuit Current 1	I_{CC1}	-	1.20	2.40	mA	V_{IN}=0V
VCC Circuit Current 2	I_{CC2}	-	1.40	2.80	mA	V_{IN}=5V
VBS Circuit Current 1	I_{BS1}	-	0.06	0.15	mA	V_{IN}=0V
VBS Circuit Current 2	I_{BS2}	-	0.06	0.15	mA	V_{IN}=5V
Control Input(HINU,HINV,HINW,LINU,LINV,LINW)						
H Level Input Current	I_{INH}	0.7	1.0	1.5	mA	V_{IN}=5V
L Level Input Current	I_{INL}	-10	-	-	µA	V_{IN}=0V
H Level Input Threshold Voltage	V_{INH}	-	-	2.6	V	
L Level Input Threshold Voltage	V_{INL}	0.8	-	-	V	
Input Hysteresis Voltage	V_{HYS}	-	0.25	-	V	
HINU-GND Resistance (Note 1)	R_{HINU}	35	50	68	kΩ	HVCC=0V, I_{HINU}=2µA
HINV-GND Resistance (Note 1)	R_{HINV}	70	100	136	kΩ	HVCC=0V, I_{HINV}=2µA
HINW-GND Resistance (Note 1)	R_{HINW}	70	100	136	kΩ	HVCC=0V, I_{HINW}=2µA
Short Circuit Current Protection(SCP)						
CIN Input Bias Current	I_{CIN}	-2	-	-	µA	CIN=0V
Trip Voltage	V_{SC}	0.455	0.480	0.505	V	
Under Voltage Locked Out(UVLO)						
VCC Trip Voltage	V_{CCUVT}	10.5	11.5	12.5	V	
VCC Release Voltage	V_{CCUVR}	11	12	13	V	
VBS Trip Voltage	V_{BSUVT}	10	11	12	V	
VBS Release Voltage	V_{BSUVR}	10.5	11.5	12.5	V	
Thermal Shutdown(TSD)						
Trip Temperature	T_{SDT}	115	130	-	°C	Monitor LVIC temperature
Hysteresis Temperature	T_{SDHYS}	-	20	-	°C	Monitor LVIC temperature
Temperature Output(VOT)						
VOT Voltage	V_{OT}	2.72	2.77	2.82	V	LVIC temperature = 90°C
		0.93	1.13	1.33	V	LVIC temperature = 25°C
Fault Output(FO)						
Output low Voltage	V_{FO}	-	-	0.95	V	I_{FO}=1mA
Leak Current	I_{FOLEAK}	-	-	10	µA	V_{FO}=5V
Output Pulse Width (Note 2)	t_{FOSC}	45	-	-	µs	During SCP Operation
	t_{FOUV}	90	-	-	µs	During VCC UVLO Operation
	t_{FOTSD}	180	-	-	µs	During TSD Operation

(Note 1) Resistance value when current from the control input pin is flowing through the internal resistor to GND.
(Note 2) FO pulse width for each protection mode is different. FO will continue to output until recovering from the error condition if the time of error condition exceeds the determined output pulse width depending on the protection mode.

Bootstrap Diode Part

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Forward Voltage	V_{FB1}	0.3	0.6	0.9	V	I_{FB}=1mA Voltage drop between HVCC-VBX (X=U,V,W)
	V_{FB2}	1.1	2.0	2.9	V	I_{FB}=100mA Voltage drop between HVCC-VBX (X=U,V,W)
Reverse Current	I_{RB}	-	-	10	µA	V_{RB}=600V
Reverse Recovery Time	t_{rrB}	-	80	-	ns	I_{FB}=0.1A

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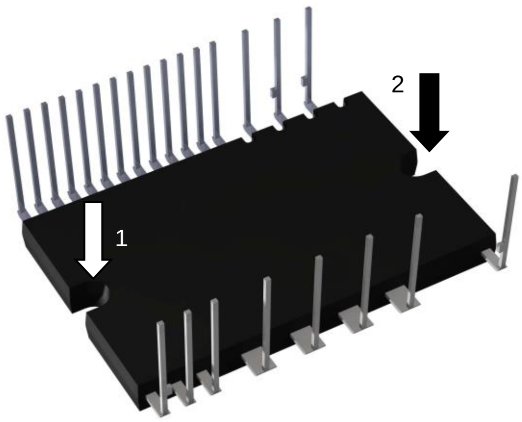
Mechanical Characteristics And Ratings

Item	Limit			Unit	Following Standard	Conditions
	Min	Typ	Max			
Mounting Torque	0.59	0.69	0.78	N･m	-	Mounting Screw M3 (Note 1) Recommended 0.69N･m (Note 2)
Pin Pulling Strength	10	-	-	s	EIAJ-ED-4701/400	Load Control Pin:4.9N Power Pin:9.8N
Pin Bending Strength	2	-	-	times	EIAJ-ED-4701/400	Load Control Pin: 2.45N Power Pin:4.9N 90deg. Bend
Weight	-	10	-	g	-	
Heat Sink Flatness	0	-	+200	µm	-	Measurement point is provided in Figure 6-1.

(Note 1) Plain washers of 8mm outside diameter (ISO 7089 to 7094) are recommended.

(Note 2) When installing a module to a heat sink, excessive uneven fastening force might apply stress to inside chips or ceramic of heat sink plate, which will break or crack or degrade a module. An example of recommended fastening sequence is shown in Figure 5. The temporary fastening torque is set to 20 to 30% of the maximum torque rating. Evenly apply thermally-conductive grease with 100µm to 200µm thickness over the contact surface between the module and the heat sink. Also, pay attention not to have any dirt left on the contact surface between the module and the heat sink.
It is recommended to install a module directly to a heat sink after applying grease. When installing a module to a heat sink, inserting a heat radiation sheet between a module and a heat sink might apply stress depending on thickness and elastic modulus of the sheet to inside chips or ceramic of heat sink plate, which will break or crack or degrade a module. When using a heat radiation sheet, it is needed to prevent IPM from bending into + side of Figure 6-2.



Temporary fastening：1→2
Permanent fastening：1→2

Figure 5. Example of Recommended Fastening Sequence

TOP VIEW

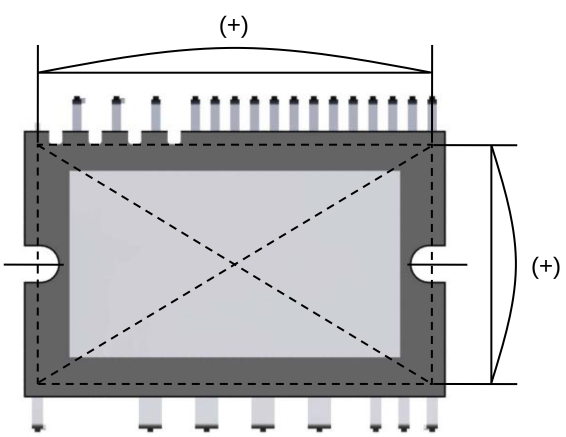


Figure 6-1. Measurement Point of Heat Sink Flatness

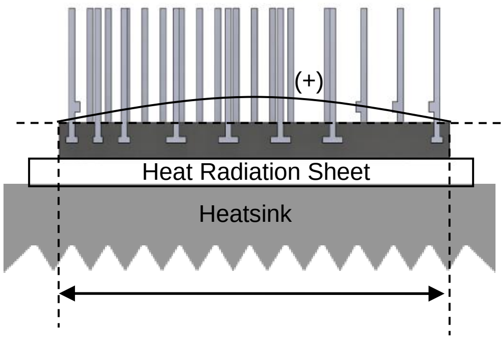


Figure 6-2. Flatness after Installing to a Heat Sink (When Using a Heat Radiation Sheet)

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Typical Performance Curve

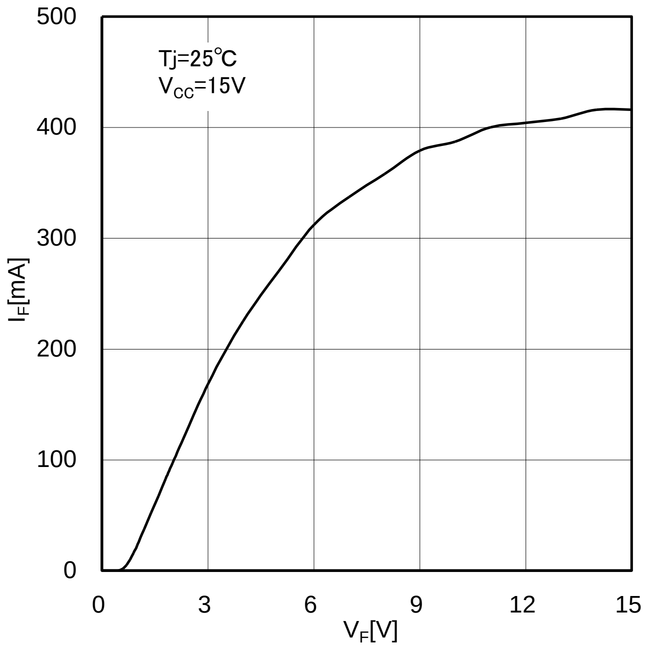

Figure 7. I_F vs V_F
(Characteristic of Bootstrap Diode I_F-V_F Curve Between HVCC-VBX pin (X=U,V,W))

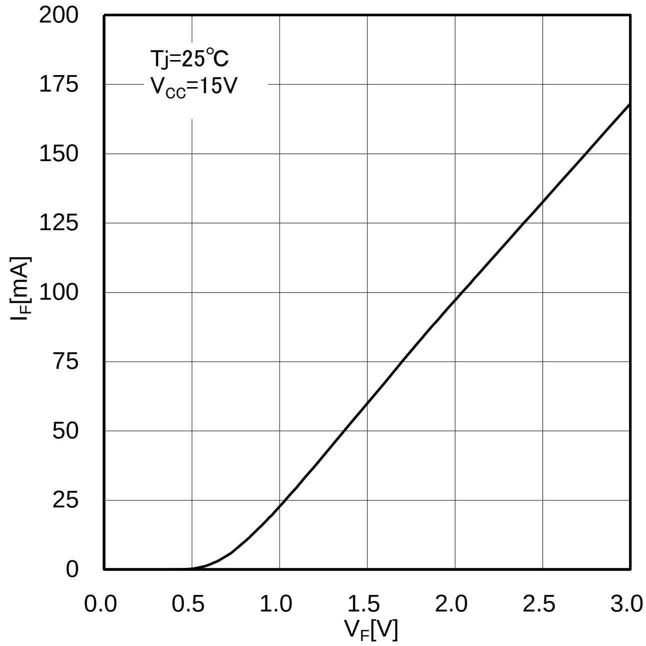

Figure 8. Magnification of Figure 7

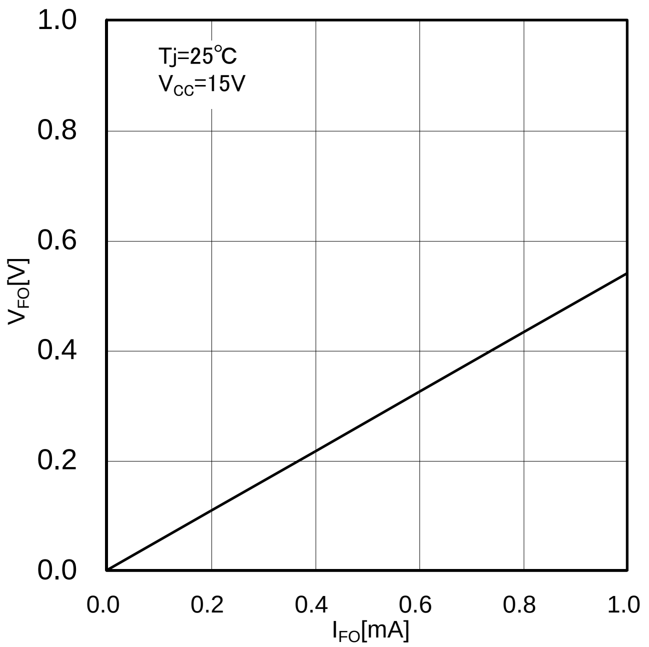

Figure 9. V_{FO} vs I_{FO}
(Characteristic of FO pin V_{FO}-I_{FO} Curve)

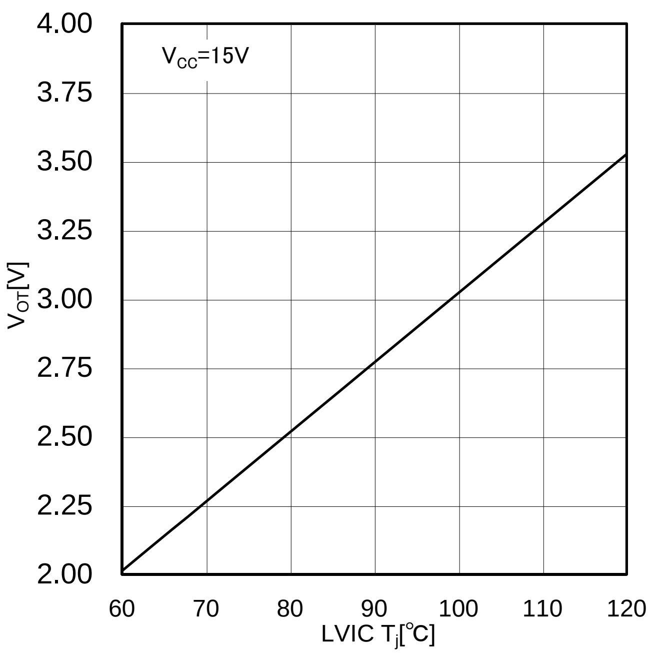

Figure 10. V_{OT} vs LVIC T_j
(Characteristic of VOT pin V_{OT}-T_j Curve)

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Timing Chart

1) Short Circuit Current Protection (protection with the external shunt resistor and RC filter)

a1. Normal operation: IGBT ON and outputs current I_C.

a2. Short circuit current detection (SCP trigger)
It is recommended to set RC time constant of 1.0µs so that IGBT shuts down within 2.0µs when SCP is triggered.

a3. All low side IGBT's gates are shut down (soft turn off).

a4. All low side IGBTs turn off.

a5. FO outputs for t_{FO}=45µs (Min).

a6. LIN=L

a7. LIN=H, but all IGBTs keep OFF during SCP=H.

a8. FO finishes output , but IGBTs don't turn on until inputting the next ON signal(LIN=L→H)
IGBT of each phase can return to normal state by inputting ON signal to each phase.

a9. Normal operation: IGBT ON and outputs current I_C.

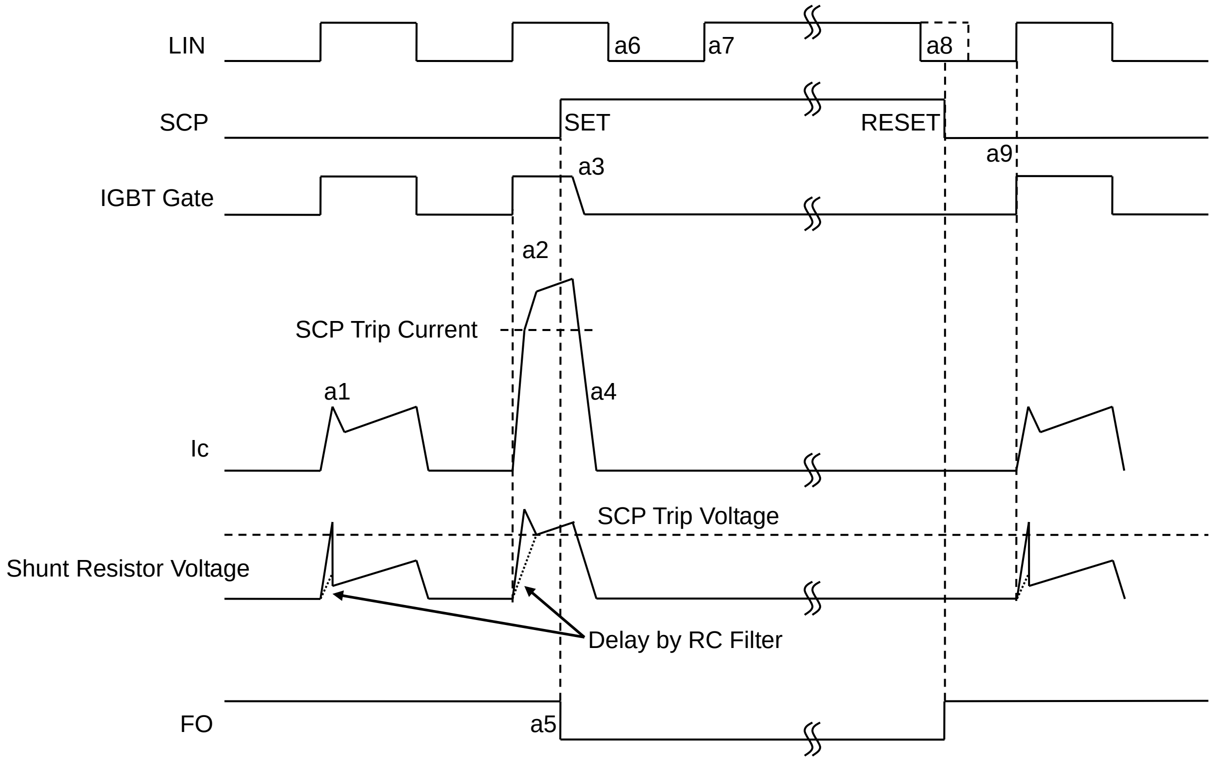

Figure 11. SCP Timing Chart

<u>Notice</u>

SCP works only for low side IGBT only.
Please select the external shunt resistance such that the SCP trip current is less than 1.7 times of the collector current rating I_c(DC).
In case of SCP trip and FO output, please stop controlling IPM quickly to avoid the abnormal state.

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2) Control Supply (LVCC) Under Voltage Locked Out (UVLO)

b1. Control supply(LVCC) voltage exceeds UVLO release level (V_{CCUVR}), but IGBT turns on by the next ON signal (LIN=L→H).IGBT of each phase can return to normal state by inputting ON signal to each phase.
b2. Normal operation: IGBT ON and outputs current I_C.
b3. LVCC drops to UVLO trip level (V_{CCUVT}).
b4. All low side IGBTs turn off in spite of control input condition.
b5. FO outputs for t_{FO}=minimum 90μs, but output is extended while LVCC is below V_{CCUVR}.
b6. LVCC reaches V_{CCUVR}.
b7. Even if LVCC reaches V_{CCUVR} during LIN=H, IGBTs don't turn on until inputting the next ON signal (LIN=L→H).
b8. Normal operation: IGBT ON and outputs current I_C.

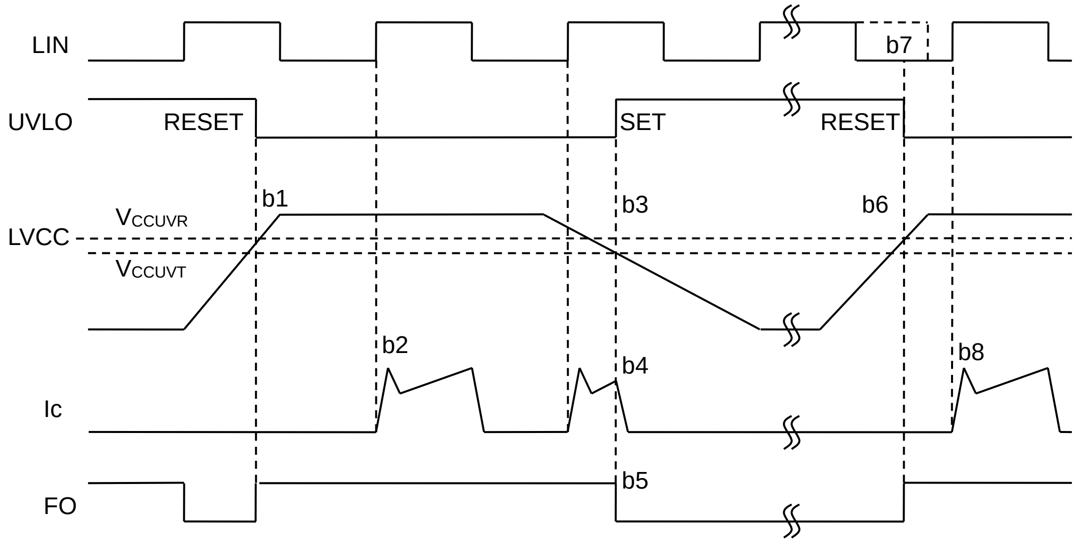

Figure 12. LVCC UVLO Timing Chart

3) Control supply (VBS) Under Voltage Locked Out (UVLO)

c1. Control supply(VBS) voltage exceeds UVLO release level (V_{BSUVR}), but IGBT turns on by the next ON signal (HIN=L→H).
c2. Normal operation: IGBT ON and outputs current I_C.
c3. VBS drops to UVLO trip level (V_{BSUVT}).
c4. Only IGBT of the corresponding phase turns off in spite of control input signal, there is no FO signal output.
c5. VBS reaches V_{BSUVR}.
c6. Even if VBS reaches V_{BSUVR} during HIN=H, IGBTs don't turn on until inputting the next ON signal (HIN=L→H).
c7. Normal operation: IGBT ON and outputs current I_C.

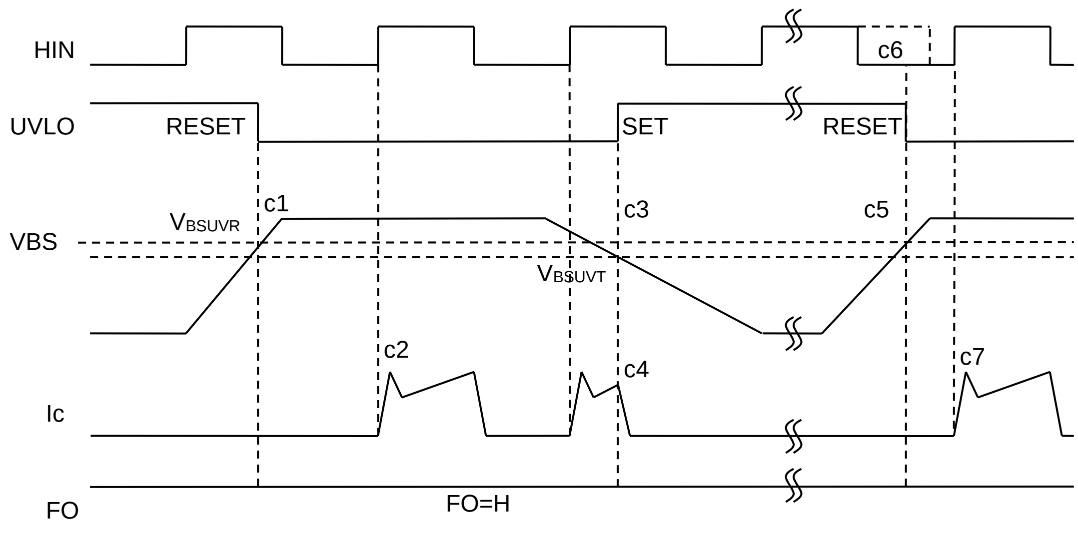

Figure 13. VBS UVLO Timing Chart

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4) Thermal Shutdown (TSD), monitoring LVIC temperature

d1. Normal operation: IGBT ON and outputs current I_C.
d2. LVIC temperature (T_j) exceeds thermal shutdown trip level (T_{SDT}).
d3. All low side IGBTs turn off in spite of control input condition.
d4. FO outputs for t_{FO}=180µs (Min),
but output is extended while T_j is above thermal shutdown release level (T_{SDT}-T_{SDHYS}).
d5. T_j drops to T_{SDT}-T_{SDHYS}
d6. Even if T_j reaches T_{SDT}-T_{SDHYS} during LIN=H, IGBTs don't turn on until inputting the next ON signal (LIN=L→H).
IGBT of each phase can return to normal state by inputting ON signal to each phase.
d7. Normal operation: IGBT ON and outputs current I_C.

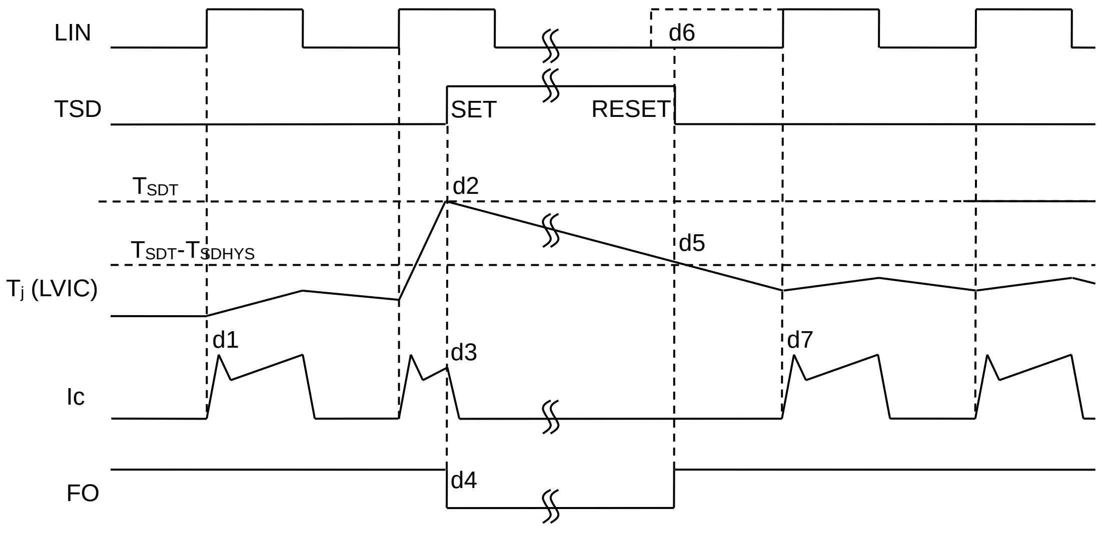

Figure 14. TSD Timing Chart

Notice

1) In case of TSD trip and FO output, please stop controlling IPM quickly to avoid the abnormal state.
2) If the cooling system is in abnormal state (e.g. heat sink comes off, fixed loosely, or cooling fan stops) when TSD trips, don't reuse IPM. This may cause the junction temperature of power chips to exceed its maximum rating of T_{jmax} (150°C).
3) TSD function detects LVIC temperature, so it cannot respond to rapid temperature rise of power chip. Therefore, TSD will not work properly in the case of rapid temperature rise like motor lock or over current.

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Application Example (one shunt resistor drive)

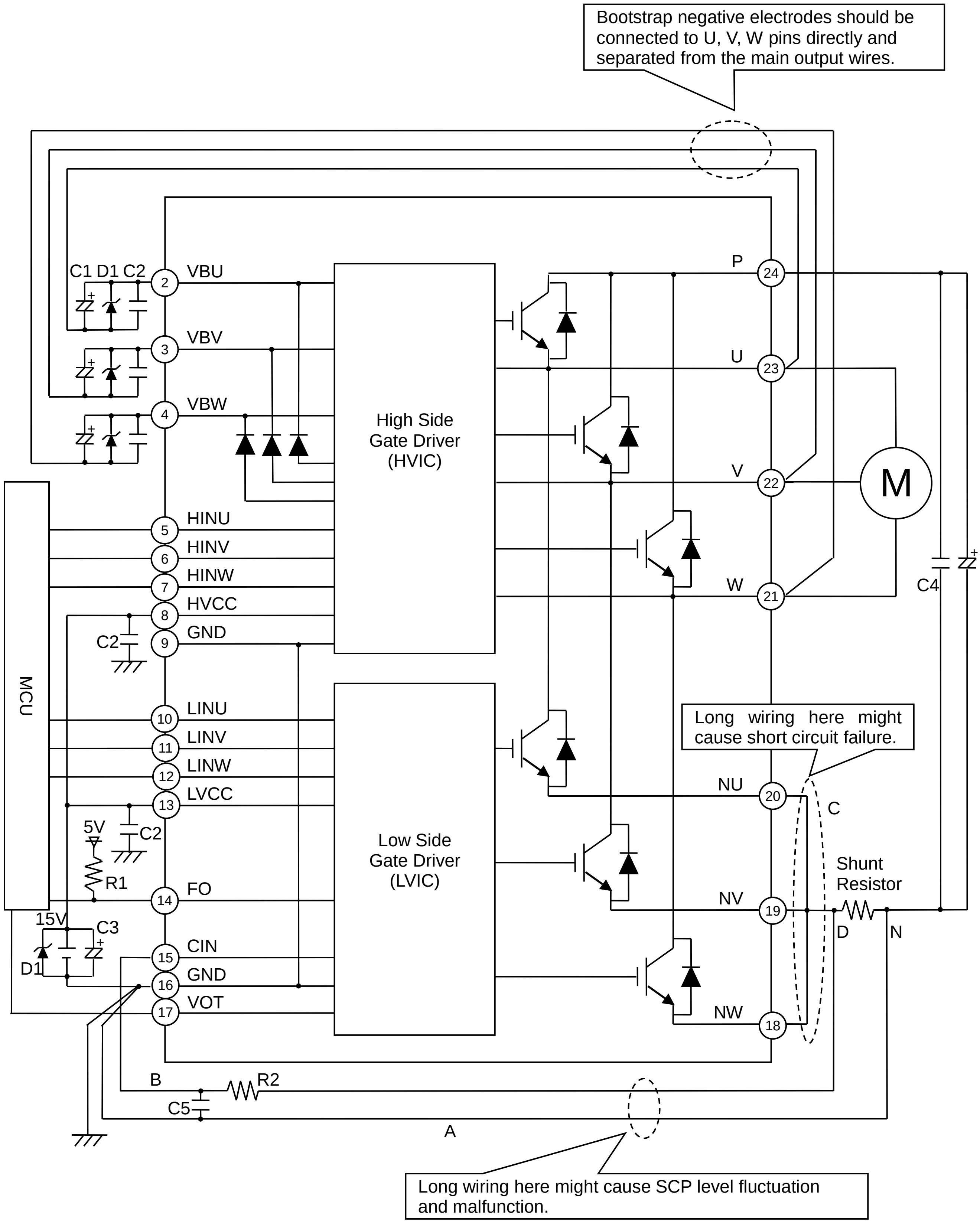

Figure 15. Example of Application Circuit

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Selection of Components Externally Connected (Refer to Figure 15)

1) VBU, VBV, VBW pin
- The bypass capacitor(good temperature, frequency characteristic electrolytic type C1: 22µF to 100µF) should be mounted as close as possible to the pin in order to prevent malfunction or destruction due to switching noise and power supply ripple. In addition, for the purpose of reducing of the power supply's impedance in wide frequency bandwidth, ceramic capacitor (good temperature, frequency and DC bias characteristic ceramic type C2: 0.1µF to 0.22µF) should also be mounted.
- Zenner diode D1(1W) should be mounted between each pair of control supply pins to prevent surge destruction.
- Line ripple voltage should meet dV/dt ≤1V/µs, V_{ripple} ≤ $2V_{p-p.}$
- The wiring from U, V, W pin should be as thick and as short as possible. They should be connected directly and separated from the main output wires.

2) HVCC, LVCC pin
- The bypass capacitor(good temperature, frequency characteristic electrolytic type C3) should be mounted as close as possible to the pin in order to prevent malfunction or destruction due to switching noise and power supply ripple. In addition, for the purpose of reducing of the power supply's impedance in wide frequency bandwidth, ceramic capacitor (good temperature, frequency and DC bias characteristic ceramic type C2: 0.1µF to 0.22µF) should also be mounted.
- Zenner diode D1(1W) should be mounted between each pair of control supply pins to prevent surge destruction.
- Line ripple voltage should meet dV/dt ≤ 1V/µs, V_{ripple} ≤ $2V_{p-p.}$

3) P pin
- To prevent surge destruction, the wiring between the smoothing capacitor and P, N pins should be as short as possible.
- Snubber capacitor(C4: 0.1µF to 0.22µF) should be mounted between the P-N pin.

4) Control Input pin (HINU, HINV, HINW, LINU, LINV, LINW)
- The wiring should be as short as possible to prevent malfunction.
- Input drive is active-high type. There is a 3.3kΩ(Min) pull-down resistor in the input circuit of IPM. When using RC coupling circuit, make sure the input signal level meet the input threshold voltage.
- Dead time of input signal should be more than specified value.
- The pull-down resistors in Control Input pins become effective when voltage supplied into LVCC and HVCC pins are in the range of recommended operating condition. Control Input pins have high impedance when power supply to LVCC and HVCC pins are off. When power supply to HVCC pin is off, the pull-down resistance of HINU, HINV, HINW pins is the value written on Page 6.

5) FO pin
- FO output is open drain type. It should be pulled up to control power supply(e.g. 5V, 15V) by a resistor that makes I_{FO} up to 1mA.I_{FO} is estimated roughly by the formula of control power supply voltage divided by pull-up resistance(R1). In the case of pulled up to 5V, R1=10kΩ is recommended.

6) CIN pin
- RC filter(R2, C5) should be mounted as close as possible to the pin in order to prevent malfunction by recovery current or switching noise. It is recommended to select tight tolerance, temp-compensated type for RC filter (R2, C5).
  The time constant R2C5 (1.0µs is recommended) should be set so that SCP current is shut down within 2µs.
  Please confirm operation on the actual application since SCP shutdown time changes depending on the PCB wiring pattern.
- The point D at which the wiring to CIN filter is divided should be near the pin of shunt resistor. NU, NV, NW pin should be connected at near NU, NV, NW pin.
- To prevent malfunction, the wiring of B should be as short as possible.

7) VOT pin (Refer to Fugure 16)
- It is recommended to insert 5.1kΩ pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between VOT and GND (control GND), the extra current calculated by VOT output voltage divided by pull down resistance flows as LVIC circuit current continuously. In the case of only using VOT for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.
- In the case of using VOT with low voltage controller (e.g. 3.3V MCU), VOT output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp diode between control supply of the controller and VOT for preventing over voltage.
- In the case of using low voltage controller like 3.3V MCU, if it is necessary to set the trip VOT level to control supply voltage (e.g. 3.3V) or more, there is the method of dividing the VOT output by resistance voltage divider circuit and then inputting to A/D converter on MCU. In that case, sum of the resistances of divider circuit should be as much as 5kΩ.
- When VOT pin is not used, please do not connect VOT pin to any other nodes.
- Please refer the application note for this product about the usage of VOT output.

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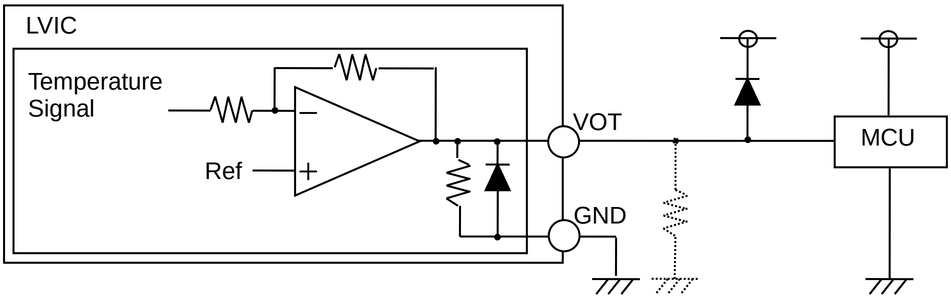
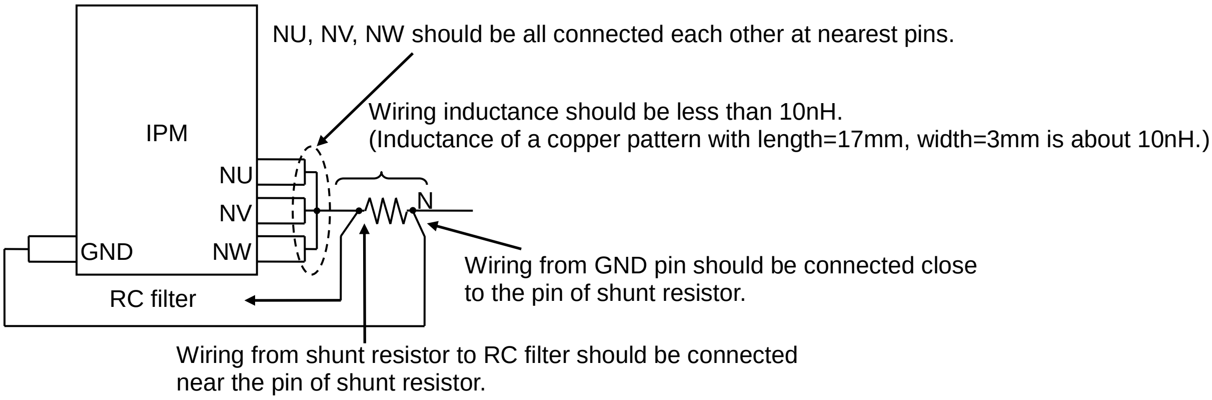


Figure 16. Example of VOT External Circuit

8) GND pin
- Two GND pins (9 & 16 pin) are connected inside IPM. Please connect one pin (16 pin is recommended.) to the 15V power supply GND outside and leave the other open.
- If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N (near the pin of shunt resistor).
- To prevent malfunction, the wiring of A should be as short as possible.

9) NU, NV, NW pin
- When operating with one-shunt resistor, please short the three pins(NU, NV, NW). In addition, to prevent malfunction, the wiring of C should be as short as possible.

10) One-shunt Resistor Drive



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

Figure 17. Wiring Pattern around the Shunt Resistor when Operating with One-shunt Resistor

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11) Three-shunt Resistors Drive

- It is not recommended to input the voltage of each shunt resistor directly to the CIN pin when IPM is operated with three shunt resistor. In that case, it is necessary to use the external protection circuit as below.
- It is necessary to set the time constant $R_u f_f$(1.0µs is recommended) of external comparator input so that IGBT stops within 2µs when short circuit occurs. Please confirm operation on the actual application since SCP shutdown time changes depending on the PCB wiring pattern.
- It is recommended for the threshold voltage VREF to be set to the same rating of short circuit trip level(V_{SC}=0.48V(Typ))
- Please select the external shunt resistance such that the SCP trip current is less than 1.7 times of the collector current rating I_c(DC).
- To prevent malfunction, the wiring of A, B, C should be as short as possible.
- OR output high level when protection works should be 0.505V(maximum V_{SC} rating) to 7V(CIN absolute maximum rating).

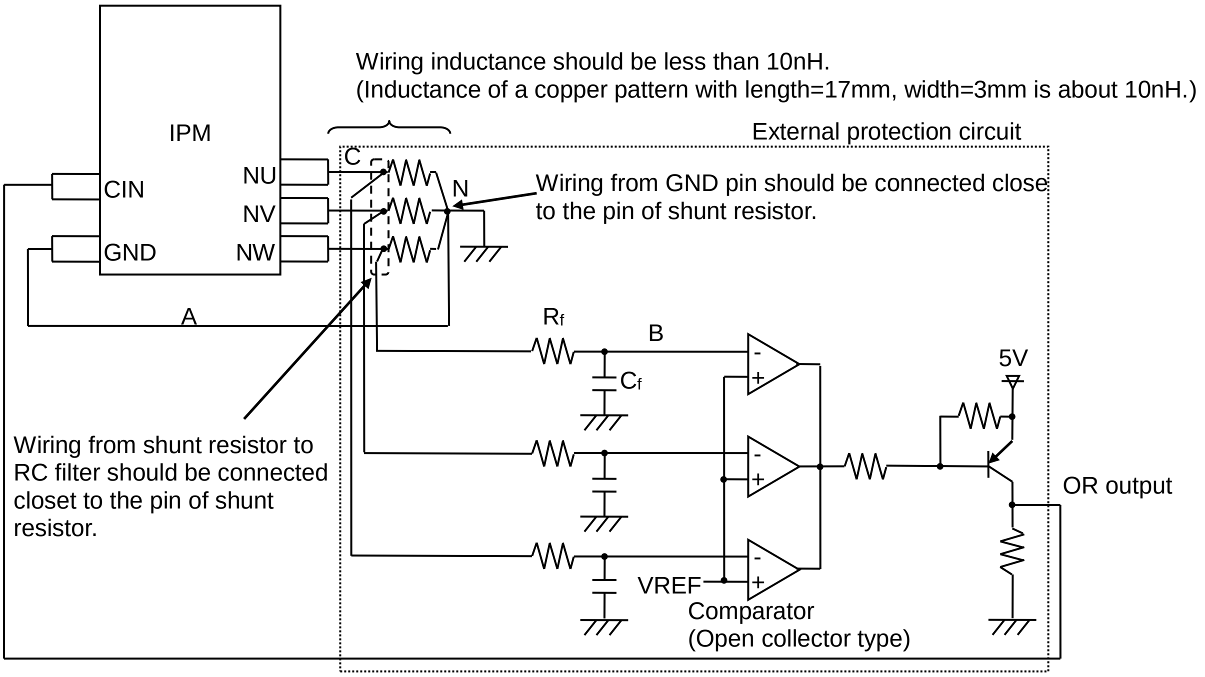

Figure 18. Wiring Pattern around the Shunt Resistor when operating with Three-shunt Resistors

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I/O Equivalence Circuit

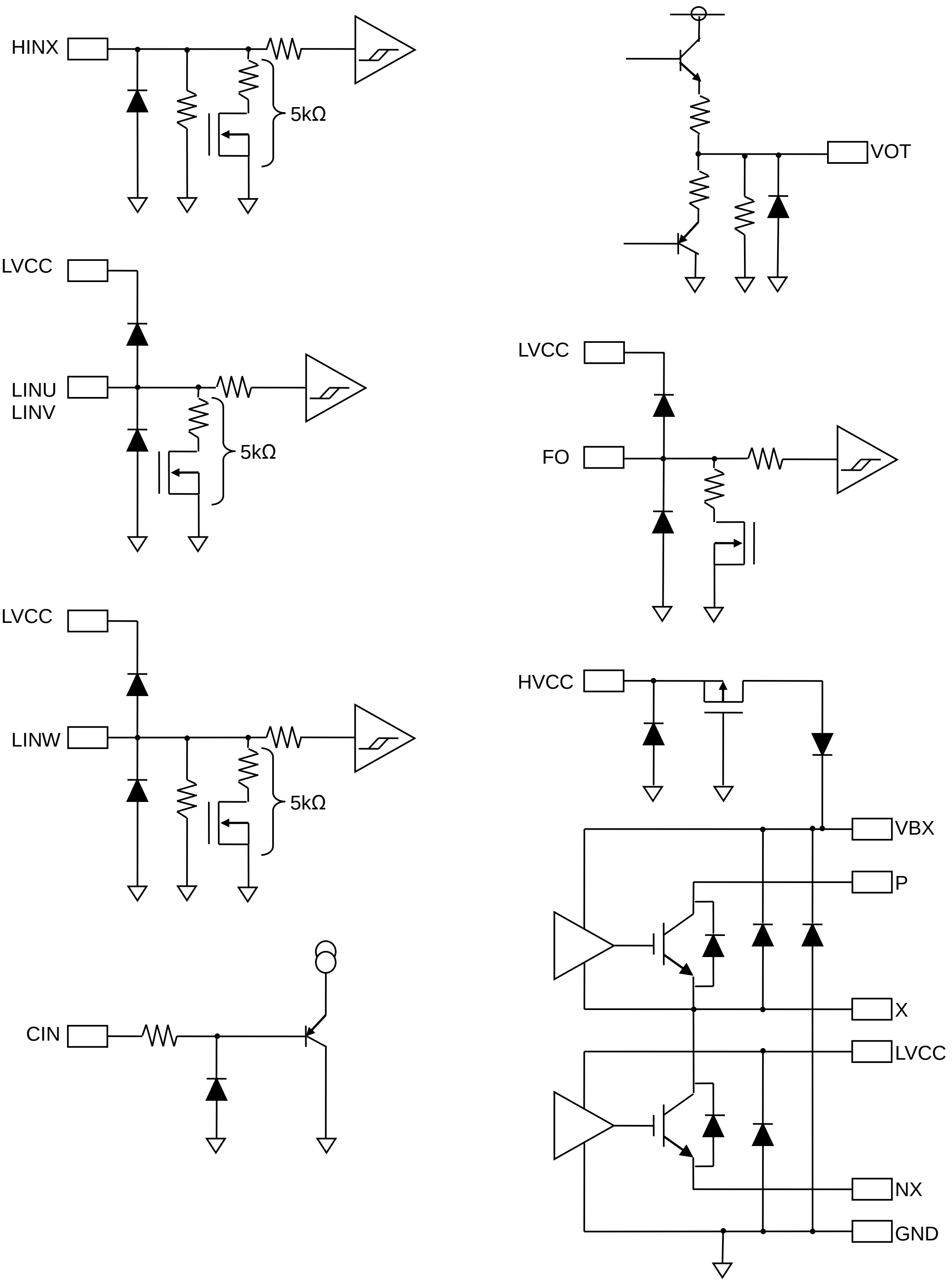

Figure 19. Input / Output Equivalent Circuit (X=U, V, W)

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IPM. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IPM's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IPM and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IPM can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IPM, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IPM has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
   When testing the IPM on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IPM to stress. Always discharge capacitors completely after each process or step. The IPM's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IPM during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IPM on the PCB. Incorrect mounting may result in damaging the IPM. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IPM are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IPM. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. **Area of Safe Operation (ASO)**
    Operate the IPM such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

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Ordering Information

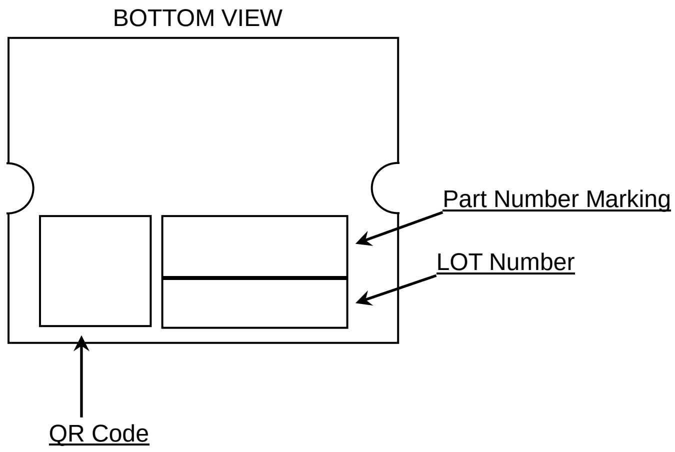
B M 6 4 3 7 5 S - xx

Part Number

Package
S:HSDIP25

Packaging and Forming Specification
-VA: Tube, Long pin type

Marking Diagram



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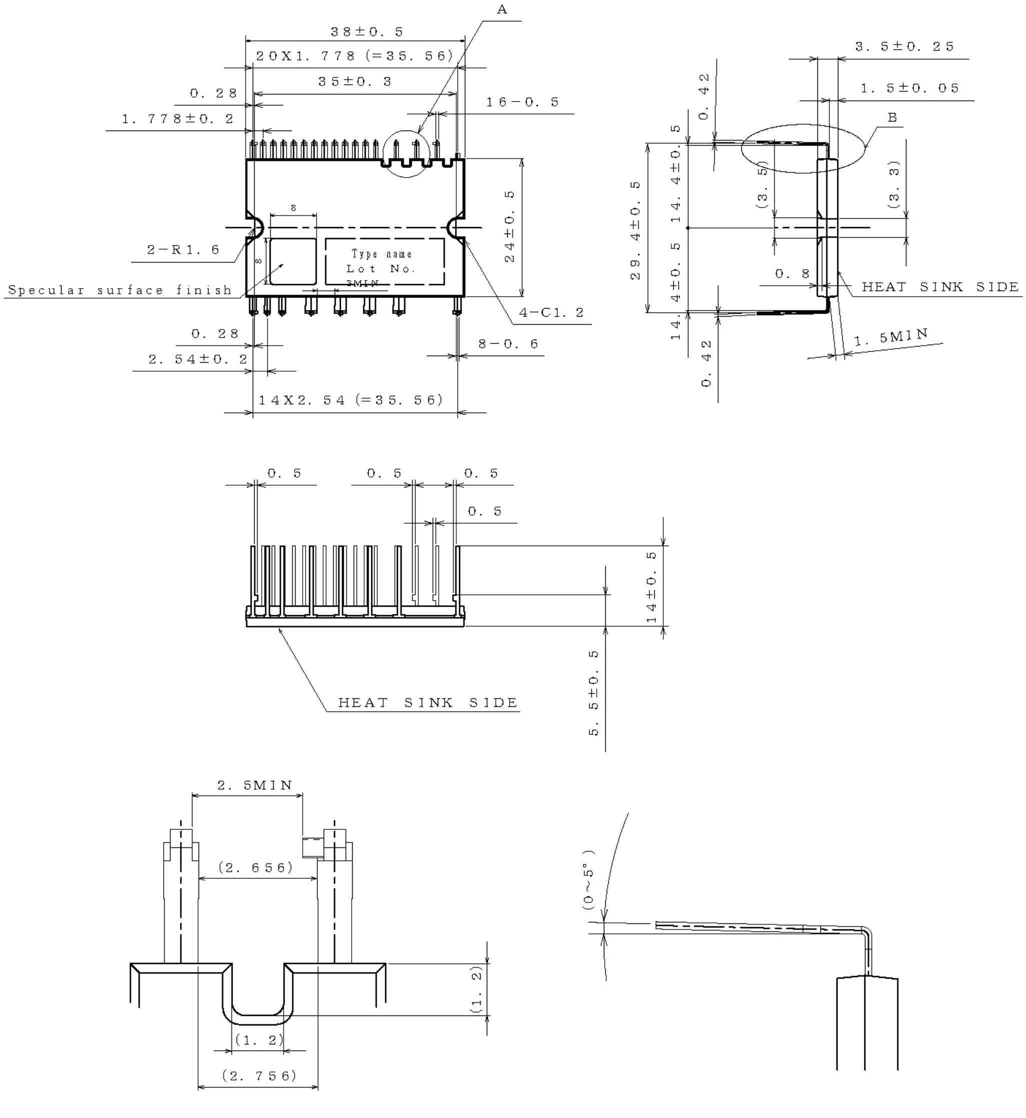
Physical Dimension, Tape and Reel Information

Package Name	HSDIP25



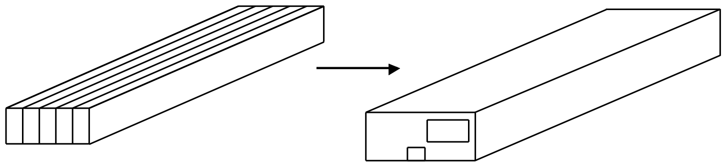
DETAIL A DETAIL B

(UNIT : mm)

PKG : HSDIP25
Drawing No. EX641−5002

<Tape and Reel information>

Container	Tube
Quantity	60pcs
Direction of feed	Direction of products is fixed in a container tube



∗When you order, please order in times the amount of package quantity.

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Revision History

Date	Revision	Changes
04.Sep.2020	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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