bq24232HA USB-Friendly Lithium-Ion Battery Charger and Power-Path Management IC

1 Features

- Fully Compliant USB Charger
  - Selectable 100-mA and 500-mA Maximum Input Current
  - 100-mA Maximum Current Limit Ensures Compliance to USB-IF Standard
  - Input-based Dynamic Power Management (V_{IN} – DPM) for Protection Against Poor USB Sources
- 28-V Input Rating With Overvoltage Protection
- Integrated Dynamic Power-Path Management (DPPM) Function Simultaneously and Independently Powers the System and Charges the Battery
- Supports up to 500-mA Charge Current With Current Monitoring Output (ISET)
- Programmable Input Current Limit up to 500 mA for Wall Adapters
- Programmable Termination Current
- Programmable Precharge and Fast-Charge Safety Timers
- Reverse Current, Short-Circuit, and Thermal Protection
- NTC Thermistor Input
- Proprietary Start-Up Sequence Limits Inrush Current
- Status Indication – Charging/Done, Power Good
- Small 3 mm × 3 mm 16-Lead QFN Package

2 Applications

- *Bluetooth*™ Devices
- Low-Power Handheld Devices

3 Description

The bq24232HA device is a highly integrated Li-ion linear charger and system power-path management device targeted at space-limited portable applications. The device operates from either a USB port or ac adapter and supports charge currents between 25 mA and 500 mA. The high-input-voltage range with input overvoltage protection supports low-cost, unregulated adapters. The USB input current limit accuracy and start-up sequence allow the bq24232HA to meet USB-IF inrush current specification. Additionally, the input dynamic power management (V_{IN} – DPM) prevents the charger from crashing poorly designed or incorrectly configured USB sources.

The bq24232HA features dynamic power-path management (DPPM) that powers the system while simultaneously and independently charging the battery. The DPPM circuit reduces the charge current when the input current limit causes the system output to fall to the DPPM threshold, thus supplying the system load at all times while monitoring the charge current separately. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination, and enables the system to run with a defective or absent battery pack. Additionally, this enables instant system turn-on even with a totally discharged battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents, enabling the use of a smaller adapter.

The battery is charged in three phases: conditioning, constant current, and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded.

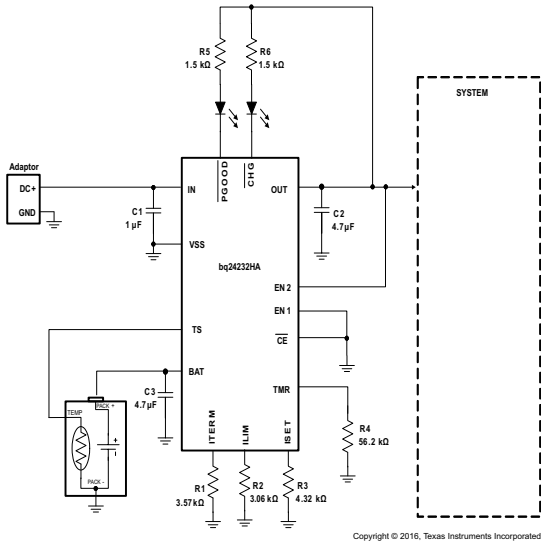
The charger power stage and charge current sense functions are fully integrated. The charger function has high-accuracy current and voltage regulation loops, charge status display, and charge termination. The input current limit and charge current are programmable using external resistors.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24232HA	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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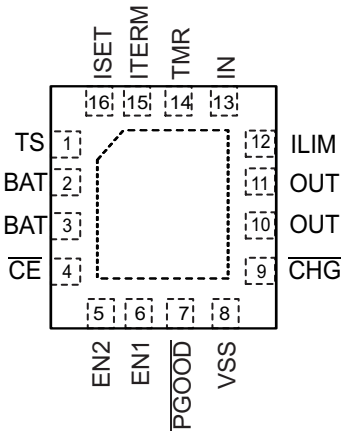
4 Revision History

DATE	REVISION	NOTES
May 2016	*	Initial release.

5 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
TS	1	I	External NTC Thermistor Input. Connect the TS input to the NTC thermistor in the battery pack. TS monitors a 10-kΩ NTC thermistor. For applications that do not utilize the TS function, connect a 10-kΩ fixed resistor from TS to VSS to maintain a valid voltage level on TS.
BAT	2, 3	I/O	Charger Power Stage Output and Battery Voltage Sense Input. Connect BAT to the positive terminal of the battery. Bypass BAT to VSS with a 4.7-μF to 47-μF ceramic capacitor.
$\overline{CE}$	4	I	Charge Enable Active-Low Input. Connect $\overline{CE}$ to a high logic level to disable battery charging. OUT is active and battery supplement mode is still available. Connect $\overline{CE}$ to a low logic level to enable the battery charger. $\overline{CE}$ is internally pulled down with ~285 kΩ. Do not leave $\overline{CE}$ unconnected to ensure proper operation.
EN2	5	I	Input Current Limit Configuration Inputs. Use EN1 and EN2 control the maximum input current and enable USB compliance. See *EN1/EN2 Settings* for the description of the operation states. EN1 and EN2 are internally pulled down with ~285 kΩ. Do not leave EN1 or EN2 unconnected to ensure proper operation.
EN1	6	I	
$\overline{PGOOD}$	7	O	Open-drain Power Good Status Indication Output. $\overline{PGOOD}$ pulls to VSS when a valid input source is detected. $\overline{PGOOD}$ is high-impedance when the input power is not within specified limits. Connect $\overline{PGOOD}$ to the desired logic voltage rail using a 1-kΩ – 100-kΩ resistor, or use with an LED for visual indication.
VSS	8	—	Ground. Connect to the thermal pad and to the ground rail of the circuit.
$\overline{CHG}$	9	O	Open-Drain Charging Status Indication Output. $\overline{CHG}$ pulls to VSS when the battery is charging. $\overline{CHG}$ is high impedance when charging is complete and when charger is disabled.
OUT	10, 11	O	System Supply Output. OUT provides a regulated output when the input is below the OVP threshold and above the regulation voltage. When the input is out of the operation range, OUT is connected to V_{BAT}. Connect OUT to the system load. Bypass OUT to VSS with a 4.7-μF to 47-μF ceramic capacitor.
ILIM	12	I	Adjustable Current Limit Programming Input. Connect a 3.06-kΩ to 7.8-kΩ resistor from ILIM to VSS to program the maximum input current (EN2 = 1, EN1 = 0). The input current includes the system load and the battery charge current. Leaving ILIM unconnected disables all charging. In USB100/500 mode (EN2 = 0, EN1 = 0/1), ILIM can be left floating.
IN	13	I	Input Power Connection. Connect IN to the connected to external DC supply (AC adapter or USB port). The input operating range is 4.35 V to 6.6 V. The input can accept voltages up to 26 V without damage but operation is suspended. Connect bypass capacitor 1 μF to 10 μF to VSS.
TMR	14	I	Timer Programming Input. TMR controls the precharge and fast-charge safety timers. Connect TMR to VSS to disable all safety timers. Connect a 18-kΩ to 72-kΩ resistor between TMR and VSS to program the timers a desired length. Leave TMR unconnected to set the timers to the 5-hour fast charge and 30-minute precharge default timer values.
ITERM	15	I	Termination Current Programming Input. Connect a 0-Ω to 15-kΩ resistor from ITERM to VSS to program the termination current. Leave ITERM unconnected to set the termination current to the internal default 10% threshold.
ISET	16	I/O	Fast-Charge Current Programming Input. Connect a 1.8-kΩ to 36-kΩ resistor from ISET to VSS to program the fast-charge current level. Charging is disabled if ISET is left unconnected. While charging, the voltage at ISET reflects the actual charging current and can be used to monitor charge current. See the *Charge Current Translator* section for more details.
Thermal Pad		—	An internal electrical connection exists between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed-circuit board. Do not use the thermal pad as the primary ground input for the device. The VSS pin must be connected to ground at all times.

Table 1. EN1/EN2 Settings

EN2	EN1	MAXIMUM INPUT CURRENT INTO IN PIN
0	0	100 mA, USB100 mode
0	1	500 mA, USB500 mode
1	0	Set by an external resistor from ILIM to VSS
1	1	Standby (USB suspend mode)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_I	Input voltage	IN (with respect to VSS	–0.3	28	V
		OUT (with respect to VSS)	–0.3	7	
		BAT (with respect to VSS)	–0.3	5	
		EN1, EN2, $\overline{CE}$, TS, ISET, $\overline{PGOOD}$, $\overline{CHG}$, ILIM, TMR, TD, ITERM (with respect to VSS)	–0.3	7	
I_I	Input current	IN		600	mA
I_O	Output current (continuous)	OUT		1700	mA
		BAT (discharge mode)		1700	
	Output sink current	$\overline{CHG}$, $\overline{PGOOD}$		15	mA
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over junction temperature range –5°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

		MIN	MAX	UNIT
V_I	IN voltage	4.35	26	V
	IN operating voltage	4.35	10.2	V
I_{IN}	Input current, IN pin		500	mA
I_{OUT}	Current, OUT pin		1500	mA
I_{BAT}	Current, BAT pin (discharging)		1500	mA
I_{CHG}	Current, BAT pin (charging)		500	mA
R_{ILIM}	Maximum input current programming resistor	3.1	7.8	kΩ
R_{ISET}	Fast-charge current programming resistor	1.8	36	kΩ
R_{TMR}	Timer programming resistor	18	72	kΩ
R_{ITERM}	Termination programming resistor	0	15	kΩ
T_J	Junction temperature	–5	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		bq24232HA RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over junction temperature range –5°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
UVLO	Undervoltage lockout	V_{IN}: 0 V → 4 V		3.2	3.3	3.4	V
$V_{hys(UVLO)}$	Hysteresis on UVLO	V_{IN}: 4 V → 0 V		200		300	mV
$V_{IN(DT)}$	Input power detection threshold	Input power detected when $V_{IN} > V_{BAT} + V_{IN(DT)}$ V_{BAT} = 3.6 V, VIN: 3.5 V → 4 V		55	95	152	mV
$V_{hys(INDT)}$	Hysteresis on $V_{IN(DT)}$	VBAT = 3.6 V, V_{IN}: 4 V → 3.5 V		20			mV
V_{OVP}	Input overvoltage protection threshold	('230) V_{IN}: 5 V → 7 V		6.4	6.6	6.8	V
		('232) V_{IN}: 5 V → 11 V		10.2	10.5	10.8	
$V_{hys(OVP)}$	Hysteresis on OVP	('230) V_{IN}: 7 V → 5V			110		mV
		('232) V_{IN}: 11 V → 5 V			213		
ILIM, TEST ISET SHORT CIRCUIT							
I_{SC}	Current source	V_{IN} > UVLO and $V_{IN} > V_{BAT}+V_{IN(DT)}$			1.3		mA
V_{SC}		V_{IN} > UVLO and $V_{IN} > V_{BAT}+V_{IN(DT)}$			502		mV
QUIESCENT CURRENT							
$I_{BAT(PDWN)}$	Sleep current into BAT pin	$\overline{CE}$ = LO or HI, input power not detected, no load on OUT pin	T_J= -5°C to 55°C			6.5	µA
			T_J= -5°C to 85°C			9.5	
$I_{IN(STDBY)}$	Standby current into IN pin	EN1= HI, EN2=HI, V_{IN} = 6 V, T_J= 85°C				50	µA
		EN1= HI, EN2=HI, V_{IN} = 10 V, T_J= 85°C				200	
I_{CC}	Active supply current, IN pin	$\overline{CE}$ = LO, V_{IN} = 6 V, no load on OUT pin, $V_{BAT} > V_{BAT(REG)}$, (EN1, EN2) ≠ (HI, HI)				1.5	mA

Electrical Characteristics (continued)

over junction temperature range –5°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER PATH						
$V_{DO(IN-OUT)}$	$V_{IN} – V_{OUT}$	V_{IN} = 4.3 V, I_{IN} = 500 mA, V_{BAT} = 4.2 V		136	237.5	mV
$V_{DO(BAT-OUT)}$	$V_{BAT} – V_{OUT}$	I_{OUT} = 500 mA, V_{IN} = 0 V, V_{BAT} > 3 V			62.5	mV
$V_{O(REG)}$	OUT pin voltage regulation	$V_{IN} > V_{OUT} + V_{DO (IN-OUT)}$	4.35	4.5	4.6	V
I_{IN}max	Maximum input current	EN1 = LO, EN2 = LO	90	95	100	mA
		EN1 = HI, EN2 = LO	450	475	500	
		EN2 = HI, EN1 = LO		K_{ILIM}/R_{ILIM}		A
K_{ILIM}	Maximum input current factor	I_{LIM} = 200 mA to 500 mA	1380	1571	1700	AΩ
I_{IN}max	Programmable input current limit range	EN2 = HI, EN1 = LO, R_{ILIM} = 3.06 kΩ to 7.8 kΩ	200		500	mA
V_{IN-DPM}	Input voltage threshold when input current is reduced	EN2 = LO, EN1 = X	4.3	4.35	4.63	V
V_{DPPM}	Output voltage threshold when charging current is reduced		$V_{O(REG)}$ – 180 mV	$V_{O(REG)}$ – 100 mV	$V_{O(REG)}$ – 30 mV	V
V_{BSUP1}	Enter battery supplement mode	V_{BAT} = 3.6 V, R_{ILIM} = 1.5 kΩ, R_{LOAD} = 10 Ω →2 Ω		$V_{OUT} ≤ V_{BAT}$ –50 mV		V
V_{BSUP2}	Exit battery supplement mode	V_{BAT} = 3.6 V, R_{ILIM} = 1.5 kΩ, R_{LOAD} = 2 Ω →10 Ω		$V_{OUT} ≥ V_{BAT}$–20 mV		V
$V_{O(SC1)}$	Output short-circuit detection threshold, power-on	V_{IN} > UVLO and $V_{IN} > V_{BAT}+V_{IN(DT)}$	0.8	0.9	1	V
$V_{O(SC2)}$	Output short-circuit detection threshold, supplement mode $V_{BAT} – V_{OUT} > V_{O(SC2)}$ indicates short circuit	V_{IN} > UVLO and $V_{IN} > V_{BAT}+V_{IN(DT)}$	200	242	300	mV

Electrical Characteristics (continued)

over junction temperature range –5°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER						
$I_{BAT(SC)}$	Source current for BAT pin short-circuit detection	V_{BAT} = 1.5 V	4	8.15	11	mA
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold	V_{BAT} rising	1.6	1.8	2	V
$V_{BAT(REG)}$	Battery charge voltage		4.25	4.31	4.35	V
V_{LOWV}	Precharge to fast-charge transition threshold	V_{IN} > UVLO and V_{IN} > V_{BAT} + $V_{IN(DT)}$	2.9	3	3.1	V
I_{CHG}	Battery fast-charge current range	$V_{BAT(REG)}$ > V_{BAT} > V_{LOWV}, V_{IN} = 5 V, $\overline{CE}$ = LO, EN1 = LO, EN2 = HI	25		500	mA
	Battery fast-charge current	$\overline{CE}$ = LO, EN1= LO, EN2 = HI, V_{BAT} > V_{LOWV}, V_{IN} = 5 V, I_{IN}max > I_{CHG}, no load on OUT pin, thermal loop and DPM loop not active	K_{ISET}/R_{ISET}			A
K_{ISET}	Fast-charge current factor	25 mA ≥ I_{CHG}≥ 500 mA	797	870	975	AΩ
$K_{IPRECHG}$	Precharge current factor	2.5 mA ≥ I_{PRECHG}≥ 30 mA	70	88	106	AΩ
I_{TERM}	Termination comparator threshold for termination detection	$\overline{CE}$ = LO, (EN1,EN2) ≠ (LO,LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPM loop and thermal loop not active	0.09 × I_{CHG}	0.1 × I_{CHG}	0.11 × I_{CHG}	A
		$\overline{CE}$ = LO, (EN1,EN2) = (LO,LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPM loop and thermal loop not active	0.027 × I_{CHG}	0.033 × I_{CHG}	0.040 × I_{CHG}	
I_{TERM}	Termination current threshold factor	I_{TERM} = 0% to 50% of I_{CHG}	K_{ITERM} × R_{ITERM} / R_{ISET}			A
$I_{BIAS(ITERM)}$	Current for external termination-setting resistor		72	75	78	µA
K_{ITERM}	K factor for termination detection threshold (externally set)	$\overline{CE}$ = LO, (EN1,EN2) ≠ (LO,LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPM loop and thermal loop not active	0.024	0.030	0.036	A
		$\overline{CE}$ = LO, (EN1,EN2) = (LO,LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPM loop and thermal loop not active	0.009	0.010	0.011	
V_{RCH}	Recharge detection threshold	V_{IN} > UVLO and V_{IN} > V_{BAT}+$V_{IN(DT)}$	$V_{BAT(REG)}$ –140 mV	$V_{BAT(REG)}$ –100 mV	$V_{BAT(REG)}$ –60 mV	V
$I_{BAT(DET)}$	Sink current for battery detection	V_{BAT}=2.5 V	5	7.5	10	mA
BATTERY-PACK NTC MONITOR(1)						
I_{NTC}	NTC bias current	V_{IN} > UVLO and V_{IN} > V_{BAT}+$V_{IN(DT)}$	72	75	79	µA
V_{HOT}	High-temperature trip point	Battery charging, V_{TS} Falling	270	300	330	mV
$V_{HYS(HOT)}$	Hysteresis on high trip point	Battery charging, V_{TS} Rising from V_{HOT}		30		mV
V_{COLD}	Low-temperature trip point	Battery charging, V_{TS} Rising	2000	2100	2200	mV
$V_{HYS(COLD)}$	Hysteresis on low trip point	Battery charging, V_{TS} Falling from V_{COLD}		300		mV
$V_{DIS(TS)}$	TS function disable threshold	TS unconnected		V_{IN} – 200 mV		V
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature	T_J rising		155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C

(1) These numbers set trip points of 0°C and 50°C while charging, with 3°C hysteresis on the trip points, with a Vishay Type 2 curve NTC with an R25 of 10 kΩ.

Electrical Characteristics (continued)

over junction temperature range –5°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC LEVELS ON EN1, EN2, $\overline{CE}$, TD						
V_{IL}	Logic LOW input voltage		0		0.4	V
V_{IH}	Logic HIGH input voltage		1.4		6.0	V
I_{IL}	Input sink current	V_{IL} = 0 V			1	µA
I_{IH}	Input source current	V_{IH} = 1.4 V			10	µA
LOGIC LEVELS ON $\overline{PGOOD}$, $\overline{CHG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V

6.6 Timing Requirements

over junction temperature range –5°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	Time measured from V_{IN}: 0 V → 5-V 1-µs rise time to $\overline{PGOOD}$ = LO		2		ms
$t_{DGL(OVP)}$	Input overvoltage blanking time			50		µs
$t_{REC(OVP)}$	Input overvoltage recovery time	Time measured from V_{IN}: 11 V → 5-V 1-µs fall time to $\overline{PGOOD}$ = LO		2		ms
POWER PATH						
$t_{DGL(SC2)}$	Deglitch time, supplement mode short circuit			250		µs
$t_{REC(SC2)}$	Recovery time, supplement mode short circuit			60		ms
BATTERY CHARGER						
$t_{DGL1(LOWV)}$	Deglitch time on precharge to fast-charge transition			25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to precharge transition			25		ms
$t_{DGL(TERM)}$	Deglitch time, termination detected			25		ms
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected			62.5		ms
$t_{DGL(NO-IN)}$	Delay time, input power loss to charger turnoff	V_{BAT} = 3.6 V. Time measured from V_{IN}: 5 V → 3 V 1-µs fall time		20		ms
BATTERY CHARGING TIMERS						
t_{PRECHG}	Precharge safety timer value	TMR = floating	1440	1800	2160	s
t_{MAXCHG}	Charge safety timer value	TMR = floating	14400	18000	21600	s
t_{PRECHG}	Precharge safety timer value	18 kΩ < R_{TMR} < 72 kΩ		R_{TMR} × K_{TMR}		s
t_{MAXCHG}	Charge safety timer value	18 kΩ < R_{TMR} < 72 kΩ		10×RTMR ×K_{TMR}		s
K_{TMR}	Timer factor		36	48	60	s/kΩ
BATTERY-PACK NTC MONITOR(1)						
$t_{DGL(TS)}$	Deglitch time, pack temperature fault detection	Battery charging, V_{TS} Falling		50		ms

(1) These numbers set trip points of 0°C and 50°C while charging, with 3°C hysteresis on the trip points, with a Vishay Type 2 curve NTC with an R25 of 10 kΩ.

6.7 Typical Characteristics

Typical Application Circuit, EN1 = 0, EN2 = 1, T_A = 25°C, unless otherwise noted.

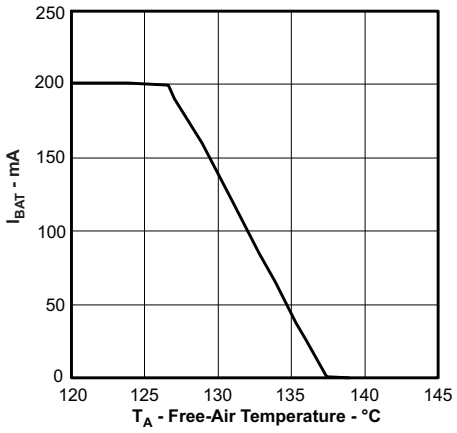
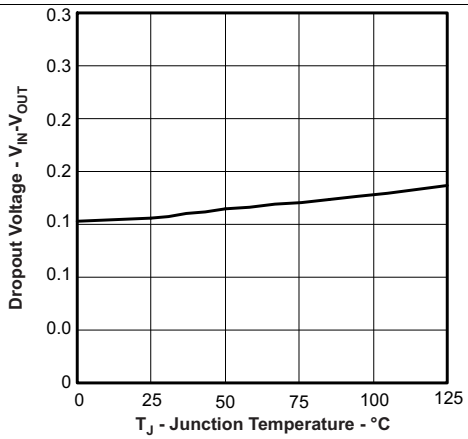
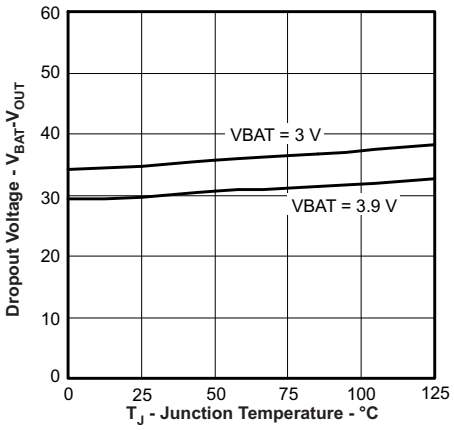


Figure 1. Thermal Regulation



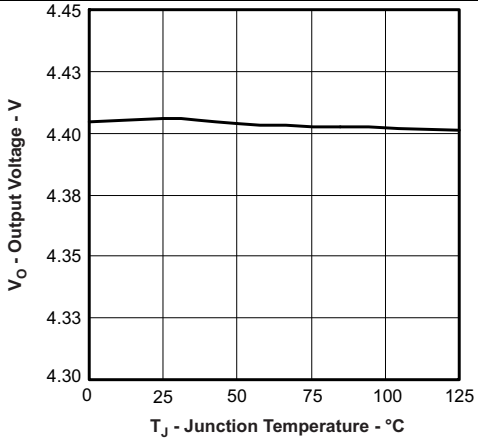
I_L = 500 mA

Figure 2. Dropout Voltage vs Temperature



I_L = 500 mA

Figure 3. Dropout Voltage vs Temperature



V_{IN} = 5 V I_L = 500 mA

Figure 4. Output Regulation Voltage vs Temperature

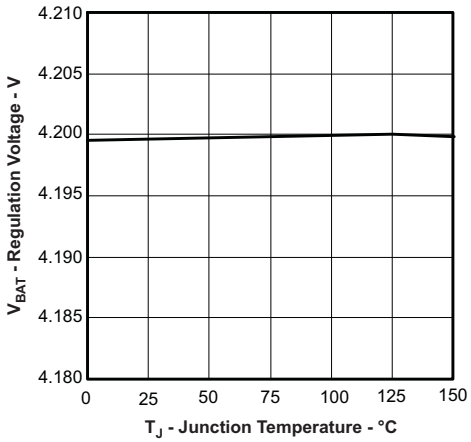
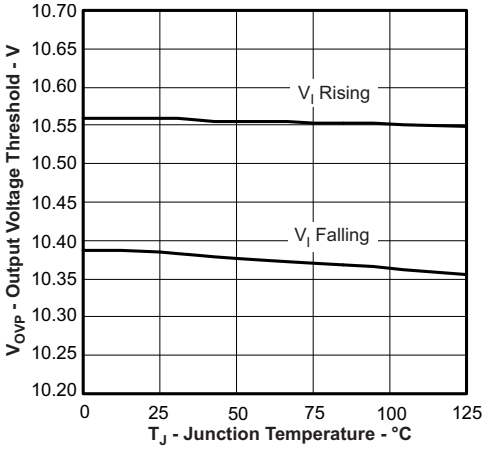


Figure 5. Battery Regulation Voltage vs Temperature



10.5 V

Figure 6. Overvoltage Protection Threshold vs Temperature

Typical Characteristics (continued)

Typical Application Circuit, EN1 = 0, EN2 = 1, T_A = 25°C, unless otherwise noted.

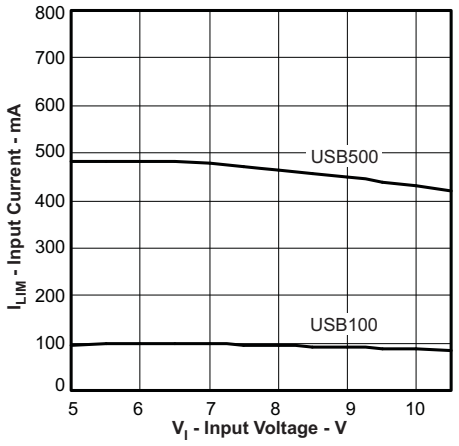
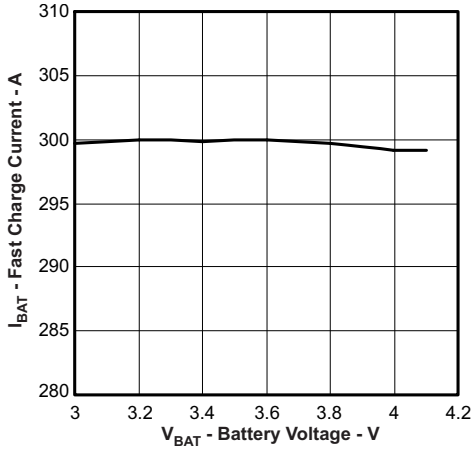
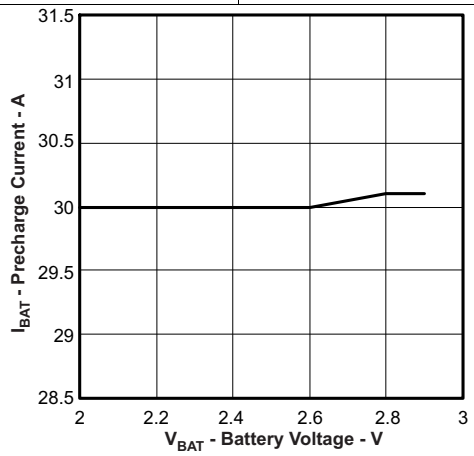


Figure 7. Input Current Limit Threshold vs Input Voltage



R_{ISET} = 3.3 kΩ

Figure 8. Fast-Charge Current vs Battery Voltage



R_{ISET} = 3.3 kΩ

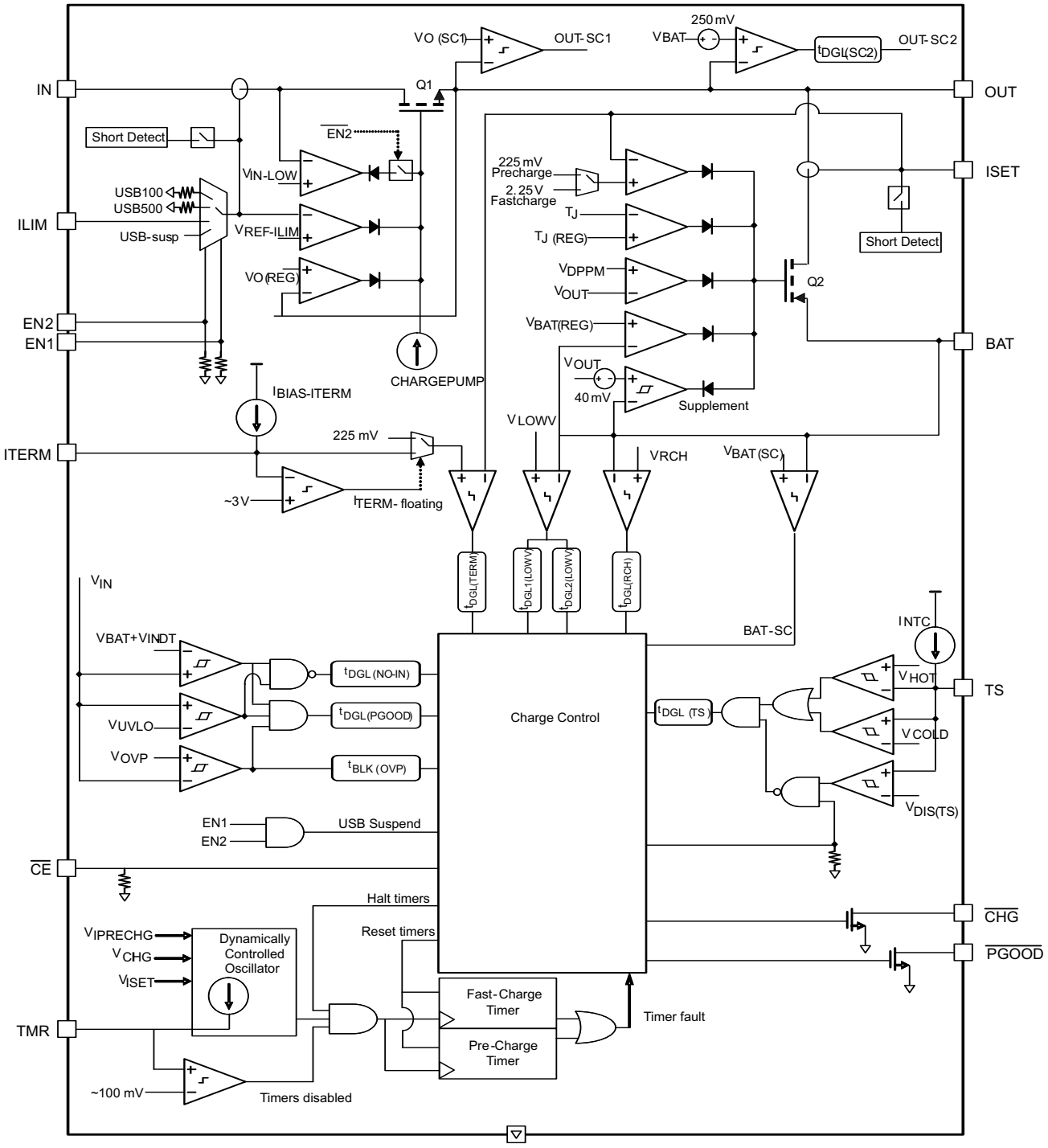
Figure 9. Precharge Current vs Battery Voltage

7 Detailed Description

7.1 Overview

The bq24232HA device is an integrated Li-ion linear charger and system power-path management device targeted at space-limited portable applications. The device powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination, and enables the system to run with a defective or absent battery pack. It also allows instant system turnon even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The devices feature dynamic power-path management (DPPM), which shares the source current between the system and battery charging and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management (V_{IN} – DPM) circuit reduces the input current limit if the input voltage falls below a threshold, preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

The bq24232HA remains in power-down mode when the input voltage at the IN pin is below the undervoltage lockout (UVLO) threshold.

During the power-down mode, the host commands at the control inputs ($\overline{CE}$, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PGOOD}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. During power-down mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

7.3.2 Power On

When V_{IN} exceeds the UVLO threshold, the bq24232HA powers up. While V_{IN} is below V_{BAT} + $V_{IN(DT)}$, the host commands at the control inputs ($\overline{CE}$, EN1, and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PGOOD}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

When V_{IN} rises above V_{BAT} + $V_{IN(DT)}$, $\overline{PGOOD}$ is low to indicate that the valid power status and the $\overline{CE}$, EN1, and EN2 inputs are read. The device enters standby mode whenever (EN1, EN2) = (1, 1) or if an input overvoltage condition occurs. In standby mode, Q1 is OFF and Q2 is ON. During standby mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

When the input voltage at IN is within the valid range: V_{IN} > UVLO **AND** V_{IN} > V_{BAT} + $V_{IN(DT)}$ **AND** V_{IN} < V_{OVP}, and the EN1 and EN2 pins indicate that the USB suspend mode is not enabled [(EN1, EN2) ≠ (HI, HI)], all internal timers and other circuit blocks are activated. The device checks for short circuits at the ISET and ILIM pins. If no short conditions exists, the device switches on the input FET Q1 with a 100-mA current limit to check for a short circuit at OUT. If V_{OUT} rises above V_{SC}, the FET Q1 switches to the current-limit threshold set by EN1, EN2, and R_{ILIM} and the device enters normal operation where the system is powered by the input source (Q1 is on), and the device continuously monitors the status of $\overline{CE}$, EN1, and EN2 as well as the input voltage conditions.

Feature Description (continued)

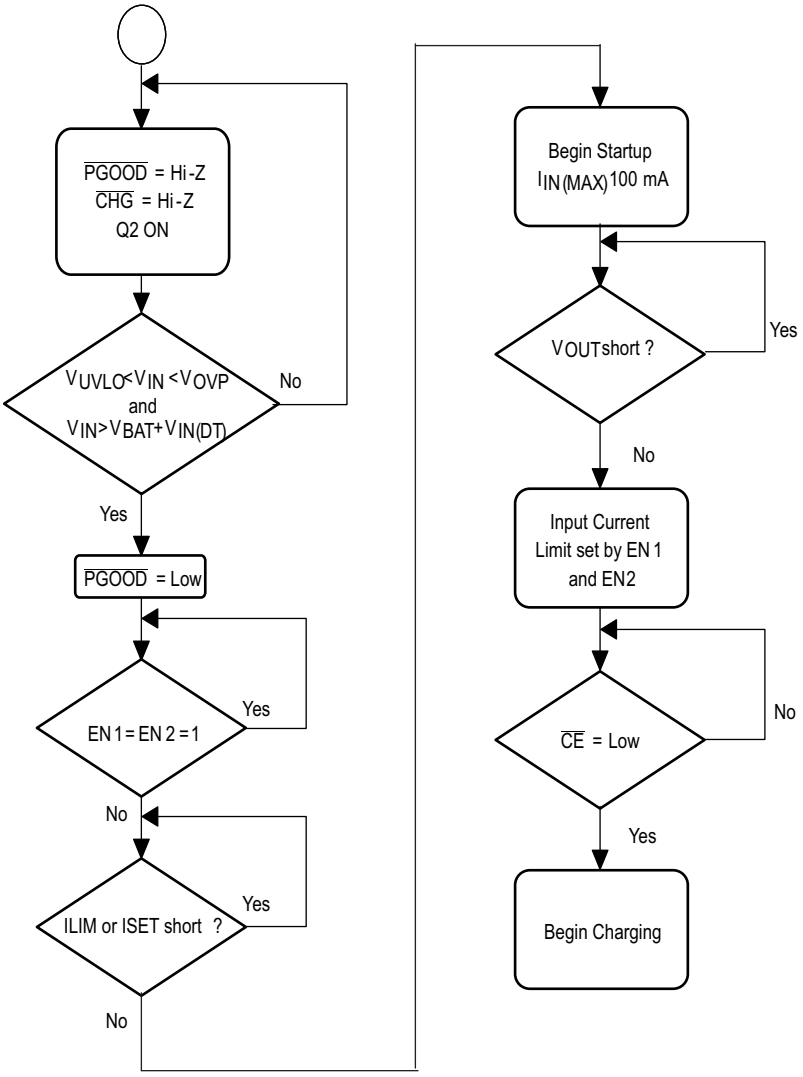


Figure 10. Start-Up Flow Diagram

7.3.3 Power-Path Management

The bq24232HA features an OUT output that powers the external load connected to the battery. This output is active whenever a source is connected to IN or BAT. The following sections discuss the behavior of OUT with a source connected to IN to charge the battery and a battery source only.

7.3.3.1 Input Source Connected – Adapter or USB

With a source connected, the power-path management circuitry of the bq24232HA monitors the input current continuously. The OUT output is regulated to a fixed voltage ($V_{O(REG)}$). The current into IN is shared between charging the battery and powering the system load at OUT. The bq24232HA has internal selectable current limits of 100 mA (USB100) and 500 mA (USB500) for charging from USB ports, as well as a resistor-programmable input current limit. See Table 1 for EN1, EN2 setting.

The bq24232HA is USB-IF compliant for the inrush current testing. The USB spec allows up to 10 μF to be hard-started, which establishes 50 μF as the maximum inrush charge value when exceeding 100 mA. The input current limit for the bq24232HA prevents the input current from exceeding this limit, even with system capacitances greater than 10 μF. Note that the input capacitance to the device must be selected small enough to prevent a violation (<10 μF), as this current is not limited.

Feature Description (continued)

The input current limit selection is controlled by the state of the EN1 and EN2 pins as shown in Table 1. When using the resistor-programmable current limit, the input current limit is set by the value of the resistor connected from the ILIM pin to VSS and is given by the Equation 1:

$$I_{IN\text{-}MAX} = K_{ILIM}/R_{ILIM} \quad (1)$$

The input current limit is adjustable up to 500 mA. The valid resistor range is 2.75 kΩ to 8.4 kΩ.

When the IN source is connected, priority is given to the system load. The DPPM and Battery Supplement modes are used to maintain the system load. Figure 11 illustrates examples of the DPPM and supplement modes. These modes are explained in detail in the following sections.

7.3.3.1.1 Input Voltage Dynamic Power Management, (V_{IN_DPM})

The bq24232HA uses the V_{IN_DPM} mode for operation from current-limited sources (including USB ports). The input voltage is monitored and compared to the $V_{IN\text{-}DPM}$ threshold (nominally ~ 4.5V). If the adaptor input voltage begins to collapse, the input current limit is reduced to prevent the supply voltage from falling further. This prevents the bq24232HA from crashing the external power source in case of a current-limited supply regardless of the input current limit setting (USB100, USB500, or external resistor-set ILIM mode)..

7.3.3.1.2 Dynamic Power Path Management (DPPM)

When the sum of the charging (BAT) and system (OUT) currents exceeds the preset maximum input current (programmed with EN1, EN2, and ILIM pins), the voltage at the OUT pin decreases. Once the voltage on the OUT pin falls to the VDPPM limit, the bq24232HA enters DPPM mode. In this mode, the charging current is reduced and power to the system is prioritized. Battery termination is disabled and the charge timer period is extended while in DPPM mode, because the charging current is less than the programmed value.

7.3.3.1.3 Battery Supplement Mode

If the system load current demand exceeds the input current limit, even with charging current reduced to zero, the OUT voltage continues to drop. When the OUT pin voltage drops below V_{BSUP1}, the partially charged battery supplements the external power source to provide current to the system. When the OUT pin voltage increases above V_{BSUP2} the device exits battery supplement mode and all system current is drawn from the external power source.

During supplement mode, the battery supplement current is not regulated; however, a short-circuit protection circuit is built in. If during battery supplement mode, the voltage at OUT drops 250 mV below the BAT voltage, the OUT output is turned off if the overload exists after $t_{DGL(SC2)}$. The short-circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. Battery termination is disabled while in supplement mode.

Feature Description (continued)

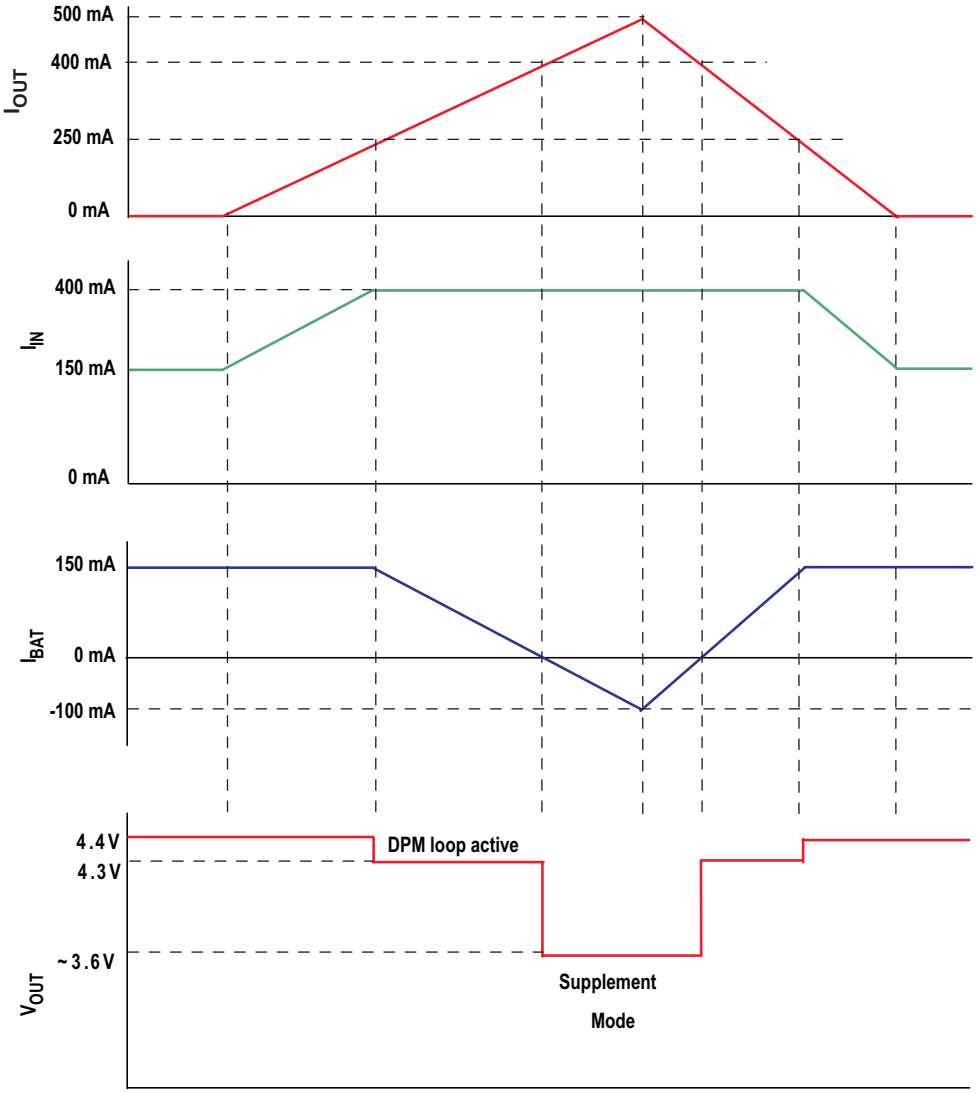


Figure 11. bq24232HA DPPM and Battery Supplement Modes (V_{OREG} = 4.4 V, V_{BAT} = 3.6 V, I_{LIM}= 400 mA, I_{CHG} = 150 mA)

7.3.3.2 Input Source not Connected

When no source is connected to the IN input, OUT is powered strictly from the battery. During this mode, the current into OUT is unregulated, similar to *Battery Supplement Mode*; however, the short-circuit circuitry is active. If the OUT voltage falls below the BAT voltage by 250 mV for longer than $t_{DGL(SC2)}$, OUT is turned off. The short-circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short-circuit remains, OUT is turned off and the counter restarts. This ON/OFF cycle continues until the overload condition is removed.

Feature Description (continued)

7.3.4 Thermal Regulation and Thermal Shutdown

The bq24232HA contain a thermal regulation loop that monitors the die temperature. If the die temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high VIN and heavy OUT system load conditions. Under these conditions, if the die temperature increases to $T_{J(OFF)}$, the input FET Q1 is turned OFF. FET Q2 is turned ON to ensure that the battery still powers the load on OUT. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the input FET Q1 is turned on and the device returns to thermal regulation. Continuous overtemperature conditions result in a hiccup mode. Safety timers are slowed proportionally to the charge current in thermal regulation. Battery termination is disabled during thermal regulation and thermal shutdown.

Note that this feature monitors the die temperature of the bq24232HA. This is not synonymous with ambient temperature. Self-heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm and the LDO mode for OUT.

A modified charge cycle with the thermal loop active is shown in Figure 12:

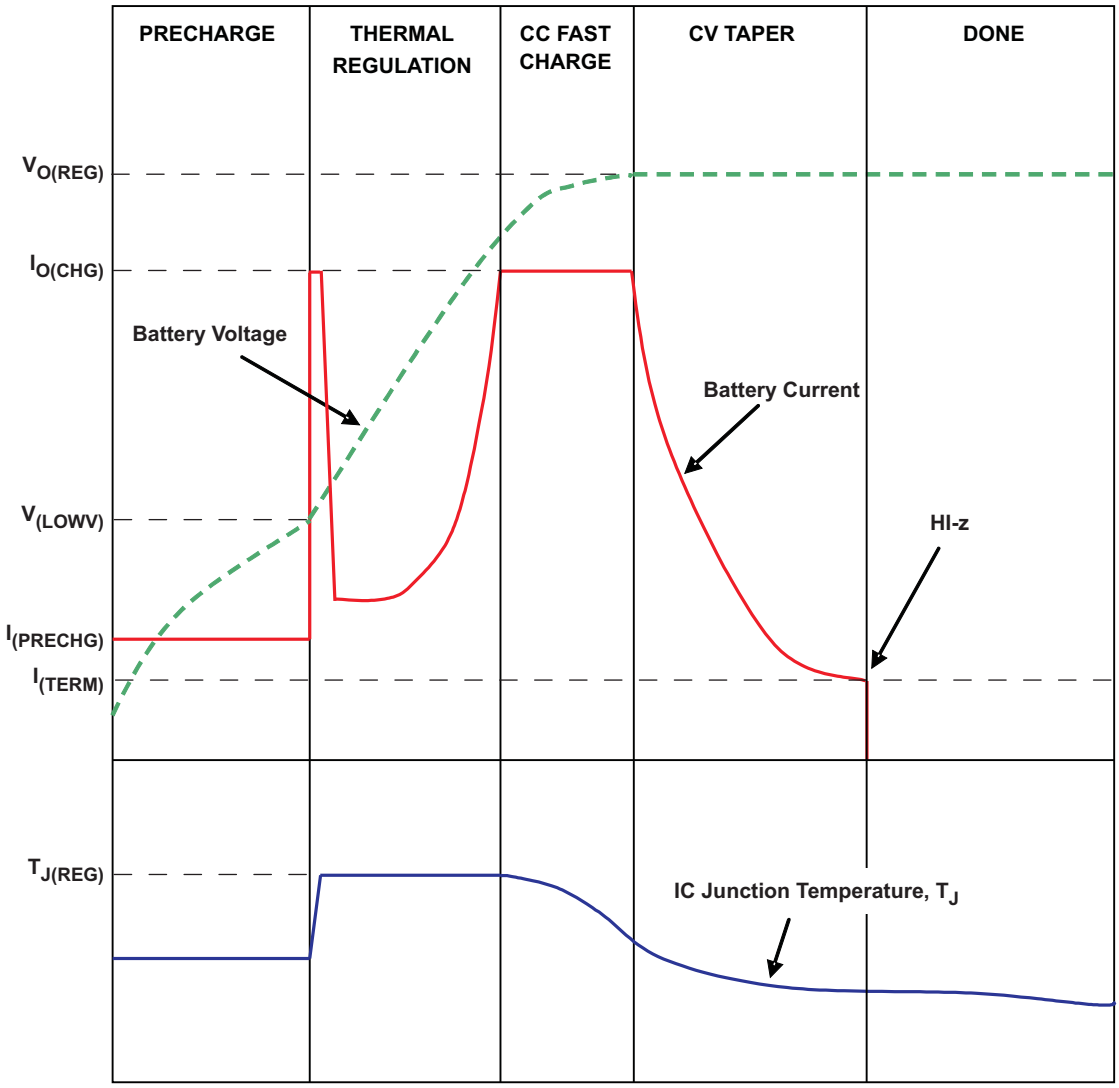


Figure 12. Modified Charge Cycle

Feature Description (continued)

7.3.5 Battery Pack Temperature Monitoring

The bq24232HA features an external battery pack temperature monitoring input. The TS input connects to the NTC resistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. Using the basic connection as shown in the *Typical Application Circuit* example, a nominal range of 0°C to 50°C is achieved using a standard 103AT – 2 type thermistor (ß = 3435) with no additional external components.

During charging, INTC is sourced to TS and the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range (V_{COLD} to V_{HOT}), charging is suspended. The timers maintain their values but suspend counting. When the voltage measured at TS returns to within the operation window, charging is resumed and the timers continue counting. When charging is suspended due to a battery pack temperature fault, the CHG pin remains low and continues to indicate charging

7.3.5.1 Modifying and Extending the Allowable Temperature Range for Charging

The nominal temperature range to allow charging is 0°C to 50°C when using a typical 103AT-2 type thermistor. However, the user can increase the range by adding two external resistors. See Figure 13 for the circuit. The values for Rs and Rp are calculated using the following equations:

$$Rs = \frac{-(R_{TH} + R_{TC}) \pm \sqrt{\left((R_{TH}+R_{TC})^2 - 4\left\{R_{TH} \times R_{TC} + \frac{V_H \times V_C}{(V_H - V_C) \times I_{TS}} \times (R_{TC} - R_{TH})\right\}\right)}}{2} \quad (2)$$

$$Rp = \frac{V_H \times (R_{TH} + R_S)}{I_{TS} \times (R_{TH} + R_S) - V_H} \quad (3)$$

where

- R_{TH}: Thermistor Hot Trip Value found in thermistor data sheet
- R_{TC}: Thermistor Cold Trip Value found in thermistor data sheet
- V_H: Hot Trip Threshold of the IC = 0.3 V nominal
- V_C: Cold Trip Threshold of the IC = 2.1 V nominal
- I_{TS}: Output Current Bias of the IC = 75 µA nominal
- NTC Thermsitor Semitec 103AT-2 Type or equivalent

Table 2 provides examples of the thermistor resistance at different temperatures and suggested typical Rs and Rp values, using 1% tolerance resistors that can extend the allowable temperature range beyond the standard 0°C – to – 50° C window.

Table 2. Example Thermistor Resistance and Suggested Typical Rs and Rp Values

COLD TEMP RESISTANCE AND TRIP THRESHOLD; Ω (°C)	HOT TEMP RESISTANCE AND TRIP THRESHOLD; Ω (°C)	EXTERNAL BIAS RESISTOR, Rs (Ω)	EXTERNAL BIAS RESISTOR, Rp (Ω)
28000 (–0.6)	4000 (51)	0	∞
28480 (–1)	3536 (55)	487	845000
28480 (–1)	3021 (60)	1000	549000
33890 (–5)	4026 (51)	76.8	158000
33890 (–5)	3536 (55)	576	150000
33890 (–5)	3021 (60)	1100	140000

RHOT and RCOLD are the thermistor resistance at the desired hot and cold temperatures, respectively. Note that the temperature window cannot be tightened more using the thermistor connected to TS, it can only be extended.

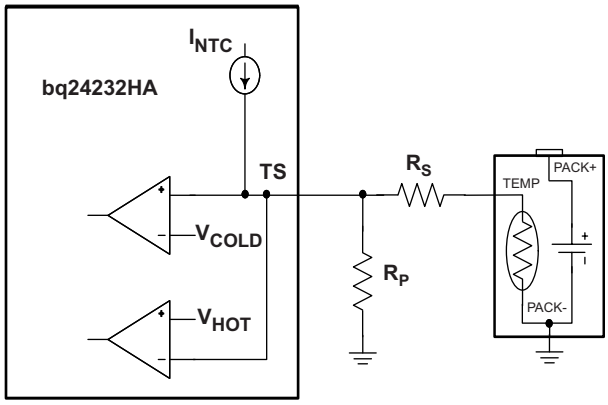


Figure 13. Extended TS Temperature Thresholds

7.4 Device Functional Modes

7.4.1 Battery Charging

Set $\overline{CE}$ low to initiate battery charging. First, the device checks for a short circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage. When the BAT voltage exceeds $V_{BAT(SC)}$, the battery charging continues. The battery is charged in three phases: conditioning precharge, constant-current fast charge (current regulation), and a constant-voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

Figure 14 illustrates a normal Li-ion charge cycle using the bq24232HA:

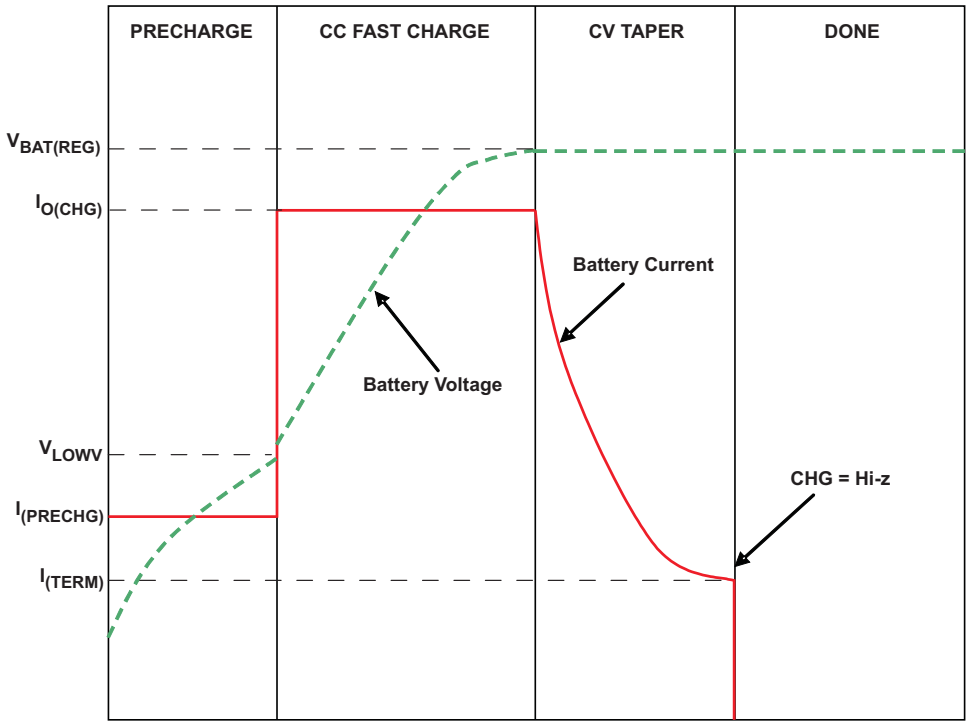


Figure 14. Normal Li-Ion Charge Cycle

Device Functional Modes (continued)

In the precharge phase, the battery is charged with the precharge current (I_{PRECHG}). Once the battery voltage crosses the V_{LOWV} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{TERM}, the $\overline{CHG}$ pin indicates *charging done* by going high impedance.

Note that termination detection is disabled whenever the charge rate is reduced because of the actions of the thermal loop, the DPPM loop, or the $V_{IN(LOW)}$ loop.

The value of the fast-charge current is set by the resistor connected from the ISET pin to VSS, and is given by the equation:

$$I_{CHG} = K_{ISET} / R_{ISET} \quad (4)$$

The charge current limit is adjustable from 25 mA to 500 mA. The valid resistor range is 1.8 kΩ to 36 kΩ. Note that if I_{CHG} is programmed as greater than the input current limit, the battery does not charge at the rate of I_{CHG}, but at the slower rate of $I_{IN(MAX)}$ (minus the load current on the OUT pin, if any). In this case, the charger timers are proportionately slowed down.

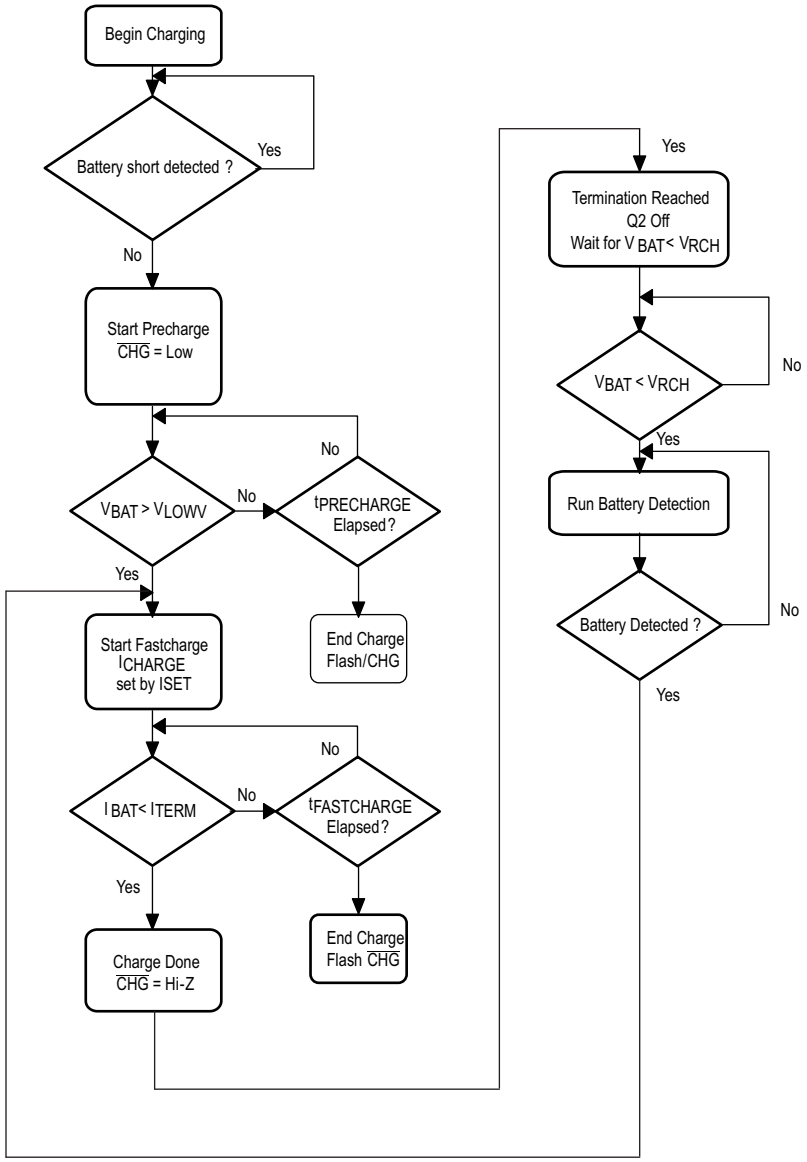


Figure 15. Battery Charging Flow Diagram

Device Functional Modes (continued)

7.4.1.1 Charge Current Translator

When the charger is enabled, internal circuits generate a current proportional to the charge current at the ISET input. The current out of ISET is 1/400 (±10%) of the charge current. This current, when applied to the external charge current programming resistor, R_{ISET}, generates an analog voltage that can be monitored by an external host to calculate the current sourced from BAT.

$$V_{ISET} = (I_{CHARGE} / 400) \times R_{ISET} \quad (5)$$

7.4.1.2 Battery Detection and Recharge

The bq24232HA automatically detects if a battery is connected or removed. Once a charge cycle is complete, the battery voltage is monitored. When the battery voltage falls below V_{RCH}, the battery detection routine is run. The detection routine first applies $I_{BAT(DET)}$ for t_{DET} to see if V_{BAT} drops below V_{LOWV}. If not, it indicates that the battery is still connected, but has discharged. If $\overline{CE}$ is low, the charger is turned on again to top off the battery. During this recharge cycle, the $\overline{CHG}$ output remains high-impedance as recharge cycles are not indicated by the $\overline{CHG}$ pin. If the BAT voltage falls below V_{LOWV} during the battery detection test, it indicates that the battery has been removed or the protector is open. Next, the precharge current is applied for t_{DET} to close the protector if possible. If the battery voltage does not rise above V_{RCH}, it indicates that the protector is closed, or a battery has been inserted, and a new charge cycle begins. If the voltage rises above V_{RCH}, the battery is determined missing and the detection routine continues. The battery detection runs until a battery is detected.

7.4.1.3 Adjustable Termination Threshold (ITERM Input)

The termination current threshold for the bq24232HA is user-programmable. Set the termination current by connecting a resistor from ITERM to VSS. For USB100, mode (EN1 = EN2 = VSS), the termination current value is calculated as:

$$I_{TERM} = 0.01 \times R_{ITERM} / R_{ISET} \quad (6)$$

In the other input current limit modes (EN1 ≠ EN2), the termination current value is calculated as:

$$I_{TERM} = 0.03 \times R_{ITERM} / R_{ISET} \quad (7)$$

The termination current is programmable up to 50% of the fast-charge current. The R_{ITERM} resistor must be less than 15 kΩ. Leave ITERM unconnected to select the default internally set termination current.

7.4.1.4 Dynamic Charge Timers (TMR Input)

The bq24232HA device contains internal safety timers for the precharge and fast-charge phases to prevent potential damage to the battery and the system. The timers begin at the start of the respective charge cycles. The timer values are programmed by connecting a resistor from TMR to VSS. The resistor value is calculated using the following equation:

$$t_{PRECHG} = K_{TMR} \times R_{TMR} \quad (8)$$

$$t_{MAXCHG} = 10 \times K_{TMR} \times R_{TMR} \quad (9)$$

Leave TMR unconnected to select the internal default timers. Disable the timers by connecting TMR to VSS. Reset the timers by toggling CE pin.

Note that timers are suspended when the device is in thermal shutdown, and the timers are slowed proportionally to the charge current when the device enters thermal regulation.

During the fast-charge phase, several events increase the timer durations.

1. The system load current activates the DPPM loop which reduces the available charging current
2. The input current is reduced because the input voltage has fallen to $V_{IN(LOW)}$
3. The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$

During each of these events, the internal timers are slowed down proportionately to the reduction in charging current. For example, if the charging current is reduced by half for two minutes, the timer clock is reduced to half the frequency and the counter counts half as fast resulting in only one minute of counted time.

Device Functional Modes (continued)

7.4.1.5 Status Indicators ($\overline{PGOOD}$, $\overline{CHG}$)

The bq24232HA contains two open-drain outputs that signal its status. The $\overline{PGOOD}$ output signals when a valid input source is connected. $\overline{PGOOD}$ is low when (V_{BAT} + $V_{IN(DT)}$) < V_{IN} < V_{OVP}. When the input voltage is outside of this range, $\overline{PGOOD}$ is high impedance.

The $\overline{CHG}$ output signals when a new charge cycle is initiated. After a charge cycle is initiated, $\overline{CHG}$ goes low once the battery is above the short-circuit threshold. $\overline{CHG}$ goes high impedance once the charge current falls below I_{TERM}. $\overline{CHG}$ remains high impedance until the input power is removed and reconnected or the $\overline{CE}$ pin is toggled. It does not signal subsequent recharge cycles.

Table 3. $\overline{PGOOD}$ Status Indicator

INPUT STATE	$\overline{PGOOD}$ OUTPUT
V_{IN} < V_{UVLO}	Hi impedance
V_{UVLO} < V_{IN} < $V_{IN(DT)}$ + V_{BAT}	Hi impedance
$V_{IN(DT)}$ + V_{BAT} < V_{IN} < V_{OVP}	Low
V_{IN} > V_{OVP}	Hi impedance

Table 4. $\overline{CHG}$ Status Indicator

CHARGE STATE	$\overline{CHG}$ OUTPUT
Charging	Low (first charge cycle)
Charging terminated	Hi impedance until power or $\overline{CE}$ is toggled
Recharging after termination	Hi impedance
Carging suspended by thermal loop	Low (first charge cycle)
Safety timers expired	Flashing at 2Hz
IC disabled or no valid input power	Hi impedance

7.4.1.5.1 Timer Fault

If the precharge timer expires before the battery voltage reaches V_{LOWV}, the bq24232HA indicates a fault condition. Additionally, if the battery current does not fall to I_{TERM} before the fast-charge timer expires, a fault is indicated. The $\overline{CHG}$ output flashes at approximately 2 Hz to indicate a fault condition.

7.4.2 Explanation of Deglitch Times and Comparator Hysteresis

Figures not to scale

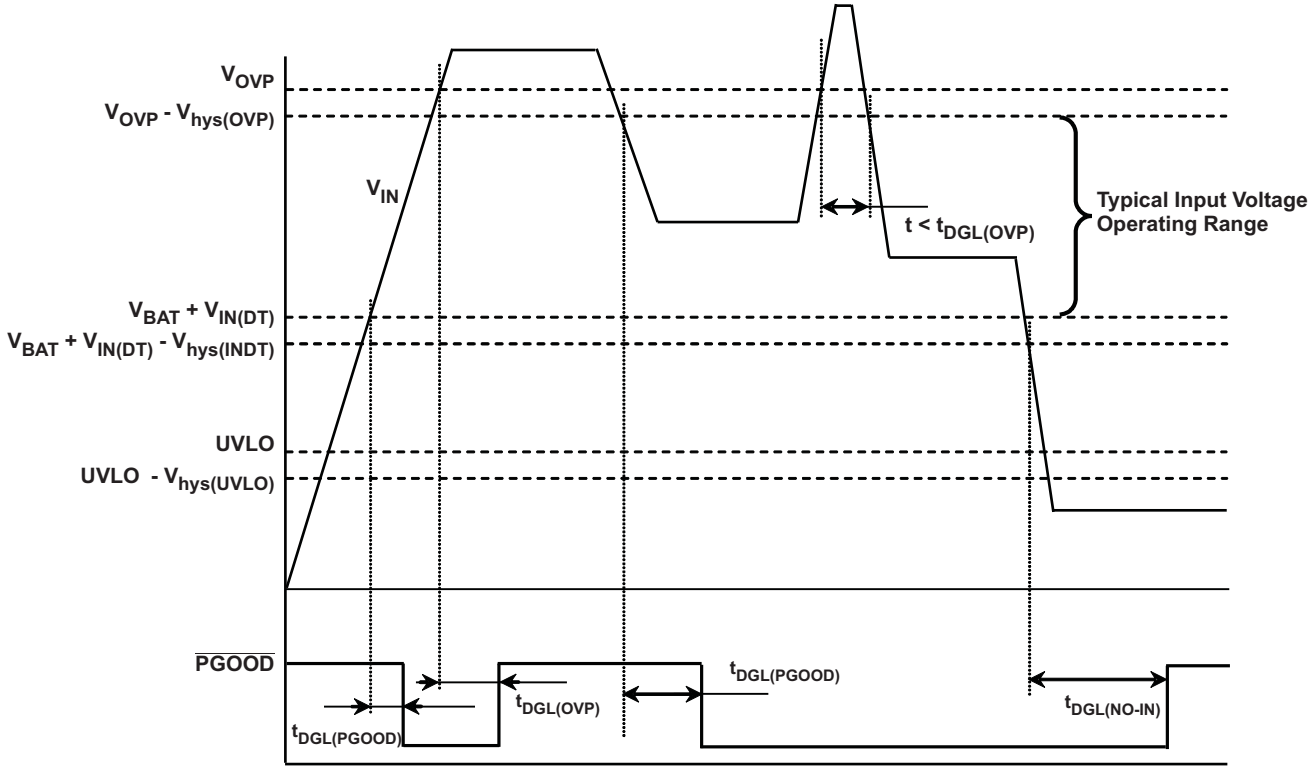


Figure 16. Power Up, Power Down

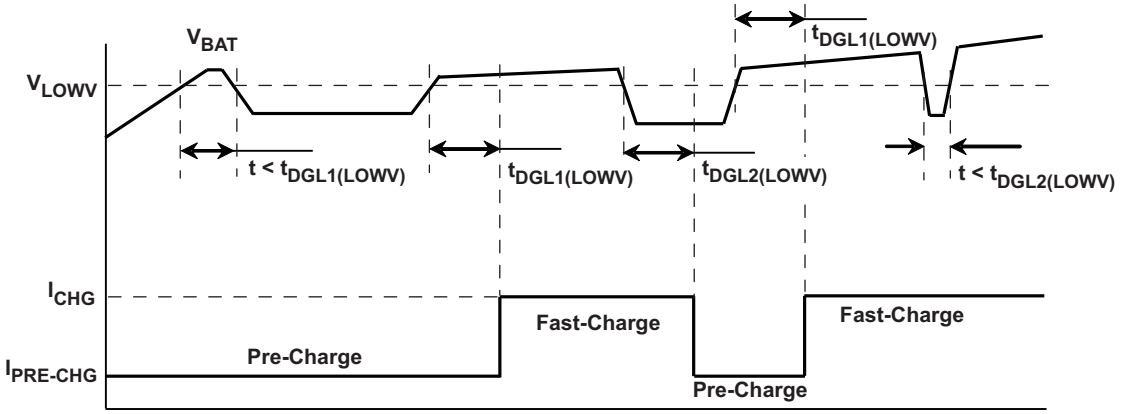


Figure 17. Pre- To Fast-Charge, Fast- To Precharge Transition – $T_{DGL1(LOWV)}$, $T_{DGL2(LOWV)}$

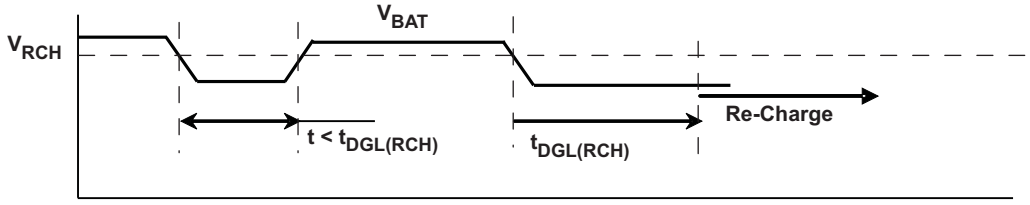


Figure 18. Recharge – $T_{DGL(RCH)}$

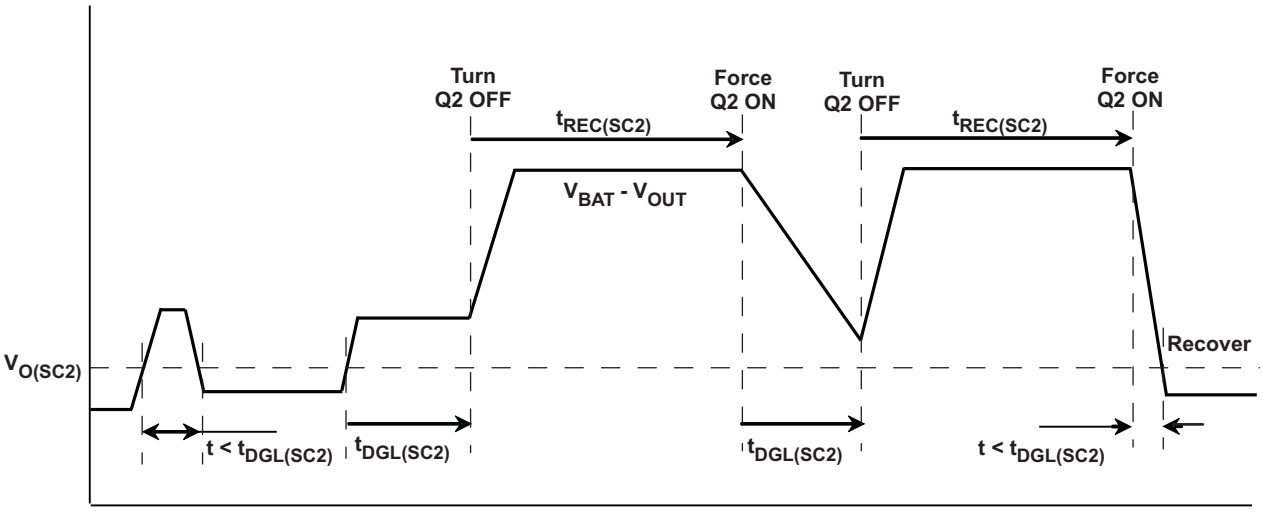


Figure 19. Out Short-Circuit – Supplement Mode

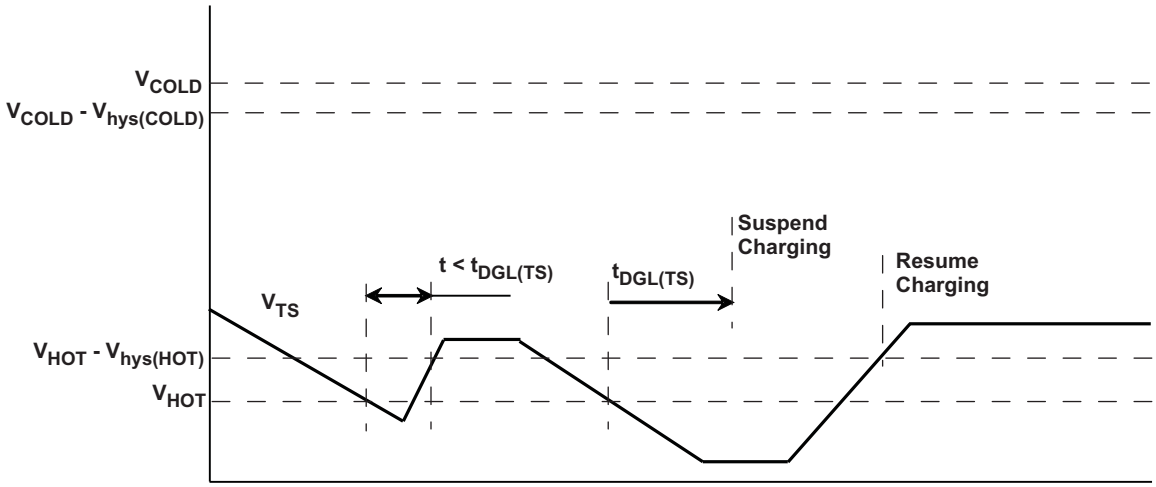


Figure 20. Battery Pack Temperature Sensing – TS Pin. Battery Temperature Increasing

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq24232HA device power the system while simultaneously and independently charging the battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The devices feature dynamic power-path management (DPPM), which shares the source current between the system and battery charging and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management (V_{IN} – DPM) circuit reduces the input current limit if the input voltage falls below a threshold, preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

The bq24232HA can be configured as host controlled for selecting different input current limits based on the input source connected; or, as a fully stand-alone device for applications that do not support multiple types of input sources.

8.2 Typical Application

See Figure 21 for the design example schematic.

V_{IN} = V_{UVLO} to V_{OVP} , $I_{FASTCHG}$ = 200 mA, $I_{IN(MAX)}$ = 500 mA, 25-mA Termination Current, ISET mode (EN1 = 0, EN2 = 1), Battery Temperature Charge Range 0°C to 50°C, 7.5-hour Fast Charge Safety Timer.

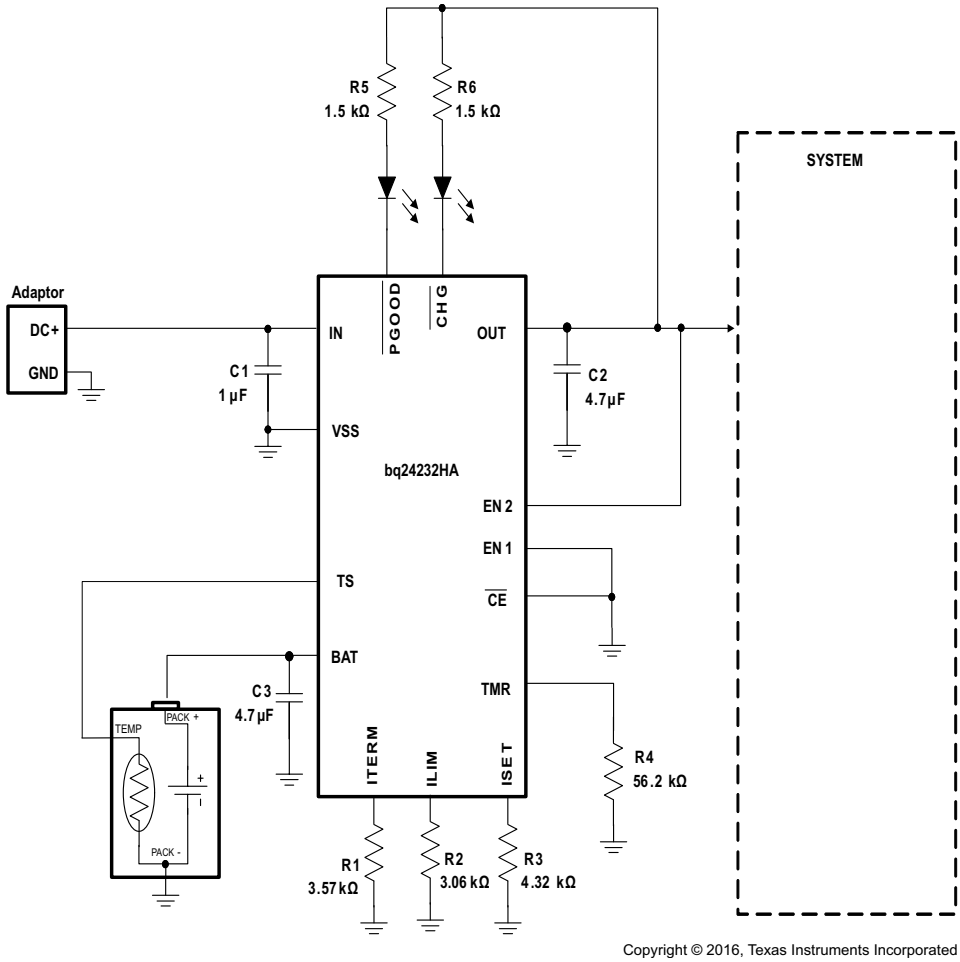


Figure 21. Using the bq24232HA in a Stand-Alone Charger Application

8.2.1 Design Requirements

- Supply voltage = 5 V
- Fast-charge current of approximately 200 mA; ISET - pin 16
- Input Current Limit =500 mA; ILIM - pin 12
- Termination Current = 25 mA - pin 15 (bq24232HA)
- Safety timer duration, Fast charge = 7.5 hours; TMR – pin 14
- TS – Battery Temperature Sense = 10 kΩ NTC (103AT-2)

8.2.2 Detailed Design Procedure

8.2.2.1 Calculations

8.2.2.1.1 Program The Fast-Charge Current (ISET):

R_{ISET} = K_{ISET} / I_{CHG}
K_{ISET} = 870 AΩ from the *Electrical Characteristics* table.
R_{ISET} = 870 AΩ/0.2 A = 4.35kΩ

Typical Application (continued)

Select the closest standard value, which for this case is 4.32 kΩ. Connect this resistor between ISET (pin 16) and V_{SS}.

8.2.2.1.2 Program The Input Current Limit (ILIM)

$R_{ILIM} = K_{ILIM} / I_{I\_MAX}$
K_{ILIM} = 1530 AΩ from the *Electrical Characteristics* table.
R_{ISET} = 1530 AΩ / 0.5 A = 3.06 kΩ

Select the closest standard value, which for this case is 3.06 kΩ. Connect this resistor between ILIM (pin 12) and V_{SS}.

8.2.2.1.3 Program The Termination Current Threshold (ITERM, bq24232HA)

$R_{ITERM} = R_{ISET} \times I_{TERM} / K_{ITERM}$

K_{ITERM} = 0.03 A from *Electrical Characteristics* table

R_{ITERM} = 4.32 kΩ × 0.025 A/0.03 A = 3.6 kΩ

Select the closest standard value, which for this case is 3.57 kΩ. Connect this resistor between ITERM (pin 15) and V_{SS}

8.2.2.1.4 Program 7.5-hour Fast-Charge Safety Timer (TMR)

$R_{TMR} = t_{MAXCHG} / (10 \times K_{TMR})$
K_{TMR} = 48 s/kΩ from the *Electrical Characteristics* table.
R_{TMR} = (7.5 hr × 3600 s/hr) / (10 × 48 s/kΩ) = 56.25 kΩ

Select the closest standard value, which for this case is 56.2 kΩ. Connect this resistor between TMR (pin 2) and V_{SS}.

8.2.2.2 TS Function

Use a 10-kΩ NTC thermistor in the battery pack (103AT). To disable the temperature sense function, use a fixed 10-kΩ resistor between the TS (pin 1) and V_{SS}. Pay close attention to the linearity of the chosen NTC so that it provides the desired hot and cold turnoff thresholds.

8.2.2.3 $\overline{CHG}$ and $\overline{PGOOD}$

LED Status: connect a 1.5-kΩ resistor in series with a LED between OUT and $\overline{CHG}$ and OUT and $\overline{PGOOD}$.

Processor Monitoring Status: connect a pullup resistor (approximately 100 kΩ) between the processor's power rail and $\overline{CHG}$ and $\overline{PGOOD}$.

8.2.2.4 Selecting IN, OUT, and BAT Pin Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input, output, and battery pins. Using the values shown on the application diagram is recommended. After evaluation of these voltage signals with real system operational conditions, the user can determine if capacitance values can be adjusted toward the minimum recommended values (dc load application) or higher values for fast, high-amplitude, pulsed load applications. Note, if the application is designed with high input voltage sources (bad adapters or wrong adapters), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16-V capacitor may be adequate for a 30-V transient (verify the tested rating with capacitor manufacturer).

Typical Application (continued)

8.2.3 Application Curves

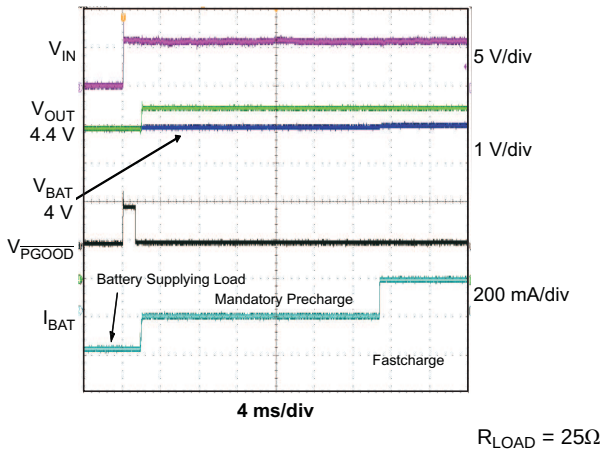


Figure 22. Adapter Plug-In With Battery Connected

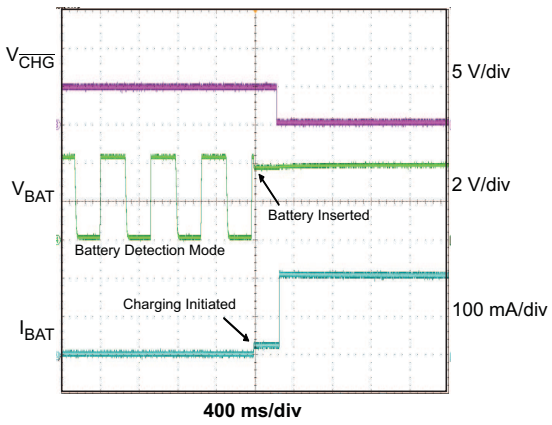


Figure 23. Battery Detection -- Insertion

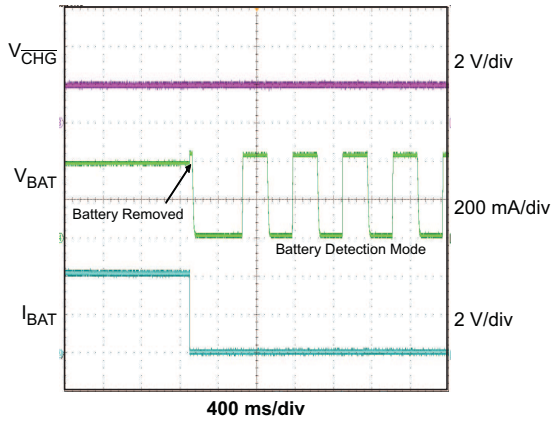


Figure 24. Battery Detection -- Removal

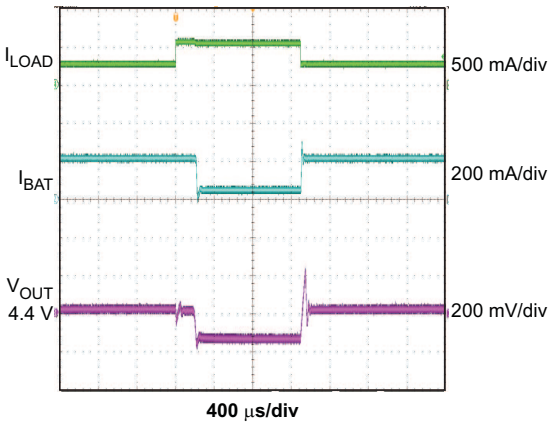


Figure 25. Entering and Exiting DPPM Mode

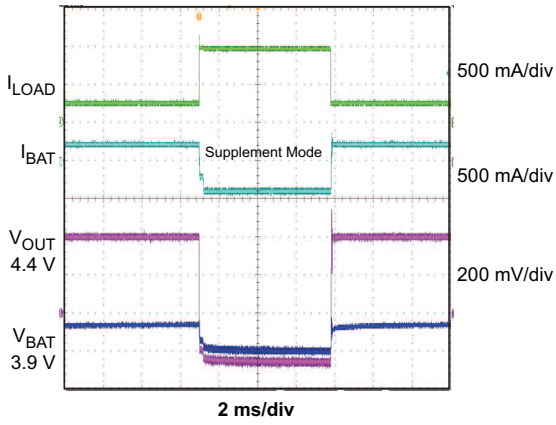


Figure 26. Entering and Exiting Battery Supplement Mode

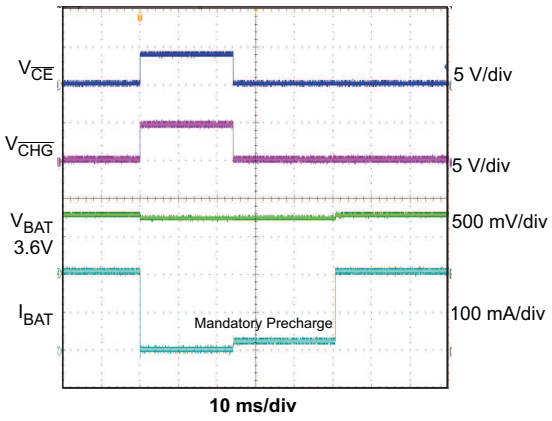


Figure 27. Charger ON/OFF Using CE

Typical Application (continued)

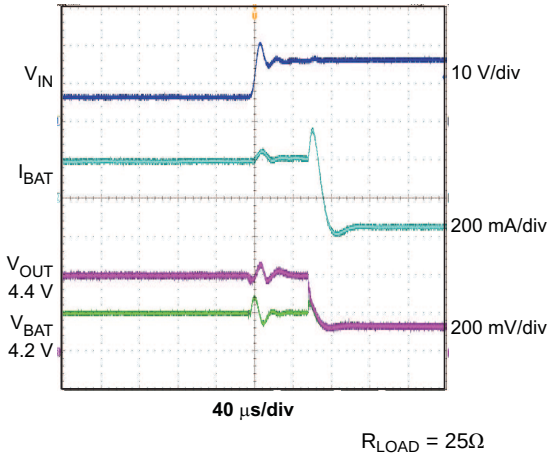


Figure 28. OVP Fault V_{IN} = 6 V to 15 V

9 Power Supply Recommendations

9.1 Requirements for OUT Output

In order to provide an output voltage on SYS, the bq24232HA requires a power supply between 4.35 V and 10 V to fully charge a battery. The supply must have at least 100 mA current rating connected to IN; or, a single-cell Li-Ion battery with voltage around 2.2 V connected to BAT. The source current rating needs to be at least 1.5 A in order to provide maximum output current to SYS.

9.2 USB Sources and Standard AC Adapters

In order for charging to occur the source voltage measured at the IN terminals of the IC, factoring in cable/trace losses from the source, must be greater than the VINDPM threshold (in USB mode), but less than the maximum values shown above. The current rating of the source must be higher than the load requirements for OUT in the application. For charging at a desired charge current of ICHRG, IIN > (ISYS+ ICHRG). The charger limits IIN to the current limit setting of EN1/EN2.

9.3 Half-Wave Adapters

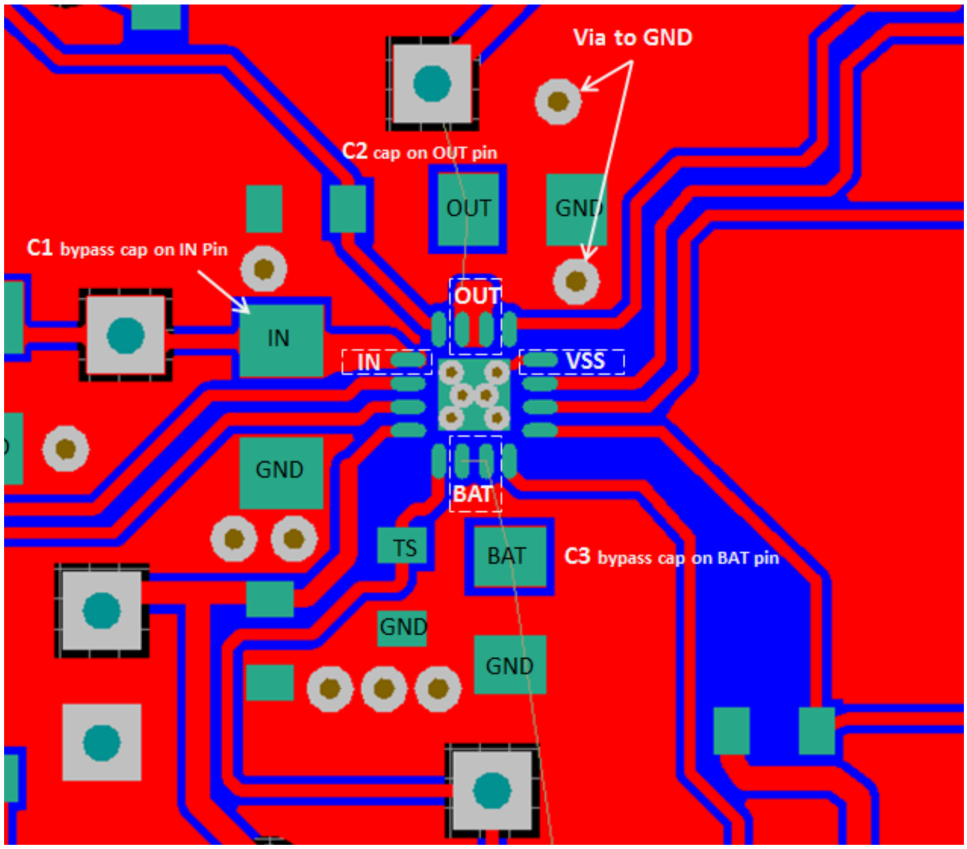
Some low-cost adapters implement a half rectifier topology, which causes the adapter output voltage to fall below the battery voltage during part of the cycle. To enable operation with low-cost adapters under those conditions, the bq24232HA keeps the charger on for at least 20 ms (typical) after the input power puts the part in sleep mode. This feature enables use of external low-cost adapters using 50-Hz networks.

10 Layout

10.1 Layout Guidelines

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) must be placed as close as possible to the bq24232HA, with short trace runs to both IN, OUT, and GND (thermal pad).
- All low-current GND connections must be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into the IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq24232HA is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed-circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application report entitled: *QFN/SON PCB Attachment* (SLUA271).

10.2 Layout Example



10.3 Thermal Considerations

The bq24232HA is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed-circuit board (PCB). The power pad must be directly connected to the Vss pin. Full PCB design guidelines for this package are provided in the application report entitled: *QFN/SON PCB Attachment* (SLUA271). The most common measure of package thermal performance is thermal impedance ($R_{\theta JA}$) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for $R_{\theta JA}$ is:

$$R_{\theta JA} = (T_J – T) / P$$

where

- T_J = Chip junction temperature
- T = Ambient temperature
- P = Device power dissipation (10)

Factors that can greatly influence the measurement and calculation of $R_{\theta JA}$ include:

1. Whether the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-ion batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically, after fast charge begins, the pack voltage increases to about 3.4 V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4 V is a good minimum voltage to use. This is easy to verify, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad must have multiple vias), the charge current and the battery voltage as a function of time. The fast-charge current starts to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P = [V_{(IN)} – V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} – V_{(BAT)}] \times I_{(BAT)} \quad (11)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for nontypical situations such as hot environments or higher than normal input source voltage. With that said, the IC still performs as described, if the thermal loop is always active.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

Application report *QFN/SON PCB Attachment*, SLUA271

11.3 Trademarks

Bluetooth is a trademark of Bluetooth SIG, Inc..
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24232HARGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-5 to 125	4232HA	Samples
BQ24232HARGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-5 to 125	4232HA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

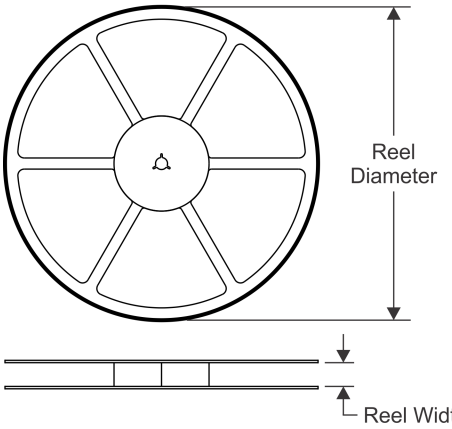
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

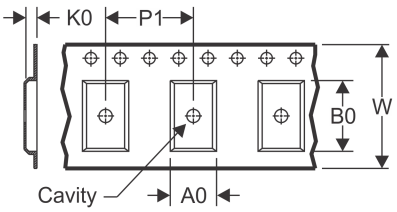
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

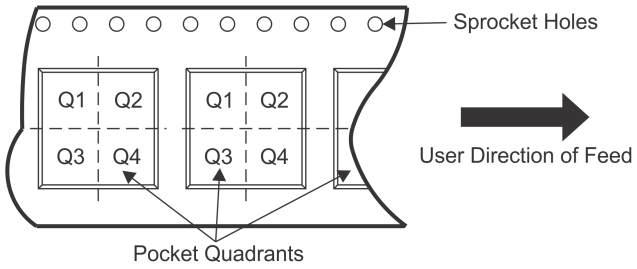


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

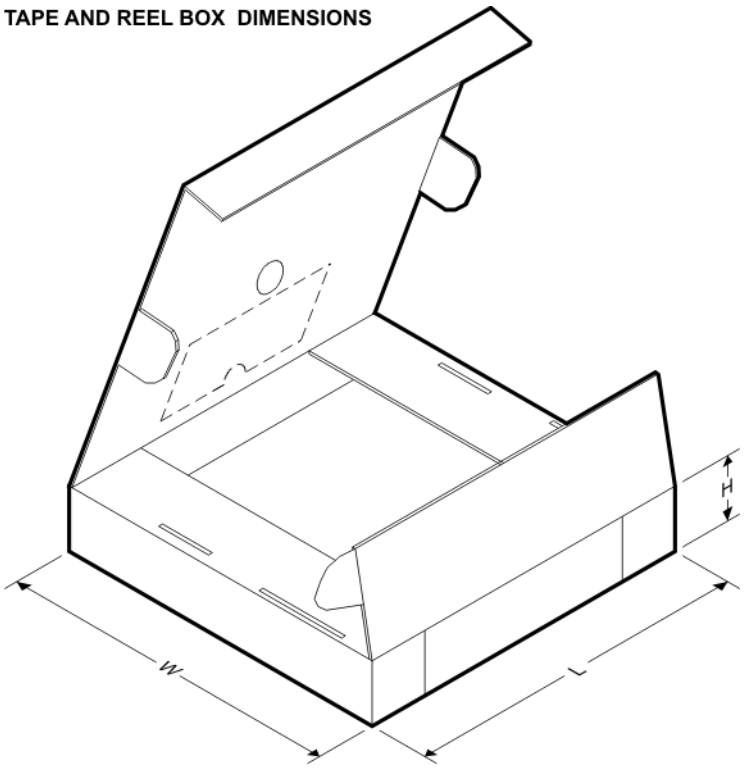
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24232HARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24232HARGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

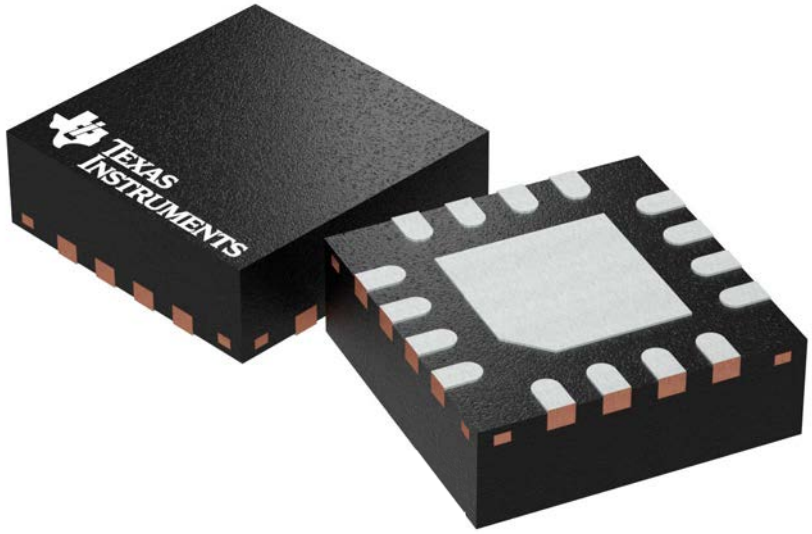


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24232HARGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
BQ24232HARGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



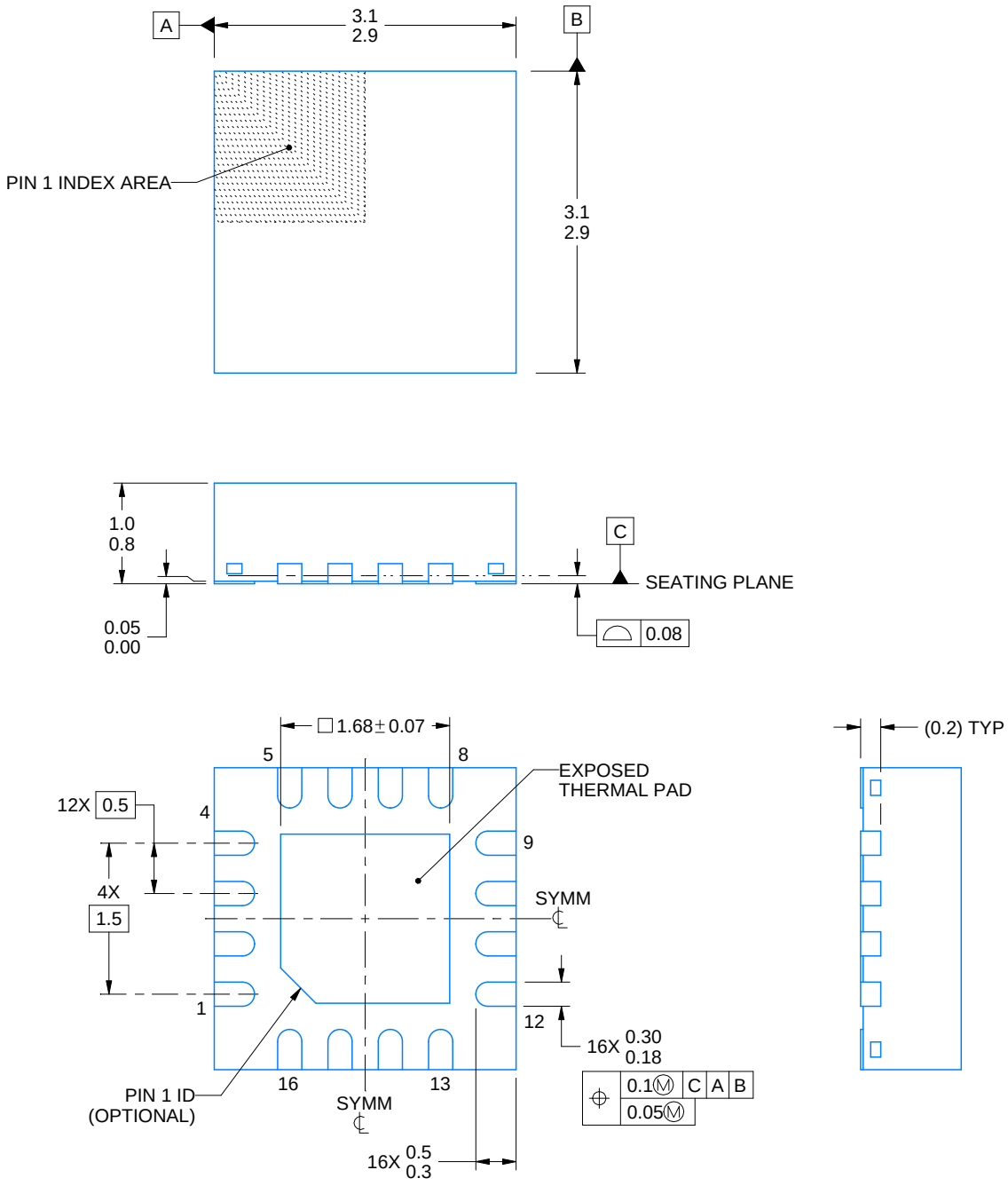
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016C

PACKAGE OUTLINE

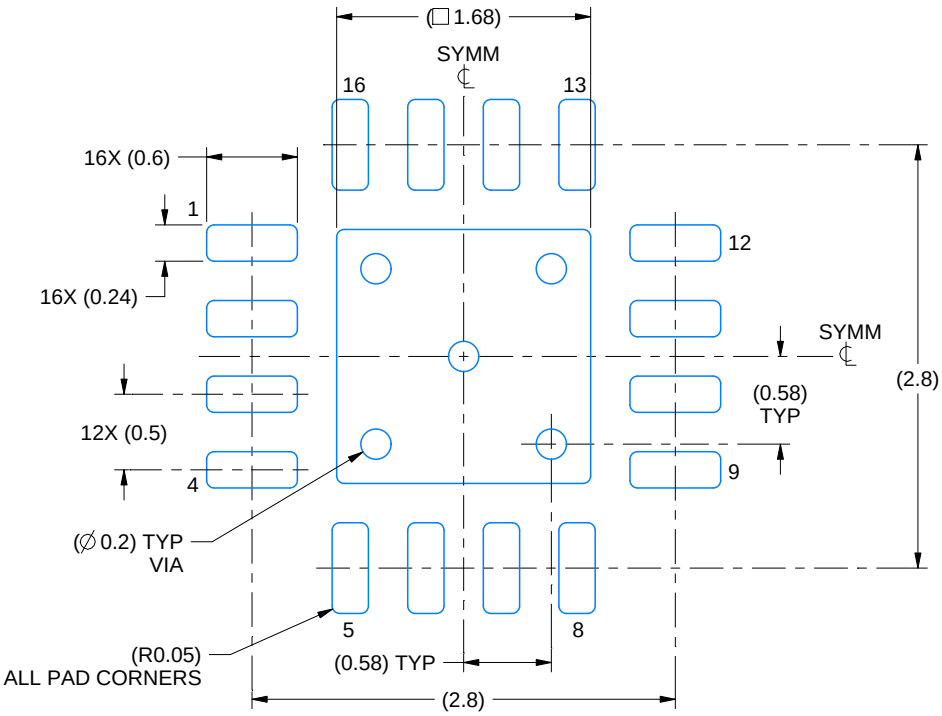
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

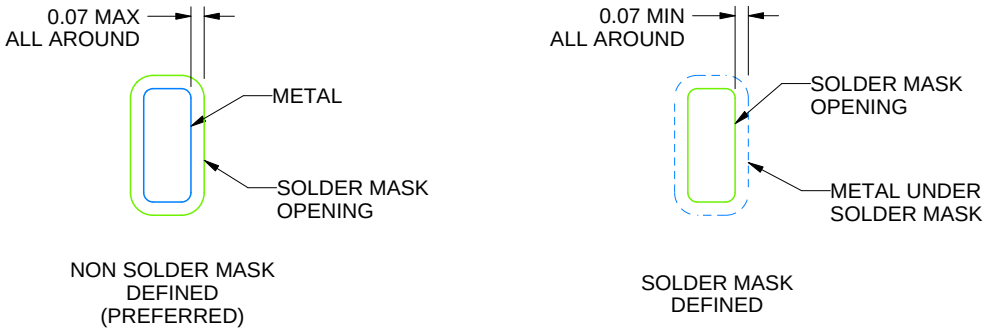


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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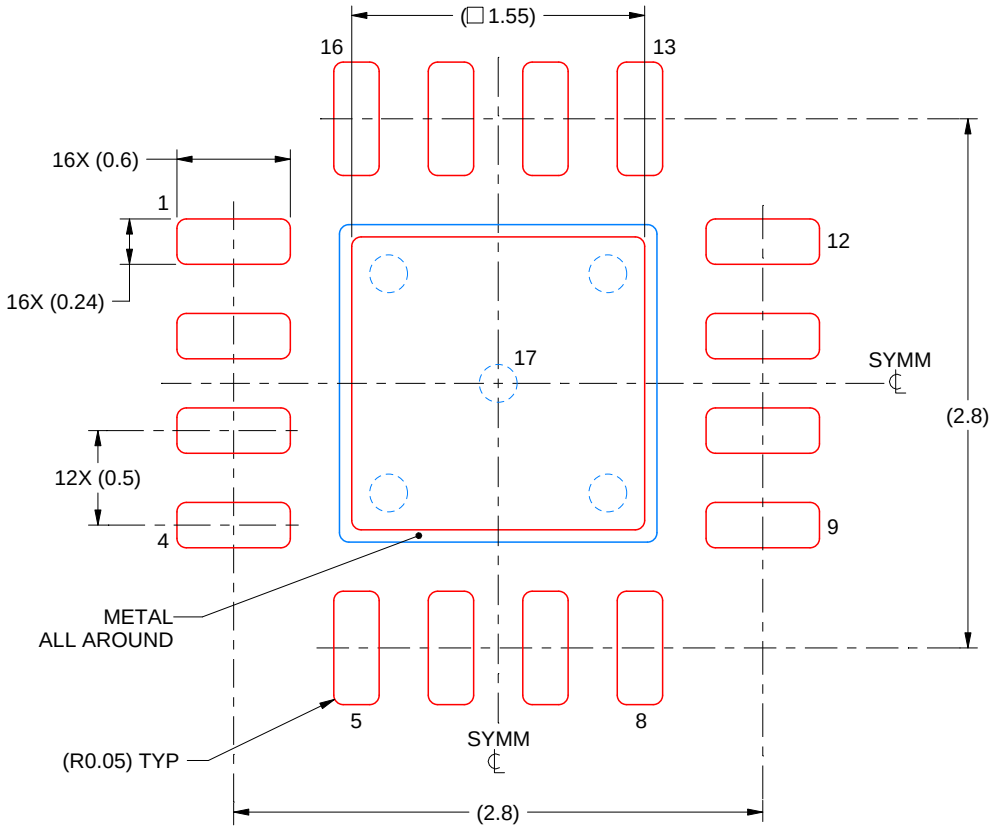
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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