FAIRCHILD
SEMICONDUCTOR®

November 2013

FDPF5N50UT

## N-Channel UniFET™ Ultra FRFET™ MOSFET
500 V, 4 A, 2 Ω

Features

- $R_{DS(on)}$ = 1.65 Ω (Typ.) @ V_{GS} = 10 V, I_D = 2 A
- Low Gate Charge (Typ. 11 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Applications

- LCD/LED TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. UniFET Ultra FRFET™ MOSFET has much superior body diode reverse recovery performance. Its trr is less than 50nsec and the reverse dv/dt immunity is 20V/nsec while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore UniFET Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

TO-220F

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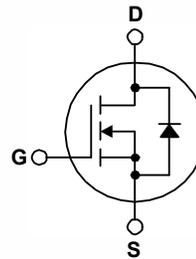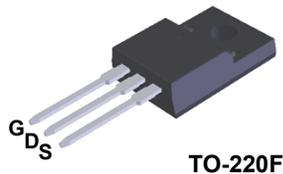
Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FDPF5N50UT	Unit
V_{DSS}	Drain to Source Voltage		500	V
V_{GSS}	Gate to Source Voltage		±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)	4*	A
		- Continuous (T_C = 100°C)	2.4*	
I_{DM}	Drain Current	- Pulsed (Note 1)	16*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		216	mJ
I_{AR}	Avalanche Current (Note 1)		4	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		8.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		20	V/ns
P_D	Power Dissipation	(T_C = 25°C)	28	W
		- Derate above 25°C	0.22	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDPF5N50UT	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDPF5N50UT	FDPF5N50UT	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V, T_J = 25°C	500	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	-	0.7	-	V/^{o}C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 400 V, T_C = 125°C	-	-	250	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2 A	-	1.65	2	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 2 A	-	4.8	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	-	485	650	pF
C_{oss}	Output Capacitance		-	65	90	pF
C_{rss}	Reverse Transfer Capacitance		-	5	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400 V, I_D = 4 A, V_{GS} = 10 V	-	11	15	nC
Q_{gs}	Gate to Source Gate Charge		-	3	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 4 A, V_{GS} = 10 V, R_G = 25 Ω	-	14	38	ns
t_r	Turn-On Rise Time		-	21	52	ns
$t_{d(off)}$	Turn-Off Delay Time		-	27	64	ns
t_f	Turn-Off Fall Time	(Note 4)	-	20	50	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	16	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 4 A	-	-	1.6	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 4 A, dI_F/dt = 100A/µs	-	36	-	ns
Q_{rr}	Reverse Recovery Charge		-	33	-	nC

Notes:

1: Repetitive rating: pulse-width limited by maximum junction temperature.

2: L = 27 mH, I_{AS} = 4 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.

3: I_{SD} ≤ 4 A, di/dt ≤ 200 A/µs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

4: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

V_{GS} = 15.0V
10.0V
8.0 V
7.0 V
6.5 V
6.0 V
5.5 V

I_D,Drain Current[A]

V_{DS},Drain-Source Voltage[V]

*Notes:
1. 250µs Pulse Test
2. T_C = 25°C
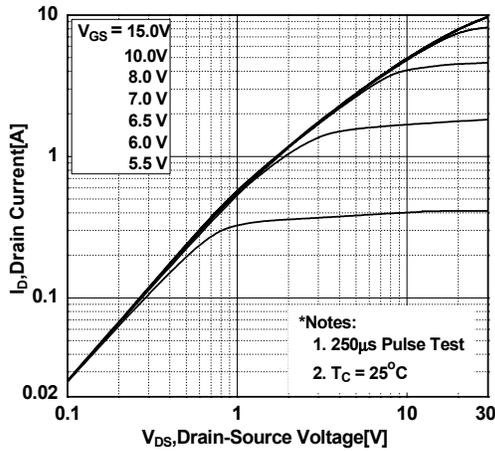
Figure 2. Transfer Characteristics

I_D,Drain Current[A]

150°C

25°C

*Notes:
1. V_{DS} = 20V
2. 250µs Pulse Test

V_{GS},Gate-Source Voltage[V]
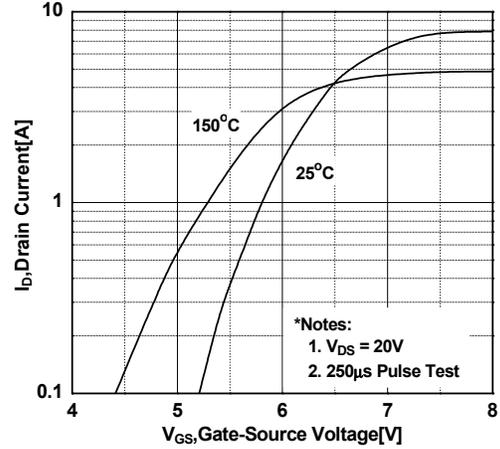
Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

$R_{DS(ON)}$ [Ω],
Drain-Source On-Resistance

V_{GS} = 10V

V_{GS} = 20V

*Note: T_J = 25°C

I_D, Drain Current [A]
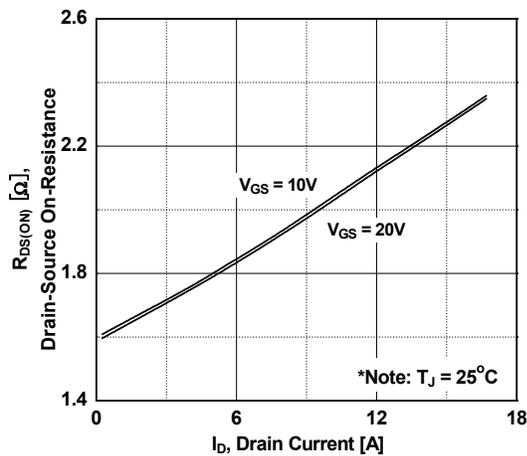
Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

I_S, Reverse Drain Current [A]

150°C

25°C

*Notes:
1. V_{GS} = 0V
2. 250µs Pulse Test

V_{SD}, Body Diode Forward Voltage [V]
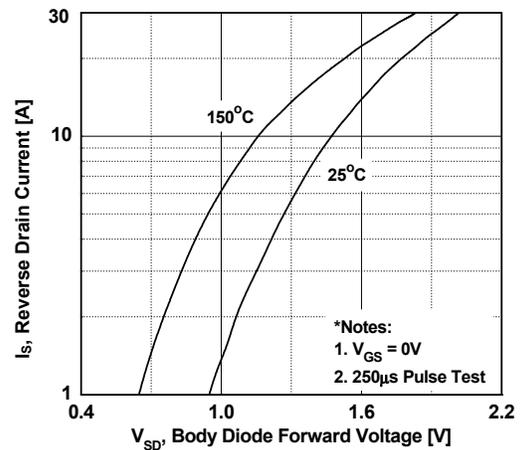
Figure 5. Capacitance Characteristics

Capacitances [pF]

C_{iss} = C_{gs} + C_{gd} (C_{ds} = shorted)
C_{oss} = C_{ds} + C_{gd}
C_{rss} = C_{gd}

*Note:
1. V_{GS} = 0V
2. f = 1MHz

C_{iss}

C_{oss}

C_{rss}

V_{DS}, Drain-Source Voltage [V]
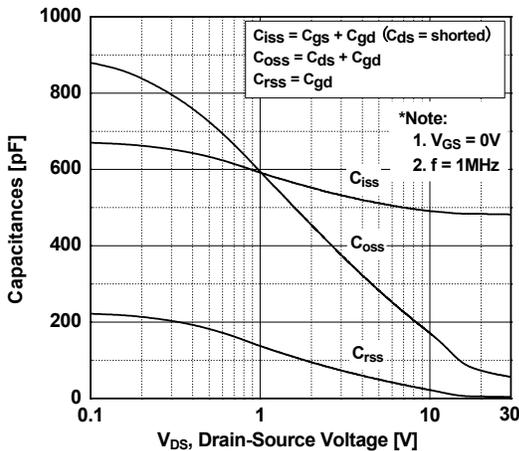
Figure 6. Gate Charge Characteristics

V_{GS}, Gate-Source Voltage [V]

V_{DS} = 100V
V_{DS} = 250V
V_{DS} = 400V

*Note: I_D = 4A

Q_g, Total Gate Charge [nC]
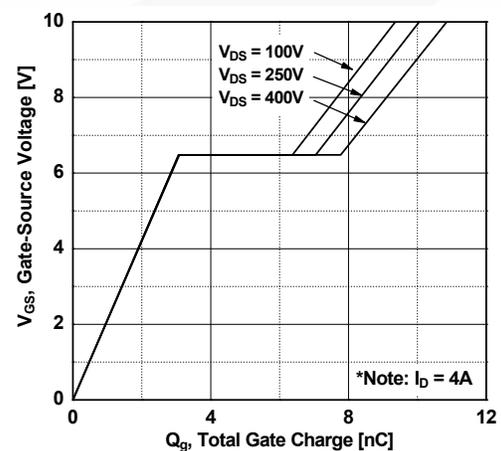
Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

*Notes:
1. $V_{GS} = 0V$
2. $I_D = 250\mu A$
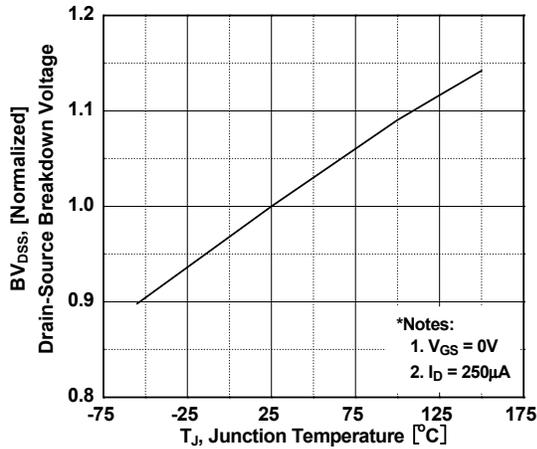
Figure 8. Maximum Safe Operating Area

Operation in This Area is Limited by $R_{DS(on)}$

*Notes:
1. $T_C = 25^oC$
2. $T_J = 150^oC$
3. Single Pulse
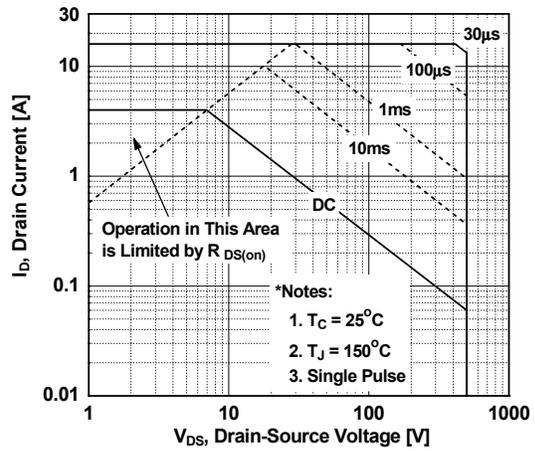
Figure 9. Maximum Drain Current vs. Case Temperature
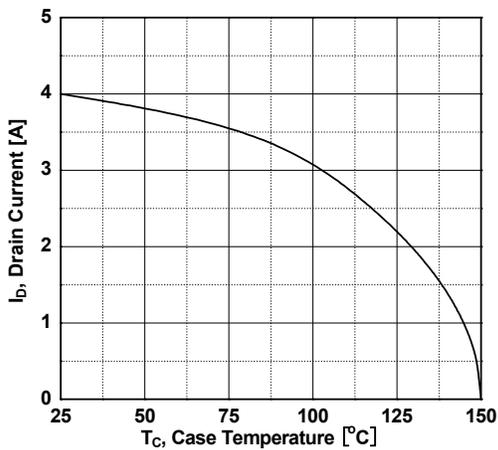
Figure 10. Transient Thermal Response Curve

*Notes:
1. $Z_{\theta JC}(t) = 4.5^oC/W$ Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$
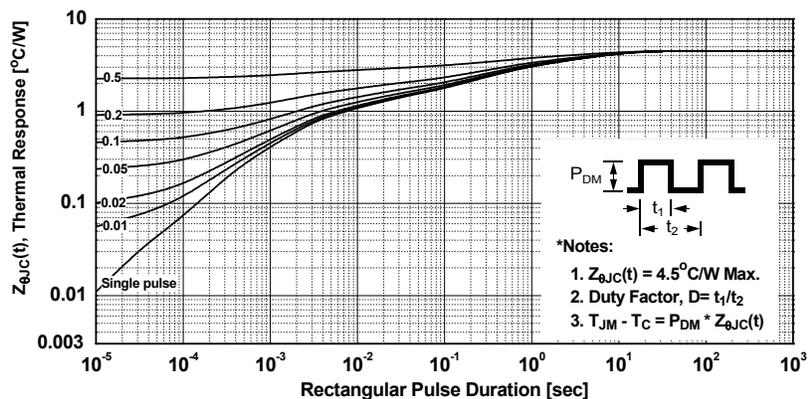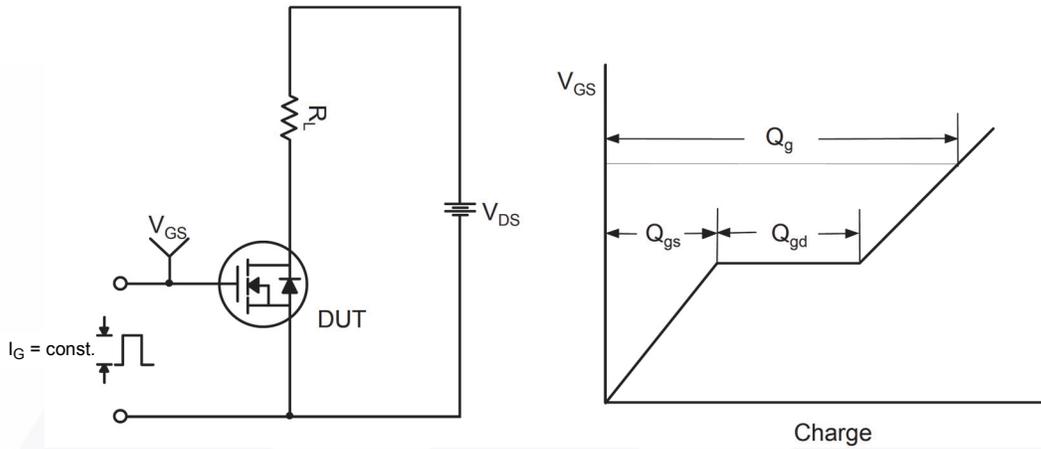
Figure 11. Gate Charge Test Circuit & Waveform
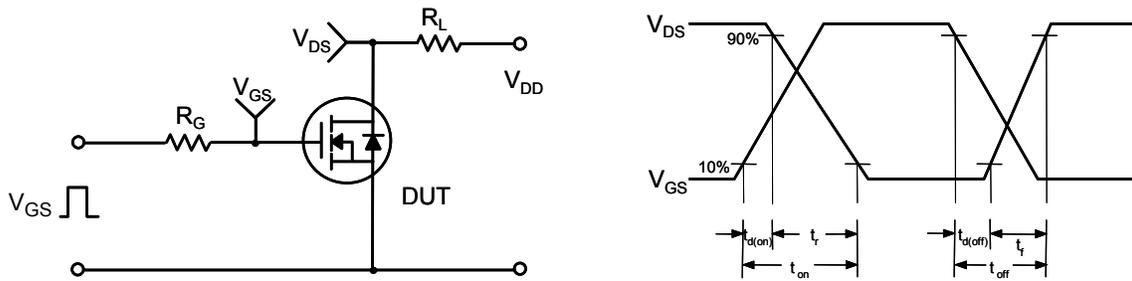
Figure 12. Resistive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$
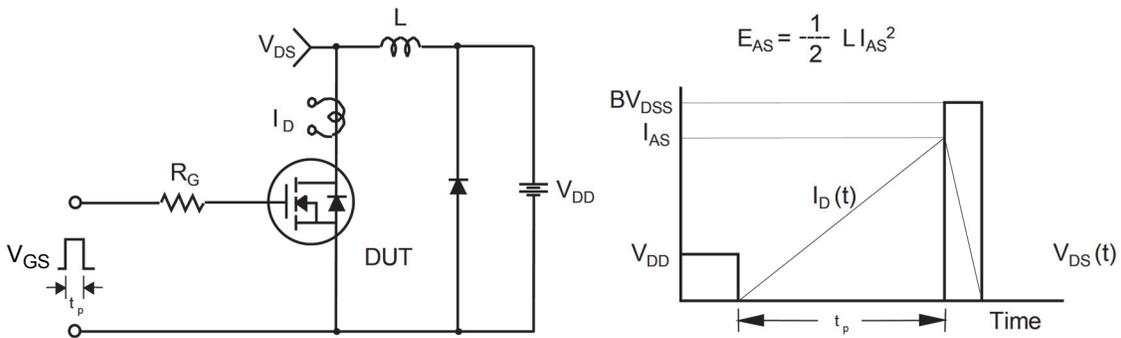
Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

- dv/dt controlled by R_G
- I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop
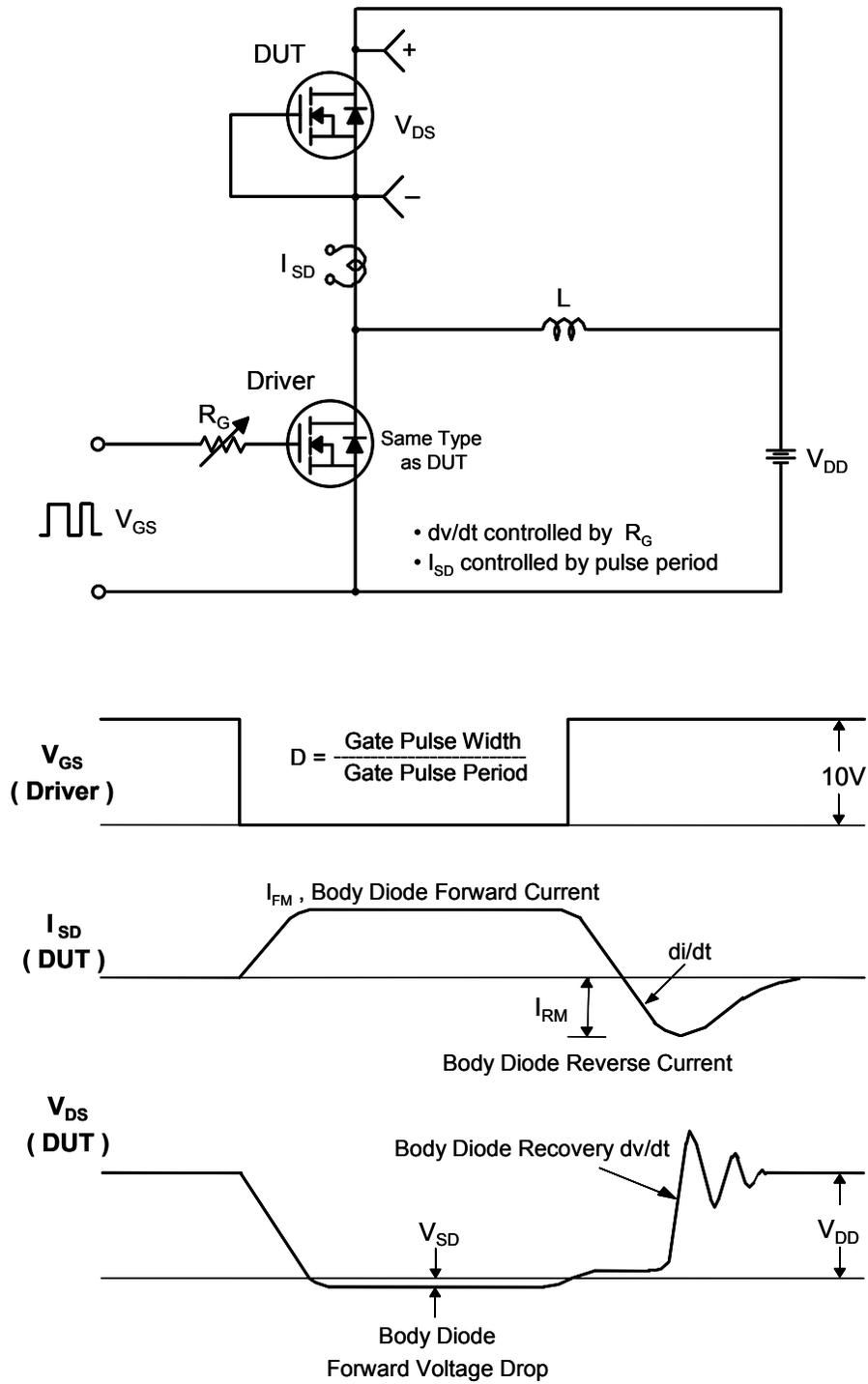
Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

Figure 15. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B. DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. OPTION 1 - WITH SUPPORT PIN HOLE.
   OPTION 2 - NO SUPPORT PIN HOLE.
G. DRAWING FILE NAME: TO220M03REV3

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