0.1 GHz to 20 GHz GaAs, Nonreflective, SP4T Switch

Data Sheet **HMC641ALP4E**

FEATURES

- Broadband frequency range: 0.1 GHz to 20 GHz
- Nonreflective 50 Ω design
- Low insertion loss: 3.0 dB at 20 GHz
- High isolation: 40 dB at 20 GHz
- High input linearity at 250 MHz to 20 GHz
  - P1dB: 24 dBm typical
  - IP3: 41 dBm typical
- High power handling
  - 26.5 dBm through path
  - 23 dBm terminated path
- Integrated 2 to 4 line decoder
- 24-lead, 4 mm × 4 mm LFCSP package
- ESD rating: 250 V (Class 1A)

APPLICATIONS

- Test instrumentation
- Microwave radios and very small aperture terminals (VSATs)
- Military radios, radars, and electronic counter measures (ECMs)
- Broadband telecommunications systems

FUNCTIONAL BLOCK DIAGRAM

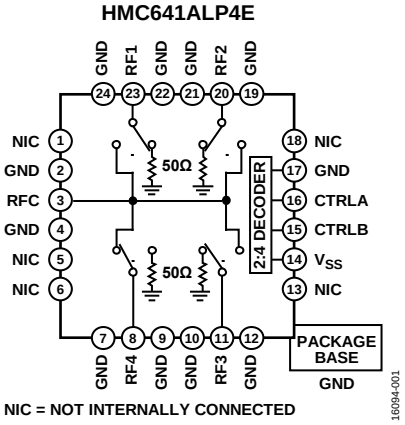

Figure 1.

GENERAL DESCRIPTION

The HMC641ALP4E is a general-purpose, nonreflective, single-pole, four-throw (SP4T) switch manufactured using a gallium arsenide (GaAs) process. This switch offers high isolation, low insertion loss, and on-chip termination of the isolated ports.

The switch operates with a negative supply voltage range of −5 V to −3 V and requires two negative logic control voltages.

The HMC641ALP4E includes an on-chip, binary 2 to 4 line decoder that provides logic control from two logic input lines.

The HMC641ALP4E comes in a 4 mm × 4 mm, 24-lead LFCSP package and operates from 0.1 GHz to 20 GHz.

Rev. B
Document Feedback

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8/2018—Rev. A to Rev. B

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Deleted Note 2, Table 2; Renumbered Sequentially ... 4
Updated Outline Dimensions ... 11
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7/2017—Rev. 00.1013 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

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SPECIFICATIONS

V_{SS} = −3 V or −5 V, V_{CTRL} = 0 V or V_{SS}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		20	GHz
INSERTION LOSS						
Between RFC and RF1 to RF4 (On)		0.1 GHz to 12 GHz		2.0	3.2	dB
		12 GHz to 20 GHz		3.0	4.2	dB
ISOLATION						
Between RFC and RF1 to RF4 (Off)		0.1 GHz to 12 GHz	30	42		dB
		12 GHz to 20 GHz	30	40		dB
RETURN LOSS						
RFC and RF1 to RF4 (On)		0.1 GHz to 12 GHz		18		dB
		12 GHz to 20 GHz		17		
RF1 to RF4 (Off)		0.1 GHz to 20 GHz		13		dB
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of radio frequency (RF) output		30		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		100		ns
INPUT LINEARITY [1]		250 MHz to 20 GHz				
1 dB Power Compression	P1dB	V_{SS} = −5 V	20	24		dBm
		V_{SS} = −3 V		22		dBm
Third-Order Intercept	IP3	10 dBm per tone, 1 MHz spacing				
		V_{SS} = −5 V		41		dBm
		V_{SS} = −3 V		41		dBm
SUPPLY		V_{SS} pin				
Voltage	V_{SS}		−5		−3	V
Current	I_{SS}			1.7	5	mA
DIGITAL CONTROL INPUTS		CTRLA and CTRLB pins				
Voltage	V_{CTL}					
Low	V_{INL}	V_{SS} = −5 V	−3		0	V
		V_{SS} = −3 V	−1		0	V
High	V_{INH}	V_{SS} = −5 V	−5		−4.2	V
		V_{SS} = −3 V	−3		−2.2	V
Current	I_{CTL}					
Low	I_{INL}			30		µA
High	I_{INH}			0.5		µA

[1] Input linearity performance degrades at frequencies less than 250 MHz.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Negative Supply Voltage (V_{SS})	−7 V
Digital Control Input Voltage	V_{SS} − 0.5 V to + 1 V
RF Input Power[1]	
(f = 250 MHz to 20 GHz, T_{CASE} = 85°C)	
V_{SS} = −5 V	
Through Path	26.5 dBm
Terminated Path	23 dBm
Hot Switching	20 dBm
V_{SS} = −3 V	
Through Path	21 dBm
Terminated Path	20 dBm
Hot Switching	17 dBm
Temperature	
Junction, T_J	150°C
Storage	−65°C to +150°C
Reflow	260°C
Junction to Case Thermal Resistance, θ_{JC}	
Through Path	201°C/W
Terminated Path	321°C/W
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

[1] For power derating at frequencies less than 250 MHz, see Figure 2.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

POWER DERATING CURVES

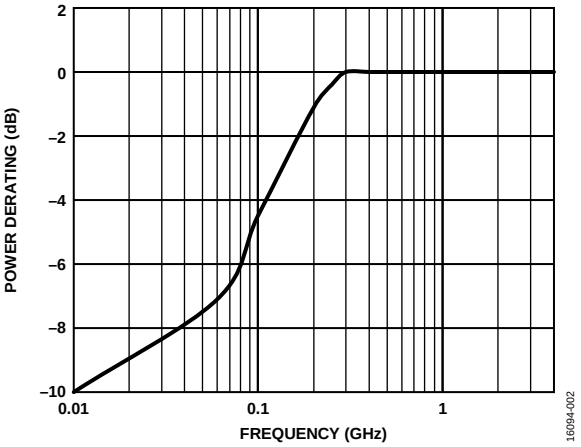
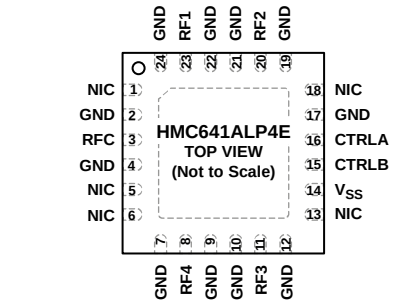


Figure 2. Power Derating at Frequencies Less than 250 MHz

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THE PINS ARE NOT CONNECTED INTERNALLY; HOWEVER, ALL DATA SHOWN IN THIS DATA SHEET IS MEASURED WITH THESE PINS CONNECTED TO RF/DC GROUND EXTERNALLY.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE RF/DC GROUND OF THE PCB.

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 6, 13, 18	NIC	Not Internally Connected. The pins are not connected internally; however, all data shown in this data sheet is measured with these pins connected to RF/dc ground externally.
2, 4, 7, 9, 10, 12, 17, 19, 21, 22, 24	GND	Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB).
3	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
8	RF4	RF4 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
11	RF3	RF3 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
14	V_{SS}	Negative Supply Voltage Pin.
15	CTRLB	Control Input 2 Pin. See Table 4 for the control voltage truth table.
16	CTRLA	Control Input 1 Pin. See Table 4 for the control voltage truth table.
20	RF2	RF2 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
23	RF1	RF1 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

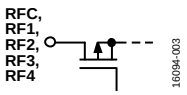


Figure 4. RFC to RF4 Interface Schematic

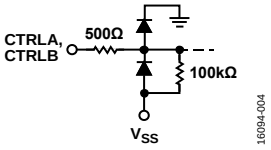


Figure 5. CTRLA and CTRLB Interface Schematic

TYPICAL PERFORMANCE CHARCTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

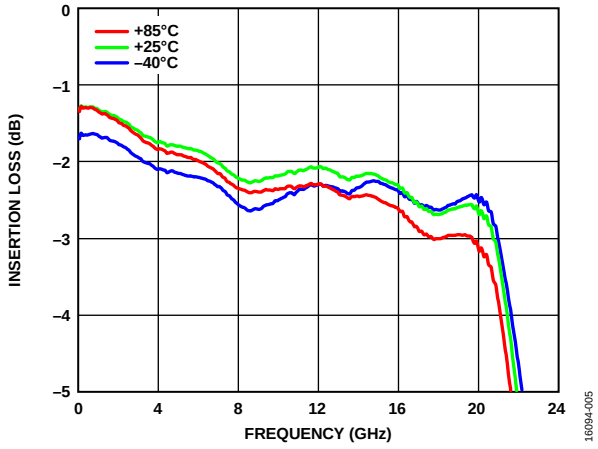


Figure 6. Insertion Loss Between RFC and RF1 vs. Frequency at Various Temperatures

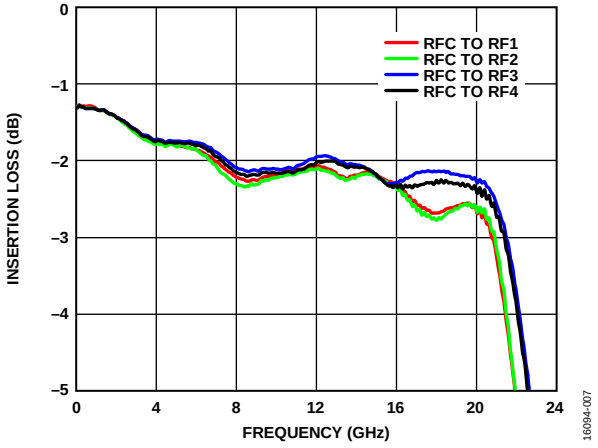


Figure 8. Insertion Loss Between RFC to RFx vs. Frequency

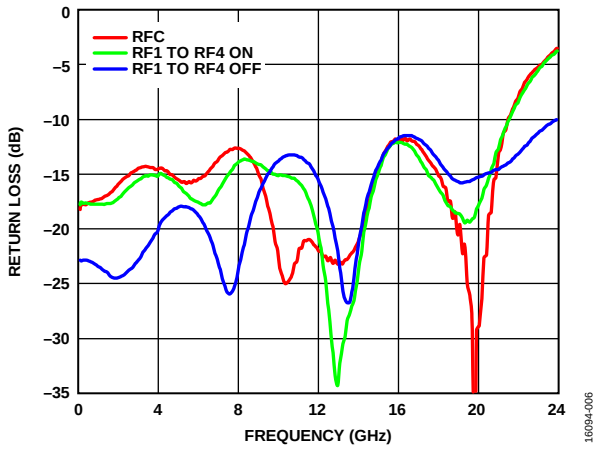


Figure 7. Return Loss for RFC, RF1 to RF4 On, and RF1 to RF4 Off vs. Frequency

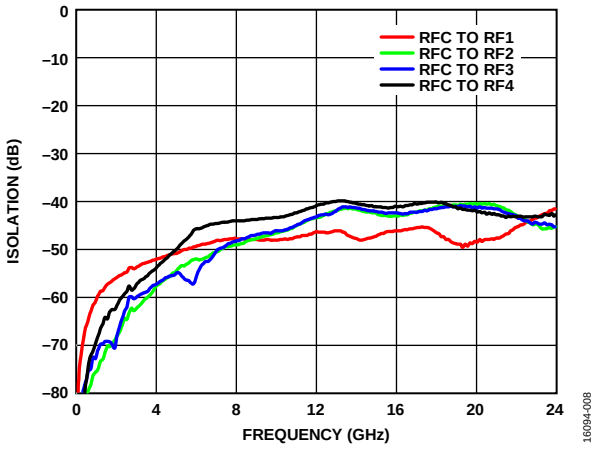


Figure 9. Isolation Between RFC and RFx vs. Frequency

INPUT POWER COMPRESSION AND IP3

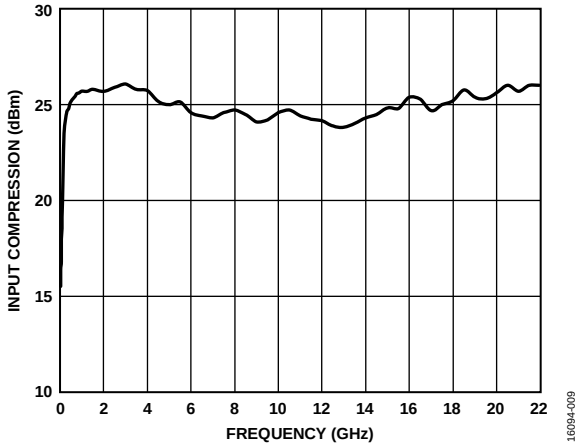


Figure 10. Input Compression vs. Frequency at Room Temperature, $V_{SS} = -5$ V

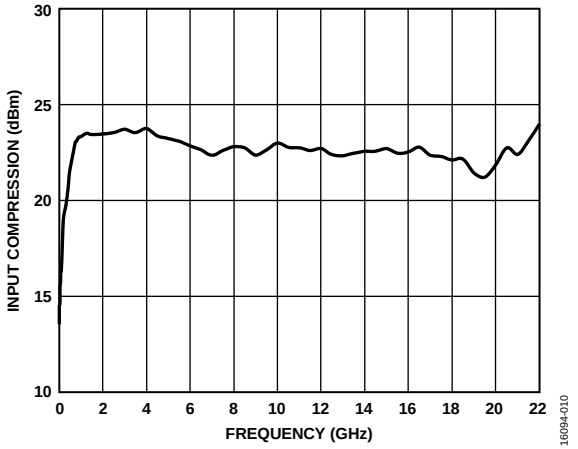


Figure 12. Input Compression vs. Frequency at Room Temperature, $V_{SS} = -3$ V

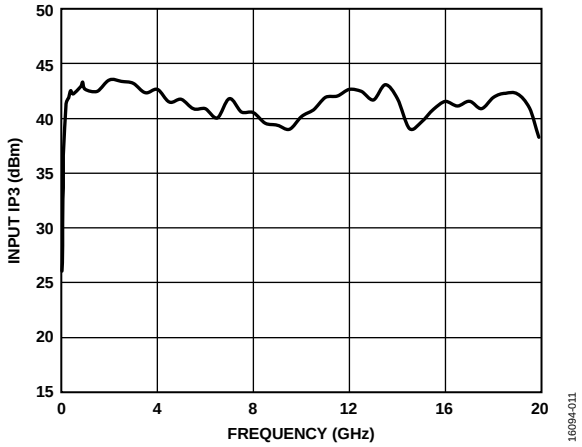


Figure 11. Input IP3 vs. Frequency at Room Temperature, $V_{SS} = -5$ V

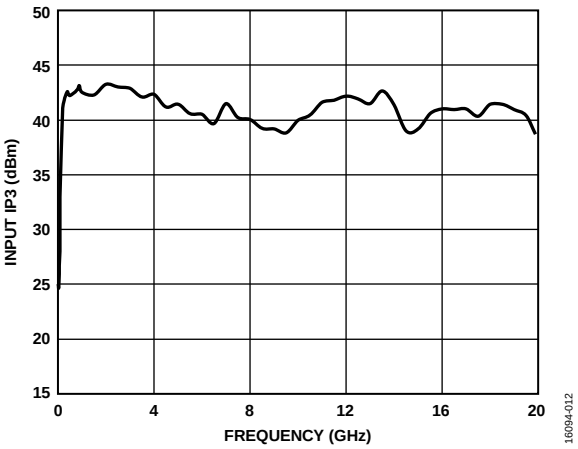


Figure 13. Input IP3 vs. Frequency at Room Temperature, $V_{SS} = -3$ V

THEORY OF OPERATION

The HMC641ALP4E requires a negative supply voltage at the V_{SS} pin and two logic control inputs at the CTRLA and CTRLB pins to control the state of the RF paths.

Depending on the logic level applied to the CTRLA pin and the CTRLB pin, one RF path is in the insertion loss state while the other three paths are in an isolation state (see Table 4). The insertion loss path conducts the RF signal between the RF throw pin and RF common pin while the isolation paths provide high loss between RF throw pins terminated to internal 50 Ω resistors and the insertion loss path.

The ideal power-up sequence is as follows:

1. Ground to the die bottom.
2. Power up V_{SS}.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the V_{SS} supply can inadvertently become forward-biased and damage the internal ESD protection structures.
4. Apply an RF input signal. The design is bidirectional; the RF input signal can be applied to the RFC pin while the RF throw pins are the outputs, or the RF input signal can be applied to the RF throw pins while the RFC pin is the output. All of the RF pins are dc-coupled to 0 V, and no dc blocking is required at the RF pins when the RF line potential is equal to 0 V.

The power-down sequence is the reverse of the power-up sequence.

Table 4. Control Voltage Truth Table

Digital Control Input		RF Paths			
CTRLA	**CTRLB**	**RFC to RF1**	**RFC to RF2**	**RFC to RF3**	**RFC to RF4**
High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

APPLICATION INFORMATION

EVALUATION BOARD

The EV1HMC641ALP4 is a 4-layer evaluation board. Each copper layer is 0.5 oz (0.7 mil) and separated by dielectric materials. Figure 14 shows the stack up for this evaluation board.

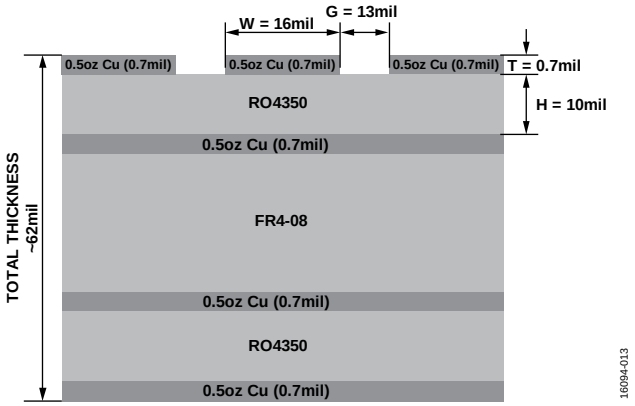


Figure 14. The EV1HMC641ALP4 Evaluation Board (Cross Sectional View)

All RF and dc traces are routed on the top copper layer whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. Top dielectric material is a 10 mil Rogers RO4350. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is approximately 62 mil, allowing the subminiature version A (SMA) launchers to be connected at the board edges.

The RF transmission lines were designed using a coplanar waveguide (CPWG) model, with trace width of 16 mil and ground clearance of 13 mil for a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, arrange as many plated through vias as possible around transmission lines and under the exposed pad of the package.

Figure 15 shows the layout of the EV1HMC641ALP4 evaluation board with component placement. Power supply port is connected to the V_{SS} test point, J8, and control voltages, CTRLA and CTRLB, are connected to the A and B test points, J6 and J7, and the ground reference is connected to the GND test point, J9. On the supply trace, V_{SS}, use a 1000 pF bypass capacitor to filter high frequency noise.

The RF input and output ports (RFC, RF1, RF2, RF3, and RF4) are connected through 50 Ω transmission lines to the SMA launchers, J1 to J5. These SMA launchers are soldered onto the board. A through calibration line connects the unpopulated J10 and J11 launchers; this transmission line estimates the loss of the PCB over the environmental conditions being evaluated, as shown in Figure 16.

Table 5 shows the evaluation board components.

Table 5. Evaluation Board Components

Component	Default Value	Description
J1 to J5		PCB mount SMA connector
J6 to J9		DC pin
J10, J11	Do not insert	PCB mount SMA connector
C1	1000 pF	Capacitor, C0402 package
U1		HMC641ALP4E SP4T switch
PCB	600-00782-00-1	Evaluation PCB

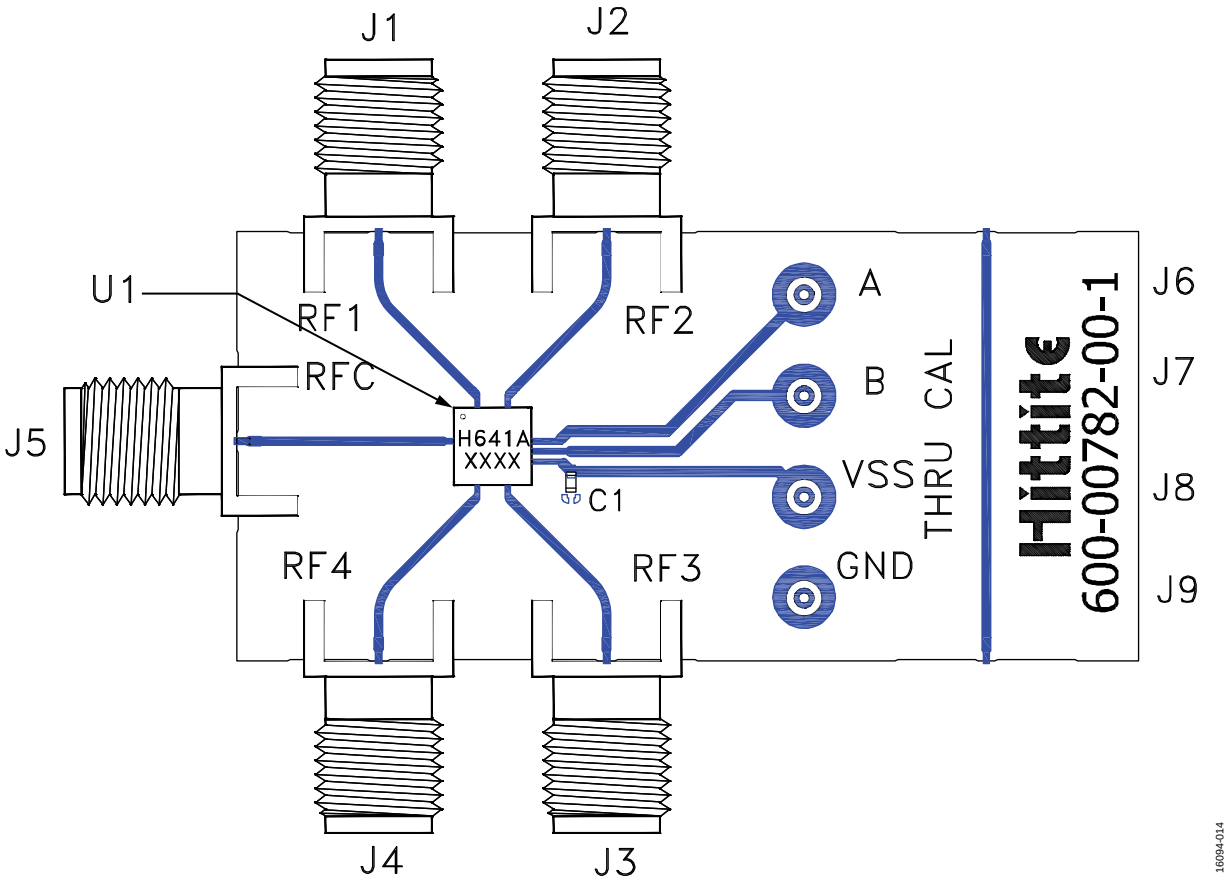


Figure 15. The EV1HMC641ALP4 Evaluation Board Component Placement

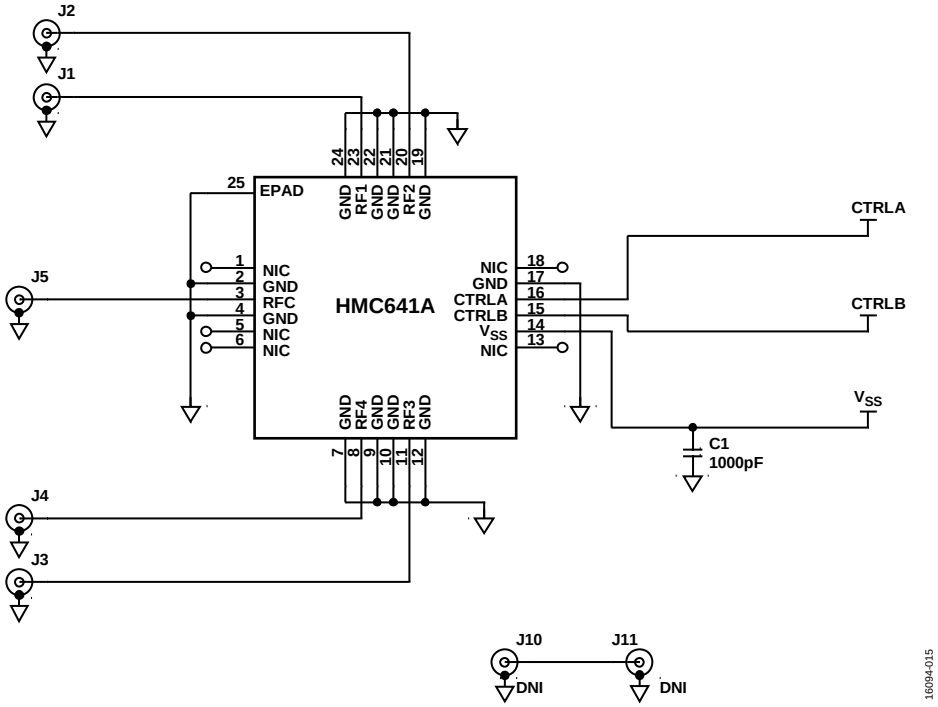


Figure 16. The EV1HMC641ALP4 Evaluation Board Schematic

OUTLINE DIMENSIONS

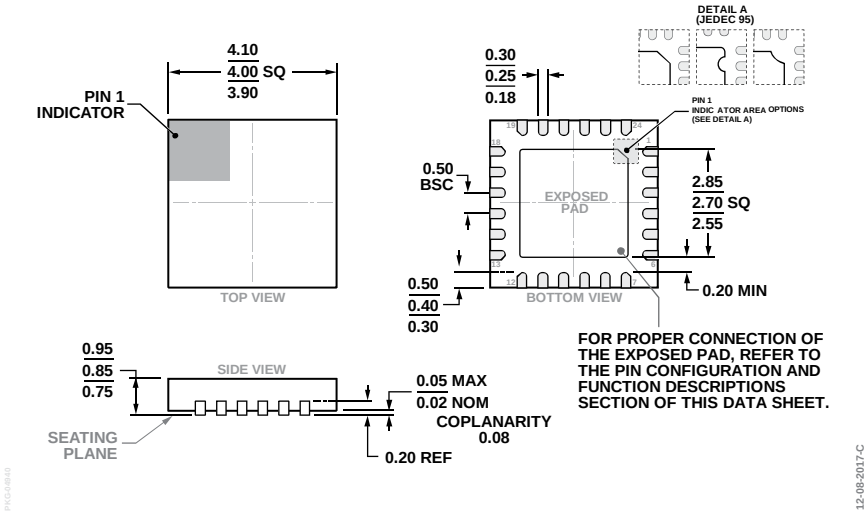


Figure 17. 24-Terminal Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.90 mm Package Height
(HCP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC641ALP4E	−40°C to +85°C	24-Terminal Lead Frame Chip Scale Package [LFCSP]	HCP-24-3
HMC641ALP4ETR	−40°C to +85°C	24-Terminal Lead Frame Chip Scale Package [LFCSP]	HCP-24-3
EV1HMC641ALP4		Evaluation Board	

[1] All models are RoHS compliant.

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