Digital Controller for Power Supply Applications with PMBus Interface

Data Sheet

ADP1055

FEATURES

- −40°C to +125°C operation
- PMBus Revision 1.2 compliant with PEC and extended manufacturer specific commands
- 32-bit password protection with command masking
- 64 address selections (16 base addresses, expandable to 64)
- 6 PWM control signals, 625 ps resolution
- Frequency from 48 kHz to 1 MHz
- Duty cycle double update rate
- Digital control loop (PID + additional pole or zero configurability)
- Programmable loop filters (CCM, DCM, low/normal temperature)
- Fast line voltage feedforward
- Adaptive dead time compensation for improved efficiency
- Remote voltage sense
- Redundant programmable OVP
- Current sense
  - Primary side cycle-by-cycle fast protection
  - Secondary side cycle-by-cycle fast overcurrent protection
  - Secondary side averaged reverse current protection using diode emulation mode with fixed debounce
- Synchronous rectifier control for improved efficiency in light load mode
- Nonlinear gain for faster transient response from DCM to CCM
- Frequency synchronization
- Soft start and soft stop functionality
- Average and peak constant current mode
- External PN junction temperature sensing
- 4 GPIOs (2 GPIOs configurable as active clamp snubber PWMs)
- Extended black box data recorder for fault recording
- User trimming on input and output voltages and currents
- Digital current sharing

APPLICATIONS

- Isolated dc-to-dc power supplies and modules
- Redundant power supply systems

GENERAL DESCRIPTION

The ADP1055 is a flexible, feature-rich digital secondary side controller that targets ac-to-dc and isolated dc-to-dc secondary side applications. The ADP1055 is optimized for minimal component count, maximum flexibility, and minimum design time. Features include differential remote voltage sense, primary and secondary side current sense, pulse-width modulation (PWM) generation, frequency synchronization, redundant OVP, and current sharing. The control loop digital filter and compensation terms are integrated and can be programmed over the PMBus™ interface. Programmable protection features include overcurrent (OCP), overvoltage (OVP) limiting, undervoltage lockout (UVLO), and external overtemperature (OTP).

The built-in EEPROM provides extensive programming of the integrated loop filter, PWM signal timing, inrush current, and soft start timing and sequencing. Reliability is improved through a built-in checksum and programmable protection circuits.

A comprehensive GUI is provided for easy design of loop filter characteristics and programming of the safety features. The industry-standard PMBus provides access to the many monitoring and system test functions. The ADP1055 is available in a 32-lead LFCSP and operates from a single 3.3 V supply.

TYPICAL APPLICATION DIAGRAM

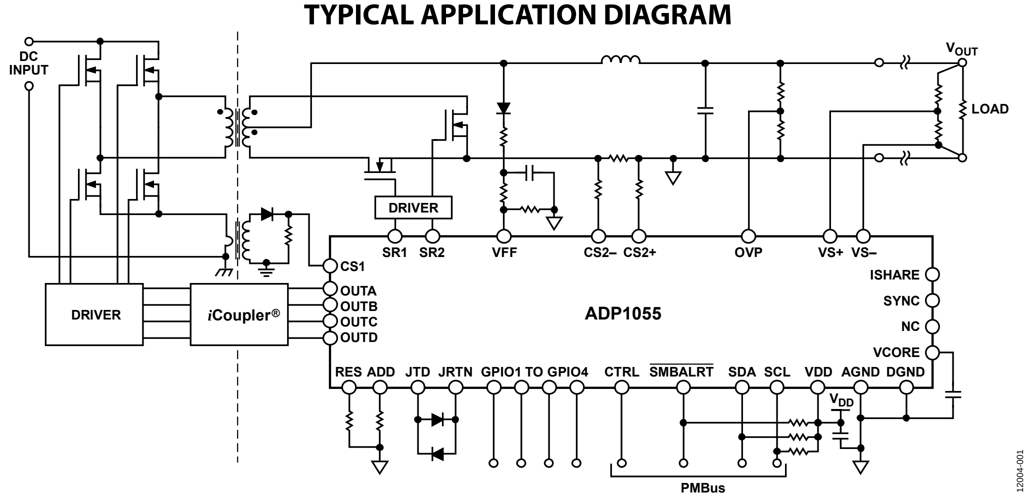


Figure 1.

Rev. A

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

3/15—Rev. 0 to Rev. A

Changes to Table 1.....7
Changes to Snubber Configuration Section.....31
Change to Debounce Bit, Table 159.....93
Changes to Supported Switching Frequencies Section.....126

3/14—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

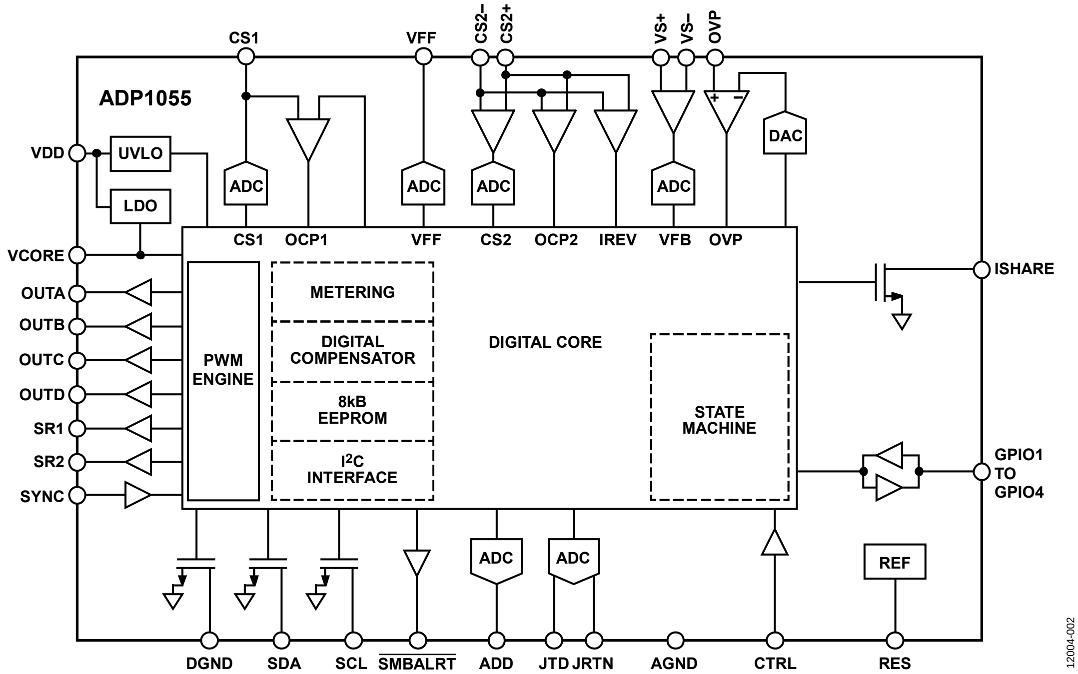


Figure 2. Functional Block Diagram (Simplified Internal Structure)

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V, T_A = −40°C to +125°C, unless otherwise noted. FSR = full-scale range.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Supply Voltage	V_{DD}	4.7 µF capacitor connected to AGND	3.0	3.3	3.6	V
Supply Current	I_{DD}	Normal operation (CTRL pin is high)		63		mA
		Normal operation (CTRL pin is low)		55		mA
		During EEPROM programming (40 ms)		I_{DD} + 8		mA
		During black box write		I_{DD} + 8		mA
		Current with VDD < VCORE POR		100		µA
POWER-ON RESET						
Power-On Reset	POR	V_{DD} rising			3.0	V
Undervoltage Lockout	UVLO	V_{DD} falling	2.75	2.85	2.97	V
Overvoltage Lockout	OVLO		3.8	4.0	4.1	V
OVLO Debounce		Set to 2 µs (Register 0xFE4D[5] = 0)		2.0		µs
		Set to 500 µs (Register 0xFE4D[5] = 1)		500		µs
VCORE PIN		0.33 µF capacitor connected to DGND				
Power-On Reset (POR)		V_{DD} falling		2.1		V
Output Voltage		T_A = 25°C		2.6		V
Maximum Time from POR to Outputs Switching		No black box recording (Register 0xFE48[1:0] = 00)		10		ms
		With black box recording (Register 0xFE48[1:0] = 01, 10, or 11)		45		ms
OSCILLATOR AND PLL						
PLL Frequency		RES = 10 kΩ (±0.1%)	190	200	210	MHz
OUTA, OUTB, OUTC, OUTD, SR1, SR2 PINS						
Output Low Voltage	V_{OL}	Sink current = 10 mA			0.8	V
Output High Voltage	V_{OH}	Source current = 10 mA	V_{DD} − 0.8			V
Rise Time		C_{LOAD} = 50 pF		3.5		ns
Fall Time		C_{LOAD} = 50 pF		1.5		ns
VOLTAGE FEEDFORWARD (VFF PIN)						
ADC Clock Frequency				1.56		MHz
Feedforward (Slow) Input Voltage Range	V_{FF}	For reporting; equivalent resolution of 12 bits	0	1	1.6	V
ADC Usable Input Voltage Range			0		1.57	V
Measurement Accuracy (Slow and Fast Feedforward)		Factory trimmed at 1.0 V				
		0% to 100% of usable input voltage range	−2.5		+2.5	% FSR
		10% to 90% of usable input voltage range	−2.0		+2.0	% FSR
		900 mV to 1.1 V	−1.5		+1.5	% FSR
Leakage Current					1.0	µA
FEEDFORWARD FUNCTION (VFF PIN)						
Feedforward (Fast) Input Voltage Range			0.6	1	1.6	V
Sampling Period for Feedforward (Fast) ADC		Equivalent resolution of 12 bits		1		µs
VS LOW SPEED ADC						
Input Voltage Range		Differential voltage from VS+ to VS−	0	1	1.6	V
Usable Input Voltage Range			0		1.55	V
ADC Clock Frequency				1.56		MHz

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ADC Update Rate		Registers are updated at this rate, equivalent resolution of 12 bits		10.5		ms
Measurement Accuracy		Factory trimmed at 1.0 V				
		0% to 100% of usable input voltage range	−2.75		+2.75	% FSR
		10% to 90% of usable input voltage range	−2.0		+2.0	% FSR
		900 mV to 1.1 V	−1.75		+1.75	% FSR
Temperature Coefficient		V_{DD} = 3.3 V, VS± = 1.0 V			110	ppm/°C
Leakage Current					1.0	µA
Common-Mode Voltage Offset Error		Maximum voltage differential from VS− to AGND of ±200 mV	−0.25		+0.25	% FSR
VS OVP DIGITAL COMPARATOR						
VS OVP Accuracy			−2.0		+2.0	% FSR
VS OVP Comparator Speed		Register 0xFE4D[3:2] = 00, equivalent resolution of 7 bits		82		µs
VS UVP DIGITAL COMPARATOR						
VS UVP Accuracy			−2.0		+2.0	% FSR
Propagation Delay		Does not include debounce time (Register 0xFE30[13:11] = 00)		80		µs
VS HIGH SPEED ADC						
Sampling Frequency				10		MHz
Equivalent Resolution				6		Bits
Dynamic Range				±50		mV
FAST OVP COMPARATOR (OVP PIN)						
Threshold Accuracy		Factory trimmed at 1.206 V	−1.2	0	+1.5	%
		Other thresholds (0.8 V to 1.6 V)	−2.0		+2.0	%
Propagation Delay (Latency)		Register 0xFE2F[1:0] = 00		40	80	ns
CURRENT SENSE 1 (CS1 PIN)						
Input Voltage Range	V_{IN}		0	1	1.6	V
Usable Input Voltage Range			0		1.56	V
ADC Clock Frequency				1.56		MHz
Update Rate		Registers are updated at this rate, equivalent resolution of 12 bits		10.5		ms
Current Sense Measurement Accuracy		Factory trimmed at 1.0 V; tested under dc input conditions				
		10% to 60% of usable input voltage range	−1.5		+1.5	% FSR
		10% to 90% of usable input voltage range	−2.0		+2.0	% FSR
		0% to 100% of usable input voltage range	−2.5		+2.5	% FSR
Current Sense Measurement				12		Bits
CS1 Fast OCP Threshold		Register 0xFE2C[2] = 0	1.17	1.2	1.23	V
		Register 0xFE2C[2] = 1	242	250	258	mV
CS1 Fast OCP Speed				40	80	ns
CS1 Accurate OCP Speed				10.5		ms
Leakage Current					1.5	µA
CURRENT SENSE 2 (CS2+, CS2− PINS)						
Current Sense Measurement Resolution		For updating registers (constant current mode enabled or disabled)		12		Bits
ADC Clock Frequency				1.56		MHz
30 mV Range[1]		Register 0xFE4F[1:0] = 00	0		30	mV
Usable Input Range			0		21	mV
60 mV Range[1]		Register 0xFE4F[1:0] = 01	0		60	mV
Usable Input Range			0		45	mV
480 mV Range[1]		Register 0xFE4F[1] = 10	0		480	mV
Usable Input Range			0		414	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Temperature Coefficient		V_{DD} = 3.3 V				
30 mV Range		0 mV to 19 mV			326	ppm/°C
		0 mV to 21 mV			354	ppm/°C
60 mV Range		0 mV to 41 mV			172	ppm/°C
		0 mV to 45 mV			194	ppm/°C
480 mV Range		0 mV to 374 mV			83	ppm/°C
		0 mV to 414 mV			84	ppm/°C
CURRENT SENSE MEASUREMENT ACCURACY (CS2+, CS2− PINS)						
30 mV Setting		0 mV to 19 mV	−2.9		+2.9	% FSR
		0 mV to 21 mV	−3.1		+3.1	% FSR
60 mV Setting		0 mV to 41 mV	−1.9		+1.9	% FSR
		0 mV to 45 mV	−2.1		+2.1	% FSR
480 mV Setting		0 mV to 374 mV	−1.5		+1.5	% FSR
		0 mV to 414 mV	−1.7		+1.7	% FSR
Internal Level Shifting Current		All ranges		25		µA
CS2 Accurate OCP Speed				2.6		ms
COMMON-MODE VOLTAGE OFFSET ERROR (CS2+, CS2− PINS)		Maximum voltage differential from CS2− to AGND of ±50 mV				
30 mV Range			−1.0		+1.0	% FSR
60 mV Range			−0.5		+0.5	% FSR
480 mV Range			−0.25		+0.25	% FSR
CS2 OCP FAST COMPARATORS (CS2+, CS2− PINS)		For CS2 fast OCP and peak constant current mode				
CS2 Forward Comparator Accuracy						
Range of 0 mV to 60 mV		Threshold set at 0 mV		−10.3		% FSR
		Threshold set at 15.24 mV		−10.1		% FSR
		Threshold set at 30.48 mV	−23.8		+16.7	% FSR
		Threshold set at 45.71 mV		−10.2		% FSR
		Threshold set at 60 mV		−10.2		% FSR
Range of 0 mV to 600 mV		Threshold set at 0 mV		−0.8		% FSR
		Threshold set at 152.4 mV		0.1		% FSR
		Threshold set at 304.8 mV	−7.1		+7.6	% FSR
		Threshold set at 457.1 mV		0.9		% FSR
		Threshold set at 600 mV		1.3		% FSR
Reverse Comparator Accuracy						
Range of 0 mV to 30 mV		Threshold set at 0 mV		−11.8		% FSR
		Threshold set at 7.62 mV		−11.8		% FSR
		Threshold set at 15.24 mV	−13.8		+16.9	% FSR
		Threshold set at 22.86 mV		12.7		% FSR
		Threshold set at 30 mV		12.5		% FSR
Range of −30 mV to 0 mV		Threshold set at 0 mV		17.1		% FSR
		Threshold set at −7.62 mV		16.9		% FSR
		Threshold set at −15.24 mV	−9.5		+23.2	% FSR
		Threshold set at −22.86 mV		17.6		% FSR
		Threshold set at −30 mV		17.4		% FSR
Propagation Delay		Register 0xFE2D[1:0] = 00 (diode emulation mode)		40	80	ns
JTD TEMPERATURE SENSE						
ADC Clock Frequency				1.56		MHz
Update Rate		For updating registers (14-bit resolution)				
Reverse Sensing Enabled				200		ms
Reverse Sensing Disabled				130		ms

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Measurement Accuracy for External Temperature Sensor		With BC847A transistor (n_f = 1.00); Register 0xFE5A[2:0] = 0x04				
Forward Temperature Sensor		Error from −40°C to +25°C	−11.7		+13.4	°C
		Error from 25°C to 125°C	−8.9		+14.7	°C
Reverse Temperature Sensor		Error from 25°C to 125°C	−9.7		+14.4	°C
CTRL, $\overline{\text{SMBALRT}}$, SYNC, GPIO1 TO GPIO4, ISHARE PINS		Digital inputs/outputs				
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		V_{DD} − 0.8			V
Propagation Delay				40		ns
GPIOx Rise Time		GPIOx configured as an output		3.5		ns
GPIOx Fall Time		GPIOx configured as an output		1.5		ns
Leakage Current		$\overline{\text{SMBALRT}}$, SYNC, GPIO1 TO GPIO4, and ISHARE pins			1.0	µA
		CTRL pin			10.0	µA
SYNC PIN		Synchronization to external frequency	50		1000	kHz
Minimum On Pulse			40			ns
Synchronization Range[2]			−10.0		+10.0	% f_{SW}
Leakage Current					1.0	µA
BLACK BOX PROGRAMMING TIME			1.2		36 × 1.2	ms
SDA/SCL PINS						
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.1			V
Output Low Voltage	V_{OL}				0.4	V
Leakage Current					1.0	µA
SERIAL BUS TIMING		See Figure 3				
Clock Operating Frequency			10	100	400	kHz
Bus Free Time	t_{BUF}	Between stop and start conditions	1.3			µs
Start Hold Time	$t_{HD;STA}$	Hold time after (repeated) start condition; after this period, the first clock is generated	0.6			µs
Start Setup Time	$t_{SU;STA}$	Repeated start condition setup time	0.6			µs
Stop Setup Time	$t_{SU;STO}$		0.6			µs
SDA Setup Time	$t_{SU;DAT}$		100			ns
SDA Hold Time	$t_{HD;DAT}$	For write and for readback	300			ns
SCL Low Timeout	$t_{TIMEOUT}$		25		35	ms
SCL Low Period	t_{LOW}		1.3			µs
SCL High Period	t_{HIGH}		0.6			µs
Clock Low Extend Time	$t_{LO;SEXT}$				25	ms
SCL, SDA Fall Time	t_F		20		300	ns
SCL, SDA Rise Time	t_R		20		300	ns
EEPROM RELIABILITY						
Endurance[3]		T_J = 85°C	10,000			Cycles
		T_J = 125°C	1000			Cycles
Data Retention[4]		T_J = 85°C	20			Years
		T_J = 125°C	15			Years

[1] Differential voltage from CS2+ to CS2−.
[2] f_{SW} is the switching frequency set in Register 0x33.
[3] Endurance is qualified as per JEDEC Standard 22, Method A117, and is measured at −40°C, +25°C, +85°C, and +125°C.
[4] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22, Method A117. Retention lifetime derates with junction temperature.

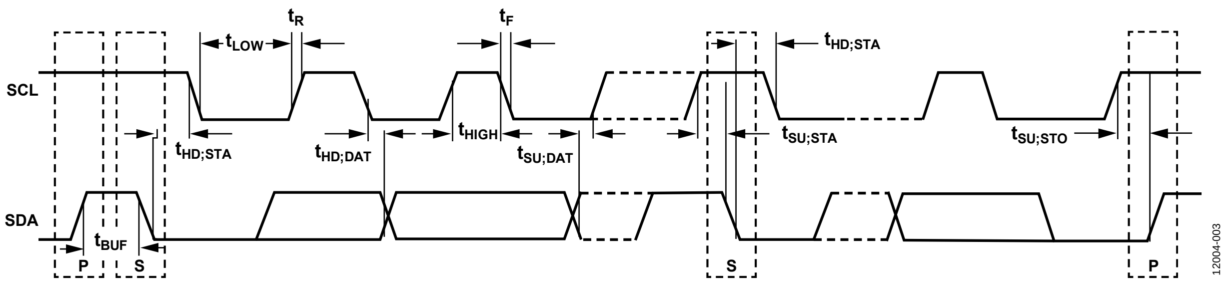


Figure 3. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous), VDD	4.2 V
Digital Pins: OUTA, OUTB, OUTC, OUTD, SR1, SR2, GPIO1, GPIO2, GPIO3, GPIO4, SMBALRT, SYNC	−0.3 V to VDD + 0.3 V
VS−, AGND, DGND	−0.3 V to +0.3 V
VS+	−0.3 V to VDD + 0.3 V
JTD, JRTN, ADD	−0.3 V to VDD + 0.3 V
CS1, CS2+, CS2−	−0.3 V to VDD + 0.3 V
SDA, SCL	−0.3 V to VDD + 0.3 V
ISHARE	−0.3 V to VDD + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C
ESD	
Charged Device Model	500 V
Human Body Model	2.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

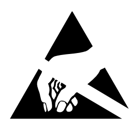
Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	44.4	6.4	°C/W

SOLDERING

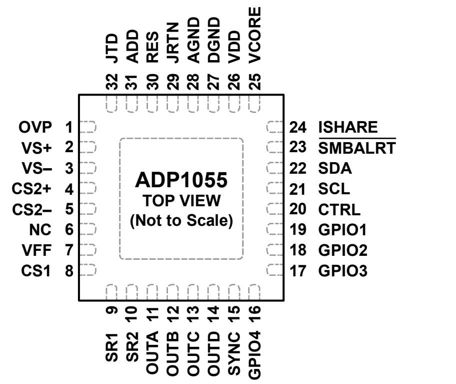
It is important to follow the correct guidelines when laying out the PCB footprint for the ADP1055 and when soldering the device onto the PCB. For detailed information about these guidelines, see the AN-772 Application Note.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. LEAVE THIS PIN UNCONNECTED.
2. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE EXPOSED PAD ON THE UNDERSIDE OF THE PACKAGE BE SOLDERED TO THE PCB AGND PLANE.

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OVP	Overvoltage Protection. This signal is referenced to AGND and is used for redundant OVP protection. The nominal voltage at this pin should be 1 V. If this pin is not used, connect it to AGND.
2	VS+	Noninverting Voltage Sense Input. This signal is referenced to VS−. The nominal input voltage at this pin is 1 V. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming. This pin is the input to the high frequency flash ADC.
3	VS−	Inverting Voltage Sense Input. There should be a low ohmic connection to AGND. The resistor divider on this input must have a tolerance specification of 0.5% or better to allow for trimming. To reduce common-mode noise, connect a 0.1 μF capacitor from VS− to AGND.
4	CS2+	Noninverting Differential Current Sense Input. This signal is referenced to CS2−. If this pin is not used, connect it to AGND.
5	CS2−	Inverting Differential Current Sense Input. If this pin is not used, connect it to AGND. This pin must have a low ohmic connection to AGND thought the sense resistor.
6	NC	No Connect. Leave this pin unconnected.
7	VFF	Voltage Feedforward. Two optional functions can be implemented using this pin: feedforward and input voltage loss detection. This pin is typically connected upstream of the output inductor through a resistor divider network in an isolated converter. The nominal voltage at this pin should be 1 V. This signal is referenced to AGND. If this pin is not used, connect it to AGND.
8	CS1	Primary Side Current Sense Input. This pin is connected to the primary side current sensing ADC and to the fast OCP comparator. This signal is referenced to PGND. The resistors on this input must have a tolerance specification of 0.5% or better to allow for trimming. If this pin is not used, connect it to AGND.
9	SR1	Synchronous Rectifier Output. This PWM output connects to the input of a FET driver. This pin can be disabled when not in use. This signal is referenced to AGND.
10	SR2	Synchronous Rectifier Output. This PWM output connects to the input of a FET driver. This pin can be disabled when not in use. This signal is referenced to AGND.
11	OUTA	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referenced to AGND.
12	OUTB	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referenced to AGND.
13	OUTC	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referenced to AGND.
14	OUTD	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referenced to AGND.
15	SYNC	Synchronization Input Signal. This pin is used as a reference for the internal PWM frequency. This signal is referenced to AGND and must have a nominal duty cycle of 50%. If this pin is not used, connect it to AGND and program Register 0xFE55[6] = 1.
16	GPIO4	Programmable General-Purpose Input/Output. If this pin is not used, connect it to AGND. This pin can also be configured as an active snubber PWM output.
17	GPIO3	Programmable General-Purpose Input/Output. If this pin is not used, connect it to AGND. This pin can also be configured as an active snubber PWM output.

Pin No.	Mnemonic	Description
18	GPIO2	Programmable General-Purpose Input/Output. If this pin is not used, connect it to AGND.
19	GPIO1	Programmable General-Purpose Input/Output. If this pin is not used, connect it to AGND.
20	CTRL	Power Supply On Input. This signal is referenced to AGND. This pin is the hardware PSON control signal. It is recommended that a 1 nF capacitor be connected from the CTRL pin to AGND for decoupling. If this pin is not used, connect it to AGND.
21	SCL	I^2C/PMBus Serial Clock Input and Output (Open Drain). This signal is referenced to AGND.
22	SDA	I^2C/PMBus Serial Data Input and Output (Open Drain). This signal is referenced to AGND.
23	$\overline{\text{SMBALRT}}$	Power-Good Output (Open Drain). This signal is referenced to AGND. This pin is also used as the PMBus $\overline{\text{ALERT}}$ signal.
24	ISHARE	Digital Current Sharing Input and Output (Open Drain). This signal is referenced to AGND.
25	VCORE	VDD for the Digital Core. Connect a decoupling capacitor of at least 330 nF (1 μF maximum) from this pin to DGND as close to the IC as possible to minimize the PCB trace length. Do not use the VCORE pin as a reference or load it in any way.
26	VDD	Positive Supply Input. This signal is referenced to AGND. Connect a 4.7 μF decoupling capacitor from this pin to AGND as close to the IC as possible to minimize the PCB trace length.
27	DGND	Digital Ground. This pin is the ground reference for the digital circuitry. Star connect to AGND.
28	AGND	IC Analog Ground.
29	JRTN	Temperature Sensor Return. If this pin is not used, connect it to AGND.
30	RES	Resistor Input. This pin sets the internal reference for the internal PLL frequency. Connect a 10 kΩ resistor (±0.1%) from RES to AGND. Do not load this pin with any capacitance. This signal is referenced to AGND.
31	ADD	I^2C/PMBus Address Select Input. Connect a resistor from ADD to AGND. This signal is referenced to AGND.
32	JTD	Thermal Sensor Input. A PN junction sensor is connected from this pin to the JRTN pin. If this pin is not used, connect it to JRTN.
	EP	Exposed Pad. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad on the underside of the package be soldered to the PCB AGND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

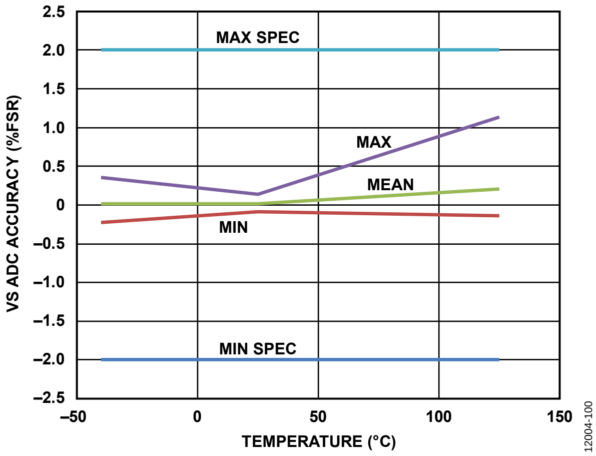


Figure 5. VS ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

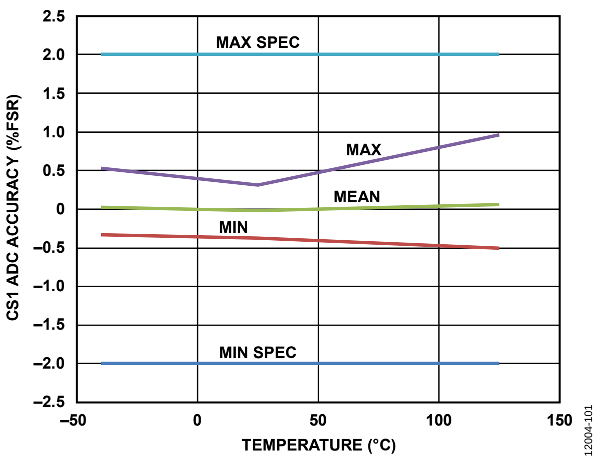


Figure 6. CS1 ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

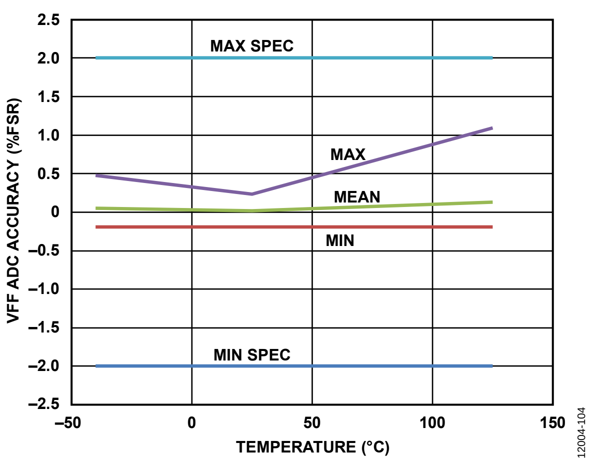


Figure 7. VFF ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

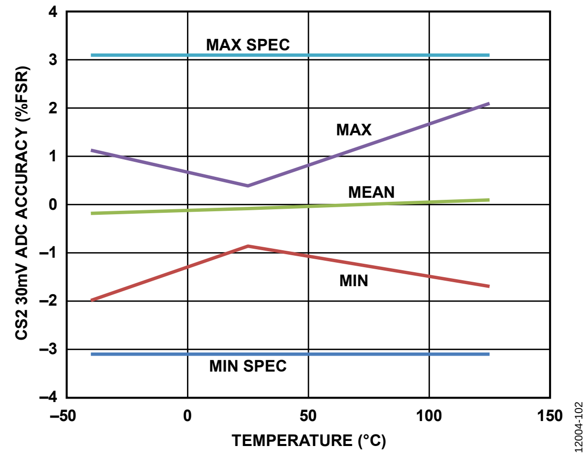


Figure 8. CS2 30 mV ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

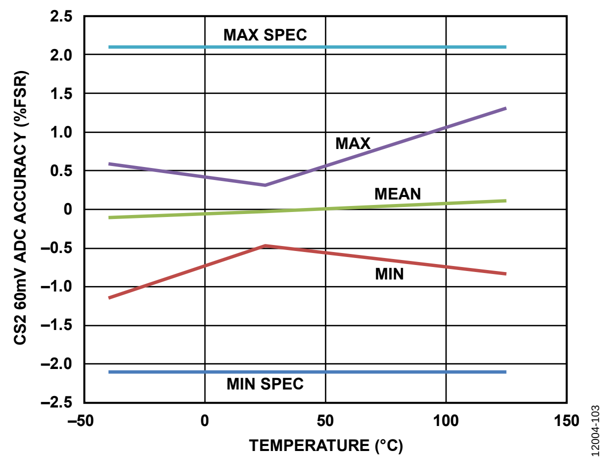


Figure 9. CS2 60 mV ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

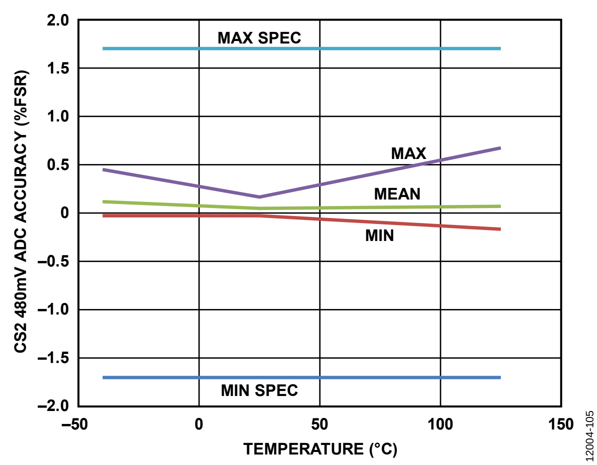


Figure 10. CS2 480 mV ADC Accuracy vs. Temperature (from 10% to 90% of FSR)

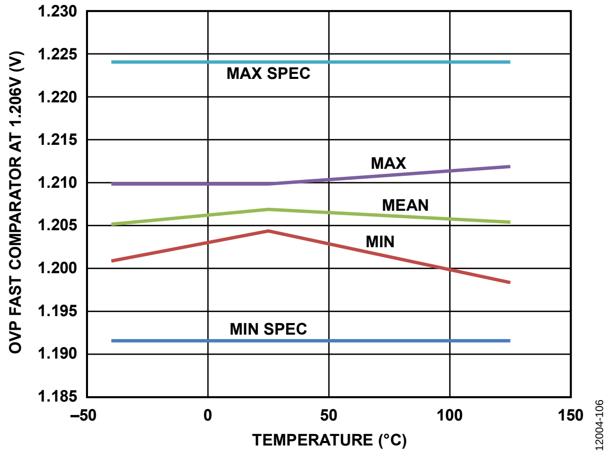


Figure 11. OVP Fast Comparator at 1.206 V vs. Temperature

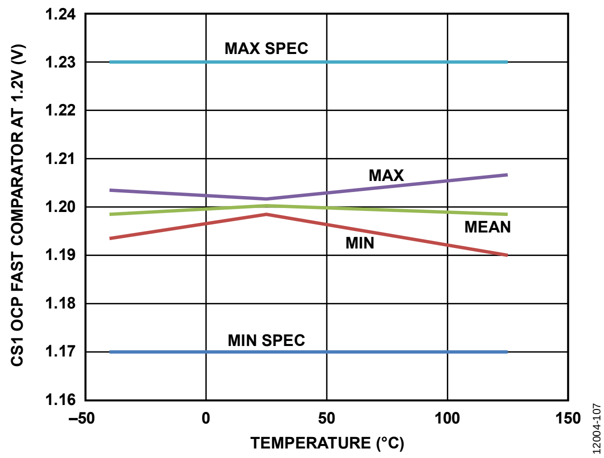


Figure 12. CS1 OCP Fast Comparator at 1.2 V vs. Temperature

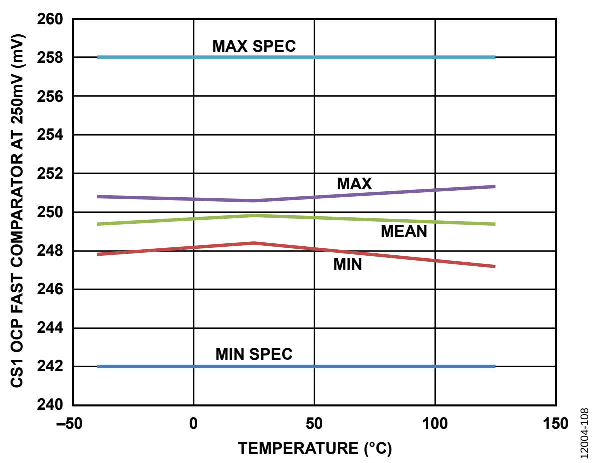


Figure 13. CS1 OCP Fast Comparator at 250 mV vs. Temperature

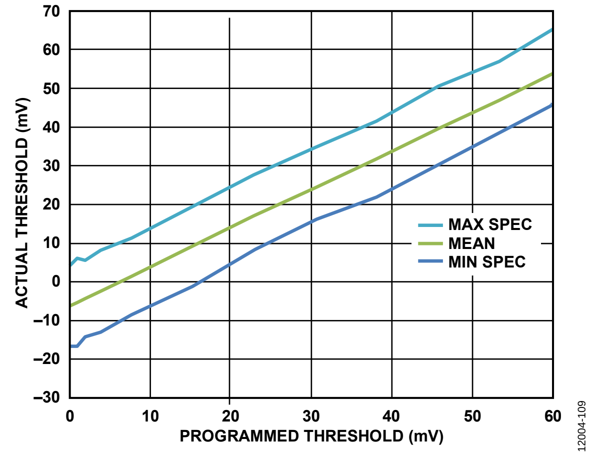


Figure 14. CS2 Forward Comparator Accuracy, 0 mV to 60 mV Range

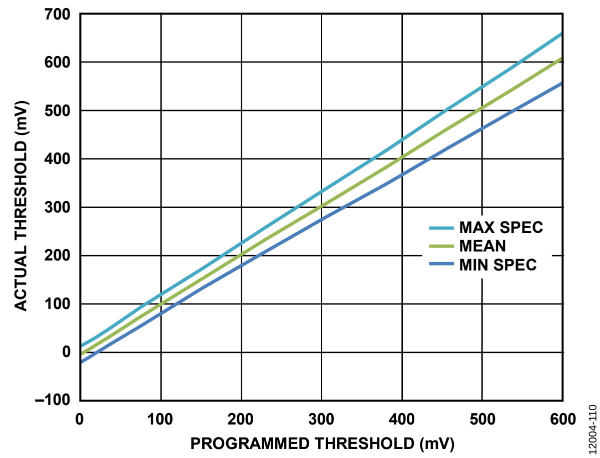


Figure 15. CS2 Forward Comparator Accuracy, 0 mV to 600 mV Range

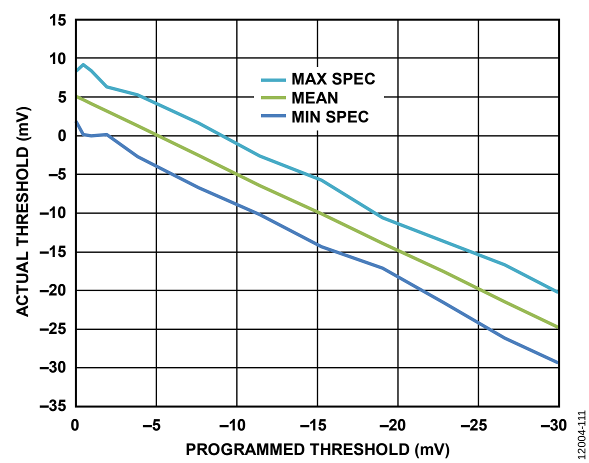


Figure 16. CS2 Reverse Comparator, 0 mV to –30 mV Range

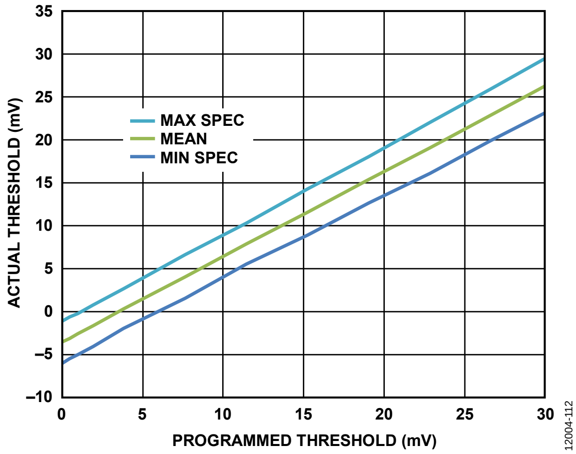


Figure 17. CS2 Reverse Comparator, 0 mV to 30 mV Range

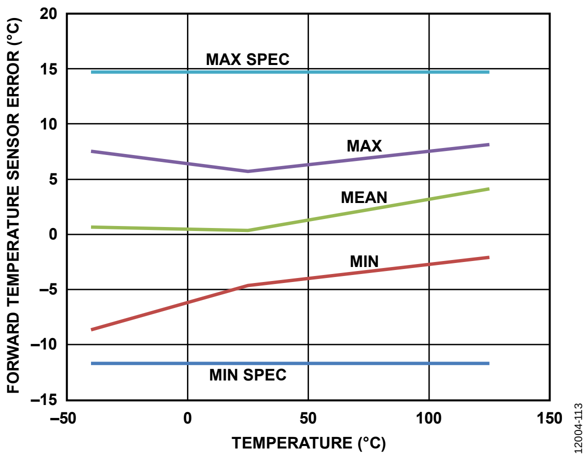


Figure 18. Forward Temperature Sensor Error vs. Temperature

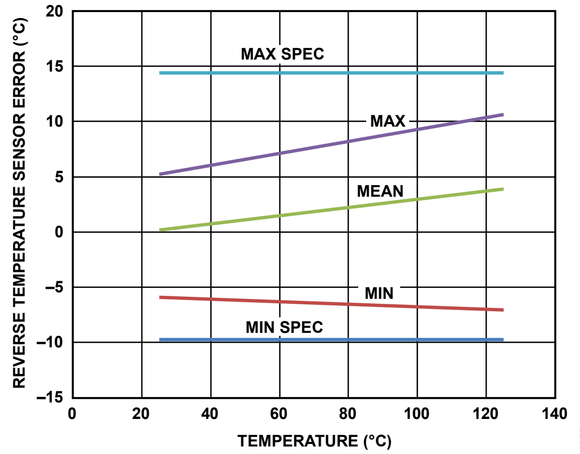


Figure 19. Reverse Temperature Sensor Error vs. Temperature

CONTROLLER ARCHITECTURE

The ADP1055 is an application specific digital controller based on finite state machine (FSM) architecture. The ADP1055 supports a subset of the PMBus Revision 1.2 standard and also has extended manufacturer specific commands to provide a feature rich digital power product.

Dedicated ADCs and comparators constitute the analog front end of the controller, feeding information to the digital core. The information is processed and used to generate the programmable PWM signals and to take action for various features such as light load or overvoltage/overcurrent protection.

The ADP1055 has six PWM outputs: OUTA to OUTD for the primary side switches and SR1 and SR2 for the secondary side synchronous rectifiers. The ADP1055 allows individual programming of the PWM outputs to form the timing of the power switches for any power topology, such as full bridge, full bridge phase shifted, current doubler, or active clamp.

Primary side information (current or voltage) is sensed and processed via the CS1 and VFF pins, whereas secondary side information is obtained via the CS2±, ISHARE, VS±, and OVP pins. A dedicated temperature sensor uses the JTD and JRTN pins. The input voltage is measured using the VFF pin and is used for line voltage feedforward. Extensive fault protection schemes are provided, and the controller also has a black box to record the state of the device (all sensor information including voltages, currents, temperatures, and flags) upon shutdown.

I^2C/PMBus communication is facilitated by the SDA, SCL, and $\overline{\text{SMBALRT}}$ pins. Four GPIO pins can be used as flag output signals or as an interrupt service routine (ISR) to trigger a PMBus fault action. The CTRL pin is used as described in the PMBus specification.

Detailed descriptions of all ADP1055 features are provided in the Theory of Operation section.

START-UP AND POWER-DOWN SEQUENCING

VDD AND VCORE PINS

The proper amount of decoupling capacitance must be placed between the VDD and AGND pins, as close as possible to the device to minimize the trace length. It is recommended that the VCORE pin not be loaded in any way.

POWER-UP AND POWER-DOWN COMMANDS

The PMBus commands OPERATION (Register 0x01) and ON_OFF_CONFIG (Register 0x02) control the power-up and power-down behavior of the ADP1055.

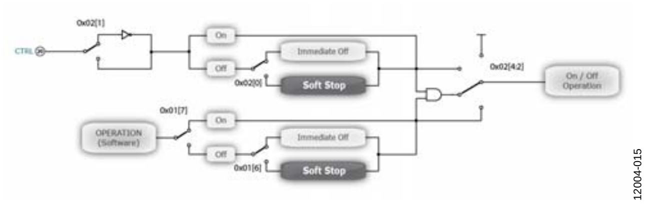


Figure 20. OPERATION (Register 0x01) and ON_OFF_CONFIG (Register 0x02)

POWER SEQUENCING

Power sequencing is controlled using Register 0x60 through Register 0x66. The delays for the turn-on command (Register 0x60, TON_DELAY) and the turn-off command (Register 0x64, TOFF_DELAY) can each be programmed from 0 ms to 1024 ms in steps of 1 ms.

The soft start ramp-up time (Register 0x61, TON_RISE) and the ramp-down time (Register 0x65, TOFF_FALL) can be programmed from 0 ms to 100 ms in steps of 1 ms.

All values are rounded to the nearest available value. If a value is programmed outside the allowed range, it is forced to the nearest legal value.

POWER-UP AND SOFT START ROUTINE

When VDD is applied to the device, a certain time elapses before the ADP1055 can regulate the power supply.

1. When VDD is above UVLO and VCORE reaches above VCORE POR through an internal regulator, the ADP1055 downloads the user settings from Page 1 of the EEPROM into the internal registers.
2. After the EEPROM download, the ADP1055 determines its address, programmed by the ADD pin and the I^2C slave base address (Register 0xD0, SLV_ADDR_SELECT).
3. The ADP1055 waits for an idle time, after which the device is ready for normal operation. If the black box must erase a page to precondition the EEPROM for storing, the idle time is extended by ~35 ms (see the Black Box Timing section).
4. If the ADP1055 is programmed to power up at this time (OPERATION is enabled), the soft start ramp begins. Otherwise, the ADP1055 waits for the OPERATION command.

The outputs start switching, depending on the configuration of the OPERATION command (Register 0x01) and the ON_OFF_CONFIG command (Register 0x02).

If the ADP1055 is programmed to be always on (Register 0x02[4] = 0), the device begins the soft start ramp. Figure 21 shows the entire soft start process.

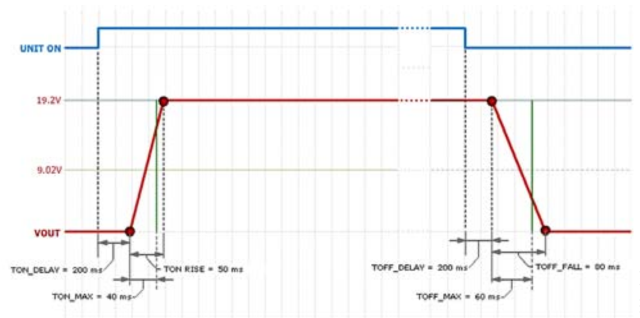


Figure 21. Example of Soft Start and Soft Stop Settings in the GUI

The soft start proceeds as follows.

1. Upon power-up, the ADP1055 waits for the programmed TON_DELAY (Register 0x60) and ramps to the regulation voltage according to the time programmed in TON_RISE (Register 0x61).
2. The soft start begins to ramp up the internal digital reference. The total duration of the soft start ramp is programmable using the TON_RISE command. The TON_MAX command specifies the maximum on time before which the output voltage must exceed the VOUT_UV_FAULT_LIMIT (Register 0x44). If the VOUT_UV_FAULT_LIMIT is set to 0, the TON_MAX value is ignored.

If the soft start from precharge function is enabled (Register 0xFE51[0] = 1), the soft start ramp starts from the current value of the output voltage sensed on VS± and, therefore, the soft start ramp time is reduced proportionally.

SOFT STOP ROUTINE

The soft stop process occurs in a manner similar to the soft start process, using the TOFF_DELAY, TOFF_MAX, and TOFF_FALL commands. These commands are the counterparts of the TON_DELAY, TON_MAX, and TON_RISE commands used for soft start. For more information about soft stop, see the Soft Stop section.

VDD/VCORE OVLO

The ADP1055 has built-in overvoltage protection (OVP) on its supply rails. When the VDD or VCORE voltage rises above the OVLO threshold, the response can be programmed using Register 0xFE4D. It is recommended that when a VDD/VCORE OVP fault occurs, the response be set to download the EEPROM before restarting the ADP1055. All features related to the OVLO function—such as debounce, fault ignore, and download EEPROM upon receiving a fault condition—are programmable using Register 0xFE4D[7:4].

VDD overvoltage is ignored when the device is downloading information from the EEPROM, even if the overvoltage occurs during the initial power-up or due to the setting of Register 0xFE4D[6]. VDD overvoltage is recognized as a fault only after the EEPROM download is complete. The ADP1055 has a 4 ms idle time after an EEPROM download.

If the VDD overvoltage occurs during the ramp-up of VDD and the ADP1055 has not initiated the EEPROM download, the device responds according to the default setting of Bit 7 in Register 0xFE4D, which is to ignore VDD OV.

CONTROL LOOP AND PWM OPERATION

VOLTAGE SENSE, FEEDBACK, AND CONTROL LOOP

The VS± pins are used for the monitoring and protection of the remote load voltage. The differential VS± input pins are the main feedback sense point for the power supply control loop. The VS± sense point on the power rail requires an external resistor divider to bring the nominal common-mode signal to 1 V at the VS± pins. This resistor divider is programmed into VOUT_SCALE_LOOP and VOUT_SCALE_MONITOR accordingly. The resistor divider is necessary because the input range is 0 V to 1.6 V. The divided-down signal is internally fed into a high frequency (HF) ADC. The HF ADC is also the high frequency feedback loop for the power supply.

OUTPUT VOLTAGE SENSE

The output voltage is fed back to the VS± pins, where it is compared with a reference set by a 12-bit DAC (see Figure 22). The difference is then fed into the flash ADC; in this configuration, the flash ADC does not see the fraction of the output voltage set by the resistor divider, but instead sees only the error voltage. The error voltage is then fed into the digital filter, which decides the duty cycle command for the next switching period. The number of samples taken by the flash ADC can be configured in Register 0xFE67[7:4] (see Table 215). The recommended configuration of this register is automatically configured using the GUI.

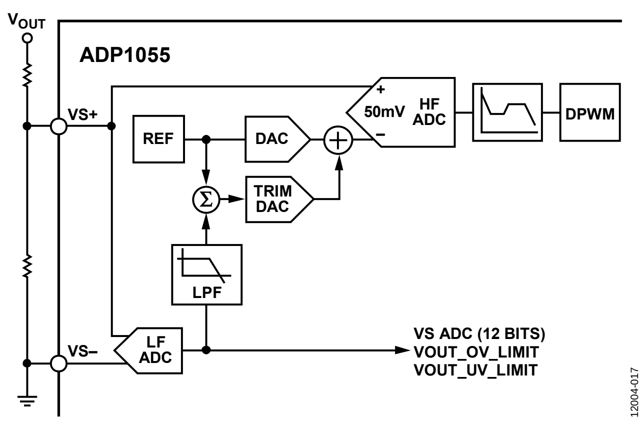


Figure 22. Output Voltage Sense and Feedback

The output voltage is also sampled using a low frequency ADC. The output voltage is fed to a low-pass filter that is used to set the output of a trim DAC; the trim DAC finely adjusts the output voltage as part of the autocorrection loop (see the Voltage Loop Autocorrection section).

DIGITAL FILTER

The loop response of the power supply can be changed using the internal programmable digital filter. A Type 3 filter architecture has been implemented. To tailor the loop response to the specific application, the low frequency gain, zero location, pole location, and high frequency gain can all be set individually (see the Digital Filter Programming Registers section). It is recommended that the Analog Devices, Inc., software GUI be used to program the filter. The software GUI displays the filter response in Bode plot format and can be used to calculate all stability criteria for the power supply.

From the sensed voltage to the duty cycle, the transfer function of the filter in z-domain is as follows:

$$H(z)=\left(\frac{D}{LFG}\times\frac{1}{(1-z^{-1})}+\frac{C}{HFG}\frac{\left(1-\frac{B}{256}z^{-1}\right)}{\left(1-\frac{A}{256}z^{-1}\right)}\times ADD\_PZ\right)$$

where:
A = filter pole register value (in decimal).
B = filter zero register value (in decimal).
C = high frequency gain register value (in decimal).
D = low frequency gain register value (in decimal).
$LFG = 5.968 \times m \times 10^6/f_{SW}$.
$HFG = 3.73\times m \times 10^5/f_{SW}$.
$m = 1$ when $48.8\text{ kHz} \le f_{SW} < 97.7\text{ kHz}$.
$m = 2$ when $97.7\text{ kHz} \le f_{SW} < 195.3\text{ kHz}$.
$m = 4$ when $195.3\text{ kHz} \le f_{SW} < 390.6\text{ kHz}$.
$m = 8$ when $390.6\text{ kHz} \le f_{SW}$.
ADD_PZ is an additional pole or additional zero that can be added to the compensator.

The additional zero takes this form:

$$1-\frac{E}{256}\times z^{-1}$$

The additional pole takes this form:

$$\frac{1}{\left(1-\frac{E}{256}\times z^{-1}\right)}$$

where E is the value (in decimal) of the additional pole zero frequency gain register (Register 0xFE60 and Register 0xFE61).

To transfer the z-domain value to the s-domain, plug the following bilinear transformation equation into the H(z) equation:

$$z(s)=\frac{2f_{SW}+s}{2f_{SW}-s}$$

where f_{SW} is the switching frequency.

The digital filter introduces an extra phase delay element into the control loop. The digital filter circuit sends the duty cycle information to the PWM circuit at the beginning of each switching cycle (unlike an analog controller, which makes decisions on the duty cycle information continuously). Therefore, the extra phase delay for phase margin, Φ, introduced by the filter block is

$$\Phi = 360 \times (f_C/f_{SW})$$

where:
f_C is the crossover frequency.
f_{SW} is the switching frequency.

At one-tenth the switching frequency, the phase delay is 36°. For double update rate, the phase delay is reduced to 18°. The GUI incorporates this phase delay into its calculations. Note that the GUI does not account for other delays such as gate driver and propagation delays.

DIGITAL FILTER PROGRAMMING REGISTERS

Three sets of registers allow three different filters to be programmed.

- Normal mode filter (used for CCM or heavy load and configured in Register 0xFE01 to Register 0xFE04)
- Light load mode filter (configured in Register 0xFE05 to Register 0xFE08)
- Soft start filter (configured in Register 0xFE09 to Register 0xFE0C)

The software GUI allows the user to program the light load mode filter in the same manner as the normal mode filter. It is recommended that the GUI be used for this purpose.

DIGITAL COMPENSATION FILTERS DURING SOFT START

The ADP1055 has a dedicated soft start filter (SSF) that can be used to fine-tune and optimize the dynamic response during the output voltage ramp-up.

During soft start, the ADP1055 determines the load condition and after the voltage reaches 12.5% of the nominal output voltage value, it determines the current load condition and switches filters accordingly to the light load mode threshold (Register 0xFE5F[3:1]). If the load current is below the light load mode threshold, the ADP1055 switches to the light load mode filter (LLF). If the load current is above the light load mode threshold, the normal mode filter is used until the end of the soft start ramp, even if the device subsequently enters light load mode based on a change to the load current.

Other configurations can be programmed to use different filters during soft start, as follows:

- Force soft start filter (Register 0xFE51[2]). This option forces the ADP1055 to use the soft start filter. In some cases, this option allows better fine-tuning of the ramp-up voltage.
- Disable light load mode during soft start (Register 0xFE51[1]). This option prevents the use of the light load mode filter during soft start, even if the light load condition is met. The light load mode filter is available for use after the end of the soft start ramp.

Figure 23 shows the use of filters during soft start.

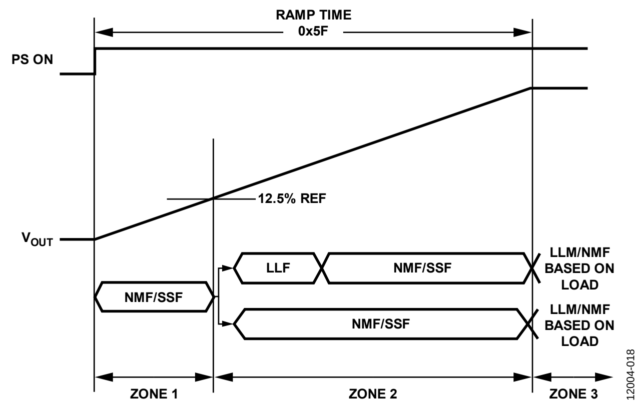


Figure 23. Digital Filters During Soft Start (Low Temperature Filter Not Shown)

As shown in Figure 23, in Zone 1, the ADP1055 starts with the normal mode filter or the soft start filter. Zone 2 begins when the voltage reaches 12.5% of the nominal output voltage value. At this point, the ADP1055 checks whether the system is in light load mode, and the choice of filter is based on the following criteria:

- If the system is in light load mode, the ADP1055 switches to the light load mode filter (unless the option to disable the LLM filter was previously selected).
- If the system is not in light load mode, the ADP1055 continues to use the filter used in Zone 1: the normal mode filter or the soft start filter.

The ADP1055 changes to the LLM filter if the load changes during Zone 2 (voltage rises from 12.5% to 100% of the soft start ramp. The filter does not revert to LLM if the load drops until after the end of soft start.

In Zone 3 the filter changes to the NMF or LLM filter, depending on the load.

FILTER TRANSITION

To avoid output voltage glitches and to provide a seamless transition from one filter to another, the ADP1055 supports programmable filter transitions. This feature allows a gradual transition from one filter to another. Filter transitions are programmed using Register 0xFE4A[2:0]. When the ADP1055 switches filters, the switching action is changed in 32 steps. The step size can be programmed over several cycles ($1t_{SW}$ to $32t_{SW}$) to avoid glitches in the output. The filter used depends on the state of the synchronous rectifiers and whether the system is in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) (see Table 5).

Table 5. State of Synchronous Rectifiers and Filter Used

Load	State of SRx Outputs		Filter Used
	Regular Mode	Diode Emulation Mode	
Medium to heavy load	SRs in CCM	SRs in CCM	Normal mode filter (Register 0xFE01 to Register 0xFE04).
Below LLM threshold	SRs in LLM	Diode emulation SRs	LLM filter (Register 0xFE05 to Register 0xFE08.) When diode emulation mode is in use, the LLM filter is activated after the LLM threshold is crossed.
Deep LLM	SRs are off	SRs are off	LLM filter (Register 0xFE05 to Register 0xFE08).

PWM AND SYNCHRONOUS RECTIFIER OUTPUTS (OUTA, OUTB, OUTC, OUTD, SR1, SR2)

The PWM and SR outputs are used for control of the primary side drivers and the synchronous rectifier drivers. These outputs can be used for several control topologies, such as full-bridge, phase-shifted ZVS configurations and interleaved, two switch forward converter configurations. Delays between the rising and falling edges can be individually programmed (see Figure 24).

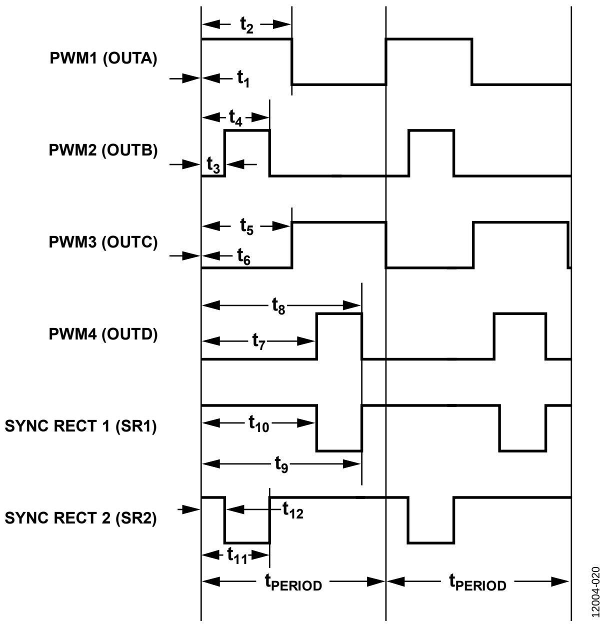


Figure 24. PWM Timing Diagram

Take special care to avoid shoot-through and cross-conduction. It is recommended that the software GUI be used to program these outputs. Figure 25 shows an example configuration to drive a full-bridge topology with synchronous rectification.

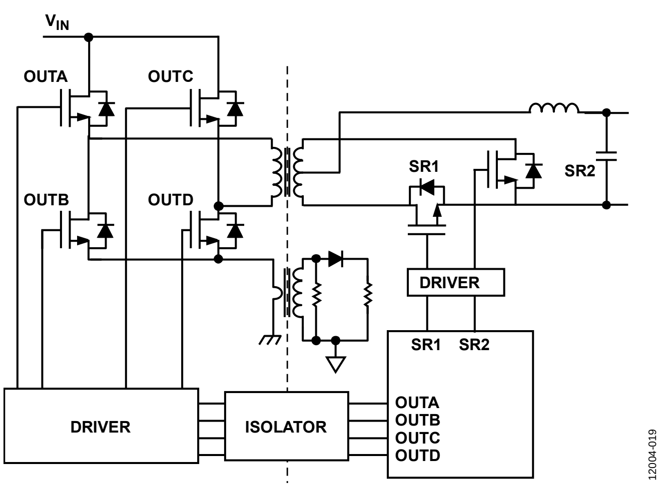


Figure 25. PWM Pin Assignment for Full-Bridge, Phase-Shifted Topology with Synchronous Rectification

Go and Auto Go Command

The PWM outputs (OUTA to OUTD) and the SR outputs (SR1 and SR2) are all synchronized with each other. Therefore, when reprogramming more than one of these outputs, it is important to first update all the registers and then latch the information into the ADP1055 at the same time. This simultaneous updating of the PWM outputs is facilitated by the GO command (Register 0xFE00). The GO command acts as a gate to apply all functions related to the commands at the same time.

The GO command gates the following functions:

- Frequency synchronization
- Line voltage feedforward
- Double update rate, volt-second balance
- Digital filter settings
- Frequency and PWM settings
- Voltage reference change

During reprogramming, the outputs are temporarily disabled. It is recommended that the PWM outputs be disabled when not in use.

The PMBus allows the user to change the voltage setting and the switching frequency on-the-fly. The auto go command (Register 0xFE5B) is an added level of protection that restricts the user from making a change to certain commands (see Table 203).

For more information about the various programmable switching frequencies and PWM timings, see the Switching Frequency Programming section.

SYNCHRONOUS RECTIFICATION

SR1 and SR2 are recommended for use as the PWM control signals when using synchronous rectification. These PWM signals can be configured much like the other PWM outputs.

MODULATION LIMIT

The modulation limit register (Register 0xFE53) can be programmed to apply a maximum duty cycle modulation limit to any PWM signal, thus acting as a clamp for the maximum modulation range of any PWM output. When modulation is enabled, the maximum modulation limit is applied to all PWM outputs collectively. As shown in Figure 26, this limit is the maximum time variation for the modulated edges from the default timing, following the configured modulation direction.

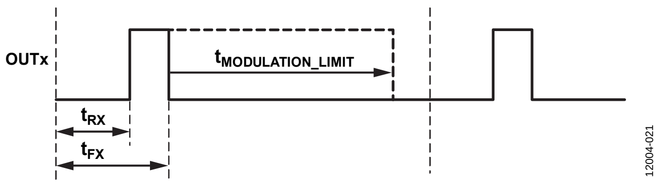


Figure 26. Modulation Limit Settings

There is no minimum duty cycle limit setting. Therefore, the user must set the rising edges and falling edges based on the case with the least modulation to enter pulse skipping mode under very light load conditions.

Each LSB in Register 0xFE53[6:0] corresponds to a unit of a base time step size. The base time step size (20 ns, 40 ns, 80 ns, or 160 ns) depends on the switching frequency; therefore, the modulation limit is based on the value in Register 0xFE53[6:0] multiplied by the corresponding base time step size. The modulated edges are prevented from extending beyond one switching cycle, but the maximum duty cycle is 100% (the minimum pulse width is 5 ns).

The GUI provided with the ADP1055 is recommended for programming this feature (see Figure 27).

Figure 27. Setting Modulation Limits (Modulation Range Shown by Arrows)

SWITCHING FREQUENCY PROGRAMMING

The FREQUENCY_SWITCH command (Register 0x33) sets the switching frequency of the ADP1055 in kilohertz. This command has two data bytes formatted in the linear data format; the programmable frequency ranges from 48 kHz to 1000 kHz.

The ADP1055 does not support every possible frequency due to the infinite combinations of exponent and mantissa values that can be programmed. If a programmed frequency does not exactly match a supported value, it is rounded up to the nearest available frequency. It is recommended that the READ_FREQUENCY command (Register 0x95) be used to determine the exact value of the switching frequency. Table 244 lists the supported frequencies.

ADCs AND TELEMETRY

Two kinds of ADCs are used in the ADP1055:

- Low frequency (LF) Σ-Δ ADCs that runs at 1.56 MHz for accurate measurement and telemetry
- High frequency (HF) flash ADCs for the feedback and control loop

Σ-Δ ADCs have a resolution of one bit and operate differently from traditional flash ADCs. The equivalent resolution obtainable depends on how long the output bit stream of the Σ-Δ ADC is sampled.

Σ-Δ ADCs also differ from Nyquist rate ADCs in that the quantization noise is not uniform across the frequency spectrum. At lower frequencies, the noise is lower, and at higher frequencies, the noise is higher (see Figure 28).

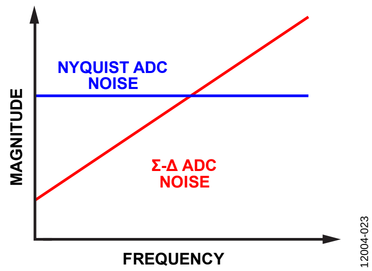


Figure 28. Noise Performance for Nyquist Rate and Σ-Δ ADCs

The low frequency ADC runs at approximately 1.56 MHz. For a specified bandwidth, the equivalent resolution can be calculated as follows:

$$\ln(1.56\ \text{MHz}/BW)/\ln 2 = N \text{ bits}$$

For example, at a bandwidth of 95 Hz, the equivalent resolution/noise is

$$\ln(1.56\ \text{MHz}/95)/\ln 2 = 14 \text{ bits}$$

At a bandwidth of 1.5 kHz, the equivalent resolution/noise is

$$\ln(1.56\ \text{MHz}/1.5\ \text{kHz})/\ln 2 = 10 \text{ bits}$$

The ADC output information is available in the value registers (Register 0xFE96 to Register 0xFEA3) or through the PMBus READ_x commands, where x = VOUT, IOUT, and so on.

ADCs FOR CURRENT SENSING

The ADP1055 has two current sense inputs: CS1 and CS2±. These inputs sense, protect, and control the primary input current and the secondary output current information. The CS1 and CS2± inputs can be calibrated to reduce errors due to external components for accurate telemetry.

CS1 ADC for Primary Side Current

The CS1 pin is typically used for the monitoring and protection of the primary side current. The primary side current is sensed using a current transformer (CT). The input signal at the CS1 pin is fed into the CS1 ADC for current monitoring. Figure 29 shows the typical configuration for the current sense. The READ_IIN command reports the average input current; this reading is updated every 10.5 ms.

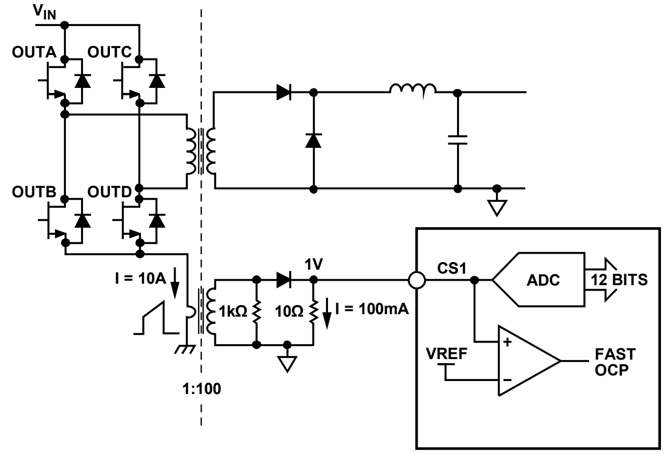


Figure 29. Current Sense 1 (CS1) Operation

CS2 ADC for Secondary Side Current

The CS2+ and CS2− pins are differential inputs used for the monitoring and protection of the secondary side current. The ADP1055 supports differential sensing using low-side current sensing with two ranges for the ADC: 30 mV and 60 mV.

The low input range is used to operate in level shifting mode, when the CS2 terminals are connected directly to the shunt resistor (see Figure 30). In this mode, a pair of internal resistors and current sources are used to perform the necessary level shifting. In this mode, only low-side current sensing is possible, and the ADC range is programmable to 30 mV or 60 mV.

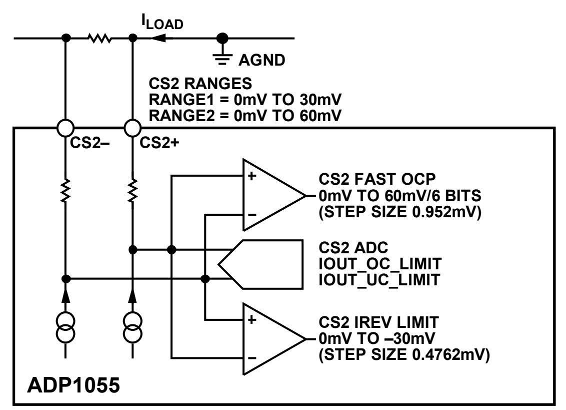


Figure 30. Differential Low-Side Sensing

An additional range of 480 mV (single-ended input only) can be used for high-side sensing or simply as an input with a higher range (see Figure 31). The high input range is used for operation in single-ended mode, where external circuitry must be provided for level shifting of the current signal.

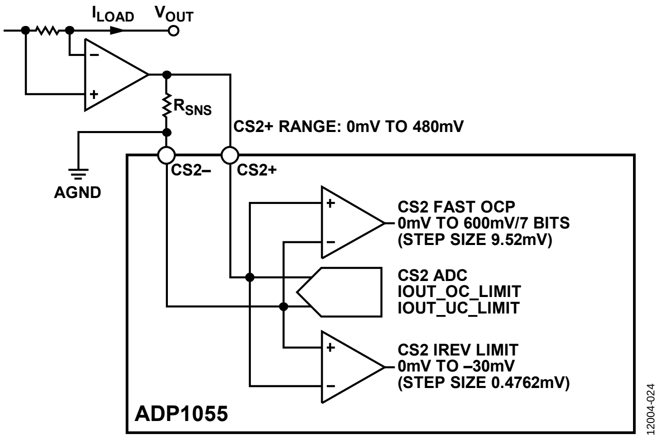


Figure 31. Single-Ended High-Side Sensing

The READ_IOUT command reports the average output current; this reading is updated every 2.6 ms.

ADCs FOR VOLTAGE SENSING

VFF ADC for Input Voltage

The VFF pin is typically used for the monitoring and protection of the primary side voltage. Figure 32 shows a typical configuration for the feedforward circuit.

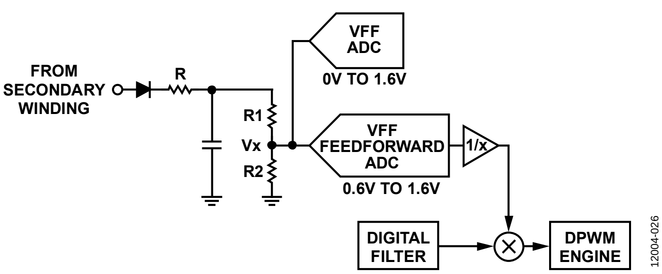


Figure 32. Feedforward Configuration

The input voltage signal can be sensed at the secondary winding of the isolation transformer before the output inductor and must be filtered by an RCD network to eliminate the voltage spike at the switch node (see Figure 32).

In nonisolated topologies, the VFF ADC is connected directly to the primary voltage via a resistive divider with some filtering to eliminate voltage spikes on the bulk capacitor when the power switch is turned on or off. The READ_VIN command reports the average input voltage; this reading is updated every 10.5 ms.

VS ADC for Output Voltage

The VS± pins of the ADP1055 are used for the monitoring, control, and protection of the power supply output. Typically, the output voltage is divided down using a resistive divider such that at the rated output, there is 1.0 V on the VS± pins. The READ_VOUT command reports the average output voltage; this reading is updated every 10.5 ms.

ADCs FOR TEMPERATURE SENSING

For information about the temperature sensing ADCs, see the Temperature Sensing section.

THEORY OF OPERATION

ACCURATE PRIMARY OVERCURRENT PROTECTION

The CS1 ADC is used to measure the average value of the primary current. The 12 MSBs of the reading (CS1_VALUE, Register 0xFE98[13:4]) are converted into PMBus format and compared to the threshold set using the PMBus command IIN_OC_FAULT_LIMIT (Register 0x5B) to make a fault decision. The fault response is set by the IIN_OC_FAULT_RESPONSE command (Register 0x5C).

PRIMARY FAST OVERCURRENT PROTECTION

The input signal on the CS1 pin is also fed into a comparator for pulse-by-pulse OCP protection. The fast OCP comparator is used to limit the peak primary current within each switching cycle. Two thresholds—the 250 mV or 1.2 V threshold—are programmable using Register 0xFE2C[2].

When the CS1 OCP threshold is crossed, the PWM outputs (OUTA to OUTD) are immediately terminated for the remainder of the switching cycle. For the full-bridge topology, where the switching period is divided into two halves, a CS1 OCP event during one half does not terminate the PWM outputs for the second half.

The CS1 OCP comparator provides programmable blanking and debounce to prevent false triggering; these features are programmable using Register 0xFE4E and Register 0xFE2C. The comparator also features a programmable timeout condition (set in Register 0xFE4E[2:0]), which specifies that the CS1 fast OCP condition must be present for a specified number of consecutive switching cycles before the IIN_OC_FAST_FAULT flag is set.

The CS1 fast OCP fault can also be set using the GPIO1 general-purpose input/output pin.

MATCHED CYCLE-BY-CYCLE CURRENT LIMIT (OCP EQUALIZATION)

For a half-bridge converter, the cycle-by-cycle limit feature cannot guarantee an equal duty cycle between the two half cycles of the switching period. The imbalances of each half cycle can cause the center point voltage of the capacitive divider to drift from $V_{IN}/2$ (half the input voltage) toward either ground or the input voltage. This drift, in turn, can lead to output voltage regulation failure, transformer saturation, and the doubling of voltage stress on the synchronous rectifiers.

To avoid these problems, the ADP1055 implements a matched cycle-by-cycle limit. This feature produces a PWM pulse width in the second half cycle that is of equal duration as the preceding pulse when a CS1 fast OCP event occurs (IIN_OC_FAST_FAULT). In other words, when a cycle-by-cycle limit is triggered, the ADP1055 forces the duty cycle in the subsequent half cycle to be exactly the same as that of the previous half cycle.

However, if the CS1 cycle-by-cycle current limit always has the highest priority to terminate the PWM outputs meaning that if a cycle-by-cycle fault occurs during the period where the duty cycle is being equalized, the cycle-by-cycle current fault takes priority. The CS1 OCP duty cycle equalization feature (Register 0xFE57[6]) can be enabled for all topology configurations. The edge selection is the same as for the volt-second balance feature.

LOW TEMPERATURE FILTER

During the soft start process, the soft start filter can be used in combination with the normal mode filter and the light load mode filter. The soft start filter can be configured as a low temperature filter. Using Register 0xFE62[1:0], the low temperature filter is activated on one of three selectable inputs: the external forward temperature reading, the external reverse temperature reading, or the rising edge of GPIO2.

The low temperature pole is activated at a temperature of 10°C; subsequent thresholds are at 6°C, 2°C, and so on, down to −14°C (Register 0xFE62[6:4]). The temperature hysteresis is programmed in steps of 5°C in Register 0xFE62[3:2]. The change of filters from one to another always takes place after a 2 sec time hysteresis plus any other filter transition speed. It is recommended that the ADP1055 GUI be used to program this feature. Table 6 summarizes the use of the filters for low and high temperatures.

Table 6. Filter Options for Low and High Temperatures

Load Condition	Low Temperature	High Temperature
Light load	Light load filter	Light load filter
Heavy load with low temperature, filter disabled	SSF/NMF with ADD_PZ	SSF/NMF with ADD_PZ
Heavy load with low temperature, filter enabled	SSF with ADD_PZ	SSF/NMF with ADD_PZ

VOLTAGE LOOP AUTOCORRECTION

Output voltage sampling is performed using the high speed Nyquist ADC. The output voltage is sampled just before the end of the switching period (t_{SW}) or just before half the switching period ($t_{SW}/2$) if double update rate is enabled. The output voltage ripple ramp changes as the input voltage changes, causing the sampling voltage to also change. Assuming a steady state condition, any dc offsets can be eliminated by sampling the output voltage synchronously with the switching frequency.

Due to the relationship between the output voltage ripple ramp and the input voltage, the average output voltage can drift to a higher value when the input voltage is at its maximum value. To correct for this drift, the ADP1055 uses a low frequency auto-correction loop based on the LF ADC on the VS± pins. Under ideal conditions, the voltage on this input is 1.0 V.

The LF ADC is trimmed in production and has high accuracy over supply, voltage, and temperature; therefore, the autocorrection loop eliminates all errors due to offsets in the high frequency ADC. The ADP1055 assumes that the voltage on the LF ADC is accurate and precise and changes the setpoint (or reference) accordingly so that the VS± pins measure 1.0 V. Any additional offset in the output voltage is due to the tolerances of the external resistor dividers alone.

The speed of the autocorrection loop can be changed using Register 0xFE4A[5:3]. This feature can also be disabled.

The autocorrection loop stores the correction value until the ADP1055 is power cycled. When the power is turned off and then on again, the autocorrection loop is repeated to maintain the most accurate output voltage.

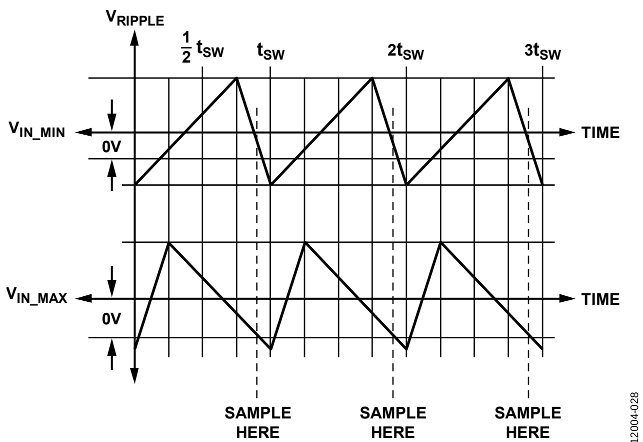


Figure 33. Output Voltage Sampling Point at Minimum and Maximum Input Voltage

NONLINEAR GAIN/RESPONSE

To enhance the dynamic performance of the power supply during a load transient, the nonlinear gain can be used. The error voltage is the reference voltage minus the divided-down output voltage by use of a resistive divider. During steady state, this error voltage is 0 V. During a transient condition, the error voltage is not zero and the digital compensator acts on the error voltage and adjusts the control input to correct for the error. This may take several switching cycles, especially during a transition from DCM to CCM. In such cases, a boosted error signal aids in reducing the settling time and can even avoid an overshoot in some cases. The ADP1055 has a programmable increase in error voltage depending on how far the absolute error voltage is with respect to 0 V. There are four ranges: 1% to 2%, 2% to 3.5%, 3.5% to 4%, and >4%.

The nonlinear gain boost is programmable in Register 0xFE5E and Register 0xFE29[0].

It is recommended that the loop gain of the power supply be measured with the highest programmed gain setting. It is also recommended that an additional gain margin of 4 dB be used when this feature is used due to the nonlinear effect.

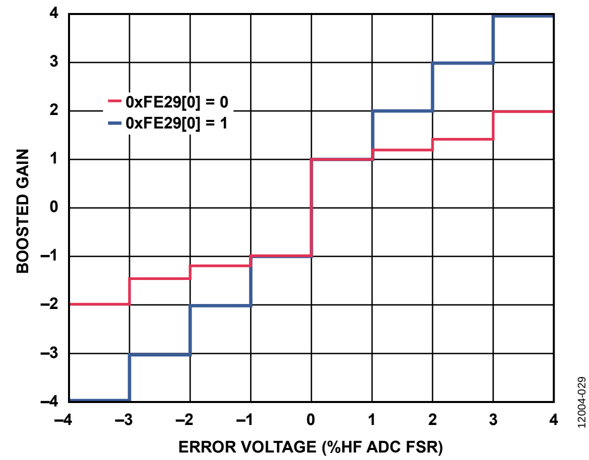


Figure 34. Ideal Settings for Nonlinear Gain (Highest Gain Setting for Highest Error)

INTEGRATOR WINDUP AND OUTPUT VOLTAGE REGULATION LOSS (OVERSHOOT PROTECTION)

The ADP1055 limits the amount of integrator gain when the output voltage is out of regulation for a long period of time due to any of the following:

- Large reduction in input voltage
- Large and sudden change in output voltage setpoint
- Excessive load

The ADP1055 limits the amount of integrator gain to prevent overshoot caused by integrator windup. When duty cycle saturation occurs due to any of these conditions, there is an inherent lag in the system because the integrator is the slowest element of the feedback control path. The ADP1055 inherently prevents the integrator gain from increasing beyond a large value, but offers an additional layer of protection. If the output voltage is out of regulation for more than a certain number of switching cycles, the reference/setpoint is set to the current output voltage, and a soft start from precharge is initiated at a rate programmed by the VOUT_TRANSITION_RATE command (Register 0x27). This behavior eliminates any overshoot in the output voltage. This setting and the number of switching cycles can be programmed in Register 0xFE4A[7:6].

ACCURATE SECONDARY OVERCURRENT PROTECTION

The CS2 ADC is used to measure the average value of the secondary current via the CS2± pins. The 12 MSBs of the reading (CS2_VALUE, Register 0xFE99[13:2]) are converted into PMBus format and compared to the configured threshold to make a fault decision. The LSB of the reading is equal to

$$CS2\ range/2^x$$

where:
CS2 range is the value set in Register 0xFE4F[1:0].
x is the number of bits in Register 0xFE4B[4:3].

Thresholds and limits can be set for CS2 using these PMBus commands: IOUT_OC_FAULT_LIMIT (Register 0x46) and IOUT_OC_WARN_LIMIT (Register 0x4A). The fault response is programmable in Register 0x47.

SECONDARY FAST OVERCURRENT PROTECTION

The input signal on the CS2± pins is also fed into two comparators for fast OCP protection. The fast OCP comparator is used to limit the instantaneous secondary current in either the positive or the negative direction. The CS2 OCP comparator also features a programmable timeout condition (set in Register 0xFE4F[6:4]), which specifies that the CS2 fast OCP condition must be present in consecutive switching cycles before the IOUT_OC_FAST_FAULT flag is set.

When the CS2 fast OCP comparator is used to sense the output inductor current instead of the load current (see Figure 1), the comparator can be used for cycle-by-cycle peak current limiting of the inductor current. Cycle-by-cycle peak current limiting is executed by the termination of the PWM outputs (OUTA to OUTD) to disable power transfer to the secondary side. In an isolated buck derived topology, the inductor current during the on time of the primary switch is a fraction of the inductor current; this feature can be used when the CS1 pin is not used. The CS2 fast OCP threshold can be set in steps of 9.52 mV for the 480 mV CS2 ADC range and in steps of 0.952 mV for the 30 mV and 60 mV CS2 ADC ranges using Register 0xFE2D.

SECONDARY FAST REVERSE CURRENT PROTECTION

A programmable comparator is used to detect reverse current. The comparator can also be used for diode emulation mode to improve light load efficiency. The IOUT_UC_FAST fault is set when the CS2 reverse comparator is asserted. After it is set, the IOUT_UC_FAST fault is cleared between 328 µs and 656 µs after the deassertion of the CS2 reverse comparator.

For all three CS2 ADC ranges (30 mV, 60 mV, and 480 mV), the threshold is programmed in Register 0xFE2E[7:2], and the debounce is programmed in Register 0xFE2E[1:0].

The operation of diode emulation mode depends on the accurate sensing of the zero crossing of the inductor current, which in turn is dependent on proper sensing of the inductor current through the sense resistor. The accuracy of the fast reverse current protection is heavily dependent on the sensing of the inductor current; proper layout techniques (Kelvin sensing) must be followed.

The fast reverse current comparator range is extended to a positive range (0 mV to 30 mV) in addition to the negative range (−30 mV to 0 mV). With this dual range, an accurate sensing of the zero crossing can be tweaked and trimmed to turn off the synchronous rectifiers at exactly the zero crossing of the inductor current by compensating for the gate driver delay and layout inadequacies and by ensuring that there is no excessive voltage stress or voltage spike across the devices.

FEEDFORWARD AND INPUT VOLTAGE SENSE

The ADP1055 supports voltage line feedforward control to improve line transient performance.

The feedforward scheme modifies the modulation value based on the VFF voltage. When the VFF input is 1 V, the line feedforward has no effect. For example, if the digital filter output remains unchanged and the VFF voltage changes to 50% of its original value (but still higher than 0.5 V), the modulation of the falling edges of OUTA to OUTD doubles (see Figure 35). The voltage line feedforward function is optional and is programmable using Register 0xFE29 and Register 0xFECD[2:0]. It is recommended that feedforward be enabled during soft start.

The VFF voltage must be set to 1 V when the nominal input voltage is applied. The voltage at the VFF pin is sampled synchronously with the switching period and, therefore, the decision to modify the PWM outputs based on input voltage is performed at this rate. Typically, the feedforward block can detect and respond to a 3% change in input voltage and make a change to the PWM outputs approximately every 1 µs.

To prevent false triggering of the feedforward block due to noise/voltage spikes on the VFF pin that are carried from the switch node, a small filter capacitor may be needed. The filter capacitor should not be too large, and the time constant should typically be much less than 1 µs. An additional ADC connected to the VFF pin is used to report the ADC value and therefore, the input value, using the resistive dividers. The primary input voltage can be calculated by multiplying Vx by the turns ratio (N1/N2), as follows:

$$V_{PRIMARY} = Vx \times (R1 + R2)/R2 \times (N1/N2)$$

For fault comparison, the input voltage is monitored using the VFF ADC, and the 9 MSBs (VFF_VALUE, Register 0xFE96[13:2]) are converted into PMBus format and compared to the threshold to make a fault decision. Fault limits and their responses can be set using PMBus commands such as VIN_UV_FAULT_LIMIT (Register 0x59), VIN_OV_FAULT_LIMIT (Register 0x55), VIN_UV_FAULT_RESPONSE (Register 0x5A), and VIN_OV_FAULT_RESPONSE (Register 0x56).

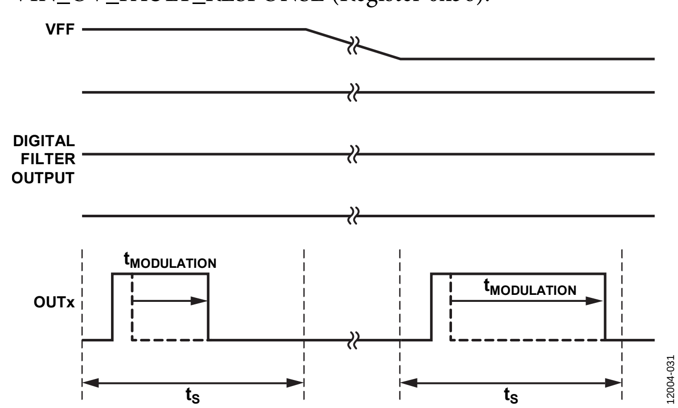


Figure 35. Feedforward Control on Modulation

ACCURATE OVERVOLTAGE AND UNDERVOLTAGE PROTECTION

Accurate overvoltage protection is provided by the PMBus commands VOUT_OV_FAULT_LIMIT (Register 0x40), VOUT_OV_FAULT_RESPONSE (Register 0x41), and VOUT_OV_WARN_LIMIT (Register 0x42).

Similarly, accurate undervoltage protection is provided by the PMBus commands VOUT_UV_WARN_LIMIT (Register 0x43), VOUT_UV_FAULT_LIMIT (Register 0x44), and VOUT_UV_FAULT_RESPONSE (Register 0x45).

All readings are obtained from the low frequency Σ-Δ ADC on the VS+ and VS− pins.

The accurate OVP fault decision is taken after a sampling interval of 82 µs (7-bit averaged value). For OVP, additional sampling time up to a maximum of 320 µs can be programmed in steps of 82 µs using Register 0xFE4D[3:2]. If additional sampling time is enabled, the OV fault condition must be present for the number of additional samples programmed before the VOUT_OV flag is set.

The nominal output voltage at the VS± pins is 1 V, and the OVP and UVP thresholds are set above and below this level. For UVP, the output voltage is monitored using the low frequency Σ-Δ ADC; the nine MSBs of the reading (VS_VALUE, Register 0xFE97[13:5]) are converted into PMBus format and compared with the output undervoltage fault limit threshold. OVP functions similarly, but uses the seven MSBs of the reading (Register 0xFE97[13:7]).

FAST OVERVOLTAGE PROTECTION

The ADP1055 has a dedicated OVP pin for redundant overvoltage protection. This pin performs fast overvoltage protection, where a comparator compares the fractional output voltage by means of resistive dividers to the voltage set by a DAC (see Figure 36). The nominal output voltage at the OVP pin is 1 V. The OVP threshold is programmable using Register 0xFE2F[7:2]. A debounce time (from 40 ns to 10 µs) can be added using Register 0xFE2F[1:0] before the fault response is taken. The fault response is set using the manufacturer specific command VOUT_OV_FAST_FAULT (Register 0xFE34).

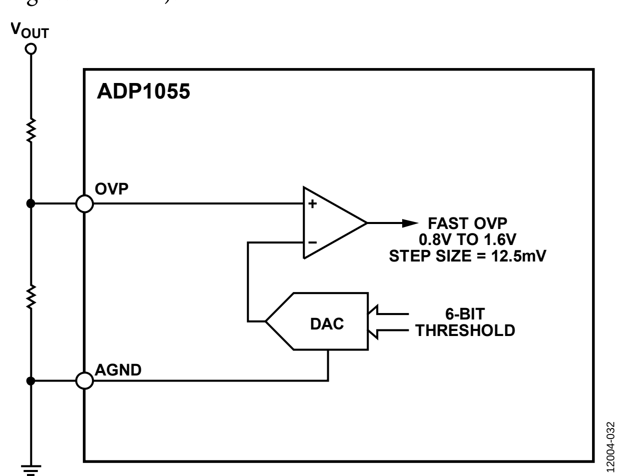


Figure 36. Fast Overvoltage Protection

EXTERNAL FREQUENCY SYNCHRONIZATION

The ADP1055 has a SYNC pin that is used for frequency synchronization. The internal digital phase-locked loop (DPLL) is capable of determining the master frequency on the SYNC pin (f_{SYNC}) and locking the internal switching frequency to the external frequency. The lock or capture range is ±10% of the switching frequency, which is programmed using the FREQUENCY_SWITCH command (Register 0x33).

The PWM outputs are synchronized to the OUTA pin at the start of the switching period. For example, consider a duty cycle on OUTA where the rising (or falling) edge of OUTA is at a time of x µs after the t = 0 of the switching period. After synchronization, the time difference between the rising edge of the external master synchronization frequency (f_{SYNC}) and the rising (or falling) edge of OUTA is x µs. The other PWM outputs are adjusted accordingly. In short, frequency synchronization also locks on to the phase.

The DPLL can recognize the external master frequency within one clock cycle and, after the DPLL has locked on to f_{SYNC}, the time required to achieve synchronization depends on how far apart f_{SYNC} and the internal switching frequency (f_{SW}) are. A typical synchronization time when f_{SYNC} jumps from 90 kHz to 110 kHz with f_{SW} = 100 kHz is approximately 200 µs. The synchronization time depends on the bandwidth of the DPLL, which is approximately $f_{SW}/25$. Therefore, a higher f_{SW} translates to a higher bandwidth.

Using the INTERLEAVE command (Register 0x37), a phase shift in steps of 22.5° can be added. Additional functions that are part of the standard PMBus INTERLEAVE command include the group ID number and the respective number in the group, both programmable using Register 0x37.

The ADP1055 supports only a specific number of switching frequencies. Due to the PWM programming resolution of 5 ns for programming the minimum and maximum PWM modulation limit, the switching frequency and the master clock frequency may not be an exact multiple of each other.

Although the DPLL can detect f_{SYNC} exactly, due to the quantization of the internal frequency settings, there is a possibility that f_{SYNC} and f_{SW} may not be the same and may differ by a small amount. To prevent the frequency from jumping from one value of f_{SW} to another (which causes the switching period to change) due to the quantization of f_{SW}, f_{SW} is set to the closest quantized value to f_{SYNC} rounded down. Due to this effect or due to a non-ideality (jitter) of the master clock, a dither can be added to the clock frequency (using Register 0xFE55[1]) of 5 ns or 10 ns. Using this dither, f_{SW} is equal to f_{SYNC} on average.

For a full-bridge topology, it is recommended that Register 0xFE55[0] = 0 so that half the switching period is an exact multiple of 5 ns.

After synchronization, if the master clock suddenly changes to 0 Hz, the ADP1055 continues to operate at the last known master frequency. However, if the device is power cycled through a soft start, the master frequency is not retained, and the ADP1055 defaults to the internal frequency set by FREQUENCY_SWITCH (Register 0x33). If the device is off and the master frequency is already present on the SYNC pin, the switching frequency is already set to the master frequency when the ADP1055 turns on.

It is recommended that the synchronization function be disabled when not in use (Register 0xFE55[6] = 1) because switching noise may be coupled into the SYNC pin.

The switching frequency can be read back using the PMBus command READ_FREQUENCY (Register 0x95).

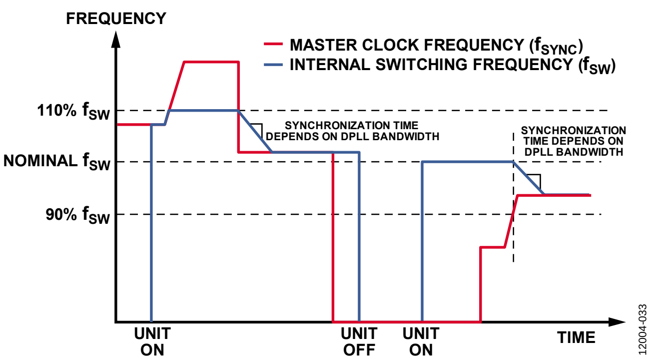


Figure 37. Tracking of SYNC Function

TEMPERATURE SENSING

The ADP1055 has two external temperature sensors. For the external temperature sensors, PN junction devices such as transistors are connected back to back; these devices are called forward diode and reverse diode (see Figure 38).

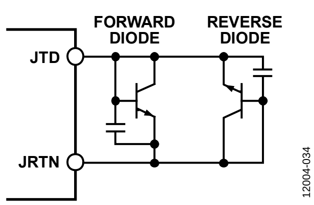


Figure 38. Temperature Sensor, Forward and Reverse Sensing

The temperature can be read using the following standard PMBus commands: READ_TEMPERATURE_2 (Register 0x8E) for the external sensing forward diode, and READ_TEMPERATURE_3 (Register 0x8F) for the external sensing reverse diode.

The ADP1055 measures the temperature readings of the external forward diode and the external reverse diode in that order. Using proprietary zero offset circuitry (patent pending), the inputs to the ADCs are zeroed out before each temperature measurement to compensate for temperature dependent offset variation, which affects the measurement result. This allows the forward and reverse sensing PN diodes to be kept far away from each other without affecting the reading significantly due to offset errors.

The ADP1055 is factory calibrated at ambient temperature for minimum error using the BC847A transistor (with $n_f = 1.00$) placed in the position of forward diode. The nonideality factor (n_f) of the transistor in $\Delta V_{BE} = n_f \times V_T \times \ln(I/I_S)$.

Care must be taken to isolate the thermal sensor so that switching noise is not coupled into the base by the parasitic capacitances from base to ground and emitter to ground. It is recommended that a low-pass filter be added by placing a large capacitor of 220 pF to 470 pF across the base emitter junction to remove any noise. Adding a reverse diode introduces an additional error due to the reverse leakage current. The reference current (I_{REF}), used for the sensing algorithm to 10 µA, can be programmed by setting Register 0xFE5A[2:0] = 0x04.

The update rate for each subsequent temperature reading (external forward reading, followed by external reverse reading) is approximately 200 ms if reverse sensing is enabled, and approximately 130 ms if reverse sensing is disabled, with 14-bit resolution (Register 0xFE5A[6:5] = 0x3).

Overtemperature protection (OTP) can be set using OT_FAULT_LIMIT (Register 0x4F), OT_FAULT_RESPONSE (Register 0x50), and OT_WARN_LIMIT (Register 0x51). OTP functions for the forward diode only. The hysteresis for OTP is the difference between the OT_FAULT_LIMIT and OT_WARN_LIMIT values. For example, if OT_FAULT_LIMIT is set to disable all PWM outputs at 125°C and OT_WARN_LIMIT is set to 115°C, the ADP1055 stops switching at 125°C and begins switching again only when the temperature falls below 115°C.

GPIO AND PGOOD SIGNALS

Four dedicated pins serve as general-purpose inputs/outputs (GPIOs). Each pin can be configured as an input or output with a programmable polarity (set in Register 0xFE40). Do not change the configuration of the pin from input to output or from output to input on the fly.

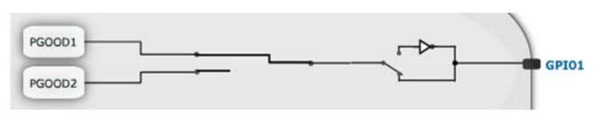


Figure 39. GPIO1 Configured as an Output with Normal Polarity

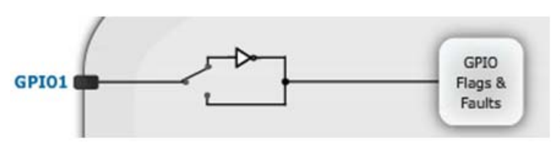


Figure 40. GPIO1 Configured as an Input with Negated Polarity

When the pin is configured as an input, a programmable action can be taken (similar to the PMBus voltage faults) using Register 0xFE39 to Register 0xFE3C (GPIOx_FAULT_RESPONSE).

When the GPIOx pin is configured as an output, internal signals known as PGOOD1 and PGOOD2 can be logically combined and output on the pin. The logic functions for the GPIO pins are programmable in Register 0xFE41 and Register 0xFE42.

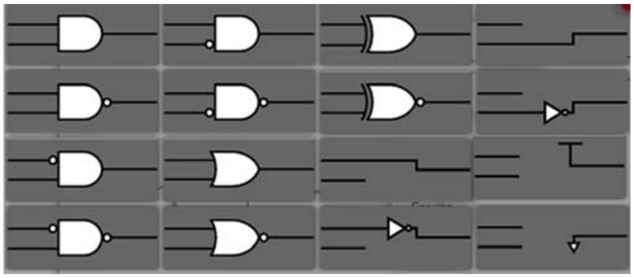


Figure 41. Logical Functions Available Using PGOOD1 (LOGIC) PGOOD2

Various flags can be programmed into PGOOD1 and PGOOD2 using Register 0xFE44 and Register 0xFE45. When coupled with the GPIOs, these flags can be used to trigger signals to provide external logic functions by means of discrete circuits. For example, in Figure 42, the overtemperature flag or the VIN_UV flag can set PGOOD2. This feature is useful for signaling the power chain downstream so that any appropriate action can be taken. A delay (debounce) can be added to the PGOODx signals using Register 0xFE43.

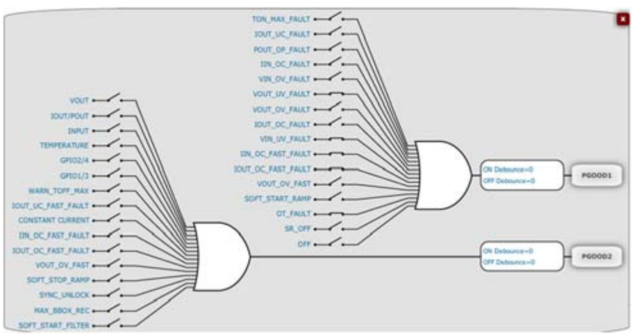


Figure 42. Signals Routed into PGOOD1 and PGOOD2

In addition to triggering the GPIOs, the PGOOD1_FAULT and PGOOD2_FAULT flags are set in Register 0xFE93[6] (FAULT_UNKNOWN[6]) and Register 0xFE93[7] (FAULT_UNKNOWN[7]) (where 0 means no fault). The same debounce applies to the flags.

The POWER_GOOD_ON register (Register 0x5E) sets the voltage that the output voltage must exceed before POWER_GOOD can be set. Similarly, the output voltage must fall below the POWER_GOOD_OFF threshold (set in Register 0x5F) for POWER_GOOD to be reset.

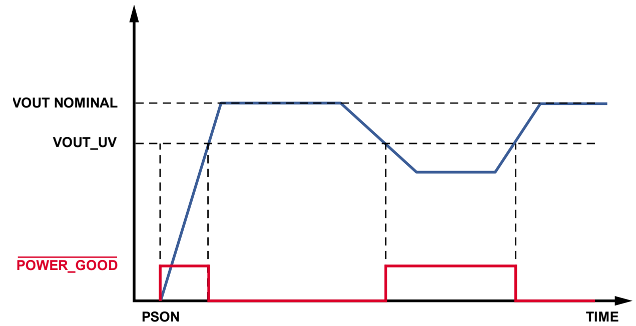


Figure 43. POWER_GOOD Flag Tripped by VOUT

Note that the PMBus signal POWER_GOOD cannot be brought out to the GPIOx pins, but it can be brought out to the SMBALRT pin. The PMBus signal POWER_GOOD is accessible through STATUS_WORD (Register 0x79[11]). POWER_GOOD is asserted (0 means power is good) only if all of the following conditions are met:

- VOUT has exceeded POWER_GOOD_ON.
- VOUT has not fallen below POWER_GOOD_OFF.
- PGOOD1_FAULT is not set.
- PGOOD2_FAULT is not set.

UVP is not associated with this flag; however, the PGOOD1_FAULT and PGOOD2_FAULT flags can be programmed to select UVP (VOUT_UV_FAULT). There is no debounce for POWER_GOOD.

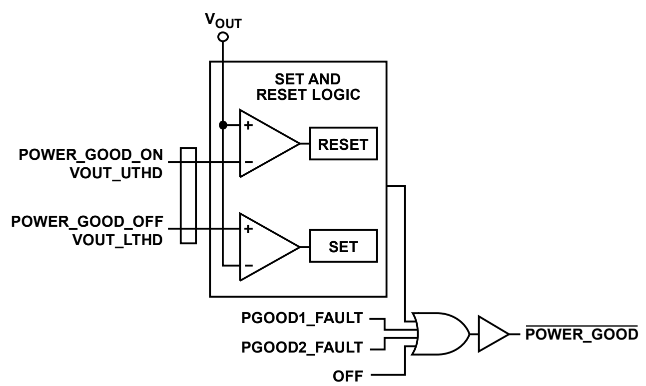


Figure 44. POWER_GOOD Signal Path

GPIO3 AND GPIO4 AS SNUBBER PWM OUTPUTS

The GPIO3 and GPIO4 pins of the ADP1055 can be configured as two signals used for an active snubber. This circuitry can be used to provide a drive signals for an active clamp.

Snubber Configuration

The on time of the snubber and the dead time of the snubber signals can be programmed using Register 0xFE63 and Register 0xFE64[5:0], respectively. The active clamp signals turn on after a selectable dead time (0 ns to 315 ns in steps of 5 ns, programmable using Register 0xFE64[5:0]). Using Register 0xFE65[7], the active clamp signals can be configured on one of the following:

- Falling edge of SR1 or SR2 signal
- Falling edge of $\overline{\text{OUTC}}$ and $\overline{\text{OUTD}}$

The snubber signal stays on for a fixed value regardless of the duty cycle and load condition programmed in Register 0xFE63. However, the snubber signal is toggled as soon as it encounters the next SRx rising edge or the next OUTx falling edge, even if the programmed on time is of a greater value.

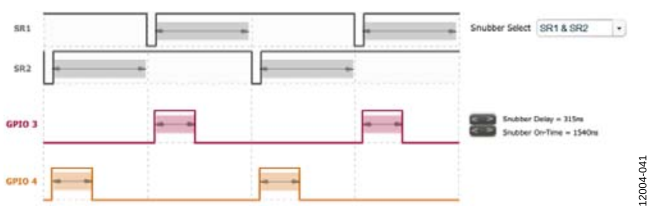


Figure 45. Active Clamp Snubber Configured on SRx Signals

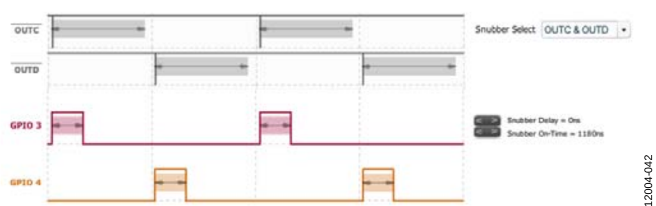


Figure 46. Active Clamp Snubber Configured on OUTx Signals

Miscellaneous Snubber Configuration

Using Register 0xFE64[7:6]), the snubber configuration can be set to one of these options:

- Option 1: Both GPIO3 and GPIO4 are configured as regular signals, as described in the GPIO and PGOOD Signals section (see Figure 47).
- Option 2: GPIO3 is configured as an active snubber PWM output; GPIO4 is configured as a regular signal (see Figure 48).
- Option 3: GPIO3 is configured as a regular signal; GPIO4 is configured as an active snubber PWM output (see Figure 49).
- Option 4: Both GPIO3 and GPIO4 are configured as active snubber PWM outputs (see Figure 50).

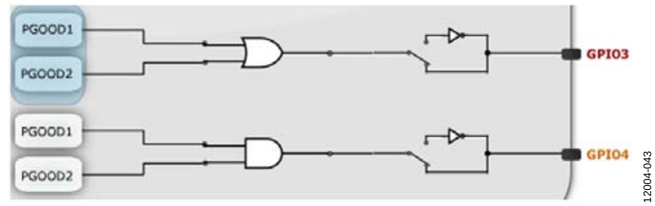


Figure 47. Option 1: GPIO3 and GPIO4 Configured as Regular Signals

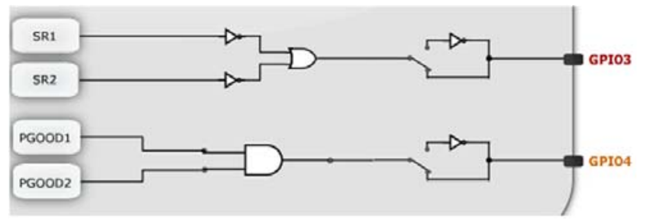


Figure 48. Option 2: GPIO3 Configured as an Active Snubber PWM Output; GPIO4 Configured as a Regular Signal

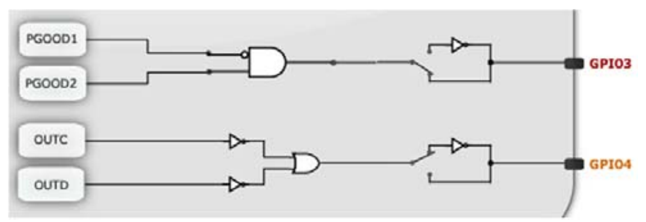


Figure 49. Option 3: GPIO3 Configured as a Regular Signal; GPIO4 Configured as an Active Snubber PWM Output

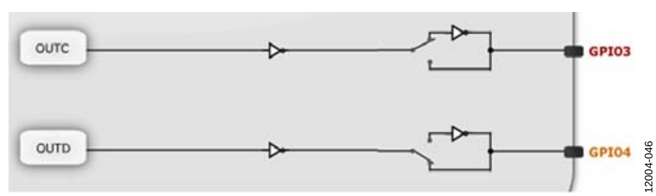


Figure 50. Option 4: GPIO3 and GPIO4 Configured as Active Snubber PWM Outputs

The GPIO polarity bit can be configured using the same bits described in the GPIO and PGOOD Signals section. The polarity bit allows true versatility with the use of either P channel or N channel FETs, depending on the application. These PWM signals can be blanked during soft start and soft stop using Register 0xFE46[14] and Register 0xFE47[14]. The signals are active as long as the system does not shut down in response to a fault condition or a PSOFF command is issued.

AVERAGE CONSTANT CURRENT MODE

The ADP1055 supports constant current (CC) mode. The constant current mode threshold is set in one of two ways:

- Using the PMBus definition of CC mode (Register 0xFE4F[2] = 0)
- Using the manufacturer specific CC mode (Register 0xFE4F[2] = 1)

In both modes, the constant current limit can be set as a percentage of the IOUT_OC_FAULT_LIMIT—for example, ±3.125%, ±6.25%, ±12.5%, ±25%, ±50%, or ±100%—using Register 0xFE5D[3:0].

In the PMBus definition of CC mode, the constant current mode is activated on a IOUT_OC_FAULT fault, and the load current is limited to the CC limit, as specified in Register 0xFE5D[3:0]. Only positive percentages are applicable when the PMBus definition of CC mode is used. The fault responses to IOUT_OC_FAULT in this case are defined as per the PMBus format. The system enters CC mode on detection of the CS2 current (~2.6 ms, 12-bit averaging of CS2 ADC). Any further changes in the current while the device is in CC mode take place according to the averaging speed selectable in Register 0xFE4F[7]. For CC mode to work properly using the PMBus faults, the IOUT_OC_FAULT debounce must be set to 0 ms.

In the manufacturer specific CC mode, the CC limit is exactly the limit that is programmed, and there is no need to trip the IOUT_OC_FAULT before entering CC mode. Fault responses to IOUT_OC_FAULT in this case are to ignore the fault or to shut down the device in response to the fault (Register 0x47[7:6] = 11). Other settings programmed in the response section (for example, Register 0x47[7:6] = 00, 01, or 10) are ignored.

Below the IOUT_OC_FAULT_LIMIT threshold, the ADP1055 operates in constant voltage mode, using the output voltage as the feedback signal for closed-loop operation.

When the ADP1055 crosses the constant current mode threshold, the CS2 current reading is used to control the output voltage regulation point. The output voltage is ramped down linearly as the load increases to ensure that the load current remains constant.

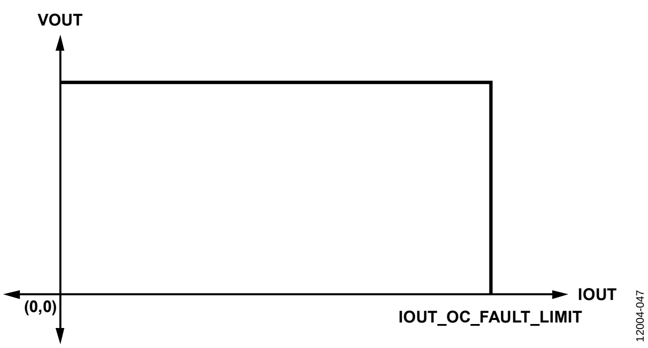


Figure 51. Typical Characteristics in Constant Current (CC) Mode

The constant current control loop has relatively low bandwidth because the current is averaged over a 328 μs period (9-bit decimation of the CS2 bit stream). The output voltage changes at a maximum rate of 1.18 V/sec at the VS± pins; therefore, the instantaneous value of the current can exceed the constant current limit for a very short period of time, depending on the severity of the transient condition.

For a faster dynamic response of the constant current mode, the turbo mode can be used. In turbo mode, the averaging time can be decreased to a period of ~41 μs (6-bit decimation of the CS2 bit stream). In turbo mode, the slew rate of the output voltage can be programmed using Register 0xFE5D[5:4].

As the output voltage is reduced to maintain a constant load current, xxx_FAULT_RESPONSE (for example, Register 0x47[7:6] = 01) can be used to program a fault response when the output voltage falls below a specific threshold set by IOUT_OC_LV_LIMIT (Register 0x48).

It is important to note that although constant current mode can be applied to any current fault (input or output current) according to the PMBus specification, the ADP1055 applies the constant current mode only to maintain a constant output current. For example, if the IOUT_UC_FAULT is programmed to enter constant current mode, the ADP1055 does not boost the output voltage to maintain the current level set by IOUT_UC_LIMIT.

Using the manufacturer specific fault response for constant current mode, the system can be forced into constant current mode at a specific threshold, and if this threshold persists for a specified amount of time (based on the debounce time), the IOUT_OC_FAULT is tripped (see Figure 52).

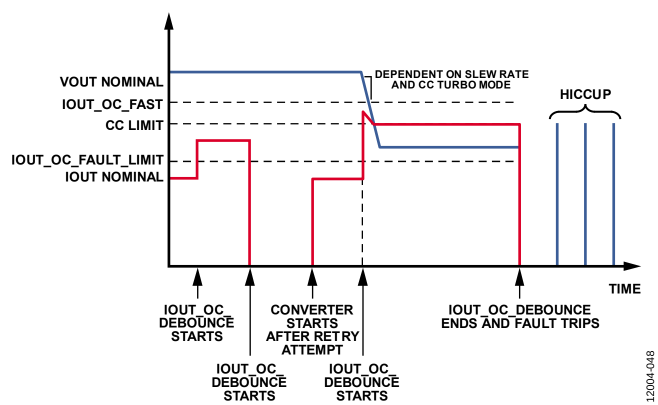


Figure 52. Constant Current with Hiccup

32-BIT KEY CODE

The ADP1055 supports a 32-bit password (key code) in addition to the EEPROM password set by Register 0xD5. This 32-bit key code enables another level of protection for the user and the manufacturer to limit access to certain commands and operations.

Entering the Key Code

The key code is a unique 32-bit pass code that is entered using the KEY_CODE command (Register 0xD7). Because this command is a block read/block write command, the first data byte of this command is the number of bytes (4). When entering the key code, the data has this format: {0x04, KeyCode[7:0], KeyCode[15:8], KeyCode[23:16], KeyCode[31:17]}. (Note the low byte to high byte order of the 32-bit key code.) After the correct key code is entered, the user has full write access to all commands, including PMBus and manufacturer specific commands such as CMD_MASK (Register 0xF4) and EXTCMD_MASK (Register 0xF5), which can be used to disable other commands using the command masking feature. The key code is also needed to change the EEPROM password (Register 0xD5).

Command Mask

The command mask feature allows any PMBus command or manufacturer specific command to be masked in the ADP1055. If the command is masked, a read or a write to that command results in a no acknowledge (NACK). PMBus commands are masked using Register 0xF4; manufacturer specific commands are masked using Register 0xF5. Using command masking, the user can block access to certain commands—such as commands that configure the switching frequency, the digital compensator, or the output voltage setpoint—while allowing access to the readback commands (READ_x, where x = IOUT, IN, VOUT, VIN, and so on). The SLV_ADDR_SELECT (Register 0xD0), EEPROM_PASSWORD (Register 0xD5), KEY_CODE (Register 0xD7), EEPROM_INFO (Register 0xF1), CMD_MASK (Register 0xF4), and EXTCMD_MASK (Register 0xF5) commands are not maskable. It is recommended that the ADP1055 GUI be used to configure the masking function (see Figure 53).

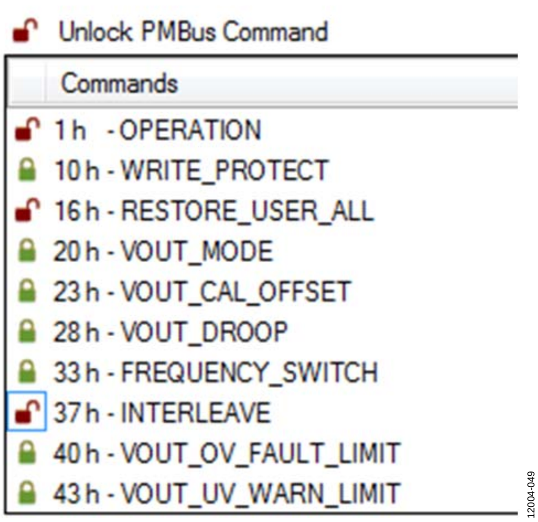


Figure 53. Snapshot of the GUI Showing Lock and Unlock of Commands

Changing the Key Code

To change the key code, first unlock the EEPROM as described in the Unlock the EEPROM section.

1. After the EEPROM is unlocked, enter the 32-bit key code (default key code is 0xFFFFFFFF) using the KEY_CODE command (Register 0xD7).
2. Enter the new key code using the same command, for example, 0x1FEEDBAC (a pneumonic for negative feedback in twos complement format).
3. The key code is now changed to the new key code. Save the new key code into the user settings page of the EEPROM using the STORE_USER_ALL command (Register 0x15).

SR PHASE-IN, SR TRANSITION, AND SR FAST PHASE-IN

The SR1 and SR2 outputs are recommended for use as the PWM control signals when using synchronous rectification for the output (or secondary) rectifiers. These PWM signals can be configured similar to other PWM outputs.

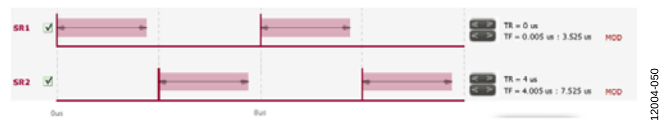


Figure 54. Example of SR Outputs in Light Load Mode (LLM)

Figure 55. Example of SR Outputs in Heavy Load (CCM)

When the mode changes from LLM to CCM, an abrupt change in the SR outputs may cause the output voltage to dip momentarily. An optional SR transition process (during which the pulse width of the SR PWM outputs is increased slowly) can be applied to the SR1 and SR2 outputs. The SR transition can be enabled by setting Register 0xFE50[5].

The speed at which the SR edges move from zero duty cycle to maximum duty cycle (as determined by the control loop) can be programmed from 5 ns per t_{SW} to 5 ns per 1024 t_{SW} (t_{SW} = switching cycle) using Register 0xFE5F[7:4].

OUTPUT VOLTAGE SLEW RATE

The output voltage slew rate (or transition rate) can be set using the PMBus VOUT_TRANSITION_RATE command (Register 0x27). The slew rate determines how quickly the output voltage is adjusted in response to a change in the digital reference.

The fastest slew rate supported by the ADP1055 is 1 kV/sec, and the slowest rate is 14.3 V/sec. A PMBus command setting of 0 sets the slew rate to the slowest setting. This slew rate is the rate that the internal setpoint reference can change; the actual change of the output voltage depends on the bandwidth of the control loop and its ability to track the reference.

The VOUT_TRANSITION_RATE command can be disabled using Register 0xFE65[2].

ADAPTIVE DEAD TIME COMPENSATION

Register 0xFE1D to Register 0xFE24 are the adaptive dead time (ADT) registers. These registers allow the dead time between

PWM edges to be adapted on the fly. The ADT feature is activated when the primary or secondary current (CS1 or CS2) falls below the threshold programmed in Register 0xFE1E. The software GUI allows the user to easily program the dead time values, and it is recommended that the GUI be used for this purpose.

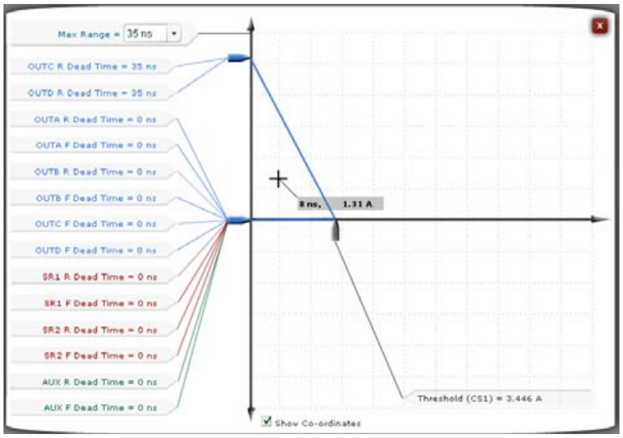


Figure 56. Adaptive Dead Time Window in the GUI

Before ADT is configured, the primary current threshold must be programmed. Each individual PWM rising and falling edge (t_1 to t_{12}) can then be programmed to have a specific dead time offset at no load (zero current). This offset can be positive or negative and is relative to the nominal edge position. When the current is between zero and the threshold, the amount of dead time is linearly adjusted in steps of 5 ns. The averaging period of the CS1/CS2 current is selected using Register 0xFE1E[7], and the speed of the dead time adjustment can also be programmed to accommodate faster or slower adjustment in Register 0xFE1D[5:0].

For example, if the CS1 threshold is set to 2 A, t_1 has a nominal rising edge of 100 ns. If the ADT setting for t_1 is 40 ns at no load, t_1 moves to 140 ns when the current is 0 A and to 120 ns when the current is 1 A. Similarly, ADT can be applied in the negative direction.

The ADT feature is useful in quasi resonant topologies where an energy transfer occurs from the inductor (generally, from one or more of the leakage inductance, magnetizing inductance, and external inductance) to the capacitor (usually the drain-source capacitance of the MOSFET power switch) for the purpose of achieving zero voltage switching (ZVS).

Generally, the condition for ensuring ZVS is that the energy in the inductor must exceed the energy in the capacitor. A resonant transition occurs when energy is dumped from the inductor to the capacitor (capacitor being charged with opposite polarity voltage). At one point, there is close to 0 V across the MOSFET, and at this point the power switch is turned on.

If this energy is not sufficient, the MOSFET turns on without ZVS. In this case, ADT can be used to wait until the resonant transition reaches its peak value so that a near ZVS turn-on is achieved.

SR DELAY

The ADP1055 is well suited for dc-to-dc converters in isolated topologies. Each time a PWM signal crosses the isolation barrier, an additional propagation delay is added due to the isolating components. The ADP1055 allows programming of an adjustable delay (0 ns to 315 ns in steps of 5 ns) using Register 0xFE52[5:0]. This delay moves both SR1 and SR2 later in time with respect to OUTA to OUTD to compensate for the added delay due to the isolating components. In this way, the edges of all PWM outputs can be aligned, and the SR delay can be applied separately as a constant dead time.

CURRENT SHARING (ISHARE PIN)

The ADP1055 supports both analog current sharing and digital current sharing. The ADP1055 can use either the CS1 current information or the CS2 current information for current sharing.

Analog Current Sharing

Analog current sharing uses the internal current sensing circuitry to provide a current reading to an external current error amplifier. Therefore, an additional differential current amplifier is not necessary.

The current reading from CS1 or CS2 can be output to the ISHARE pin in the form of a digital bit stream, which is the output of the current sense ADC (see Figure 57). The bit stream is proportional to the current delivered by this unit to the load. By filtering this digital bit stream using an external RC filter, the current information is turned into an analog voltage that is proportional to the current delivered by this unit to the load. This voltage can be compared to the share bus voltage. If the unit is not supplying enough current, an error signal can be applied to the VS± feedback point. This signal causes the unit to increase its output voltage and, in turn, its current contribution to the load.

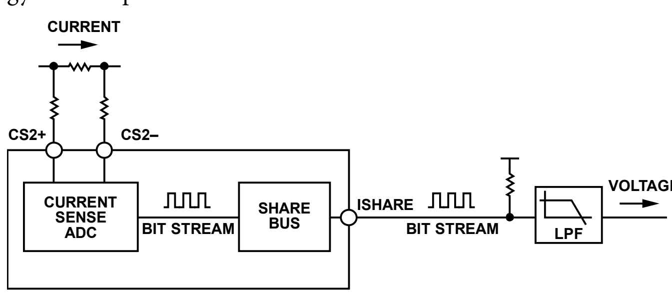


Figure 57. Analog Current Share Configuration

Digital Share Bus

The digital share bus scheme is similar in principle to the traditional analog share bus scheme. The difference is that instead of using a voltage on the share bus to represent current, a digital word is used.

The ADP1055 outputs a digital word onto the share bus. The digital word is a function of the current that the power supply is providing (the higher the current, the larger the digital word).

The power supply with the highest current controls the bus (master). A power supply that is putting out less current (slave) sees that another supply is providing more power to the load than it is.

During the next cycle, the slave increases its current output contribution by increasing its output voltage. This cycle continues until the slave outputs the same current as the master, within a programmable tolerance range. Figure 58 shows the configuration of the digital share bus.

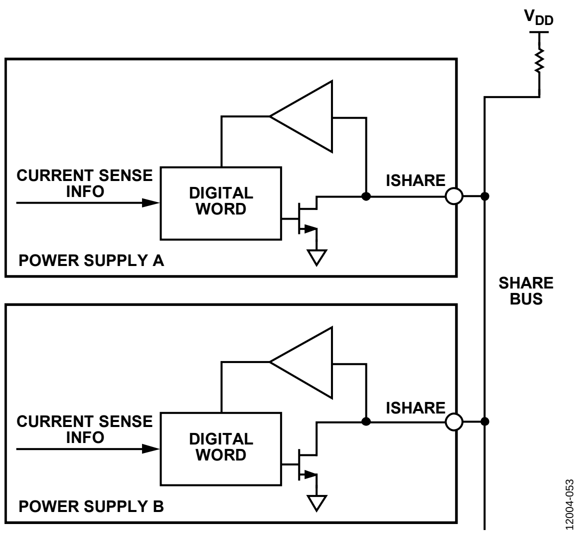


Figure 58. Digital Current Share Configuration

The digital share bus is based on a single-wire communication bus principle; that is, the clock and data signals are contained together.

When two or more ADP1055 devices are connected, they synchronize their share bus timing. This synchronization is performed by the start bit at the beginning of a communications frame. If a new ADP1055 is hot-swapped onto an existing digital share bus, the device waits to begin sharing until the next frame. The new ADP1055 monitors the share bus until it sees a stop bit, which designates the end of a share frame. It then performs synchronization with the other ADP1055 devices during the next start bit. The digital share bus frame is shown in Figure 60.

Figure 59 shows the possible signals on the share bus.

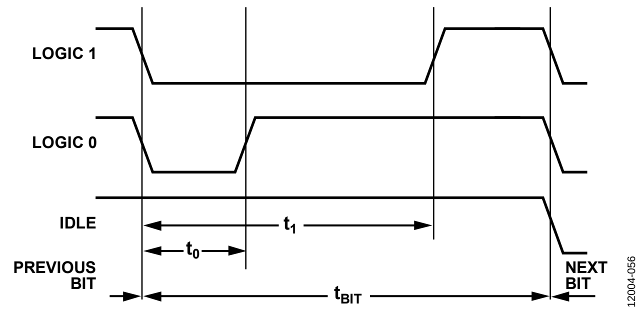


Figure 59. Share Bus High, Low, and Idle Bits

The length of a bit (t_{BIT}) is fixed at 10 µs. A Logic 1 is defined as a high-to-low transition at the start of the bit and a low-to-high transition at 75% of t_{BIT}. A Logic 0 is defined as a high-to-low transition at the start of the bit and a low-to-high transition at 25% of t_{BIT}.

The bus is idle when it is high during the whole period of t_{BIT}. All other activity on the bus is illegal. Glitches up to t_{GLITCH} (200 ns) are ignored.

The digital word that represents the current information is eight bits long. The ADP1055 takes the eight MSBs of the CS1 or CS2 reading (the current share signal specified in Register 0xFE2B[3]) and uses this reading as the digital word. When read, the share bus value at any given time is equal to the CS1 or CS2 current reading (see Figure 61).

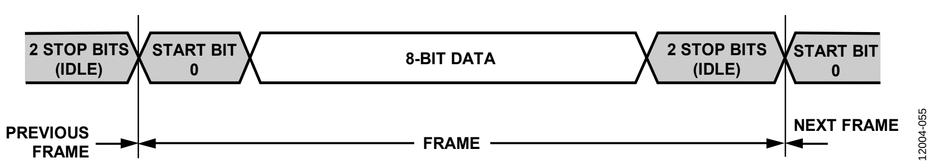


Figure 60. Digital Current Share Frame Timing Diagram

Digital Share Bus Scheme

Each power supply compares the digital word that it is outputting with the digital words of all the other supplies on the bus.

Round 1

In Round 1, every supply first places its MSB on the bus. If a supply senses that its MSB is the same as the value on the bus, it continues to Round 2. If a supply senses that its MSB is less than the value on the bus, it means that this supply must be a slave.

When a supply becomes a slave, it stops communicating on the share bus because it knows that it is not the master. The supply then increases its output voltage in an attempt to share more current.

If two units have the same MSB, they both continue to Round 2 because either of them may be the master.

Round 2

In Round 2, all supplies that are still communicating on the bus place their second MSB on the share bus. If a supply senses that its MSB is less than the value on the bus, it means that this supply must be a slave and it stops communicating on the share bus.

Round 3 to Round 8

The same algorithm is repeated for up to eight rounds to allow supplies to compare their digital words and, in this way, to determine whether each unit is the master or a slave.

Digital Share Bus Configuration

The digital share bus can be configured in various ways. The bandwidth of the share bus loop is programmable in Register 0xFE2B[2:0]. The extent to which a slave tries to match the current of the master is programmable in Register 0xFE2A[3:0]. The slave moves up 1 LSB for every share bus transaction (eight data bits plus start and stop bits; see the description of Register 0xFE2B in Table 156). The master moves down x LSBs per share bus transaction, where x is the share bus setting in Register 0xFE2A[7:4]. The maximum limit for the output voltage of the slave is 400 mV at the VS± pins. The ISHARE_FAULT is set when the current share loop reaches its maximum value, that is, 400 mV at the VS± pins. It is recommended that there be a load line of 5 mΩ to 10 mΩ between the output terminals of the power supply to the load.

DROOP SHARING

The droop sharing functionality is implemented using the VOUT_DROOP command (Register 0x28). Using this command, a fixed amount of load line in mV/A can be applied to the output voltage. The output voltage is continuously sampled with a selectable rate (set in Register 0xFE65[1:0]) before the droop is applied. Under droop current sharing, the output voltage changes at a rate determined by the VOUT_TRANSITION_ RATE command. Setting 0xFE65[2] = 1 changes the internal voltage reference to the fastest internal supported rate.

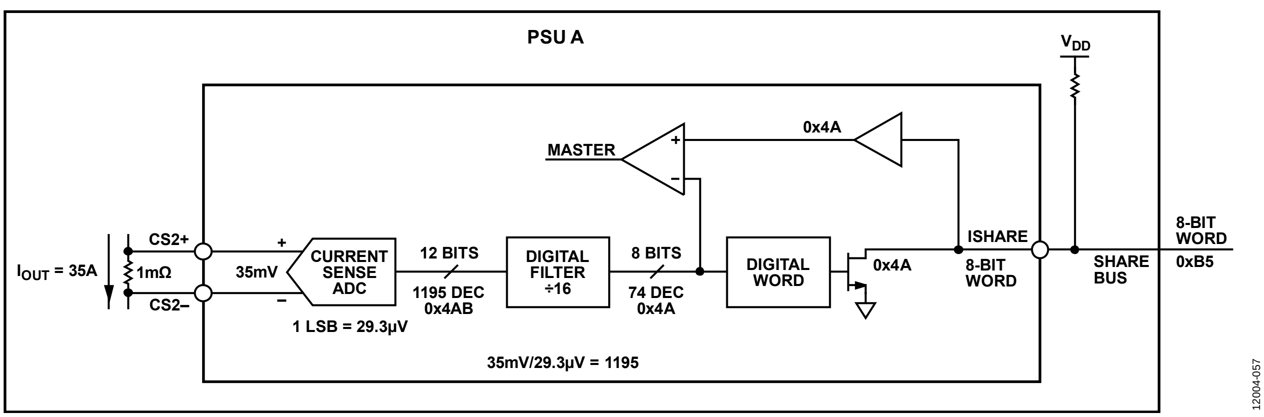
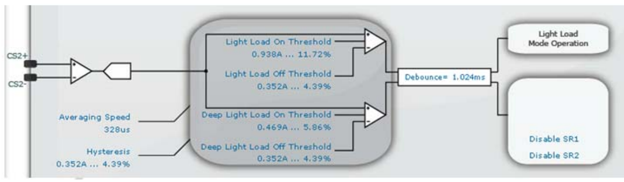


Figure 61. How the Share Bus Generates the Digital Word to Place on the Digital Share Bus

LIGHT LOAD MODE AND DEEP LIGHT LOAD MODE

To facilitate a reduction of power loss at light loads, the ADP1055 supports light load mode and deep light load mode. The threshold, speed, and hysteresis for deep light load mode are selectable in Register 0xFE4B. In deep light load mode, a selectable set of PWM outputs can be disabled using Register 0xFE4C. Typical examples include shutting down the synchronous rectifiers or shutting down certain PWM outputs in an interleaved topology for phase shedding.



12004-058

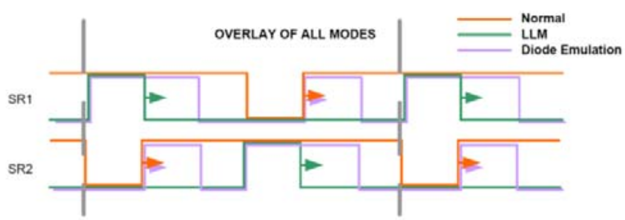
Figure 62. Light Load Settings in the GUI

The threshold, speed, and hysteresis for light load mode are programmed in Register 0xFE5F. In SR light load mode (SR LLM), the synchronous rectifiers operate in the forward conduction mode only; that is, they are turned off during the freewheeling period of the switching period in a buck derived isolated topology (either half wave or full wave rectifier on the output). In this way, the loss associated with the diode drop of the MOSFET is minimized by turning the channel of the MOSFET on, as well as maintaining the output inductor in discontinuous conduction mode (DCM). The rising and falling edges of the synchronous rectifiers in SR LLM are programmed in Register 0xFE19 to Register 0xFE1C.

When entering SR LLM from SR normal mode or deep LLM, or when exiting SR LLM to SR normal mode based on the hysteresis level, the SR edges move as programmed by the phase-in speed in Register 0xFE5F[7:4].

The SR LLM settings (Register 0xFE19 to Register 0xFE1C) determine the minimum and maximum rising and falling edges of the SR PWM outputs in SR LLM mode. If the load demands a duty cycle between the minimum and maximum settings, the SR edges are adjusted according to the required duty cycle for OUTA to OUTD.

To enable the deep light load mode, the light load mode threshold must be greater than zero.



12004-059

Figure 63. Overlay of All SR Modes

PULSE SKIPPING

The ADP1055 supports a pulse skipping mode in which a PWM pulse is not turned on for the entire switching period. Pulse skipping can be activated by setting Register 0xFE50[1] = 1.

The ADP1055 enters pulse skipping mode when the required duty cycle is less than the modulation value set in Register 0xFE53. Register 0xFE50[0] = 0 sets all modulated edges to the start of the switching period. In the case of negative edge modulation, this setting can cause the PWM outputs to be inverted; therefore, setting Register 0xFE50[0] = 1 programs the device to make the PWM outputs = 0 V in pulse skipping. For topologies such as the full-bridge phase shifted topology, where two PWM outputs are on without modulation for half the switching period, the setting in Register 0xFE50[4] allows the ADP1055 to disable such PWM outputs whether modulation is enabled or not.

SOFT STOP

The ADP1055 supports soft stop functionality. Soft stop can be enabled for normal shutdown of the power supply using the OPERATION and ON_OFF_CONFIG commands, as described in the Power-Up and Power-Down section. Soft stop can also be enabled during a fault triggered condition using Register 0xFE51[7:6]. The soft stop time is programmed using the TOFF_DELAY and TOFF_FALL commands (Register 0x64 and Register 0x65). During soft stop, various faults such as OTP, OVP, and GPIO faults can be masked using Register 0xFE47. To maintain a zero output voltage, the SR1 and SR2 PWM outputs can be programmed to stay on for an additional time (see the description of Register 0xFE50[7:6] in Table 193).

DUTY CYCLE DOUBLE UPDATE RATE

The ADP1055 senses the output voltage just before the beginning of the switching period and, depending on the error voltage, the next duty cycle command is initiated. Because a transient condition can occur at any time between switching periods, the one-cycle update of the duty cycle causes a phase loss that is equal to

$$\Phi = 360 \times (t_d \times f_C)$$

where:
t_d is the combined delay of the ADC sampling plus the loop calculations for the compensator plus any additional propagation delay.
f_C is the crossover frequency.

The minimum delay for the system is $D \times t_{SW}$ because it is only after $D \times t_{SW}$ that the effect of the duty cycle command takes place. Due to this phase loss (which increases as the crossover frequency approaches the switching frequency), the crossover frequency of the system cannot be widened with satisfactory phase margin. To reduce the phase loss, the ADP1055 uses a double update rate for the duty cycle, whereby the output voltage is sampled just before half the switching period and the new duty cycle command is issued. In this way, the phase loss from two subsequent duty cycle commands is halved to $D \times t_{SW}/2$.

Duty cycle double update rate is optional and is enabled by setting Register 0xFE57[0] = 1. When using the duty cycle double update rate, it is recommended that duty balance also be enabled (Register 0xFE57[7] = 1).

DUTY BALANCE, VOLT-SECOND BALANCE, AND FLUX BALANCING

For power topologies that use the first and third quadrant of the BH curve, it is recommended that duty balance be enabled when using double update rate. Due to the nature of double update rate, it is possible that the average magnetizing current (and therefore the flux density of the transformer core) is not zero, but is equal to some positive or negative dc level. To prevent flux walking and an imbalance in the transformer, a combination of the duty balance and volt-second balance features can be used. In interleaved topologies, the volt-second balance feature can also be used for current balancing to ensure that each interleaved phase contributes equal power.

For example, if a full bridge topology requires the diagonal edges of the H bridge to be equalized, the algorithm for duty balance averages the duty cycle over several switching cycles. Duty balance is a purely digital correction that is applied to the PWM edges based on past duty cycles and does not take into account any feedback from an ADC, as is the case for volt-second balance.

Duty balance is enabled by setting Register 0xFE57[7] = 1; the speed at which the duty cycle is balanced is controlled by setting Register 0xFE57[5:4]. Additionally, the extent to which duty cycle correction (maximum of ±160 ns for duty balance and volt-second balance each) can take place is specified using Register 0xFE57[2:1].

Volt-second balance uses a sample-and-hold circuit (patent pending) that samples the peak current during both halves of the switching period. This feature is configured using Register 0xFE56. The recommended settings for using the volt-second balance feature are as follows.

1. Use Register 0xFE56 to set the positive and negative edges. Bits[7:4] set the positive period of integration, and Bits[3:0] set the negative period of integration. The edges are logically AND'ed together.

   Typically, the diagonal edges of the H bridge are balanced. For example, in a full bridge topology, a setting of 10010110 for Register 0xFE56 causes the device to sample the peak current at the end of the logical AND of OUTA and OUTD (Peak 1) and the logical AND of OUTB and OUTC (Peak 2). If Peak 1 > Peak 2, the result is positive and the duty cycle of the selected edges is reduced. If Peak 2 > Peak 1, the result is negative and the duty cycle of the selected edges is increased.
2. Apply edge correction. Using the same example, negative edge correction is applied to OUTA and OUTD, whereas positive edge correction is applied to OUTB and OUTC. Appropriate edge correction is applied to the SR outputs as well.
3. Enable volt-second balance by setting Register 0xFE25[6] = 1. This setting is gated by a GO command (Register 0xFE00). Volt-second balance is automatically disabled when the voltage on the CS1 pin is below 25 mV.

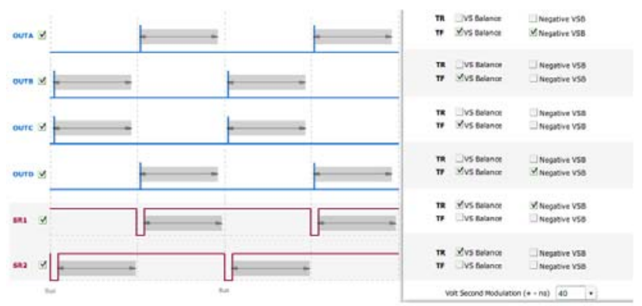


Figure 64. Volt-Second Balance with Register 0xFE56 = 0x96

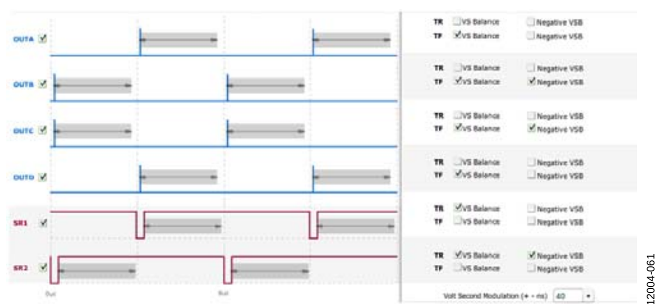


Figure 65. Volt-Second Balance with Register 0xFE56 = 0x69

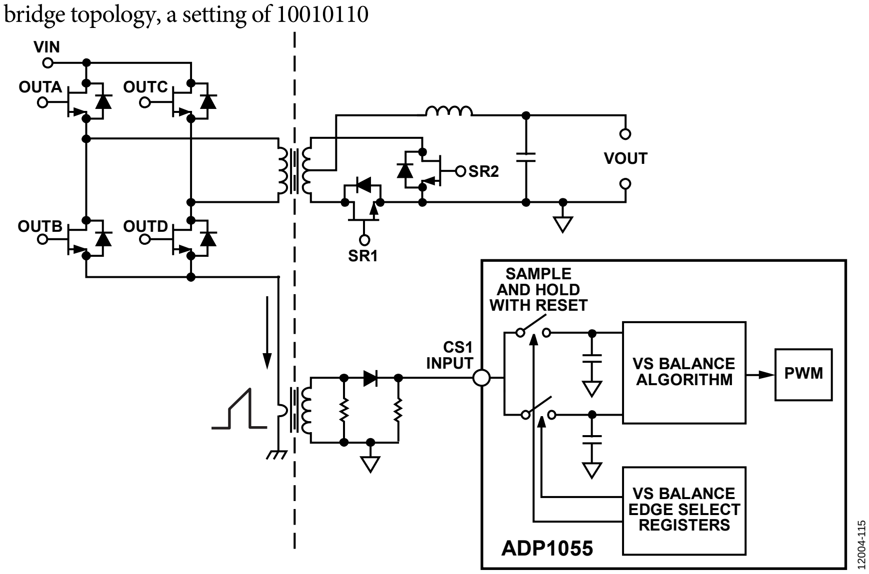


Figure 66. Simplified Internal Structure of the Volt-Second Balance Circuit

FAULT RESPONSES AND STATE MACHINE MECHANICS

When a potentially abnormal condition occurs in the power supply that is regulated by the ADP1055, a flag is asserted and the system waits for a programmed debounce time. If the flag is continuously asserted until the end of the debounce time, it is latched as a fault. The fault is then processed according to the programmed fault response setting. The fault is cleared only when the flag condition is removed. The debounce circuitry is reset when the flag condition is removed; until then the fault remains set.

PRIORITY OF FAULTS

The response to each fault is configurable and is based on a priority level (see Table 7). A higher number indicates a higher priority.

Table 7. Priority of Faults

Priority	Fault and Configured Fault Response
12 (highest)	Voltage fault: disable output
11	Voltage fault: shutdown with no retry
10	Current fault: shutdown with no retry
9	Voltage fault: shutdown with limited retry
8	Current fault: shutdown with limited retry
7	Voltage fault: shutdown with unlimited retry
6	Current fault: shutdown with unlimited retry
5	Voltage fault: wait delay and shutdown with limited or unlimited retry
4	Current fault: constant current with wait delay
3	Current fault: constant current without tripping VOUT_LV
2	Current fault: constant current mode
1 (lowest)	Voltage fault: ignore fault

FLAGS

The ADP1055 has an extensive set of flags that are set when certain limits, conditions, and thresholds are exceeded. The response to these flags is individually programmable. Flags can be ignored or used to trigger actions such as turning off certain PWM outputs or entering constant current mode. Flags can also be used to turn off the power supply. The ADP1055 can be programmed to respond when these flags are reset.

The ADP1055 also has a set of latched fault registers (Register 0xFE8C to Register 0xFE93). The latched fault registers have the same flags as the PMBus STATUS_x commands (Register 0x7A to Register 0x80), but the flags in the latched registers remain set so that intermittent faults can be detected. The CLEAR_FAULTS command (Register 0x03) clears the latched fault registers and resets all the flags.

FIRST FAULT ID (FFID)

The first fault ID (FFID) information is used to capture the first fault that caused the system to shut down. Register 0xFE95 contains the ID of the first fault that caused the system to shut down. Faults captured in the first fault ID register have configured actions of shutdown immediate, shutdown with retries, and disable PWM outputs with watchdog timeout. The contents of Register 0xFE95 cannot be overwritten unless the information is first cleared.

The FFID can be cleared by the CLEAR_FAULTS command (Register 0x03), by a power cycle of the device, or by a PSON signal using Register 0x01, Register 0x02, or both. If the black box feature is enabled, the FFID can also be cleared when the information is saved into the black box.

Table 8. Example First Fault ID Scenarios

Test Setup	Condition	Result
OCP has retry/delay of 100 ms with Priority 10, debounce = 0. OVP has retry/delay of 200 ms with Priority 9, debounce = 0.	OCP occurs at t = 0. OVP occurs at t = 10 ms.	OCP fault is processed due to smaller debounce time (no retry time), as well as higher priority.
OCP has retry/delay of 100 ms with Priority 10, debounce = 0. OVP has retry/delay of 0 ms with Priority 11, debounce = 0.	OCP occurs at t = 0. OVP occurs at t = 10 ms.	OCP fault is processed at t = 0; device waits 100 ms before action is taken. OCP fault is replaced by OVP, and then OVP fault is processed at t = 10 ms due to higher priority even though retry delay is larger.
OCP has retry/delay of 100 ms with Priority 8, debounce = 5 ms. OVP has retry/delay of 200 ms with Priority 9, debounce = 100 ms.	OCP occurs at t = 50 ms. OVP occurs at t = 0.	OVP is registered as a fault at t = 100 ms. OCP is registered as a fault at t = 55 ms. However, at t = 100 ms, OCP loses priority and OVP is processed due to higher priority. Exception: If delay of OCP was smaller (for example, 5 ms), then OCP action is processed.
OCP has retry/delay of 100 ms with Priority 8, debounce = 0. OVP has retry/delay of 200 ms with Priority 7, debounce = 0.	OCP occurs at t = 0. OVP occurs at t = 0.	OCP fault is processed due to higher priority.

Using the priority of faults (see the Priority of Faults section), the fault that causes the ADP1055 to shut down is the one stored in the FFID. For example, a configuration includes these faults:

- OVP fault with a delay of 100 ms and five retry times
- OCP fault with an action to shut down immediately with a 0 ms delay

If the OVP fault occurs and after the third retry attempt, the OCP fault occurs, the OCP fault is stored in the FFID register. On the other hand, if all five OVP retries occur before the OCP fault occurs, the OVP fault is stored in the FFID. This statement is true only if Register 0xFE_48[1:0] is set to 01. If it is set to 10, the FFID is set to OVP on the first retry time.

Note that warning flags such as IOUT_OC_WARN and VOUT_OV_WARN do not have debounce times.

The ADP1055 has a fault handler that can detect and track faults and, in the case where a fault is programmed to shut down and retry (restart) the system, the fault handler cycles the ADP1055 through a shutdown and soft start procedure. Throughout the soft start ramp, the fault handler continues to monitor the device for any faults that can trigger a fault response. Soft start blanking can be configured to ignore faults during the soft start ramp.

If a fault condition triggers a shutdown-retry cycle, the fault handler tracks the number of retry attempts of the programmed fault response and permanently shuts down the device when the configured number of retry times is reached. A shutdown-retry cycle is considered successful if the triggering fault is cleared at the end of the soft start ramp, at which point voltage regulation is achieved. Following a successful retry attempt, the fault handler removes the fault from its queue, clears all retry attempt counters, and monitors the device for the next highest priority fault.

Debounce times can be added to a flag condition to effectively delay the fault condition beyond the end of the soft start ramp. Note that the fault handler considers this a successful retry attempt (because no fault is seen when transitioning from soft start to normal operation). The fault handler clears the fault and resets the retry counters. For example, consider a TON_RISE time of 10 ms, with a fault response set to shut down and retry three times, and a flag condition that occurs during the soft start ramp (t_1 < 10 ms). If the debounce time (t_d) is small enough such that $t_1 + t_d$ < TON_RISE, the fault condition is latched before the end of the soft start ramp, and the ADP1055 shuts down and retries accordingly, while incrementing the retry counter.

After three retries, the ADP1055 shuts down, requiring a power-up to start again. However, if the debounce time (t_d) is large enough such that $t_1 + t_d$ > TON_RISE, the fault condition is latched after the ADP1055 transitions from soft start to normal operation. In this scenario, the fault condition is cleared and the retry counter is reset at the end of the soft start ramp.

The delayed fault initiates another set of three shutdown-retry cycles. This behavior effectively causes the system to retry indefinitely, even though the fault response is programmed to retry only three times.

A notable exception is TON_MAX_FAULT when overshoot protection is enabled. If the ADP1055 detects an out-of-regulation condition for x consecutive switching cycles during the soft start ramp (that is, the output voltage does not track the desired ramp-up voltage), the ADP1055 tries to remedy the situation by exiting soft start and retrying. As a result, the soft start ramp ends prematurely, which has the effect of resetting the retry counter.

Table 9 provides a summary of faults and respective debounce times.

FAULT CONDITION DURING SOFT START AND SOFT STOP

If a fault condition occurs during soft start, the controller responds as programmed unless the flag is blanked. Flag blanking during soft start and soft stop is programmed in Register 0xFE46 and Register 0xF47, respectively.

If a fault (for example, TON_MAX or IIN_OC) occurs at any time during the soft start process with an action set to a value other than shutdown, the remainder of the soft start ramp continues at the transition rate specified by the PMBus command VOUT_TRANSITION_RATE (Register 0x27).

During soft start, the TON_MAX fault is valid; after output regulation is reached, the UVP fault is valid. This means that the system does not start monitoring for UVP fault until after the soft-start ramp-up.

WATCHDOG TIMER

In the case where the voltage fault response is set to disable the outputs and wait for the faults to clear (Bits[7:6] = 11), the ADP1055 disables the PWM outputs but does not immediately shut down and restart through a soft start cycle. The ADP1055 keeps the PWM outputs disabled until the fault is cleared, after which the PWM outputs are reenabled.

If the fault is not cleared, the system can potentially remain in a dormant condition for an infinitely long time. To prevent this condition, a watchdog timer can be set to time out the fault condition. The WDT_SETTING command (Register 0xFE3F) is used to set a timeout of 0 sec, 1 sec, 5 sec, or 10 sec, after which the system shuts down, captures the FFID, and requires a power-up (CTRL pin or OPERATION command) to restart.

Table 9. Summary of Faults with Debounce Times

Function/PMBus Command	Pin	Comments	Debounce	LSB	Fault response Command
VOUT_OV_FAST	OVP	An analog comparator on this pin provides this protection.	0xFE2F[1:0]		VOUT_OV_FAST_ RESPONSE
VOUT_OV	VS±	The ADC on this pin is averaged every 82 µs with 7-bit accuracy for this fault. This information is compared with the VOUT_OV_FAULT_LIMIT to set the flag.	0xFE30[3:0]	$1.6/2^7$	VOUT_OV_FAULT_ RESPONSE
VOUT_OV_WARN	VS±	Same as VOUT_OV.	N/A	$1.6/2^7$	N/A
VOUT_UV_WARN	VS±	Same as VOUT_UV.	N/A	$1.6/2^9$	N/A
VOUT_UV	VS±	The ADC on this pin is averaged every 328 µs with 9-bit accuracy for this fault. This information is compared with the VOUT_UV_FAULT_LIMIT to set the flag.	0xFE30[10:8]	$1.6/2^9$	VOUT_UV_FAULT_R ESPONSE
IOUT_OC	CS2±	The ADC on this pin is averaged every 2.6 ms with 12-bit accuracy for this fault. This information is compared with the IOUT_OC_FAULT_LIMIT to set the flag.	0xFE31[3:0]	IOUT_OC: CS2_Range/2^{12}	IOUT_OC_ FAULT_RESPONSE
		The ADC on this pin is averaged every 328 µs with 9-bit accuracy for CC mode. This information is compared with the IOUT_OC_FAULT_LIMIT ± the threshold set in Register 0xFE5D[2:0] to enter CC mode. For turbo mode, the averaging is every 41 µs with an equivalent 6-bit resolution.		CC mode: CS2_Range/2^9 CC turbo mode: CS2_Range/2^6	
IOUT_OC_LV	CS2±	The ADC on this pin is averaged every 10.5 ms with 12-bit accuracy for this fault. This information is compared with the IOUT_OC_LV_FAULT_LIMIT to set the flag.	0xFE30[15:14]	CS2_Range/2^{12}	
IOUT_OC_FAST	CS2±	An analog comparator on this pin provides this protection.	0xFE2D[1:0]		IOUT_OC_FAST_ FAULT_RESPONSE
IOUT_UC	CS2±	The ADC on this pin is averaged every 10.5 ms with 12-bit accuracy for this fault. This information is compared with IOUT_UC_FAULT_LIMIT to set the flag.	0xFE31[7:4]	IOUT_UC: CS2_Range/2^{12}	IOUT_UC_FAULT_ RESPONSE
		The ADC on this pin is averaged every 328 µs with 9-bit accuracy for constant current mode. This information is compared with the IOUT_UC_FAULT_LIMIT ± the threshold set in Register 0xFE5D[2:0] to enter CC mode. For turbo mode, the averaging is every 41 µs with an equivalent 6-bit resolution.		CC mode: CS2_Range/2^9 CC turbo mode: CS2_Range/2^6	
IOUT_UC_FAST	CS2±	An analog comparator on this pin provides this protection.	0xFE2E[0]		IOUT_UC_FAST_ FAULT_RESPONSE
IIN_OC	CS1	The ADC on this pin is averaged every 10.5 ms with 12-bit accuracy for this fault. This information is compared with the IOUT_OC_FAULT_LIMIT to set the flag.	0xFE31[11:8]	$1.6/2^{12}$	IIN_OC_FAULT_ RESPONSE
IIN_OC_FAST	CS1	An analog comparator on this pin provides this protection.	0xFE2C[1:0]		IIN_OC_FAST_ FAULT_RESPONSE
ISHARE	CS2±	When maximum limit to change output voltage is reached.	0xFE31[15:12]		ISHARE_FAULT_ RESPONSE
IOUT_OC_WARN	CS2±	Same as IOUT_OC.	N/A	CS2_Range/2^{12}	
VIN_LOW	VFF	The ADC on this pin is averaged every 328 µs with 9-bit accuracy for this fault. This information is compared with the VIN_LOW to set the flag.		$1.6/2^9$	
VIN_UV	VFF	The ADC on this pin is averaged every 328 µs with 9-bit accuracy for this fault. This information is compared with the VIN_UV_FAULT_LIMIT to set the flag.	0xFE30[13:11]	$1.6/2^9$	VIN_UV_FAULT_ RESPONSE
VIN_UV_WARN	VFF	Same as VIN_UV.	N/A		N/A
VIN_OV	VFF	The ADC on this pin is averaged every 328 µs with 9-bit accuracy for this fault. This information is compared with the VIN_OV_FAULT_LIMIT to set the flag.	0xFE30[7:4]	$1.6/2^9$	VIN_OV_FAULT_ RESPONSE
VIN_OV_WARN	VFF	Same as VIN_OV.	N/A		
POUT_OP	N/A	The multiplication of VS and CS2 ADCs averaged every 2.6 ms with 11-bit accuracy for this fault. This information is compared with the POUT_OP_FAULT_LIMIT to set the flag.	0xFE32[11:8]		POUT_OP_FAULT_ RESPONSE

Function/PMBus Command	Pin	Comments	Debounce	LSB	Fault response Command
OT	N/A	The ADC on this pin is averaged every 200 ms with 14-bit accuracy for this fault to provide two consecutive readings (external forward and external reverse temperature sensors). This information is compared with the OT_FAULT_LIMIT to set the flag. If external reverse is disabled, the averaging is performed every 130 ms.	0xFE32[3:0]		OT_FAULT_ RESPONSE
OT_WARN	N/A	Same as OT.	N/A		
GPIOx_FAULT	GPIOx	Immediate.	0xFE32[15:0]		GPIOx_FAULT_ RESPONSE
TON_MAX	N/A	Immediate.	0xFE32[7:4]	$1.6/2^9$ for VS	TON_MAX_FAULT_ RESPONSE
TON_MAX_WARN	N/A		N/A	$1.6/2^9$ for VS	
VDD/VCORE_OV	VDD VCORE	Immediate.	0xFE4D[5]		0xFE4D[6]
VDD UV	VDD	Immediate.	0xFE4D[4]		Shutdown

STANDARD PMBUS FLAGS

Figure 67 shows the standard PMBus flags supported by the ADP1055.

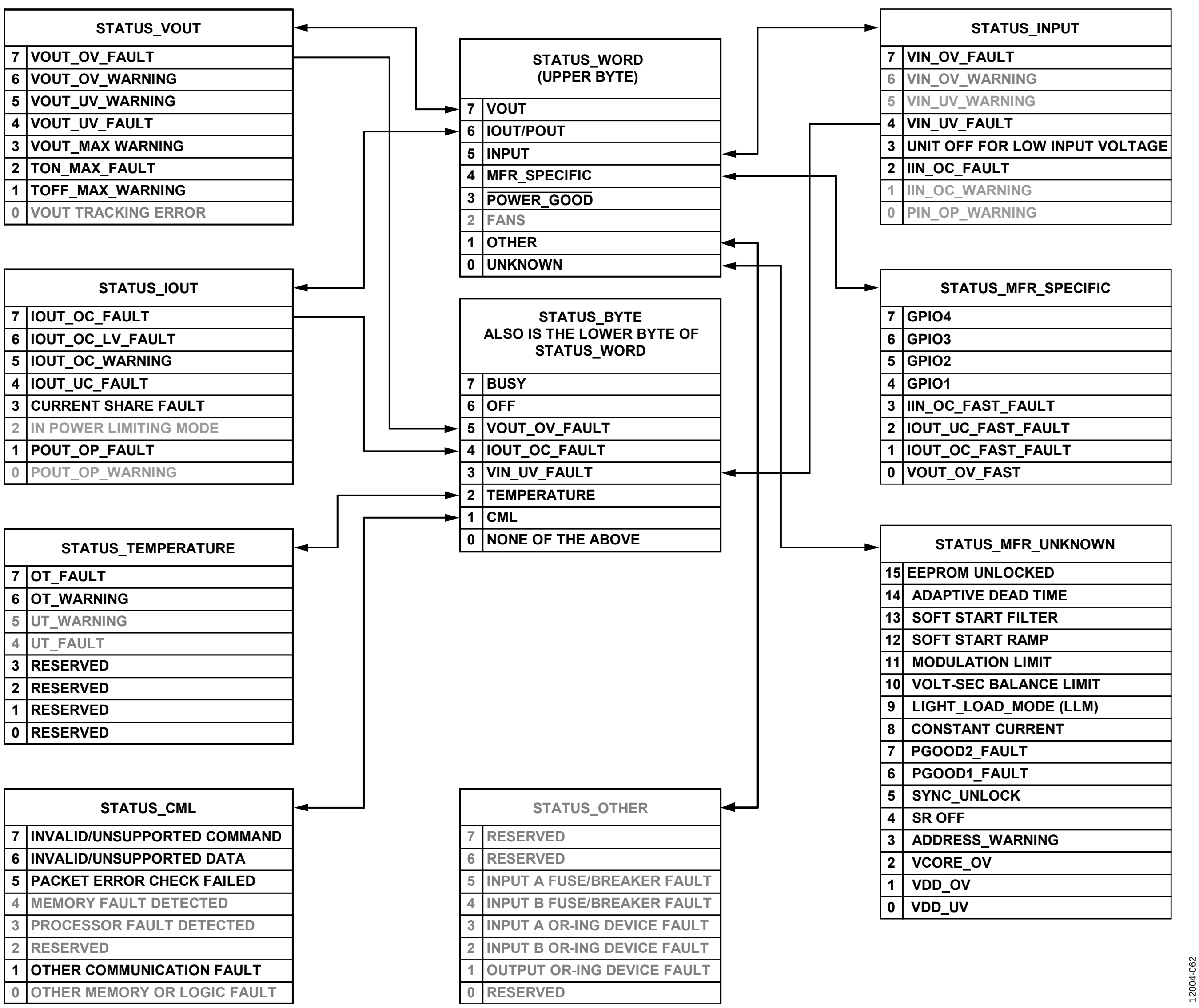


Figure 67. Standard PMBus Flags Supported by the ADP1055

BLACK BOX FEATURE

BLACK BOX OPERATION

The ADP1055 supports a configurable black box feature. Using this feature, the device records to the EEPROM vital data about the faults that cause the system to shut down. Two dedicated EEPROM pages are used for this purpose: Page 2 and Page 3.

When the ADP1055 encounters a fault with the action to shut down the device, a snapshot of the current telemetry is taken, as well as the first fault that caused the shutdown (see Figure 68). If the black box feature is enabled, this information is saved to the EEPROM before the device shuts down.

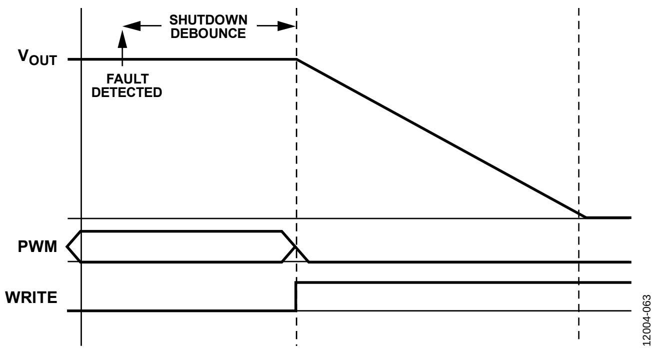


Figure 68. Black Box Write Operation

This black box feature is extremely helpful in troubleshooting a failed system during testing and evaluation. If a system is recalled for failure analysis, it is possible to read this information from the EEPROM to help investigate the root cause of the failure.

Only a limited number of writes to the EEPROM are allowed. Using Register 0xFE48[1:0], the user can set the level of information that is logged in the black box, as follows:

- No recording.
- Only record telemetry just before the final shutdown.
- Record telemetry of final shutdown and all intermittent retry attempts (if device is set to shut down and retry).
- Record telemetry of final shutdown, all retry attempts, and normal power-down operations using the CTRL pin or the OPERATION command.

Using Register 0xFE48[2], the user can program the maximum number of records to 158,000 (recommended when the ambient temperature of the ADP1055 is less than 85°C) or to 16,000 (when the ambient temperature of the ADP1055 is less than 125°C). If the number of records exceeds the programmed value, the recording of data to the EEPROM is halted and the STATUS_CML bit (Register 0x7E[0]) is set and remains set. Data accumulated after the limit is reached is not reliable and should be ignored.

If a device experiences multiple concurrent faults, the ID of the first fault that triggers the system to shut down is captured in the FIRST_FAULT_ID register (Register 0xFE95). The FFID and all flag status and telemetry data are captured in the black box at every write to the black box (see the Black Box Contents section for a list of the data saved). The last valid byte of each record is a PEC byte, which is used to calculate the validity of each record stored in the EEPROM.

Following each recording, the record number (Rec_No) is incremented, and this number is compared to the maximum allowed number of records. If Rec_No equals the maximum record number (158,000 or 16,000), no additional black box recording is allowed because the EEPROM has reached its maximum allowed erase program cycles and any additional recording is unreliable.

BLACK BOX CONTENTS

Page 2 and Page 3 of the EEPROM are reserved for black box operation. The size of each EEPROM page is 512 bytes; each page is composed of eight records with 64 bytes each. Page 2 and Page 3 combined give a total of 16 records, which function as a circular buffer for recording black box information.

The EEPROM is a page erase memory, and an entire page must be erased before the page can be written to. Due to the page erase requirement of the EEPROM, after writing the eighth record of any page, the next page is automatically erased to allow for continuous black box recording.

Each time a record is written in the black box, the device increments the record number. Each EEPROM write records the registers listed in Table 10.

PEC Byte

The packet error checking (PEC) byte at the end of each black box record is specific to each record and is calculated using a CRC-8 polynomial: $C(x) = x^8 + x^2 + x^1 + 1$. The PEC byte is calculated on the first four bytes of each record (called the header block), one byte at a time. In a write to EEPROM, the PEC byte is appended to the data and is the last valid byte of that record. In a read from EEPROM, the header block of each record is used to calculate an expected PEC code, and this internally calculated PEC code is compared to the received PEC byte. If the comparison fails, the PEC_ERR bit (STATUS_CML[5]) is set, and that record is discarded because the validity of the data has been compromised.

Table 10. Contents of Black Box Records

Byte	Register Address	Register Name
Header Block		
1	Rec_No[7:0]	
2	Rec_No[15:8]	
3	Rec_No[23:16]	
4	0xFE95	FIRST_FAULT_ID[7:0]
Data Block		
5	0x78	STATUS_WORD[7:0] (same as STATUS_BYTE[7:0])
6	0x79	STATUS_WORD[15:8]
7	0x7A	STATUS_VOUT
8	0x7B	STATUS_IOUT
9	0x7C	STATUS_INPUT
10	0x7D	STATUS_TEMPERATURE
11	0x7E	STATUS_CML
12	0x7F	STATUS_OTHER
13	0x80	STATUS_MFR_SPECIFIC
14	0xFE94	STATUS_UNKNOWN[7:0]
15	0xFE94	STATUS_UNKNOWN[15:8]
16	0x88	READ_VIN[7:0]
17	0x88	READ_VIN[15:8]
18	0x89	READ_IIN[7:0]
19	0x89	READ_IIN[15:8]
20	0x8B	READ_VOUT[7:0]
21	0x8B	READ_VOUT[15:8]
22	0x8C	READ_IOUT[7:0]
23	0x8C	READ_IOUT[15:8]
24	0x8D	Reserved[7:0]
25	0x8D	Reserved[15:8]
26	0x8E	READ_TEMPERATURE_2[7:0]
27	0x8E	READ_TEMPERATURE_2[15:8]
28	0x8F	READ_TEMPERATURE_3[7:0]
29	0x8F	READ_TEMPERATURE_3[15:8]
30	0x94	READ_DUTY_CYCLE[7:0]
31	0x94	READ_DUTY_CYCLE[15:8]
32	0x95	READ_FREQUENCY[7:0]
33	0x95	READ_FREQUENCY[15:8]
34	0x96	READ_POUT[7:0]
35	0x96	READ_POUT[15:8]
PEC Block		
36	PEC[7:0]	
Undefined Block		
37 … 64		

BLACK BOX TIMING

Two EEPROM pages (Page 2 and Page 3) are used to store the black box data; each page contains eight records. Due to the page erase requirement of the EEPROM, when the black box has completed writing the last record to either page (Rec_No = 8n − 1; n > 0, that is, 7, 15, 23, 31, and so on), a page erase operation is automatically initiated on the other page. The erase operation takes an additional 32 ms to complete.

During the erase operation, any PMBus transaction to the device receives a no acknowledge (NACK), and the busy bit (Bit 7) of STATUS_BYTE is set accordingly. At the end of the erase operation, the device resumes normal operation. The minimum time required to program a complete black box record is calculated as follows:

$$T_{PROG\_BBOX\ (MIN)} = (num\_of\_bytes + 1) \times T_{PROG}$$

where:
T_{PROG} = 30.72 µs.
num_of_bytes = 36 (36 bytes in each black box record).

If the erase operation is part of the sequence of saving data to the black box, the additional erase time is added to $T_{PROG\_BBOX\ (MIN)}$, as follows:

$$T_{PROG\_BBOX\ (MIN)} = \sim 1.2\ ms$$
$$T_{ERASE} = \sim 32\ ms$$
$$T_{PROG\_BBOX\ (MAX)} = \sim 33.2\ ms$$

When black box writing is enabled with the option to record retry attempts (Register 0xFE48[1:0] = 10 or 11), data can be saved between every unsuccessful attempt to restart the device. It is recommended that the minimum retry time be set to a value greater than 1.2 ms. If the retry time is insufficient for black box recording, the device prolongs the retry time so that the recording can finish before attempting to restart the power supply. This delay may result in inconsistent retry times between successive restart attempts. The retry time is programmed using the PMBus commands xxx_FAULT_RESPONSE, where xxx refers to the various configurable faults for that device.

At every eighth recording, the T_{ERASE} time is added to the $T_{PROG\_BBOX\ (MIN)}$ time, resulting in the $T_{PROG\_BBOX\ (MAX)}$ time. If the retry time is less than the maximum time, the device again delays the restart attempt to wait for the completion of the black box recording and the successive page erase.

Black box operation is a direct result of a fault condition that triggers a power supply shutdown. To ensure that the black box is written to in the event of a brownout condition, a holdup capacitor on the VDD pin is recommended to ensure that all the information is written to the black box before the ADP1055 reaches the UVLO threshold. (Instead of a holdup capacitor, an equivalent capacitor from the rail where 3.3 V is derived can be used to maintain the VDD voltage above UVLO.) The capacitor must be large enough to maintain power to the system over a time that exceeds $T_{PROG\_BBOX\ (MIN)}$ which is approximately 10 µF on a 10 V rail until VDD falls below UVLO.

BLACK BOX READBACK

Two dedicated commands can be used to read back the contents of the black box data stored in the EEPROM. The READ_BLACKBOX_CURR command (Register 0xF2) is a block read command that returns the current record N (last record saved) with all related data, as defined in the Black Box Contents section. The READ_BLACKBOX_PREV command (Register 0xF3) is a block read command that returns the data for the previous record N − 1 (next-to-last record saved). Because these commands are block read commands, the first byte received is called the BYTE_COUNT and indicates to the PMBus master how many more bytes to read. In the ADP1055, BYTE_COUNT = 36.

For information about how to read from the EEPROM directly using these commands, see the Read Operation (Byte Read and Block Read) section. It is recommended that the GUI be used to read back the contents of the black box; the black box data is readily available in the GUI, which displays the data in a graphical format.

BLACK BOX POWER SEQUENCING

When the ADP1055 is powered up, the contents of the user settings in the EEPROM are downloaded into the internal registers. Immediately after this, the contents of the black box data (that is, Page 2 and Page 3) are read from the EEPROM by the device to determine the last valid Rec_No saved and to determine whether a page erase operation is required before starting up the device in normal mode.

If the highest Rec_No is located on the last record of either page (that is, the next record to store data is at the start of the other page) and the other page has not been erased, the ADP1055 automatically initiates a page erase to the other page to prepare it for further black box recording. The ADP1055 performs a soft start sequence only after the page erase is completed.

POWER SUPPLY CALIBRATION AND TRIM

The ADP1055 allows the entire power supply to be calibrated and trimmed digitally in the production environment. The device can calibrate items including the output voltage, input voltage, input current, and input power, and it can trim for tolerance errors introduced by sense resistors, current transformers, and resistor dividers, as well as for its own internal circuitry.

The ADP1055 is factory trimmed, but it can be retrimmed by the user to compensate for the errors introduced by external components. The ADP1055 GUI allows the user to revert the trim settings to their factory default values using the RESTORE_ DEFAULT_ALL command (Register 0x12). To unlock the trim registers for write access, perform consecutive writes to TRIM_ PASSWORD (Register 0xD6) using the correct password. This password is the same one used to unlock the EEPROM using EEPROM_PASSWORD (Register 0xD5). The factory default password is 0xFF.

The ADP1055 allows the user enough trim capability to trim for external components with a tolerance of 0.5% or better. If the ADP1055 is not trimmed in the production environment, it is recommended that components with a tolerance of 0.1% or better be used for the inputs to CS1, VFF, and VS± to meet the data sheet specifications.

VOLTAGE CALIBRATION AND TRIM

The voltage sense point can be calibrated digitally to minimize errors due to external components using the VOUT_TRIM command (Register 0x22). This calibration can be performed in the production environment, and the settings can be stored in the EEPROM of the ADP1055.

The voltage sense inputs are optimized for sensing signals at 1 V. In a 12 V system, a 12:1 resistor divider is required to reduce the 12 V signal down to 1 V. It is recommended that the output voltage of the power supply be reduced to 1 V at this pin for best performance. The tolerance of the resistor divider introduces errors that must be trimmed. The ADP1055 has enough trim range to trim out errors introduced by resistors with a tolerance of 0.5% or better.

The VS ADC produces a digital code equal to VS±/1.6 × 4096.

The VS± inputs require a gain trim. The following steps should be performed before any other trim routine.

1. Set the output regulation point to 100% of the nominal value.
2. Enable the power supply with no load current. The power supply output voltage is divided down by the resistor divider to give 1 V across the VS+ and VS− differential input pins.
3. Adjust the VS trim register (Register 0xFE80) until the VS± voltage value in Register 0xFE97[13:2] reads 1010 0000 0000 when there is 1.0 V on the pins.

CS1 TRIM

The current sense can be calibrated using a dc or ac signal to minimize errors due to external components.

Using a DC Signal

A known voltage (Vx) is applied at the CS1 pin. The CS1 ADC should output a digital code equal to Vx/1.6 × 4096. Adjust the CS1 gain trim register (Register 0xFE82) until the CS1 ADC value in Register 0xFE98 reads the correct digital code. For example, Register 0xFE98[13:2] reads a value of 1010 0000 0000 when there is 1.0 V on the CS1 pin.

Using an AC Signal

A known current (Ix) is applied to the CS1 pin. This current passes through a current transformer, a diode rectifier, and an external resistor (R_{CS1}) to convert the current information to a voltage (Vx). This voltage is fed into the CS1 pin. The voltage (Vx) is calculated as follows:

$$Vx = Ix \times (N1/N2) \times R_{CS1}$$

where *N1*/*N2* is the turns ratio of the current transformer.

The CS1 ADC outputs a digital code equal to Vx/1.6 × 4096. Adjust the CS1 gain trim register (Register 0xFE82) until the CS1 ADC value in Register 0xFE98 reads the correct digital code.

VFF CALIBRATION AND TRIM

The VFF feedforward ADC (see Figure 32) is used for voltage line feedforward and is factory trimmed. This ADC cannot be trimmed by the user.

The VFF slow ADC requires a gain trim.

1. Enable the power supply with full load current at the nominal input voltage. The secondary peak reverse voltage on the output rectifiers is filtered by an external RCD circuit (see Figure 32).
2. To trim the VFF ADC, reverse-calculate the primary voltage as follows:

   $$V_{PRIMARY} = Vx \times (R1 + R2)/R2 \times (N1/N2)$$

   where:
   Vx is the voltage at the VFF pin.
   N1/*N2* is the turns ratio. }
3. Adjust the VFF gain trim register (Register 0xFE81) until this calculated voltage is equal to the desired primary input voltage. For example, Register 0xFE96[13:2] reads a value of 1010 0000 0000 when there is 1.0 V on the VFF pin.

The resistors in Figure 32 are sized such that the first time constant, RC, is long enough to prevent overcharging of the capacitor (roughly 200 ns in a typical application), whereas the second time constant, (R1 + R2) × C, is long enough to keep the average voltage constant during the rectifier off time.

PMBUS DIGITAL COMMUNICATION

The PMBus slave with PEC allows a device to interface to a PMBus compliant master device, as specified by the *PMBus Power System Management Protocol Specification* (Revision 1.2, September 6, 2010). The PMBus slave is a 2-wire interface that can be used to communicate with other PMBus compliant devices and is compatible in a multimaster, multislave bus configuration. The PMBus slave can communicate with master PMBus devices that support packet error checking (PEC), as well as with master devices that do not support PEC.

FEATURES

The function of the PMBus slave is to decode the command sent from the master device and respond as requested. Communication is established using an I^2C-like 2-wire interface with a clock line (SCL) and data line (SDA). The PMBus slave is designed to externally move chunks of 8-bit data (bytes) while maintaining compliance with the PMBus protocol. The PMBus protocol is based on the *SMBus Specification* (Version 2.0, August 2000). The SMBus specification is, in turn, based on the Philips *I^2C Bus Specification* (Version 2.1, January 2000). The PMBus incorporates the following features:

- Slave operation on multiple device systems
- 7-bit addressing
- 100 kbits/sec and 400 kbits/sec data rates
- Packet error checking
- Support for the Group Command Protocol
- Support for the Alert Response Address Protocol with arbitration
- General call address support
- Support for clock low extension (clock stretching)
- Separate multiple byte receive and transmit FIFO
- Extensive fault monitoring

OVERVIEW

The PMBus slave module is a 2-wire interface that can be used to communicate with other PMBus compliant devices. Its transfer protocol is based on the Philips I^2C transfer mechanism. The ADP1055 is always configured as a slave device in the overall system. The ADP1055 communicates with the master device using one data pin (SDA) and one clock pin (SCL). Because the ADP1055 is a slave device, it cannot generate the clock signal. However, it is capable of clock-stretching the SCL line to put the master device in a wait state when it is not ready to respond to the master's request.

Communication is initiated when the master device sends a command to the PMBus slave device. Commands can be read or write commands, in which case data is transferred between the devices in a byte wide format. Commands can also be send commands, in which case the command is executed by the slave device upon receiving the stop bit. The stop bit is the last bit in a complete data transfer, as defined in the PMBus/SMBus/I^2C communication protocol. During communication, the master and slave devices send acknowledge or no acknowledge bits as a method of handshaking between devices.

In addition, the PMBus slave on the ADP1055 supports packet error checking (PEC) to improve reliability and communication robustness. The ADP1055 can communicate with master PMBus devices that support PEC, as well as with master devices that do not support PEC. See the SMBus specification for a more detailed description of the communication protocol.

When communicating with the master device, it is possible for illegal or corrupted data to be received by the PMBus slave device. In this case, the PMBus slave device should respond to the invalid command or data, as defined by the PMBus specification, and indicate to the master device that an error or fault condition has occurred. This method of handshaking can be used as a first level of defense against inadvertent programming of the slave device that can potentially damage the chip or system.

The PMBus specification defines a set of generic PMBus commands that is recommended for a power management system. However, each PMBus device manufacturer can choose to implement and support certain commands as it deems fit for its system. In addition, the PMBus device manufacturer can choose to implement manufacturer-specific commands whose functions are not included in the generic PMBus command set. The list of standard PMBus and manufacturer-specific commands can be found in the Standard PMBus Commands Supported by the ADP1055 section and Manufacturer Specific Commands section.

TRANSFER PROTOCOL

The PMBus slave follows the transfer protocol of the *SMBus Specification* (Version 2.0), which is based on the fundamental transfer protocol format of the Philips *I^2C Bus Specification* (Version 2.1). Data transfers are byte wide, lower byte first. Each byte is transmitted serially, most significant bit (MSB) first. Figure 69 shows a basic transfer.

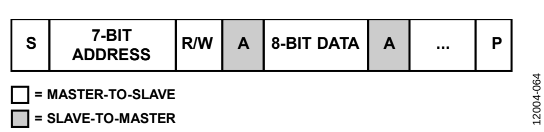


Figure 69. Basic Data Transfer

For an in-depth discussion of the transfer protocols, see the SMBus and I^2C specifications.

DATA TRANSFER COMMANDS

Data transfer using the PMBus slave is established using PMBus commands. The PMBus specification requires that all PMBus commands start with a slave address with the R/$\overline{W}$ bit cleared (set to 0), followed by the command code. (The only exception is $\overline{SMBALRT}$ Alert Response Address Protocol.)

All PMBus commands supported by the ADP1055 device follow one of the protocol types shown in Figure 70 to Figure 77. (For PMBus master devices that do not support PEC, the PEC byte is removed.) Figure 70 to Figure 77 use the following abbreviations:

- S = start condition
- P = stop condition
- Sr = repeated start condition
- W = write bit (0)
- R = read bit (1)
- A = acknowledge bit (0)
- NA = no acknowledge bit (1)

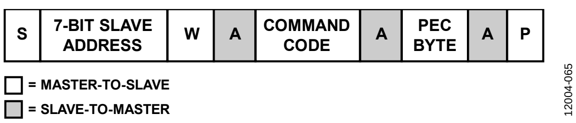


Figure 70. Send Protocol with PEC

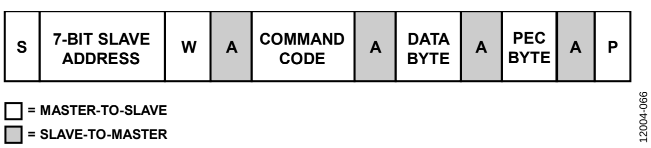


Figure 71. Write Byte Protocol with PEC

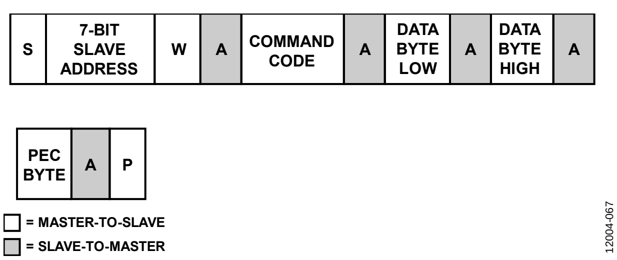


Figure 72. Write Word Protocol with PEC

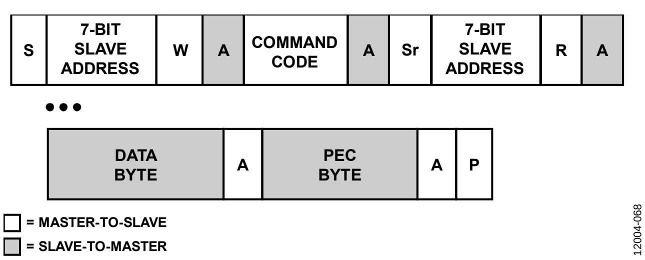


Figure 73. Read Byte Protocol with PEC

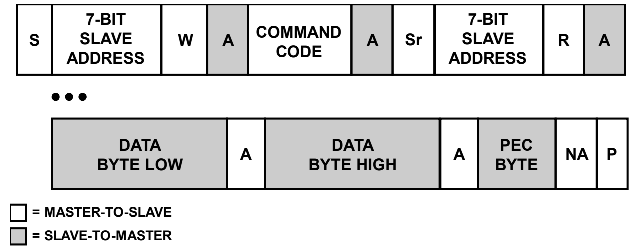


Figure 74. Read Word Protocol with PEC

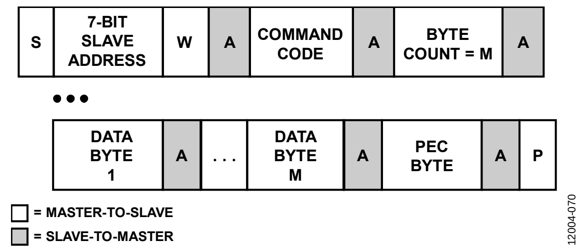


Figure 75. Block Write Protocol with PEC

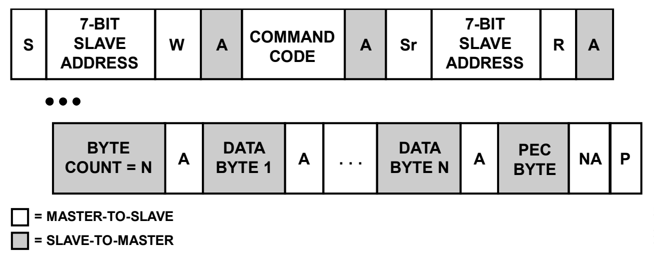


Figure 76. Block Read Protocol with PEC

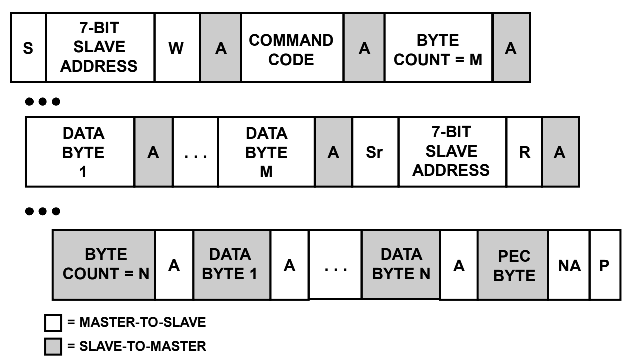


Figure 77. Block Write and Block Read Protocol with PEC

The PMBus slave module of the ADP1055 also supports manufacturer-specific extended commands. These commands follow the same protocol as the standard PMBus commands. However, the command code consists of two bytes:

- Command code extension: 0xFE
- Extended command code: 0x00 to 0xFF

Using the manufacturer-specific extended commands, the PMBus device manufacturer can add an additional 256 manufacturer-specific commands to its PMBus command set.

GROUP COMMAND PROTOCOL

In addition to the communication protocols described in the Data Transfer Commands section, the PMBus slave supports a special group command in which commands are sent to multiple slaves in a single serial transmission. The commands to each slave can be different from one another, with each set of {slave-address, command} separated by a repeated start (Sr) bit (see Figure 78). At the end of a transmission to all slaves, a single stop (P) bit is sent to initiate concurrent execution of the received commands by all slaves.

Note that the PEC byte transmitted to each slave is calculated using only its slave address, command code, and data bytes.

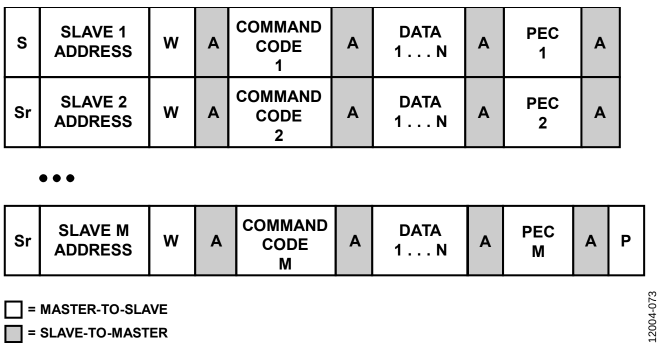


Figure 78. Group Command Protocol with PEC

CLOCK GENERATION AND STRETCHING

The ADP1055 is always a PMBus slave device in the overall system; therefore, the device never needs to generate the clock, which is done by the master device in the system. However, the PMBus slave device is capable of clock stretching to put the master in a wait state. By stretching the SCL signal during the low period, the slave device communicates to the master device that it is not ready and that the master device must wait.

Conditions where the PMBus slave device stretches the SCL line low include the following:

- Master device is transmitting at a higher baud rate than the slave device.
- Receive FIFO buffer of the slave device is full and must be read before continuing to prevent a data overflow condition.
- Slave device is not ready to send data that the master has requested.

Note that the slave device can stretch the SCL line only during the low period. Also, whereas the I^{2}C specification allows indefinite stretching of the SCL line, the PMBus specification limits the maximum time that the SCL line can be stretched, or held low, to 25 ms, after which the ADP1055 must release the communication lines and reset its state machine.

START AND STOP CONDITIONS

Start and stop conditions involve serial data transitions while the serial clock is at a logic high level. The PMBus slave device monitors the SDA and SCL lines to detect the start and stop conditions and transition its internal state machine accordingly. Figure 79 shows typical start and stop conditions.

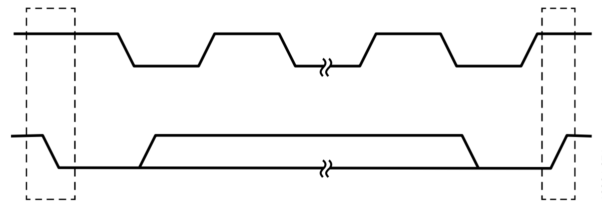


Figure 79. Start and Stop Transitions

REPEATED START CONDITION

In general, a repeated start (Sr) condition is the absence of a stop condition between two transfers. The PMBus communication protocol makes use of the repeated start condition only when performing a read access (read byte, read word, and block read). Other uses of the repeated start condition are not allowed.

GENERAL CALL SUPPORT

The PMBus slave is capable of decoding and acknowledging a general call address. The PMBus device responds to both its own address and the general call address (0x00).

Note that all PMBus commands must start with the slave address with the R/$\overline{W}$ bit cleared (set to 0), followed by the command code. This is also true when using the general call address to communicate with the PMBus slave device. The only exception to this rule is when the $\overline{\text{SMBALRT}}$ alert response address is used.

ALERT RESPONSE ADDRESS (ARA)

If a PMBus slave device supports the $\overline{\text{SMBALRT}}$ hardware pin to interrupt the master on a fault condition, the SMBus Alert Response Address Protocol must be supported to allow communication between the master and slave on the device that triggers the fault.

When the $\overline{\text{SMBALRT}}$ pin on the slave is asserted, the master queries the address of the slave device that triggered the fault by sending the alert response address (0001 to 100x). In response to this address, the slave with the asserted $\overline{\text{SMBALRT}}$ pin acknowledges (ACKs) the address and responds with its own slave address (7-bit address and plus 0). If multiple slave devices have their $\overline{\text{SMBALRT}}$ pins asserted, the slave with the lowest address wins the arbitration and subsequently deasserts its $\overline{\text{SMBALRT}}$ pin.

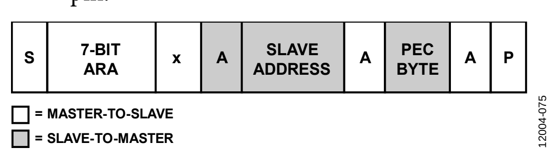


Figure 80. ARA Protocol with PEC

PMBUS ADDRESS SELECTION

Control of the ADP1055 is implemented via the I²C interface. The ADP1055 device is connected to the I²C bus as a slave device under the control of a master device. The PMBus address of the ADP1055 is set by connecting an external resistor from the ADD pin to AGND. Table 11 lists the recommended resistor values and associated PMBus addresses.

Table 11. PMBus Address Settings

PMBus Addr 1	PMBus Addr 2	PMBus Addr 3	PMBus Addr 4	1% Resistor (Ω) (E96 series)
0x40	0x50	0x60	0x70	210 (or connect to AGND)
0x41	0x51	0x61	0x71	750
0x42	0x52	0x62	0x72	1330
0x43	0x53	0x63	0x73	2050
0x44	0x54	0x64	0x74	2670
0x45	0x55	0x65	0x75	3570
0x46	0x56	0x66	0x76	4420
0x47	0x57	0x67	0x77	5360
0x48	0x58	0x68	0x78	6340
0x49	0x59	0x69	0x79	7320
0x4A	0x5A	0x6A	0x7A	8450
0x4B	0x5B	0x6B	0x7B	9530
0x4C	0x5C	0x6C	0x7C	10,700
0x4D	0x5D	0x6D	0x7D	12,100
0x4E	0x5E	0x6E	0x7E	13,700
0x4F	0x5F	0x6F	0x7F	15,000 (or connect to VDD)

Using a resistor enables the selection of 16 different base addresses from 0x40 to 0x4F. Additional addresses can be selected using the SLV_ADDR_SELECT command (Register 0xD0). For example, a device can be programmed to have an address of 0x65 by connecting a 3.57 kΩ resistor at the ADD pin and programming Register 0xD0[5:4] to 10 and saving to the EEPROM. The next time that the power is cycled to the ADP1055, the device responds to an address of 0x65. Other addresses can be selected.

If an incorrect resistor value is used and the resulting I²C address is close to a threshold between two addresses, the STATUS_UNKNOWN flag is set (Register 0xFE94[3]). It is recommended that 1% tolerance resistors be used on the ADD pin. However, 5% resistors can be selected, but the use of some of the addresses will not be allowed due to the overlap of address ranges.

In addition to its programmed address, the ADP1055 responds to the standard PMBus broadcast address (general call) of 0x00.

FAST MODE

Fast mode (400 kHz) uses essentially the same mechanics as the standard mode of operation; the electrical specifications and timing are most affected. The PMBus slave is capable of communicating with a master device operating in standard mode (100 kHz) or fast mode.

10-BIT ADDRESSING

The PMBus slave device does not support 10-bit addressing as defined in the I²C specification.

PACKET ERROR CHECKING

The PMBus controller implements packet error checking (PEC) to improve reliability and communication robustness. Packet error checking is implemented by appending a PEC byte at the end of the message transfer. The PEC byte is calculated using a CRC-8 algorithm on all ADDR, CMD, and DATA bytes from the start to stop bits (excluding the ACK, NACK, start, restart, and stop bits). The PEC byte is appended to the end of the message by the device that supplied the last data byte. The receiver of the PEC byte is responsible for calculating its internal PEC code and comparing it to the received PEC byte.

The ADP1055 can communicate with master PMBus devices that support PEC, as well as with master devices that do not support PEC. If a PEC byte is available, the PMBus device checks the PEC byte and issues an acknowledge (ACK) if the PEC byte is correct. If the PEC byte comparison fails, the PMBus device issues a no acknowledge (NACK) in response to the PEC byte and does not process the command sent from the master.

The PMBus device uses built-in hardware to calculate the PEC code using the CRC-8 polynomial, $C(x) = x^8 + x^2 + x^1 + 1$. The PEC code is calculated one byte at a time, in the order that it is received. In a read transaction, the PMBus device appends the PEC byte following the last data byte. In a write transaction, the PMBus device compares the received PEC byte to the internally calculated PEC code.

ELECTRICAL SPECIFICATIONS

All logic complies with the Electrical Specification outlined in the *PMBus Power System Management Protocol Specification Part 1*, Revision 1.2, dated September 6, 2010.

FAULT CONDITIONS

The PMBus protocol provides a comprehensive set of fault conditions that must be monitored and reported. These fault conditions can be grouped into two major categories: communication faults and monitoring faults.

Communication faults are error conditions associated with the data transfer mechanism of the PMBus protocol (see the following sections for more information).

Monitoring faults are error conditions associated with the operation of the PMBus device, such as output overvoltage protection, and are specific to each PMBus device. For more information about the monitoring fault conditions, see the Fault Responses and State Machine Mechanics section.

TIMEOUT CONDITIONS

The SMBus specification, Version 2.0, includes three clock stretching specifications related to timeout conditions. The timeout conditions are described in the following sections.

$T_{TIMEOUT}$

A timeout condition occurs if any single SCL clock pulse is held low for longer than the $T_{TIMEOUT\ MIN}$ of 25 ms. Upon detecting the timeout condition, the PMBus slave device has 10 ms to abort the transfer, release the bus lines, and be ready to accept a new start condition. The device initiating the timeout is required to hold the SCL clock line low for at least $T_{TIMEOUT\ MAX}$ = 35 ms, guaranteeing that the slave device is given enough time to reset its communication protocol.

$T_{LOW:SEXT}$

The $T_{LOW:SEXT}$ = 25 ms specification is defined as the cumulative time that the SCL line is held low by the slave device in any one message from the start to the stop condition. The PMBus slave device is guaranteed by design not to violate this specification. If the slave device violates this specification, the master is allowed to abort the transaction in progress and issue a stop condition at the conclusion of the byte transfer in progress.

$T_{LOW:MEXT}$

The $T_{LOW:MEXT}$ = 10 ms specification is defined as the cumulative time that the SCL line is held low by the master device in any one byte of a message between the start-to-acknowledge, acknowledge-to-acknowledge, or acknowledge-to-stop. If this specification is violated, the PMBus device treats it as a timeout condition and aborts the transfer. This check is not implemented in the ADP1055.

DATA TRANSMISSION FAULTS

Data transmission faults occur when two communicating devices violate the PMBus communication protocol. The following items are taken from the PMBus specification (Revision 1.2, September 6, 2010). See the PMBus specification for more information about each fault condition.

Corrupted Data, PEC (Item 10.8.1)

This item refers to parity error checking. The PMBus slave device compares the received PEC byte with the calculated expected PEC byte of each transmission, starting from the start bit to the stop bit. If the comparison fails, it responds as follows:

- Send a no acknowledge (NACK) for the PEC byte.
- Flush and ignore the received command and data.
- Set the CML bit (Bit 1) in the STATUS_BYTE register.
- Set the PEC bit (Bit 5) in the STATUS_CML register.
- Notify the host through $\overline{\text{SMBALRT}}$, if enabled.

Sending Too Few Bits (Item 10.8.2)

Transmission is interrupted by a start or stop condition before a complete byte (eight bits) has been sent. Not supported; any transmitted data is ignored.

Reading Too Few Bits (Item 10.8.3)

Transmission is interrupted by a start or stop condition before a complete byte (eight bits) has been read. Not supported; any received data is ignored.

Hosts Sends or Reads Too Few Bytes (Item 10.8.4)

If a host ends a packet with a stop condition before the required bytes are sent/received, it is assumed that the host intended to stop the transfer. Therefore, the PMBus slave does not consider this to be an error and takes no action, except to flush any remaining bytes in the transmit FIFO.

Host Sends Too Many Bytes (Item 10.8.5)

If a host sends more bytes than are expected for the corresponding command, the PMBus slave considers this a data transmission fault and responds as follows:

- Send a no acknowledge (NACK) for all unexpected bytes as they are received.
- Flush and ignore the received command and data.
- Sets the CML bit (Bit 1) in the STATUS_BYTE register.
- Set the invalid/unsupported data bit (Bit 6) in the STATUS_CML register.
- Notify the host through $\overline{\text{SMBALRT}}$, if enabled.

Host Reads Too Many Bytes (Item 10.8.6)

If a host reads more bytes than are expected for the corresponding command, the PMBus slave considers this a data transmission fault and responds as follows:

- Send all 1s (0xFF) as long as the host continues to request data.
- Set the CML bit (Bit 1) in the STATUS_BYTE register.
- Set the Other bit (Bit 1) in the STATUS_CML register.
- Notify host through $\overline{\text{SMBALRT}}$, if enabled.

Device Busy (Item 10.8.7)

PMBus slave device is too busy to respond to a request from the master device. This error can occur if the slave device is busy accessing the EEPROM (for example, erasing a page, downloading from EEPROM, or uploading to EEPROM). The PMBus slave considers this a data transmission fault and responds as follows:

- Send an acknowledge (ACK) for the address byte.
- Send a no acknowledge (NACK) for the command and data bytes.
- Send all 1s (0xFF) as long as the host continues to request data.
- Set the busy bit (Bit 7) in the STATUS_BYTE register.
- Notify the host through $\overline{\text{SMBALRT}}$, if enabled.

DATA CONTENT FAULTS

Data content faults occur when data transmission is successful, but the PMBus slave device cannot process the data that is received from the master device.

Improperly Set Read Bit in the Address Byte (Item 10.9.1)

All PMBus commands start with a slave address with the R/$\overline{\text{W}}$ bit cleared to 0, followed by the command code. The only exception is the transmission of the SMBus alert response address (0001 to 100x). If a host starts a PMBus transaction with R/$\overline{\text{W}}$ set in the address phase (equivalent to an I^2C read), the PMBus slave considers this a data content fault and responds as follows:

- Send an acknowledge (ACK) for the address byte.
- Send a no acknowledge (NACK) for the command and data bytes.
- Send all 1s (0xFF) as long as the host continues to request data.
- Set the CML bit (Bit 1) in the STATUS_BYTE register.
- Set the Other bit (Bit 1) in the STATUS_CML register.
- Notify the host through $\overline{\text{SMBALRT}}$, if enabled.

Invalid or Unsupported Command Code (Item 10.9.2)

If an invalid or unsupported command code is sent to the PMBus slave, the code is considered to be a data content fault, and the PMBus slave responds as follows:

- Send a no acknowledge (NACK) for the illegal/unsupported command byte and data bytes.
- Flush and ignore the received command and data.
- Set the CML bit (Bit 1) in the STATUS_BYTE register.
- Set the invalid/unsupported command bit (Bit 7) in the STATUS_CML register.
- Notify the host through $\overline{\text{SMBALRT}}$, if enabled.

Invalid or Unsupported Data (Item 10.9.3)

If invalid or unsupported data is sent to the PMBus slave (for certain commands), the PMBus slave considers this to be a data content fault and responds as follows:

- Send an acknowledge (ACK) for the unsupported data bytes (cannot send a no acknowledge (NACK) for the data because the decoding happens only after the data is acknowledged and sent to the decoding unit).
- Flush and ignore the received command and data.
- Set the CML bit (Bit 1) in the STATUS_BYTE register.
- Set the invalid/unsupported data received bit (Bit 6) in the STATUS_CML register.
- Notify the host through $\overline{\text{SMBALRT}}$, if enabled.

Data Out of Range Fault (Item 10.9.4)

Data sent to the PMBus slave that is out of range is treated as a data content fault. See the Invalid or Unsupported Data (Item 10.9.3) section for the actions taken by the PMBus device.

Reserved Bits (Item 10.9.5)

Accesses to reserved bits are not a fault. Writes to reserved bits are ignored, and reads from reserved bits return 0s.

Write to Read-Only Commands

If a host performs a write to a read-only command, the PMBus slave considers this a data content fault and responds as follows:

- Send a no acknowledge (NACK) for all unexpected data bytes as they are received.
- Flush and ignore the received command and data.
- Set the CML bit (Bit 1) in the STATUS_BYTE register.
- Set the invalid/unsupported data received bit (Bit 6) in the STATUS_CML register.
- Notify the host through $\overline{\text{SMBALRT}}$, if enabled.

Note that this is the same error described in the Host Sends Too Many Bytes (Item 10.8.5) section.

Read from Write-Only Commands

If a host performs a read from a write-only command, the PMBus slave considers this a data content fault and responds as follows:

- Send all 1s (0xFF) as long as the host continues to request data.
- Set the CML bit (Bit 1) in the STATUS_BYTE register.
- Set the Other bit (Bit 1) in the STATUS_CML register.

Note that this is the same error described in the Host Reads Too Many Bytes (Item 10.8.6) section.

LAYOUT GUIDELINES

This section describes best practices to ensure optimal performance of the ADP1055. In general, place all components as close to the ADP1055 as possible. All signals should be referenced to their respective grounds.

CS2+ AND CS2– PINS

Route the traces from the sense resistor to the ADP1055 parallel to each other. Keep the traces close together and as far from the switch nodes as possible.

VS+ AND VS– PINS

Route the traces from the remote voltage sense point to the ADP1055 parallel to each other. Keep the traces close together and as far from the switch nodes as possible. Place a 100 nF capacitor from VS– to AGND to reduce common-mode noise.

VDD PIN

Place decoupling capacitors as close to the device as possible. A 4.7 µF capacitor from VDD to AGND is recommended.

SDA AND SCL PINS

Route the traces to the SDA and SCL pins parallel to each other. Keep the traces close together and as far from the switch nodes as possible. It may be advantageous to add a filtering circuit, as shown in Figure 81.

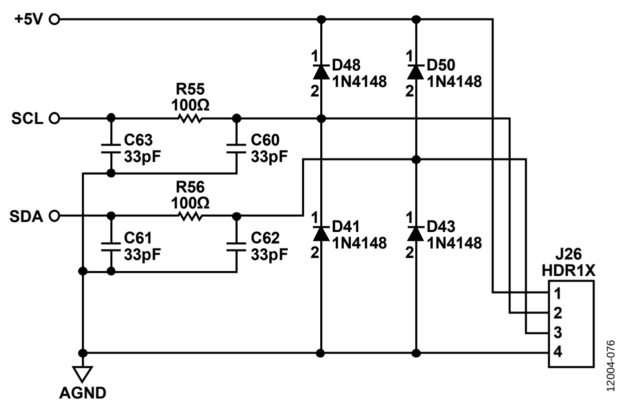


Figure 81. I²C Filtering Circuit

CS1 PIN

Route the traces from the current sense transformer to the ADP1055 parallel to each other. Keep the traces close together and as far from the switch nodes as possible.

EXPOSED PAD

Solder the exposed thermal pad on the underside of the ADP1055 package to the PCB AGND plane.

VCORE PIN

Place a 330 nF decoupling capacitor from the VCORE pin to DGND, as close to the device as possible.

RES PIN

Place a 10 kΩ, 0.1% resistor from the RES pin to AGND, as close to the device as possible.

JTD AND JRTN PINS

Route a single trace to the ADP1055 from the junction diode using a trace to JRTN. If single-ended sensing is preferred, tie the return to AGND using a dedicated trace. Make sure to lay out the temperature sensor by isolating it and keeping it away from any direct switch nodes. It is recommended that a 220 nF to 470 nF capacitor be placed between the base-emitter junctions of the thermal sensor.

OVP PIN

Route the OVP traces away from any switching nodes to avoid spuriously tripping the comparator at that pin.

SYNC PIN

It is important to route the trace to the SYNC pin to prevent any noise from being coupled to the information in the signal. It is recommended that this trace be kept away from switch nodes and routed as an internal layer so that the AGND plane acts as a shield to this trace.

AGND AND DGND

Create an AGND ground plane (preferably in the inner layer) and make a single-point (star) connection to the power supply system ground. Connect DGND to AGND with a very short trace using a star connection. It may be advantageous to have an entire VDD plane as an additional layer for noise immunity.

EEPROM

The ADP1055 has a built-in EEPROM controller that is used to communicate with the embedded 8k × 8-byte EEPROM. The EEPROM, also called Flash®/EE, is partitioned into two major blocks: the INFO block and the main block. The INFO block contains 128 8-bit bytes (for internal use only), and the main block contains 8k 8-bit bytes. The main block is further partitioned into 16 pages; each page contains 512 bytes.

OVERVIEW

The EEPROM controller provides an interface between the ADP1055 core logic and the built-in Flash/EE. The user can control data access to and from the EEPROM through this controller interface. Different I^2C commands are available for the different operations to the EEPROM.

Communication is initiated by the master device sending a command to the I^2C slave device to access data from or send data to the EEPROM. Using read and write commands, data is transferred between devices in a byte wide format. Using a read command, data is received from the EEPROM and transmitted to the master device. Using a write command, data is received from the master device and stored in the EEPROM through the EEPROM controller. Send commands are also supported; a send command is executed by the slave device upon receiving the stop bit. The stop bit is the last bit in a complete data transfer, as defined in the I^2C communication protocol. For a complete description of the I^2C protocol, see the Philips *I^2C Bus Specification*, Version 2.1, dated January 2000.

PAGE ERASE OPERATION

The main block consists of 16 equivalent pages of 512 bytes each, numbered Page 0 to Page 15. Page 0 and Page 1 of the main block are reserved for storing the default settings and user settings, respectively. Page 2 and Page 3 are reserved for storing the black box information, and Page 4 and Page 5 are used to store the GUI settings and factory tracking information. The user cannot perform a page erase operation to any of Page 0 to Page 5.

Only Page 6 to Page 15 of the main block can be used to store data. To erase any page from Page 6 to Page 15, the EEPROM must first be unlocked for access. For instructions on how to unlock the EEPROM, see the Unlock the EEPROM section.

Page 6 to Page 15 of the main block can be individually erased using the EEPROM_PAGE_ERASE command (Register 0xD4).

For example, to perform a page erase of Page 10, execute the following command:

S	7-BIT SLAVE ADDRESS	$\overline{W}$	A	COMMAND CODE	A	DATA BYTE	A	P

□ = MASTER-TO-SLAVE
■ = SLAVE-TO-MASTER

12004-077

Figure 82. Example Erase Command

In this example, command code = 0xD4 and data byte = 0x0A.

Wait at least 35 ms for the page erase operation to complete before executing the next I^2C command.

The EEPROM allows erasing of whole pages only; therefore, to change the data of any single byte in a page, the entire page must first be erased (set high) for that byte to be writable. Subsequent writes to any bytes in that page are allowed as long as that byte has not been written to a logic low previously.

READ OPERATION (BYTE READ AND BLOCK READ)

Read from Main Block, Page 0 to Page 5

Page 0 and Page 1 of the main block are reserved for storing the default settings and user settings, respectively. Page 2 and Page 3 are reserved for storing the black box information, and Page 4 and Page 5 are used to store the GUI settings and factory tracking information. These pages are intended to prevent third-party access to this data. To read a page from Page 0 to Page 5, the user must first unlock the EEPROM (see the Unlock the EEPROM section). After the EEPROM is unlocked, Page 0 to Page 5 are readable using the EEPROM_PAGE_xx commands, as described in the Read from Main Block, Page 6 to Page 15 section. Note that when the EEPROM is locked, a read from Page 0 to Page 5 returns invalid data.

Read from Main Block, Page 6 to Page 15

Data in Page 6 to Page 15 of the main block is always readable, even with the EEPROM locked. The data in the EEPROM main block can be read one byte at a time or in multiple bytes in series using the EEPROM_PAGE_xx commands (Register 0xB0 to Register 0xBF).

Before executing this command, the user must program the number of bytes to read using the EEPROM_NUM_RD_BYTES command (Register 0xD2). The user can also program the offset from the page boundary where the first read byte is returned using the EEPROM_ADDR_OFFSET command (Register 0xD3).

In the following example, three bytes from Page 6 are read from the EEPROM, starting from the fifth byte of that page.

1. Set the number of return bytes = 3.

S	7-BIT SLAVE ADDRESS	$\overline{W}$	A	0xD2	A	0x03	A	P

□ = MASTER-TO-SLAVE
■ = SLAVE-TO-MASTER

12004-078

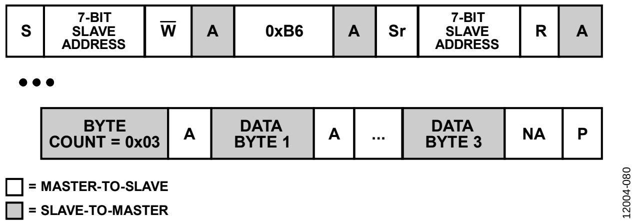
2. Set address offset = 5.

S	7-BIT SLAVE ADDRESS	$\overline{W}$	A	0xD3	A	0x00	A	0x05	A	P

□ = MASTER-TO-SLAVE
■ = SLAVE-TO-MASTER

12004-079

3. Read three bytes from Page 6.



Note that the block read command can read a maximum of 255 bytes for any single transaction.

WRITE OPERATION (BYTE WRITE AND BLOCK WRITE)

Write to Main Block, Page 0 and Page 5

Page 0 and Page 1 of the main block are reserved for storing the default settings and user settings, respectively. Page 2 through Page 5 of the main block are reserved for storing the black box information, GUI settings, and factory tracking information. The user cannot perform a direct write operation to any page from Page 0 to Page 5 using the EEPROM_PAGE_00 to EEPROM_PAGE_05 commands. A user write to these pages returns a no acknowledge. To program the register contents of Page 1 of the main block, it is recommended that the STORE_USER_ALL command be used (Register 0x15). See the Save Register Settings to User Settings section.

Write to Main Block, Page 6 to Page 15

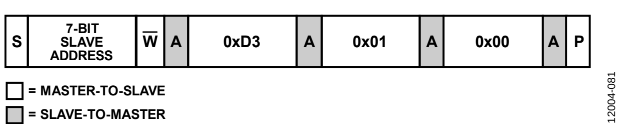
Before performing a write to Page 6 through Page 15 of the main block, the user must first unlock the EEPROM (see the Unlock the EEPROM section).

Data in Page 6 to Page 15 of the EEPROM main block can be programmed (written to) one byte at a time or in multiple bytes in series using the EEPROM_PAGE_xx commands (Register 0xB6 to Register 0xBF). Before executing this command, the user can program the offset from the page boundary where the first byte is written using the EEPROM_ADDR_OFFSET command (Register 0xD3).

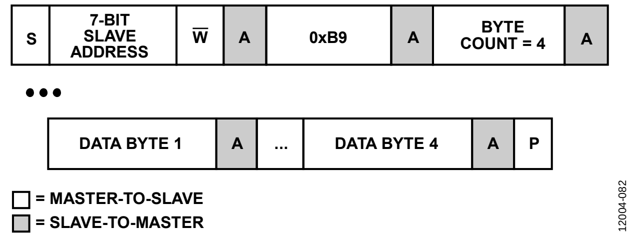
If the targeted page has not yet been erased, the user can erase the page as described in the Page Erase Operation section.

In the following example, four bytes are written to Page 9, starting from the 256^{th} byte of that page.

1. Set address offset = 256.



2. Write four bytes to Page 9.



Note that the block write command can write a maximum of 255 bytes for any single transaction.

EEPROM PASSWORD

On power-up, the EEPROM is locked and protected from accidental writes or erases. Only reads from Page 6 to Page 15 of the main block are allowed when the EEPROM is locked. Before any data can be written (programmed) to the EEPROM, the EEPROM must be unlocked for write access. After it is unlocked, the EEPROM is opened for reading, writing, and erasing.

Unlock the EEPROM

To unlock the EEPROM, perform two consecutive writes with the correct password (default = 0xFF) using the EEPROM_PASSWORD command (Register 0xD5). The EEPROM_UNLOCKED flag (Register 0xFE93, Bit 15) is set to indicate that the EEPROM is unlocked for write access.

Lock the EEPROM

To lock the EEPROM, write any byte other than the correct password using the EEPROM_PASSWORD command (Register 0xD5). The EEPROM_UNLOCKED flag (Register 0xFE93, Bit 15) is cleared to indicate that the EEPROM is locked from write access.

Change the EEPROM Password

To change the EEPROM password, follow these steps:

1. Enter the correct 32-bit key code using the KEY_CODE command (Register 0xD7).
2. Write the old password using the EEPROM_PASSWORD command (Register 0xD5).
3. Immediately write the new password using the EEPROM_PASSWORD command (Register 0xD5).

The password is now changed to the new password. Save the new password to the user settings by executing the STORE_USER_ALL command (Register 0x15).

DOWNLOADING EEPROM SETTINGS TO INTERNAL REGISTERS

Download User Settings to Registers

The user settings are stored in Page 1 of the EEPROM main block. These settings are downloaded from the EEPROM into the registers under the following conditions:

- On power-up. The user settings are automatically downloaded into the internal registers, powering the ADP1055 up in a state previously saved by the user.
- On execution of the RESTORE_USER_ALL command (Register 0x16). This command allows the user to force a download of the user settings from Page 1 of the EEPROM main block into the internal registers.

Download Factory Default Settings to Registers

The factory default settings are stored in Page 0 of the EEPROM main block. The factory default settings can be downloaded from the EEPROM into the internal registers using the RESTORE_DEFAULT_ALL command (Register 0x12).

Note that when this command is executed, the key code and EEPROM passwords are also reset to their default factory settings of 0xFFFFFFFF and 0xFF, respectively.

SAVING REGISTER SETTINGS TO THE EEPROM

The register settings cannot be saved to the factory default settings located in Page 0 of the EEPROM main block. This is to prevent the user from accidentally overriding the factory trim settings and default register settings.

Save Register Settings to User Settings

The register settings can be saved to the user settings located in Page 1 of the EEPROM main block using the STORE_USER_ALL command (Register 0x15). Before this command can be executed, the EEPROM must first be unlocked for writing (see the Unlock the EEPROM section).

After the register settings are saved to the user settings, any subsequent power cycle automatically downloads the latest stored user information from the EEPROM into the internal registers.

Note that execution of the STORE_USER_ALL command automatically performs a page erase to Page 1 of the EEPROM main block, after which the register settings are stored in the EEPROM. Therefore, it is important to wait at least 35 ms for the operation to complete before executing the next I^2C command.

EEPROM CRC CHECKSUM

As a simple method of checking that the values downloaded from the EEPROM are consistent with the internal registers, a CRC checksum is implemented.

- When the data from the internal registers is saved to the EEPROM (Page 1 of the main block), the total number of 1s from all the registers is counted and written into the EEPROM as the last byte of information. This is called the CRC checksum.
- When the data is downloaded from the EEPROM into the internal registers, a similar counter that sums all 1s from the values loaded into the registers is saved. This value is compared with the CRC checksum from the previous upload operation.

If the values match, the download operation was successful. If the values differ, the EEPROM download operation failed, and the EEPROM CRC fault flag is set (Bit 4 of Register 0x7E).

To read the EEPROM CRC checksum value, execute the EEPROM_CRC_CHKSUM command (Register 0xD1). This command returns the CRC checksum accumulated in the counter during the download operation.

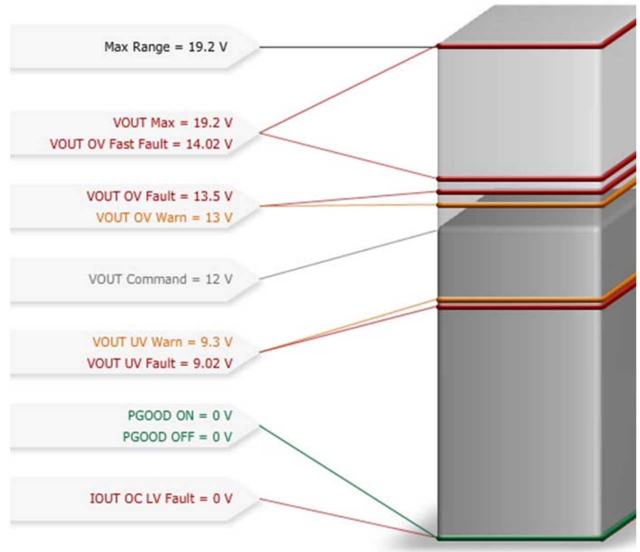
Note that the CRC checksum is an 8-bit cyclical accumulator that wraps around to 0 when 255 is reached.

SOFTWARE GUI

A free software GUI is available for programming and configuring the ADP1055. The GUI is designed to be intuitive to power supply designers and dramatically reduces power supply design and development time.

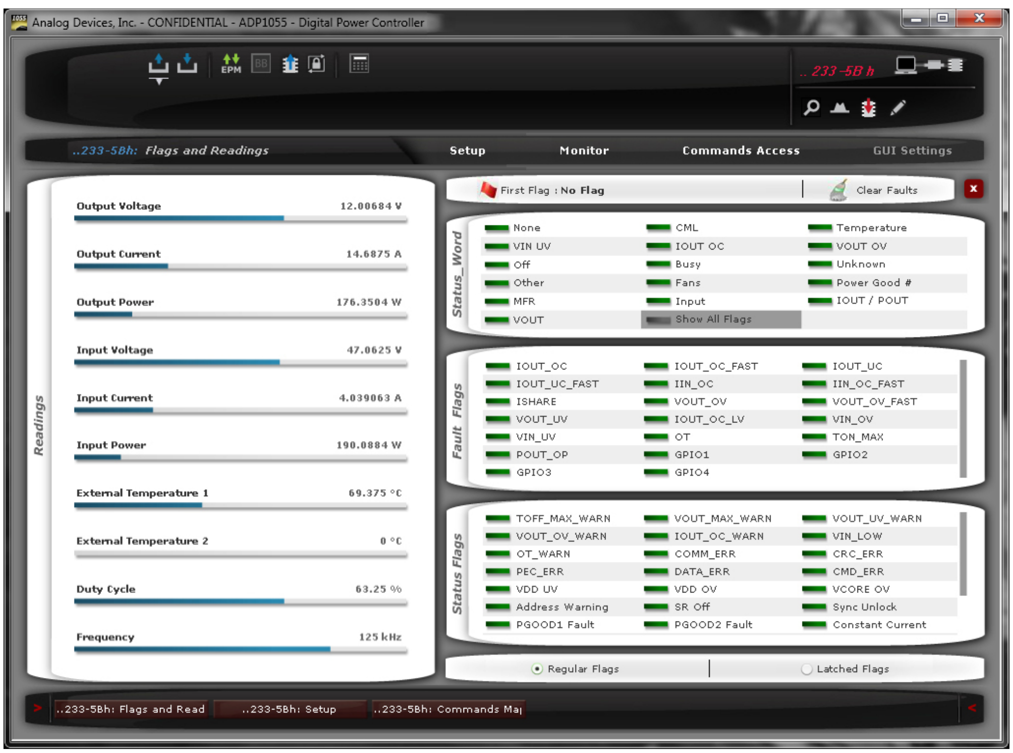
The software includes filter design and power supply PWM topology windows. The GUI is also an information center, displaying the status of all readings, monitoring, and flags on the ADP1055. The GUI takes into account all PMBus conversions; the user need only enter the voltage and current settings (or thresholds) in volts and amperes. All PMBus flags and readings are also displayed in the GUI. For more information about the GUI, see the ADP1055 product page).

Evaluation boards are also available; for more information, see the ADP1055 product page).



12004-083

Figure 83. Voltage Settings Window of the ADP1055 GUI



12004-084

Figure 84. Monitor Window of the ADP1055 GUI

STANDARD PMBUS COMMANDS SUPPORTED BY THE ADP1055

Table 12 lists the standard PMBus commands that are implemented on the ADP1055. Many of these commands are implemented in registers, which share the same hexadecimal value as the PMBus command code. All commands are maskable with the exceptions noted in Table 12.

Table 12. PMBus Command List

Command Code	Command Name
0x01	OPERATION
0x02	ON_OFF_CONFIG
0x03	CLEAR_FAULTS
0x10	WRITE_PROTECT
0x12	RESTORE_DEFAULT_ALL
0x15	STORE_USER_ALL[1]
0x16	RESTORE_USER_ALL[1]
0x19	CAPABILITY
0x1B	SMBALERT_MASK
0x20	VOUT_MODE
0x21	VOUT_COMMAND
0x22	VOUT_TRIM
0x23	VOUT_CAL_OFFSET
0x24	VOUT_MAX
0x27	VOUT_TRANSITION_RATE
0x28	VOUT_DROOP
0x29	VOUT_SCALE_LOOP
0x2A	VOUT_SCALE_MONITOR
0x33	FREQUENCY_SWITCH
0x35	VIN_ON
0x36	VIN_OFF
0x37	INTERLEAVE
0x38	IOUT_CAL_GAIN
0x39	IOUT_CAL_OFFSET
0x40	VOUT_OV_FAULT_LIMIT
0x41	VOUT_OV_FAULT_RESPONSE
0x42	VOUT_OV_WARN_LIMIT
0x43	VOUT_UV_WARN_LIMIT
0x44	VOUT_UV_FAULT_LIMIT
0x45	VOUT_UV_FAULT_RESPONSE
0x46	IOUT_OC_FAULT_LIMIT
0x47	IOUT_OC_FAULT_RESPONSE
0x48	IOUT_OC_LV_FAULT_LIMIT
0x49	IOUT_OC_LV_FAULT_RESPONSE
0x4A	IOUT_OC_WARN_LIMIT
0x4B	IOUT_UC_FAULT_LIMIT
0x4C	IOUT_UC_FAULT_RESPONSE
0x4F	OT_FAULT_LIMIT
0x50	OT_FAULT_RESPONSE
0x51	OT_WARN_LIMIT
0x55	VIN_OV_FAULT_LIMIT
0x56	VIN_OV_FAULT_RESPONSE
0x59	VIN_UV_FAULT_LIMIT
0x5A	VIN_UV_FAULT_RESPONSE
0x5B	IIN_OC_FAULT_LIMIT
0x5C	IIN_OC_FAULT_RESPONSE
0x5E	POWER_GOOD_ON
0x5F	POWER_GOOD_OFF
0x60	TON_DELAY
0x61	TON_RISE
0x62	TON_MAX_FAULT_LIMIT
0x63	TON_MAX_FAULT_RESPONSE
0x64	TOFF_DELAY
0x65	TOFF_FALL
0x66	TOFF_MAX_WARN_LIMIT
0x68	POUT_OP_FAULT_LIMIT
0x69	POUT_OP_FAULT_RESPONSE
0x78	STATUS_BYTE
0x79	STATUS_WORD
0x7A	STATUS_VOUT
0x7B	STATUS_IOUT
0x7C	STATUS_INPUT
0x7D	STATUS_TEMPERATURE
0x7E	STATUS_CML
0x7F	STATUS_OTHER
0x80	STATUS_MFR_SPECIFIC
0x88	READ_VIN
0x89	READ_IIN
0x8B	READ_VOUT
0x8C	READ_IOUT
0x8D	Reserved
0x8E	READ_TEMPERATURE_2
0x8F	READ_TEMPERATURE_3
0x94	READ_DUTY_CYCLE
0x95	READ_FREQUENCY
0x96	READ_POUT
0x98	PMBUS_REVISION
0x99	MFR_ID
0x9A	MFR_MODEL
0x9B	MFR_REVISION
0x9C	MFR_LOCATION
0x9D	MFR_DATE
0x9E	MFR_SERIAL
0xAD	IC_DEVICE_ID
0xAE	IC_DEVICE_REV
0xB0	EEPROM_PAGE_00
0xB1	EEPROM_PAGE_01
0xB2	EEPROM_PAGE_02
0xB3	EEPROM_PAGE_03
0xB4	EEPROM_PAGE_04
0xB5	EEPROM_PAGE_05
0xB6	EEPROM_PAGE_06
0xB7	EEPROM_PAGE_07
0xB8	EEPROM_PAGE_08

Command Code	Command Name
0xB9	EEPROM_PAGE_09
0xBA	EEPROM_PAGE_10
0xBB	EEPROM_PAGE_11
0xBC	EEPROM_PAGE_12
0xBD	EEPROM_PAGE_13
0xBE	EEPROM_PAGE_14
0xBF	EEPROM_PAGE_15
0xD0	SLV_ADDR_SELECT[1]
0xD1	EEPROM_CRC_CHKSUM
0xD2	EEPROM_NUM_RD_BYTES

Command Code	Command Name
0xD3	EEPROM_ADDR_OFFSET
0xD4	EEPROM_PAGE_ERASE
0xD5	EEPROM_PASSWORD[1]
0xD6	TRIM_PASSWORD
0xD7	KEY_CODE[1]
0xF1	EEPROM_INFO[1]
0xF2	READ_BLACKBOX_CURR
0xF3	READ_BLACKBOX_PREV
0xF4	CMD_MASK[1]
0xF5	EXTCMD_MASK[1]

[1] This command is not maskable.

MANUFACTURER SPECIFIC COMMANDS

Table 13 lists the manufacturer-specific PMBus commands that are implemented on the ADP1055. These commands are implemented in registers, which share the same hexadecimal value as the PMBus command code. All commands are maskable.

Table 13. Manufacturer Specific Command List

Command Code	Command Name
0xFE00	GO_CMD
0xFE01	NM_DIGFILT_LF_GAIN_SETTING
0xFE02	NM_DIGFILT_ZERO_SETTING
0xFE03	NM_DIGFILT_POLE_SETTING
0xFE04	NM_DIGFILT_HF_GAIN_SETTING
0xFE05	LLM_DIGFILT_LF_GAIN_SETTING
0xFE06	LLM_DIGFILT_ZERO_SETTING
0xFE07	LLM_DIGFILT_POLE_SETTING
0xFE08	LLM_DIGFILT_HF_GAIN_SETTING
0xFE09	SS_DIGFILT_LF_GAIN_SETTING
0xFE0A	SS_DIGFILT_ZERO_SETTING
0xFE0B	SS_DIGFILT_POLE_SETTING
0xFE0C	SS_DIGFILT_HF_GAIN_SETTING
0xFE0D	OUTA_REDGE_SETTING
0xFE0E	OUTA_FEDGE_SETTING
0xFE0F	OUTB_REDGE_SETTING
0xFE10	OUTB_FEDGE_SETTING
0xFE11	OUTC_REDGE_SETTING
0xFE12	OUTC_FEDGE_SETTING
0xFE13	OUTD_REDGE_SETTING
0xFE14	OUTD_FEDGE_SETTING
0xFE15	SR1_REDGE_SETTING
0xFE16	SR1_FEDGE_SETTING
0xFE17	SR2_REDGE_SETTING
0xFE18	SR2_FEDGE_SETTING
0xFE19	SR1_REDGE_LLM_SETTING
0xFE1A	SR1_FEDGE_LLM_SETTING
0xFE1B	SR2_REDGE_LLM_SETTING
0xFE1C	SR2_FEDGE_LLM_SETTING
0xFE1D	ADT_CONFIG
0xFE1E	ADT_THRESHOLD
0xFE1F	OUTA_DEAD_TIME
0xFE20	OUTB_DEAD_TIME
0xFE21	OUTC_DEAD_TIME
0xFE22	OUTD_DEAD_TIME
0xFE23	SR1_DEAD_TIME
0xFE24	SR2_DEAD_TIME
0xFE25	VSBAL_SETTING
0xFE26	VSBAL_OUTA_B
0xFE27	VSBAL_OUTC_D
0xFE28	VSBAL_SR1_2
0xFE29	FFWD_SETTING
0xFE2A	ISHARE_SETTING
0xFE2B	ISHARE_BANDWIDTH
0xFE2C	IIN_OC_FAST_SETTING
0xFE2D	IOUT_OC_FAST_SETTING
0xFE2E	IOUT_UC_FAST_SETTING
0xFE2F	VOUT_OV_FAST_SETTING
0xFE30	DEBOUNCE_SETTING_1
0xFE31	DEBOUNCE_SETTING_2
0xFE32	DEBOUNCE_SETTING_3
0xFE33	DEBOUNCE_SETTING_4
0xFE34	VOUT_OV_FAST_FAULT_RESPONSE
0xFE35	IOUT_OC_FAST_FAULT_RESPONSE
0xFE36	IOUT_UC_FAST_FAULT_RESPONSE
0xFE37	IIN_OC_FAST_FAULT_RESPONSE
0xFE38	ISHARE_FAULT_RESPONSE
0xFE39	GPIO1_FAULT_RESPONSE
0xFE3A	GPIO2_FAULT_RESPONSE
0xFE3B	GPIO3_FAULT_RESPONSE
0xFE3C	GPIO4_FAULT_RESPONSE
0xFE3D	PWM_FAULT_MASK
0xFE3E	DELAY_TIME_UNIT
0xFE3F	WDT_SETTING
0xFE40	GPIO_SETTING
0xFE41	GPIO1_2_KARNAUGH_MAP
0xFE42	GPIO3_4_KARNAUGH_MAP
0xFE43	PGOOD_FAULT_DEB
0xFE44	PGOOD1_FAULT_SELECT
0xFE45	PGOOD2_FAULT_SELECT
0xFE46	SOFT_START_BLANKING
0xFE47	SOFT_STOP_BLANKING
0xFE48	BLACKBOX_SETTING
0xFE49	PWM_DISABLE_SETTING
0xFE4A	FILTER_TRANSITION
0xFE4B	DEEP_LLM_SETTING
0xFE4C	DEEP_LLM_DISABLE_SETTING
0xFE4D	OVP_FAULT_CONFIG
0xFE4E	CS1_SETTING
0xFE4F	CS2_SETTING
0xFE50	PULSE_SKIP_AND_SHUTDOWN
0xFE51	SOFT_START_SETTING
0xFE52	SR_DELAY
0xFE53	MODULATION_LIMIT
0xFE55	SYNC
0xFE56	DUTY_BAL_EDGESEL
0xFE57	DOUBLE_UPD_RATE
0xFE58	VIN_SCALE_MONITOR
0xFE59	IIN_CAL_GAIN
0xFE5A	TSNS_SETTING
0xFE5B	AUTO_GO_CMD
0xFE5C	DIODE_EMULATION
0xFE5D	CS2_CONST_CUR_MODE
0xFE5E	NL_ERR_GAIN_FACTOR
0xFE5F	SR_SETTING
0xFE60	NOMINAL_TEMP_POLE

Command Code	Command Name
0xFE61	LOW_TEMP_POLE
0xFE62	LOW_TEMP_SETTING
0xFE63	GPIO3_4_SNUBBER_ON_TIME
0xFE64	GPIO3_4_SNUBBER_DELAY
0xFE65	VOUT_DROOP_SETTING
0xFE66	NL_BURST_MODE
0xFE67	HF_ADC_CONFIG
0xFE80	VS_TRIM
0xFE81	VFF_GAIN_TRIM
0xFE82	CS1_GAIN_TRIM
0xFE86	TSNS_EXTFWD_GAIN_TRIM
0xFE87	TSNS_EXTFWD_OFFSET_TRIM
0xFE88	TSNS_EXTREV_GAIN_TRIM
0xFE89	TSNS_EXTREV_OFFSET_TRIM
0xFE8C	FAULT_VOUT
0xFE8D	FAULT_IOUT
0xFE8E	FAULT_INPUT
0xFE8F	FAULT_TEMPERATURE

Command Code	Command Name
0xFE90	FAULT_CML
0xFE91	FAULT_OTHER
0xFE92	FAULT_MFR_SPECIFIC
0xFE93	FAULT_UNKNOWN
0xFE94	STATUS_UNKNOWN
0xFE95	FIRST_FAULT_ID
0xFE96	VFF_VALUE
0xFE97	VS_VALUE
0xFE98	CS1_VALUE
0xFE99	CS2_VALUE
0xFE9A	POUT_VALUE
0xFE9B	Reserved
0xFE9C	TSNS_EXTFWD_VALUE
0xFE9D	TSNS_EXTREV_VALUE
0xFE9F	MODULATION_VALUE
0xFEA0	ISHARE_VALUE
0xFEA3	ADD_ADC_VALUE

STANDARD PMBUS COMMAND DESCRIPTIONS

STANDARD PMBUS COMMANDS

OPERATION

The OPERATION command, in conjunction with the CTRL pin, is used to turn the device on and off. Illegal values are 11xxxxxx.

Table 14. Register 0x01—OPERATION

Bits	Bit Name	R/W	Description
[7:6]	Enable	R/W	These bits determine the device response to the OPERATION command. 00 = immediate off (no sequencing). 01 = soft off (power down according to the programmed TOFF_DELAY and TOFF_FALL). 10 = device on. 11 = reserved.
[5:0]	Reserved	R	Reserved.

ON_OFF_CONFIG

The ON_OFF_CONFIG command configures the combination of the CTRL pin input and the OPERATION command needed to turn the device on and off, including how the device responds when power is applied. Illegal values are xxx100xx.

Table 15. Register 0x02—ON_OFF_CONFIG

Bits	Bit Name	R/W	Description
[7:5]	Reserved	R	Reserved.
4	Power-up control	R/W	Sets the device power-up response. 0 = device powers up when power is present. 1 = device powers up only when commanded by the CTRL pin and the OPERATION command.
3	Command enable	R/W	Controls how the device responds to the OPERATION command. 0 = ignores OPERATION command. 1 = the OPERATION command must be set to 1 to enable the device (in addition to setting Bit 2).
2	Pin enable	R/W	Controls how the device responds to the value of the CTRL pin. 0 = ignores the CTRL pin. 1 = CTRL pin must be asserted to enable the device (in addition to setting Bit 3).
1	CTRL pin polarity	R/W	Sets the polarity of the CTRL pin. 0 = active low. 1 = active high.
0	CTRL pin power-down action	R/W	Actions to take on power-down when power-down is activated by the CTRL pin. 0 = uses the TOFF_DELAY and TOFF_FALL values to stop the transfer of energy to the output. 1 = turns off the output and stops energy transfer to the output as quickly as possible.

CLEAR_FAULTS

The CLEAR_FAULTS command is a send byte, no data. This command clears all fault bits in all PMBus status registers simultaneously.

Table 16. Register 0x03—CLEAR_FAULTS

Bits	Bit Name	Type	Description
N/A	CLEAR_FAULTS	Send	Clears all bits in the PMBus status registers (Register 0x78 to Register 0x7E) simultaneously.

WRITE_PROTECT

The WRITE_PROTECT command is used to protect the PMBus device against accidental writes. Reads to the device are allowed regardless of the setting of this command.

Table 17. Register 0x10—WRITE_PROTECT

Bits	Bit Name	R/W	Description
7	Write Protect 1	R/W	Setting this bit disables writes to all commands except WRITE_PROTECT.
6	Write Protect 2	R/W	Setting this bit disables writes to all commands except WRITE_PROTECT, OPERATION, and PAGE.
5	Write Protect 3	R/W	Setting this bit disables writes to all commands except WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND.
[4:0]	Reserved	R	Reserved.

RESTORE_DEFAULT_ALL

Table 18. Register 0x12—RESTORE_DEFAULT_ALL

Bits	Bit Name	Type	Description
N/A	RESTORE_DEFAULT_ALL	Send	This command downloads the factory default settings from the EEPROM into operating memory. It also resets the EEPROM password and the key code to their default values.

STORE_USER_ALL

Table 19. Register 0x15—STORE_USER_ALL

Bits	Bit Name	Type	Description
N/A	STORE_USER_ALL	Send	This command copies the entire contents of operating memory into the EEPROM (Page 1 of the main block) as the user settings.

RESTORE_USER_ALL

Table 20. Register 0x16—RESTORE_USER_ALL

Bits	Bit Name	Type	Description
N/A	RESTORE_USER_ALL	Send	This command downloads the stored user settings from EEPROM into operating memory.

CAPABILITY

This command allows host systems to determine the capabilities of the PMBus device (default value is 0xB0).

Table 21. Register 0x19—CAPABILITY

Bits	Bit Name	R/W	Description
7	Packet error checking	R	Checks packet error capability of the device. 1 = supported.
[6:5]	Maximum bus speed	R	Checks the PMBus speed capability of the device. 01 = maximum bus speed is 400 kHz.
4	$\overline{\text{SMBALRT}}$	R	Checks support for the $\overline{\text{SMBALRT}}$ pin and the SMBus Alert Response Address Protocol. 1 = supported.
[3:0]	Reserved	R	Reserved.

SMBALERT_MASK

Table 22. Register 0x1B—SMBALERT_MASK

Bits	Bit Name	R/W	Description
[15:8]	STATUS_x command code	W	Command code of the STATUS_x mask register to update.
[7:0]	Mask byte	W	Update mask register with this value.

VOUT_MODE

The VOUT_MODE command sets the data format for output voltage related data. The data byte for the VOUT_MODE command consists of a 3-bit mode and 5-bit exponent parameter. The 3-bit mode determines whether the device uses linear format or direct format for the output voltage related commands. The 5-bit parameter sets the exponent value for linear format. VOUT_MODE[7:5] must be equal to 000.

Table 23. Register 0x20—VOUT_MODE

Bits	Bit Name	R/W	Description
[7:5]	Mode	R	Returns the output voltage data format. The value is fixed at 000, which means that only linear data format is supported.
[4:0]	Exponent-N	R/W	Twos complement N exponent used in the output voltage related commands in linear data format ($V = Y \times 2^N$).

VOUT_COMMAND

The VOUT_COMMAND command sets the output voltage. Exponent N is set using VOUT_MODE[4:0]. Bits[7:5] must be equal to 000.

Table 24. Register 0x21—VOUT_COMMAND (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[15:0]	Mantissa-Y	R/W	16-bit unsigned integer Y value for linear data format ($V = Y \times 2^N$). N is defined using VOUT_MODE[4:0].

VOUT_TRIM

The VOUT_TRIM command applies a fixed offset voltage to the VOUT_COMMAND value.

Table 25. Register 0x22—VOUT_TRIM

Bits	Bit Name	R/W	Description
[15:0]	Offset trim	R/W	Twos complement integer used to apply a fixed offset voltage to the VOUT_COMMAND value.

VOUT_CAL_OFFSET

The VOUT_CAL_OFFSET command is used to apply a fixed offset voltage to the VOUT_COMMAND value.

Table 26. Register 0x23—VOUT_CAL_OFFSET

Bits	Bit Name	R/W	Description
[15:0]	Offset trim	R/W	Twos complement integer used to apply a fixed offset voltage to the VOUT_COMMAND value.

VOUT_MAX

The VOUT_MAX command sets an upper limit on the output voltage. Exponent N is set using VOUT_MODE[4:0].

Table 27. Register 0x24—VOUT_MAX

Bits	Bit Name	R/W	Description
[15:0]	Mantissa-Y	R/W	Sets the output voltage upper limit. 16-bit unsigned integer Y value for linear data format ($V = Y \times 2^N$).

VOUT_TRANSITION_RATE

When the device receives a VOUT_COMMAND or OPERATION command that causes the output voltage to change, this command sets the output transition rate (or slew rate), in mV/µs, at which the VS± pins change voltage.

Table 28. Register 0x27—VOUT_TRANSITION_RATE

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

VOUT_DROOP

The VOUT_DROOP command sets the rate, in mV/A, at which the output voltage decreases (or increases) with increasing (or decreasing) output current.

Table 29. Register 0x28—VOUT_DROOP

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

VOUT_SCALE_LOOP

The VOUT_SCALE_LOOP command sets the gain (K_R) by which the commanded voltage (V_{OUT}) is scaled to generate the internal reference voltage (V_{REF}). $V_{REF} = V_{OUT} \times K_R$, where $K_R = Y \times 2^N$.

Table 30. Register 0x29—VOUT_SCALE_LOOP

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

VOUT_SCALE_MONITOR

The VOUT_SCALE_MONITOR command sets the gain (K_{VOUT}) by which the sensed output voltage at the DUT (V_{OUT_DUT}) is scaled to generate the reading for the READ_VOUT command. READ_VOUT = $V_{OUT\_DUT} \times K_{VOUT}$, where $K_{VOUT} = Y \times 2^N$.

Table 31. Register 0x2A—VOUT_SCALE_MONITOR

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

FREQUENCY_SWITCH

The FREQUENCY_SWITCH command sets the switching frequency (in kHz) for the PMBus device. For a list of all supported switching frequencies, see Table 244.

Table 32. Register 0x33—FREQUENCY_SWITCH (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

VIN_ON

The VIN_ON command sets the value of the input voltage (V rms) at which the device starts power conversion. Setting VIN_ON = 0 effectively disables this function.

Table 33. Register 0x35—VIN_ON

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

VIN_OFF

The VIN_OFF command sets the value of the input voltage (V rms) at which the device stops power conversion. VIN_OFF is not checked until the device reaches the regulation voltage or TON_MAX has expired.

Table 34. Register 0x36—VIN_OFF

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

INTERLEAVE

The INTERLEAVE command is used to arrange multiple devices so that their switching periods can be distributed in time.

Table 35. Register 0x37—INTERLEAVE

Bits	Bit Name	R/W	Description
[15:12]	Reserved	R	Reserved.
[11:8]	Group ID number	R/W	Group identification number.
[7:4]	Number in group	R/W	Number of units in the group.
[3:0]	Interleave order	R/W	Interleave order for this unit. 0000 = 0 × 22.5° (0 × t_{SW}/16). 0001 = 1 × 22.5° (1 × t_{SW}/16). 0010 = 2 × 22.5° (2 × t_{SW}/16). 0011 = 3 × 22.5° (3 × t_{SW}/16). … 1111 = 15 × 22.5° (15 × t_{SW}/16).

IOUT_CAL_GAIN

The IOUT_CAL_GAIN command sets the ratio of the voltage at the current sense pins to the sensed current (in mΩ).

Table 36. Register 0x38—IOUT_CAL_GAIN

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

IOUT_CAL_OFFSET

The IOUT_CAL_OFFSET command is used to null any offsets in the output current sensing circuit (in amperes).

Table 37. Register 0x39—IOUT_CAL_OFFSET

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT command sets the upper voltage threshold (in volts) measured at the sense/output pin that causes an overvoltage fault condition. The exponent N is set using VOUT_MODE[4:0].

Table 38. Register 0x40—VOUT_OV_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:0]	Mantissa-Y	R/W	Unsigned Y-mantissa used in output voltage related commands in linear data format ($V = Y \times 2^N$).

VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE command instructs the device on the actions to take due to an output overvoltage fault. The device notifies the host and sets the VOUT_OV_FAULT bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the VOUT_OV_FAULT bit in the STATUS_VOUT register.

Table 39. Register 0x41—VOUT_OV_FAULT_RESPONSE

<table>
<tr><th>Bits</th><th>Bit Name</th><th>R/W</th><th colspan="4">Description</th></tr>
<tr><td rowspan="6">[7:6]</td><td rowspan="6">Response</td><td rowspan="6">R/W</td><td colspan="4">Determines the device response to an overvoltage fault condition.</td></tr>
<tr><td>Bit 7</td><td>Bit 6</td><td colspan="2">Response</td></tr>
<tr><td>0</td><td>0</td><td colspan="2">Do nothing.</td></tr>
<tr><td>0</td><td>1</td><td colspan="2">Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.</td></tr>
<tr><td rowspan="10">[5:3]</td><td rowspan="10">Retry setting</td><td rowspan="10">R/W</td><td colspan="4">Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.</td></tr>
<tr><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Number of Retries</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Infinite</td></tr>
<tr><td>[2:0]</td><td>Delay time</td><td>R/W</td><td colspan="4">Number of delay time units (see Register 0xFE3E).</td></tr>
</table>

VOUT_OV_WARN_LIMIT

The VOUT_OV_WARN_LIMIT command sets the upper voltage threshold (in volts) measured at the sense/output pin that causes an overvoltage warning condition. The exponent N is set using VOUT_MODE[4:0]. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the VOUT_OV_WARNING bit in the STATUS_VOUT register.

Table 40. Register 0x42—VOUT_OV_WARN_LIMIT

Bits	Bit Name	R/W	Description
[15:0]	Mantissa-Y	R/W	Unsigned Y-mantissa used in output voltage related commands in linear data format ($V = Y \times 2^N$).

VOUT_UV_WARN_LIMIT

The VOUT_UV_WARN_LIMIT command sets the lower voltage threshold (in volts) measured at the sense/output pin that causes an undervoltage warning condition. The exponent N is set using VOUT_MODE[4:0]. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the VOUT_UV_WARNING bit in the STATUS_VOUT register.

Table 41. Register 0x43—VOUT_UV_WARN_LIMIT

Bits	Bit Name	R/W	Description
[15:0]	Mantissa-Y	R/W	Unsigned Y-mantissa used in output voltage related commands in linear data format ($V = Y \times 2^N$).

VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT command sets the threshold value (in volts) measured at the sense/output pin that causes an undervoltage fault condition. The exponent N is set using VOUT_MODE[4:0].

Table 42. Register 0x44—VOUT_UV_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:0]	Mantissa-Y	R/W	Unsigned Y-mantissa used in output voltage related commands in linear data format ($V = Y \times 2^N$).

VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE command instructs the device on actions to take due to an output undervoltage fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the VOUT_UV_FAULT bit in the STATUS_VOUT register.

Table 43. Register 0x45—VOUT_UV_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to an undervoltage fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Do nothing.	
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].	
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).	
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).			

IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the threshold value (in amperes) measured at the sense pins that causes an overcurrent fault condition.

Table 44. Register 0x46—IOUT_OC_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE command instructs the device on actions to take due to an output overcurrent fault condition. The device notifies the host and sets the IOUT_OC_FAULT bit in the STATUS_BYTE register, the IOUT bit in the STATUS_WORD register, and the IOUT_OC_FAULT bit in the STATUS_IOUT register.

Table 45. Register 0x47—IOUT_OC_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to an overcurrent fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT.	
			0	1	Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT. If V_{OUT} falls below the IOUT_OC_LV_FAULT_LIMIT, respond as programmed by the retry setting (Bits[5:3]).	
			1	0	Continue operation in current limiting mode for the delay time (Bits[2:0]). If the device is still in current limiting mode, respond as programmed by the retry setting (Bits[5:3]).	
			1	1	Shut down, disable the output, and respond as programmed by the retry setting (Bits[5:3]).	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).			

IOUT_OC_LV_FAULT_LIMIT

The IOUT_OC_LV_FAULT_LIMIT command sets the lower voltage threshold (in volts) measured at the sense/output pin that causes an undervoltage-in-CLM fault condition. This limit applies only when the device is operating in current limiting mode (CLM).

Table 46. Register 0x48—IOUT_OC_LV_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:0]	Mantissa-Y	R/W	Unsigned Y-mantissa used in output voltage related commands in linear data format ($V = Y \times 2^N$). N is specified by VOUT_MODE[4:0].

IOUT_OC_LV_FAULT_RESPONSE

The IOUT_OC_LV_FAULT_RESPONSE command instructs the device on actions to take due to an output undervoltage-in-CLM fault condition. The device notifies the host and sets the IOUT_OC_FAULT bit in the STATUS_BYTE register, the IOUT bit in the STATUS_WORD register, and the IOUT_OC_LV_FAULT bit in the STATUS_IOUT register.

Table 47. Register 0x49—IOUT_OC_LV_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to an undervoltage-in-CLM fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Do nothing.	
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].	
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).	
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).			

IOUT_OC_WARN_LIMIT

The IOUT_OC_WARN_LIMIT command sets the current (in amperes) measured at the sense/output pin that causes an overcurrent warning condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the IOUT bit in the STATUS_WORD register, and the IOUT_OC_WARNING bit in the STATUS_IOUT register.

Table 48. Register 0x4A—IOUT_OC_WARN_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

IOUT_UC_FAULT_LIMIT

The IOUT_UC_FAULT_LIMIT command sets the current (in amperes) measured at the sense/output pin that causes an undercurrent fault condition.

Table 49. Register 0x4B—IOUT_UC_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

IOUT_UC_FAULT_RESPONSE

The IOUT_UC_FAULT_RESPONSE command instructs the device on actions to take due to an output undercurrent fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the IOUT bit in the STATUS_WORD register, and the IOUT_UC_FAULT bit in the STATUS_IOUT register.

Table 50. Register 0x4C—IOUT_UC_FAULT_RESPONSE

<table>
<tr><th>Bits</th><th>Bit Name</th><th>R/W</th><th colspan="4">Description</th></tr>
<tr><td rowspan="6">[7:6]</td><td rowspan="6">Response</td><td rowspan="6">R/W</td><td colspan="4">Determines the device response to an undercurrent fault condition.</td></tr>
<tr><td>Bit 7</td><td>Bit 6</td><td colspan="2">Response</td></tr>
<tr><td>0</td><td>0</td><td colspan="2">Do nothing.</td></tr>
<tr><td>0</td><td>1</td><td colspan="2">Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT. If V_{OUT} falls below the IOUT_OC_LV_FAULT_LIMIT, respond as programmed by the retry setting (Bits[5:3]).</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">Continue operation in current limiting mode for the delay time (Bits[2:0]). If the device is still in current limiting mode, respond as programmed by the retry setting (Bits[5:3]).</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">Shut down, disable the output, and respond as programmed by the retry setting (Bits[5:3]).</td></tr>
<tr><td rowspan="10">[5:3]</td><td rowspan="10">Retry setting</td><td rowspan="10">R/W</td><td colspan="4">Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.</td></tr>
<tr><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Number of Retries</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Infinite</td></tr>
<tr><td>[2:0]</td><td>Delay times</td><td>R/W</td><td colspan="4">Number of delay time units (see Register 0xFE3E).</td></tr>
</table>

OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the threshold value (in °C) that causes an overtemperature fault condition.

Table 51. Register 0x4F—OT_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE command instructs the device on actions to take due to an overtemperature fault condition. The device notifies the host and sets the TEMPERATURE bit in the STATUS_BYTE register and the OT_FAULT bit in the STATUS_TEMPERATURE register.

Table 52. Register 0x50—OT_FAULT_RESPONSE

<table>
<tr><th>Bits</th><th>Bit Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>[7:6]</td><td>Response</td><td>R/W</td><td>Determine the device response to an overtemperature fault condition.
<table>
<tr><th>Bit 7</th><th>Bit 6</th><th>Response</th></tr>
<tr><td>0</td><td>0</td><td>Do nothing.</td></tr>
<tr><td>0</td><td>1</td><td>Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].</td></tr>
<tr><td>1</td><td>0</td><td>Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).</td></tr>
<tr><td>1</td><td>1</td><td>Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.</td></tr>
</table></td></tr>
<tr><td>[5:3]</td><td>Retry setting</td><td>R/W</td><td>Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.
<table>
<tr><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Number of Retries</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Infinite</td></tr>
</table></td></tr>
<tr><td>[2:0]</td><td>Delay times</td><td>R/W</td><td>Number of delay time units (see Register 0xFE3E).</td></tr>
</table>

OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the threshold value (in °C) for an overtemperature warning condition. The device notifies the host and sets the TEMPERATURE bit in the STATUS_BYTE register and the OT_WARNING bit in the STATUS_TEMPERATURE register.

Table 53. Register 0x51—OT_WARN_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the upper voltage threshold (in volts) measured at the sense/input pin that causes an overvoltage fault condition.

Table 54. Register 0x55—VIN_OV_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on the actions to take due to an input overvoltage fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the INPUT bit in the STATUS_WORD register, and the VIN_OV_FAULT bit in the STATUS_INPUT register.

Table 55. Register 0x56—VIN_OV_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to an input overvoltage fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Do nothing.	
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].	
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).	
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).			

VIN_UV_FAULT_LIMIT

The VIN_UV_FAULT_LIMIT command sets the lower voltage threshold (in volts) measured at the sense/input pin that causes an undervoltage fault condition.

Table 56. Register 0x59—VIN_UV_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

VIN_UV_FAULT_RESPONSE

The VIN_UV_FAULT_RESPONSE command instructs the device on the actions to take due to an input undervoltage fault condition. The device notifies the host and sets the VIN_UV_FAULT bit in the STATUS_BYTE register, the INPUT bit in the STATUS_WORD register, and the VIN_UV_FAULT bit in the STATUS_INPUT register.

Table 57. Register 0x5A—VIN_UV_FAULT_RESPONSE

Bits	Bit Name	R/W	Description		
[7:6]	Response	R/W	Determines the device response to an input undervoltage fault condition.		
			Bit 7	**Bit 6**	**Response**
			0	0	Do nothing.
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.

Bits	Bit Name	R/W	Description
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.
			Bit 5 / Bit 4 / Bit 3: Number of Retries
			0 / 0 / 0: 0
			0 / 0 / 1: 1
			0 / 1 / 0: 2
			0 / 1 / 1: 3
			1 / 0 / 0: 4
			1 / 0 / 1: 5
			1 / 1 / 0: 6
			1 / 1 / 1: Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).

IIN_OC_FAULT_LIMIT

The IIN_OC_FAULT_LIMIT command sets the threshold value (in amperes) measured at the sense/input pin that causes an overcurrent fault condition.

Table 58. Register 0x5B—IIN_OC_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

IIN_OC_FAULT_RESPONSE

The IIN_OC_FAULT_RESPONSE command instructs the device on actions to take due to an input overcurrent fault condition. The device notifies the host and sets the OTHER bit in the STATUS_BYTE register, the INPUT bit in the STATUS_WORD register, and the IIN_OC_FAULT bit in the STATUS_INPUT register.

Table 59. Register 0x5C—IIN_OC_FAULT_RESPONSE

Bits	Bit Name	R/W	Description
[7:6]	Response	R/W	Determines the device response to an input overcurrent fault condition.
			Bit 7 / Bit 6: Response
			0 / 0: Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT.
			0 / 1: Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT. If V_{OUT} falls below the IOUT_OC_LV_FAULT_LIMIT, respond as programmed by the retry setting (Bits[5:3]).
			1 / 0: Continue operation in current limiting mode for the delay time (Bits[2:0]). If the device is still in current limiting mode, respond as programmed by the retry setting (Bits[5:3]).
			1 / 1: Shut down, disable the output, and respond as programmed by the retry setting (Bits[5:3]).
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.
			Bit 5 / Bit 4 / Bit 3: Number of Retries
			0 / 0 / 0: 0
			0 / 0 / 1: 1
			0 / 1 / 0: 2
			0 / 1 / 1: 3
			1 / 0 / 0: 4
			1 / 0 / 1: 5
			1 / 1 / 0: 6
			1 / 1 / 1: Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).

POWER_GOOD_ON

The POWER_GOOD_ON command sets the output voltage (in volts) at which the POWER_GOOD signal is asserted.

Table 60. Register 0x5E—POWER_GOOD_ON

Bits	Bit Name	R/W	Description
[15:0]	Mantissa-Y	R/W	Unsigned Y-mantissa used in output voltage related commands in linear data format ($V = Y \times 2^N$).

POWER_GOOD_OFF

The POWER_GOOD_OFF command sets the output voltage (in volts) at which the POWER_GOOD signal is deasserted.

Table 61. Register 0x5F—POWER_GOOD_OFF

Bits	Bit Name	R/W	Description
[15:0]	Mantissa-Y	R/W	Unsigned Y-mantissa used in output voltage related commands in linear data format ($V = Y \times 2^N$).

TON_DELAY

The TON_DELAY command sets the turn-on delay time in milliseconds (ms) from start (ON_OFF_CONFIG) until V_{OUT} starts to rise. The range is 0 ms to 1023 ms, in steps of 1 ms. The calculated value is rounded down.

Table 62. Register 0x60—TON_DELAY

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

TON_RISE

The TON_RISE command sets the rise time (in ms) from when V_{OUT} starts to rise until the voltage enters the regulation band.

Table 63. Register 0x61—TON_RISE

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

TON_MAX_FAULT_LIMIT

The TON_MAX_FAULT_LIMIT command sets the upper time threshold (in ms) from power-up to the VOUT_UV_FAULT limit.

Table 64. Register 0x62—TON_MAX_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

TON_MAX_FAULT_RESPONSE

The TON_MAX_FAULT_RESPONSE command instructs the device on the actions to take due to a TON_MAX fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the TON_MAX_FAULT bit in the STATUS_VOUT register.

Table 65. Register 0x63—TON_MAX_FAULT_RESPONSE

Bits	Bit Name	R/W	Description		
[7:6]	Response	R/W	Determines the device response to a TON_MAX fault condition.		
			Bit 7	**Bit 6**	**Response**
			0	0	Do nothing.
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.

Bits	Bit Name	R/W	Description			
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).			

TOFF_DELAY

The TOFF_DELAY command sets the turn-off delay time in milliseconds (ms) from stop (ON_OFF_CONFIG) until the device stops transferring energy to the output. The range is 0 ms to 1023 ms, in steps of 1 ms. The calculated value is rounded down.

Table 66. Register 0x64—TOFF_DELAY

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

TOFF_FALL

The TOFF_FALL command sets the fall time (in ms) from the end of the turn-off delay time to voltage = 0 V.

Table 67. Register 0x65—TOFF_FALL

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

TOFF_MAX_WARN_LIMIT

The TOFF_MAX_WARN_LIMIT command sets the upper time threshold (in ms) that causes a TOFF_MAX warning condition, that is, the time it takes to power down the output voltage from V_{OUT} to 12.5% of V_{OUT}. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE register, the VOUT bit in the STATUS_WORD register, and the TOFF_MAX_WARNING bit in the STATUS_VOUT register.

Table 68. Register 0x66—TOFF_MAX_WARN_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

POUT_OP_FAULT_LIMIT

The POUT_OP_FAULT_LIMIT command sets the upper power threshold (in watts) measured at the sense/output pin that causes an output overpower fault condition.

Table 69. Register 0x68—POUT_OP_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

POUT_OP_FAULT_RESPONSE

The POUT_OP_FAULT_RESPONSE command instructs the device on the actions to take due to an output overpower fault condition. The device notifies the host and sets the IOUT_OC_FAULT bit in the STATUS_BYTE register, the IOUT/POUT bit in the STATUS_WORD register, and the POUT_OP_FAULT bit in the STATUS_IOUT register.

Table 70. Register 0x69—POUT_OP_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to an overpower fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Do nothing.	
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].	
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).	
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).			

STATUS_BYTE

The STATUS_BYTE register returns the lower byte of the STATUS_WORD register. A value of 1 in this command indicates that a fault has occurred. As per the PMBus standard, the BUSY bit is writable to allow the user to clear that latched bit using a write command with a 1 to Bit 7, similar to other STATUS_xxx commands. The other bits in this register cannot be cleared with a write to the STATUS_BYTE command, but should be cleared with a write to the STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMP, or STATUS_CML command.

Table 71. Register 0x78—STATUS_BYTE

Bits	Bit Name	R/W	Description
7	BUSY	R/W	This bit is asserted if the device is busy and unable to respond.
6	POWER_OFF	R	This bit is asserted if the unit is not providing power to the output.
5	VOUT_OV_FAULT	R	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	R	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	R	An input undervoltage fault has occurred.
2	TEMPERATURE	R	A temperature fault or warning has occurred.
1	CML	R	A communications, memory, or logic fault has occurred.
0	NONE_OF_THE_ABOVE	R	A fault or warning not listed in Bits[7:1] has occurred.

STATUS_WORD

The STATUS_WORD register returns the upper and lower bytes of the STATUS_WORD command. A value of 1 in this command indicates that a fault has occurred.

Table 72. Register 0x79—STATUS_WORD

Bits	Bit Name	R/W	Description
15	VOUT	R	Output voltage fault or warning. A bit in STATUS_VOUT is set.
14	IOUT/POUT	R	Output current or output power fault or warning. A bit in STATUS_IOUT is set.
13	INPUT	R	Input voltage, input current, or input power fault or warning. A bit in STATUS_INPUT is set.
12	MFR	R	Manufacturer-specific fault or warning.
11	$\overline{\text{POWER\_GOOD}}$	R	$\overline{\text{POWER\_GOOD}}$ is a negation of POWER_GOOD, which means that the output power is not good. This bit is set when the sensed V_{OUT} is less than the limit programmed in the POWER_GOOD_OFF command.
10	FANS	R	Not supported.
9	OTHER	R	A bit in STATUS_OTHER is set.
8	UNKNOWN	R	A fault or warning not listed in STATUS_WORD[15:1].
7	BUSY	R/W	This bit is asserted if the device is busy and unable to respond.
6	POWER_OFF	R	This bit is asserted if the unit is not providing power to the output.
5	VOUT_OV_FAULT	R	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	R	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	R	An input undervoltage fault has occurred.
2	TEMPERATURE	R	A temperature fault or warning has occurred.
1	CML	R	A communications, memory, or logic fault has occurred.
0	NONE_OF_THE_ABOVE	R	A fault or warning not listed in Bits[7:1] has occurred.

STATUS_VOUT

The STATUS_VOUT register returns the status of the output voltage. A value of 1 in this command indicates that a fault has occurred.

Table 73. Register 0x7A—STATUS_VOUT

Bits	Bit Name	R/W	Description
7	VOUT_OV_FAULT	R/W	An output overvoltage fault has occurred.
6	VOUT_OV_WARN	R/W	An output overvoltage warning has occurred.
5	VOUT_UV_WARN	R/W	An output undervoltage warning has occurred.
4	VOUT_UV_FAULT	R/W	An output undervoltage fault has occurred.
3	VOUT_MAX_WARN	R/W	An attempt was made to set the output voltage to a value greater than the VOUT_MAX command.
2	TON_MAX_FAULT	R/W	The device took too long to power up without reaching the VOUT_UV fault limit.
1	TOFF_MAX_WARN	R/W	The device took too long to power down to 12.5% of its output voltage.
0	VOUT_TRACKING_ERR	R	Not supported.

STATUS_IOUT

The STATUS_IOUT register returns the status of the output current. A value of 1 in this command indicates that a fault has occurred.

Table 74. Register 0x7B—STATUS_IOUT

Bits	Bit Name	R/W	Description
7	IOUT_OC_FAULT	R/W	An output overcurrent fault has occurred.
6	IOUT_OC_LV_FAULT	R/W	An output overcurrent fault and a low voltage fault have occurred.
5	IOUT_OC_WARN	R/W	An output overcurrent warning has occurred.
4	IOUT_UC_FAULT	R/W	An output undercurrent fault has occurred.
3	ISHARE_FAULT	R/W	A current sharing fault has occurred.
2	PLIM_MODE	R	Not supported.
1	POUT_OP_FAULT	R/W	An output overpower fault has occurred.
0	POUT_OP_WARN	R	Not supported.

STATUS_INPUT

The STATUS_INPUT register returns the status of the input. A value of 1 in this command indicates that a fault has occurred.

Table 75. Register 0x7C—STATUS_INPUT

Bits	Bit Name	R/W	Description
7	VIN_OV_FAULT	R/W	An input overvoltage fault has occurred.
6	VIN_OV_WARN	R	Not supported.
5	VIN_UV_WARN	R	Not supported.
4	VIN_UV_FAULT	R/W	An input undervoltage fault has occurred.
3	VIN_LOW	R/W	The device is off due to insufficient input voltage; that is, the input voltage is below the turn-off threshold.
2	IIN_OC_FAULT	R/W	An input overcurrent fault has occurred.
1	IIN_OC_WARN	R	Not supported.
0	PIN_OP_WARN	R	Not supported.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE register returns temperature status. A value of 1 in this command indicates that a fault has occurred.

Table 76. Register 0x7D—STATUS_TEMPERATURE

Bits	Bit Name	R/W	Description
7	OT_FAULT	R/W	An overtemperature fault has occurred.
6	OT_WARN	R/W	An overtemperature warning has occurred.
5	UT_WARN	R	Not supported.
4	UT_FAULT	R	Not supported.
[3:0]	Reserved	R	Reserved.

STATUS_CML

The STATUS_CML register returns communications, memory, and logic (CML) status. A value of 1 in this command indicates that a fault has occurred.

Table 77. Register 0x7E—STATUS_CML

Bits	Bit Name	R/W	Description
7	CMD_ERR	R/W	Invalid or unsupported command received.
6	DATA_ERR	R/W	Invalid or unsupported data received.
5	PEC_ERR	R/W	Packet error check failed.
4	CRC_ERR	R/W	Memory fault detected (for example, a CRC error).
3	PROC_ERR	R	Not supported.
2	Reserved	R	Reserved.
1	COMM_ERR	R/W	Other communication fault not specified by Bits[7:2].
0	MEM_ERR	R/W	Other memory or logic fault not specified by Bits[7:2]. This bit is set if the black box record number has been reached (Register 0xFE48[2]).

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC register returns the status of manufacturer specific faults. A value of 1 in this command indicates that a fault has occurred.

Table 78. Register 0x80—STATUS_MFR_SPECIFIC

Bits	Bit Name	R/W	Description
7	GPIO4_FAULT	R/W	GPIO4 fault received.
6	GPIO3_FAULT	R/W	GPIO3 fault received.
5	GPIO2_FAULT	R/W	GPIO2 fault received.
4	GPIO1_FAULT	R/W	GPIO1 fault received.
3	IIN_OC_FAST_FAULT	R/W	Fast input overcurrent fault received.
2	IOUT_UC_FAST_FAULT	R/W	Fast output reverse current fault received.
1	IOUT_OC_FAST_FAULT	R/W	Fast output overcurrent current fault received.
0	VOUT_OV_FAST_FAULT	R/W	Fast output overvoltage fault received.

READ_VIN

The READ_VIN command returns the input voltage value (V) in linear data format ($X = Y \times 2^N$).

Table 79. Register 0x88—READ_VIN

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

READ_IIN

The READ_IIN command returns the input current value (A) in linear data format ($X = Y \times 2^N$).

Table 80. Register 0x89—READ_IIN

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

READ_VOUT

The READ_VOUT command returns the output voltage value (V) in linear data format ($V = Y \times 2^N$). Exponent N is set using VOUT_MODE[4:0].

Table 81. Register 0x8B—READ_VOUT

Bits	Bit Name	R/W	Description
[15:0]	Mantissa-Y	R	Unsigned Y-mantissa used in output voltage related commands in linear data format ($V = Y \times 2^N$).

READ_IOUT

The READ_IOUT command returns the output current value (A) in linear data format ($V = Y \times 2^N$).

Table 82. Register 0x8C—READ_IOUT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

Reserved

This register is reserved.

Table 83. Register 0x8D—Reserved

Bits	Bit Name	R/W	Description
[15:0]	Reserved	R	Reserved.

READ_TEMPERATURE_2

The READ_TEMPERATURE_2 command returns the External 1 (forward diode) temperature (°C) in linear data format ($X = Y \times 2^N$).

Table 84. Register 0x8E—READ_TEMPERATURE_2

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

READ_TEMPERATURE_3

The READ_TEMPERATURE_3 command returns the External 2 (reverse diode) temperature (°C) in linear data format ($X = Y \times 2^N$).

Table 85. Register 0x8F—READ_TEMPERATURE_3

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

READ_DUTY_CYCLE

The READ_DUTY_CYCLE command returns the duty cycle (%) in linear data format ($X = Y \times 2^N$).

Table 86. Register 0x94—READ_DUTY_CYCLE

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

READ_FREQUENCY

The READ_FREQUENCY command returns the actual switching frequency value (kHz) in linear data format ($X = Y \times 2^N$).

Table 87. Register 0x95—READ_FREQUENCY

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

READ_POUT

The READ_POUT command returns the output power (W) in linear data format ($X = Y \times 2^N$).

Table 88. Register 0x96—READ_POUT

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

PMBUS_REVISION

The PMBUS_REVISION command returns the PMBus version information. The ADP1055 is compliant with PMBus Revision 1.2. Reading this command results in a value of 0x22.

Table 89. Register 0x98—PMBUS_REVISION

Bits	Bit Name	R/W	Description
[7:4]	Part 1 revision	R	Compliant to PMBus Part 1 specification: 0010 = Revision 1.2.
[3:0]	Part 2 revision	R	Compliant to PMBus Part 2 specification: 0010 = Revision 1.2.

MFR_ID

The MFR_ID register stores the manufacturer ID. This register can store 23 bytes.

Table 90. Register 0x99—MFR_ID

Bits	Bit Name	R/W	Description
[7:0]	MFR_ID	Block read/write	Return the manufacturer's ID.

MFR_MODEL

The MFR_MODEL register stores the manufacturer model number. This register can store 19 bytes.

Table 91. Register 0x9A—MFR_MODEL

Bits	Bit Name	R/W	Description
[7:0]	Model	Block read/write	Return the manufacturer's model number.

MFR_REVISION

The MFR_REVISION register stores the manufacturer revision number. This register can store 23 bytes.

Table 92. Register 0x9B—MFR_REVISION

Bits	Bit Name	R/W	Description
[7:0]	Revision	Block read/write	Return the manufacturer's revision number.

MFR_LOCATION

The MFR_LOCATION register stores the manufacturer location. This register can store nine bytes.

Table 93. Register 0x9C—MFR_LOCATION

Bits	Bit Name	R/W	Description
[7:0]	Location	Block read/write	Return the manufacturer's location.

MFR_DATE

The MFR_DATE register stores the manufacturer date. This register can store 11 bytes.

Table 94. Register 0x9D—MFR_DATE

Bits	Bit Name	R/W	Description
[7:0]	Date	Block read/write	Return the manufacturer's date.

MFR_SERIAL

The MFR_SERIAL register stores the manufacturer serial number. This register can store 13 bytes.

Table 95. Register 0x9E—MFR_SERIAL

Bits	Bit Name	R/W	Description
[7:0]	Serial No	Block read/write	Return the manufacturer's serial number.

IC_DEVICE_ID

The IC_DEVICE_ID register stores the ID and device number of the ADP1055. The default values are 0x02, 0x41, 0x55.

Table 96. Register 0xAD—IC_DEVICE_ID

Bits	Bit Name	R/W	Description
[7:0]	Revision	Block read/write	Return the IC's ID and device number: 0x02, 0x41, 0x55.

IC_DEVICE_REV

The IC_DEVICE_REV register stores the device revision number of the ADP1055. The default values are 0x01 and 0xREV.

Table 97. Register 0xAE—IC_DEVICE_REV

Bits	Bit Name	R/W	Description
[7:0]	Revision	Block read/write	Device revision number: 0x01 0x11.

EEPROM_PAGE_00 Through EEPROM_PAGE_15 Commands

Register 0xB0 through Register 0xBF are read/write block commands. The EEPROM_PAGE_00 through EEPROM_PAGE_15 commands are used to read data from the EEPROM (Page 0 through Page 15) and to write data to the EEPROM (Page 6 through Page 15). For example, EEPROM_PAGE_07 reads from and writes to Page 7 of the EEPROM main block; EEPROM_PAGE_11 reads from and writes to Page 11 of the EEPROM main block. For more information, see the EEPROM section.

EEPROM_PAGE_00

Table 98. Register 0xB0—EEPROM_PAGE_00

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_00	Block read	Reserved by manufacturer for storing the default settings.

EEPROM_PAGE_01

Table 99. Register 0xB1—EEPROM_PAGE_01

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_01	Block read	Reserved by manufacturer for storing the user settings.

EEPROM_PAGE_02

Table 100. Register 0xB2—EEPROM_PAGE_02

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_02	Block read	Reserved by manufacturer for storing black box information.

EEPROM_PAGE_03

Table 101. Register 0xB3—EEPROM_PAGE_03

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_03	Block read	Reserved by manufacturer for storing black box information.

EEPROM_PAGE_04

Table 102. Register 0xB4—EEPROM_PAGE_04

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_04	Block read	Reserved by manufacturer for storing GUI settings.

EEPROM_PAGE_05

Table 103. Register 0xB5—EEPROM_PAGE_05

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_05	Block read	Reserved by manufacturer for storing factory tracking settings.

EEPROM_PAGE_06

Table 104. Register 0xB6—EEPROM_PAGE_06

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_06	Block read/write	Block read/write of Page 6 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_PAGE_07

Table 105. Register 0xB7—EEPROM_PAGE_07

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_07	Block read/write	Block read/write of Page 7 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_PAGE_08

Table 106. Register 0xB8—EEPROM_PAGE_08

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_08	Block read/write	Block read/write of Page 8 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_PAGE_09

Table 107. Register 0xB9—EEPROM_PAGE_09

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_09	Block read/write	Block read/write of Page 9 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_PAGE_10

Table 108. Register 0xBA—EEPROM_PAGE_10

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_10	Block read/write	Block read/write of Page 10 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_PAGE_11

Table 109. Register 0xBB—EEPROM_PAGE_11

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_11	Block read/write	Block read/write of Page 11 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_PAGE_12

Table 110. Register 0xBC—EEPROM_PAGE_12

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_12	Block read/write	Block read/write of Page 12 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_PAGE_13

Table 111. Register 0xBD—EEPROM_PAGE_13

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_13	Block read/write	Block read/write of Page 13 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_PAGE_14

Table 112. Register 0xBE—EEPROM_PAGE_14

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_14	Block read/write	Block read/write of Page 14 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_PAGE_15

Table 113. Register 0xBF—EEPROM_PAGE_15

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_PAGE_15	Block read/write	Block read/write of Page 15 of the EEPROM main block. The EEPROM must first be unlocked.

SLV_ADDR_SELECT

On first power-up, a read to this command using the general call address (0x00) returns the I^2C slave address of the ADP1055. Any subsequent writes to this register overwrite this information.

Table 114. Register 0xD0—SLV_ADDR_SELECT

Bits	Bit Name	R/W	Description
[7:6]	Reserved	R	Returns 01.
[5:4]	Address, high byte	R/W	00 = 0x40 to 0x4F (default address set by selecting resistor on the ADD pin). 01 = 0x50 to 0x5F. 10 = 0x60 to 0x6F. 11 = 0x70 to 0x7F.
[3:0]	Address, low byte	R/W	Low byte of slave address (determined by the resistor value on the ADD pin).

EEPROM_CRC_CHKSUM

Table 115. Register 0xD1—EEPROM_CRC_CHKSUM

Bits	Bit Name	R/W	Description
[7:0]	CRC checksum	R	Return the CRC checksum value from the EEPROM download operation.

EEPROM_NUM_RD_BYTES

Table 116. Register 0xD2—EEPROM_NUM_RD_BYTES

Bits	Bit Name	R/W	Description
[7:0]	Number of read bytes returned	R/W	Set the number of read bytes returned when using the EEPROM_PAGE_xx commands.

EEPROM_ADDR_OFFSET

Table 117. Register 0xD3—EEPROM_ADDR_OFFSET

Bits	Bit Name	R/W	Description
[15:0]	Address offset	R/W	Sets the address offset of the current EEPROM page.

EEPROM_PAGE_ERASE

Table 118. Register 0xD4—EEPROM_PAGE_ERASE

Bits	Bit Name	R/W	Description
[7:0]	Page erase	W	Perform a page erase on the selected EEPROM page (Page 6 to Page 15). Wait 35 ms after each page erase operation. The EEPROM must first be unlocked. Page 0 to Page 5 are reserved and their contents must not be erased.

EEPROM_PASSWORD

Table 119. Register 0xD5—EEPROM_PASSWORD

Bits	Bit Name	R/W	Description
[7:0]	EEPROM password	W	Write the password to this register two consecutive times to unlock the EEPROM and/or to change the EEPROM password. The factory default password is 0xFF. To lock the EEPROM, type any value other than the password to this register.

TRIM_PASSWORD

Table 120. Register 0xD6—TRIM_PASSWORD

Bits	Bit Name	R/W	Description
[7:0]	Trim password	W	Write the password to this register to unlock the trim registers for write access. Write the trim password twice to unlock the register; write any other value to exit. The trim password is the same as the EEPROM password (0xFF).

KEY_CODE

Table 121. Register 0xD7—KEY_CODE

Bits	Bit Name	R/W	Description
[31:0]	Keycode	Block read/ write	Write the 32-bit keycode to this command to unlock access to Command 0xF4 and Command 0xF5. Write the key code password twice to unlock the commands; write any other value to lock them. The factory default password is 0xFFFFFFFF. The procedure includes a block write of four bytes. The readback returns five bytes; the fifth byte is 0 if locked or 1 if unlocked.

EEPROM_INFO

Table 122. Register 0xF1—EEPROM_INFO

Bits	Bit Name	R/W	Description
[7:0]	EEPROM_INFO	Block read	Block read of the manufacturer data in the EEPROM.

READ_BLACKBOX_CURR

Table 123. Register 0xF2—READ_BLACKBOX_CURR

Bits	Bit Name	R/W	Description
VAR		Block read	This command returns the data for the current record N (last record saved in the black box). For information about the contents of the black box record, see the Black Box Contents section.

READ_BLACKBOX_PREV

Table 124. Register 0xF3—READ_BLACKBOX_PREV

Bits	Bit Name	R/W	Description
VAR		Block read	This command returns the data for the previous record N − 1 (next-to-last record saved in the black box). For information about the contents of the black box record, see the Black Box Contents section.

CMD_MASK

The CMD_MASK command allows any PMBus command to be masked in the ADP1055. If the command is masked, a read or a write to that command results in a no acknowledge (NACK). The STORE_USER_ALL (Register 0x15) and RESTORE_USER_ALL (Register 0x16) commands are not maskable.

Table 125. Register 0xF4—CMD_MASK

Bits	Bit Name	R/W	Description
VAR	Command masking	Block read/write	This command can be used to disable (mask) any of the standard PMBus commands (Command 0x01 to Command 0xFF). To use this command, the correct key code must be written. Block count = 0x20 (32 bytes) Mask[255:0] = Masking status bits. [0] = Command 0x00. … [255] = Command 0xFF.

EXTCMD_MASK

The EXTCMD_MASK command allows any manufacturer specific command to be masked in the ADP1055. If the command is masked, a read or a write to that command results in a no acknowledge (NACK).

Table 126. Register 0xF5—EXTCMD_MASK

Bits	Bit Name	R/W	Description
VAR	Command masking	Block read/write	This command can be used to disable (mask) any of the manufacturer specific PMBus commands (Command 0xFE00 to Command 0xFEA3). To use this command, the correct key code must be written. Block count = 0x15 (21 bytes) Mask[167:0] = Masking status bits. [0] = Command 0xFE00. … [167] = Command 0xFEA7.

MANUFACTURER SPECIFIC PMBUS COMMAND DESCRIPTIONS

Table 127. Register 0xFE00—GO_CMD

Bits	Bit Name	R/W	Description
7	Reserved	R/W	Reserved.
6	SYNC	W	This bit latches Register 0xFE55.
5	VFF	W	This bit latches Register 0xFE29.
4	Double update rate, VS balance	W	This bit latches Register 0xFE57 and Register 0xFE25.
3	Filter GO	W	This bit latches Register 0xFE4A, Register 0xFE01 to Register 0xFE0C, Register 0xFE5E, and Register 0xFE66.
2	Frequency GO	W	Update switching frequency programmed by FREQUENCY_SWITCH command (Register 0x33).
1	PWM GO	W	Update Register 0xFE0D to Register 0xFE1C, Register 0xFE1F to Register 0xFE24, and Register 0xFE15 to Register 0xFE1C
0	Voltage reference GO	W	Update reference voltage commanded by the VOUT_COMMAND (Register 0x21).

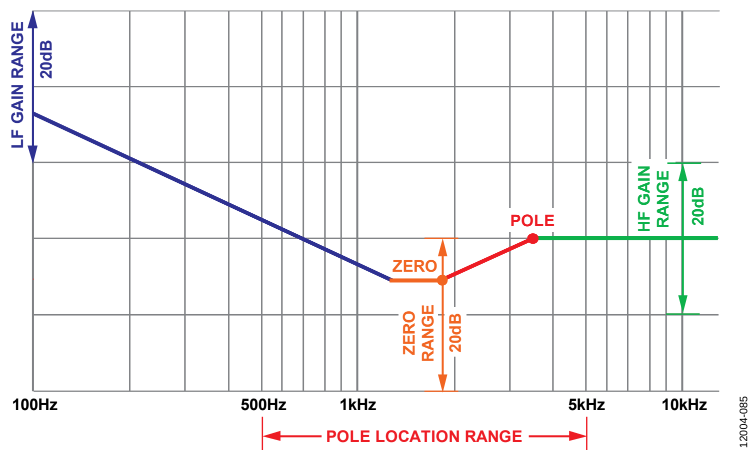


Figure 85. Digital Filter Programmability

Table 128. Register 0xFE01—NM_DIGFILT_LF_GAIN_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	LF gain setting	R/W	This register determines the low frequency gain of the loop response in normal mode. It is programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 85.

Table 129. Register 0xFE02—NM_DIGFILT_ZERO_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	Zero setting	R/W	This register determines the position of the final zero in normal mode. See Figure 85.

Table 130. Register 0xFE03—NM_DIGFILT_POLE_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	Pole setting	R/W	This register determines the position of the final pole in normal mode. See Figure 85.

Table 131. Register 0xFE04—NM_DIGFILT_HF_GAIN_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	HF gain setting	R/W	This register determines the high frequency gain of the loop response in normal mode. It is programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 85.

Table 132. Register 0xFE05—LLM_DIGFILT_LF_GAIN_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	LF gain setting	R/W	This register determines the low frequency gain of the loop response in light load mode. It is programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 85.

Table 133. Register 0xFE06—LLM_DIGFILT_ZERO_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	Zero setting	R/W	This register determines the position of the final zero in light load mode. See Figure 85.

Table 134. Register 0xFE07—LLM_DIGFILT_POLE_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	Pole setting	R/W	This register determines the position of the final pole in light load mode. See Figure 85.

Table 135. Register 0xFE08—LLM_DIGFILT_HF_GAIN_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	HF gain setting	R/W	This register determines the high frequency gain of the loop response in light load mode. It is programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 85.

Table 136. Register 0xFE09—SS_DIGFILT_LF_GAIN_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	LF gain setting	R/W	This register determines the low frequency gain of the loop response in soft start mode. It is programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 85.

Table 137. Register 0xFE0A—SS_DIGFILT_ZERO_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	Zero setting	R/W	This register determines the position of the final zero in soft start mode. See Figure 85.

Table 138. Register 0xFE0B—SS_DIGFILT_POLE_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	Pole setting	R/W	This register determines the position of the final pole in soft start mode. See Figure 85.

Table 139. Register 0xFE0C—SS_DIGFILT_HF_GAIN_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:0]	HF gain setting	R/W	This register determines the high frequency gain of the loop response in soft start mode. It is programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 85.

Table 140. Register 0xFE0D, Register 0xFE0F, Register 0xFE11, Register 0xFE13—OUTA_REDGE_SETTING, OUTB_REDGE_SETTING, OUTC_REDGE_SETTING, OUTD_REDGE_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[15:4]	t_1, t_3, t_5, t_7	R/W	This register contains the 12-bit t_1, t_3, t_5, t_7 time. Each LSB corresponds to 5 ns resolution. The minimum and maximum possible duty cycle is 0% and 100%, respectively.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_1, t_3, t_5, t_7 edge. 0 = no PWM modulation of the t_1, t_3, t_5, t_7 edge.
2	t_1, t_3, t_5, t_7 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_1, t_3, t_5, t_7 right. 0 = positive sign. Increase of PWM modulation moves t_1, t_3, t_5, t_7 left.
[1:0]	Reserved	R	Reserved.

Table 141. Register 0xFE0E, Register 0xFE10, Register 0xFE12, Register 0xFE14—OUTA_FEDGE_SETTING, OUTB_FEDGE_SETTING, OUTC_FEDGE_SETTING, OUTD_FEDGE_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[15:4]	t_2, t_4, t_6, t_8	R/W	This register contains the 12-bit t_2, t_4, t_6, t_8 time. Each LSB corresponds to 5 ns resolution. The minimum and maximum possible duty cycle is 0% and 100%, respectively.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_2, t_4, t_6, t_8 edge. 0 = no PWM modulation of the t_2, t_4, t_6, t_8 edge.
2	t_2, t_4, t_6, t_8 sign	R/W	1 = negative sign. Increase of PWM modulation moves t_2, t_4, t_6, t_8 right. 0 = positive sign. Increase of PWM modulation moves t_2, t_4, t_6, t_8 left.
[1:0]	Reserved	R	Reserved.

Table 142. Register 0xFE15, Register 0xFE17—SR1_REDGE_SETTING, SR2_REDGE_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[15:4]	t_9, t_{11}	R/W	This register contains the 12-bit t_9, t_{11} time. Each LSB corresponds to 5 ns resolution. The minimum and maximum possible duty cycle is 0% and 100%, respectively.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_9, t_{11} edge. 0 = no PWM modulation of the t_9, t_{11} edge.
2	t_9, t_{11} sign	R/W	1 = negative sign. Increase of PWM modulation moves t_9, t_{11} right. 0 = positive sign. Increase of PWM modulation moves t_9, t_{11} left.
[1:0]	Reserved	R	Reserved.

Table 143. Register 0xFE16, Register 0xFE18—SR1_FEDGE_SETTING, SR2_FEDGE_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[15:4]	t_{10}, t_{12}	R/W	This register contains the 12-bit t_{10}, t_{12} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{10}, t_{12} edge. 0 = no PWM modulation of the t_{10}, t_{12} edge.
2	t_{10}, t_{12} sign	R/W	1 = negative sign. Increase of PWM modulation moves t_{10}, t_{12} right. 0 = positive sign. Increase of PWM modulation moves t_{10}, t_{12} left.
[1:0]	Reserved	R	Reserved.

Table 144. Register 0xFE19, Register 0xFE1B—SR1_REDGE_LLM_SETTING, SR2_REDGE_LLM_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[15:4]	t_9, t_{11}	R/W	This register contains the 12-bit t_9, t_{11} time. Each LSB corresponds to 5 ns resolution. This is the SR setting in light load mode. The minimum and maximum possible duty cycle is 0% and 100%, respectively.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_9, t_{11} edge. 0 = no PWM modulation of the t_9, t_{11} edge.
2	t_9, t_{11} sign	R/W	1 = negative sign. Increase of PWM modulation moves t_9, t_{11} right. 0 = positive sign. Increase of PWM modulation moves t_9, t_{11} left.
[1:0]	Reserved	R	Reserved.

Table 145. Register 0xFE1A, Register 0xFE1C—SR1_FEDGE_LLM_SETTING, SR2_FEDGE_LLM_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[15:4]	t_{10}, t_{12}	R/W	This register contains the 12-bit t_{10}, t_{12} time. Each LSB corresponds to 5 ns resolution. This is the SR setting in light load mode. The minimum and maximum possible duty cycle is 0% and 100%, respectively.
3	Modulate Enable	R/W	1 = PWM modulation acts on the t_{10}, t_{12} edge. 0 = no PWM modulation of the t_{10}, t_{12} edge.
2	t_{10}, t_{12} sign	R/W	1 = negative sign. Increase of PWM modulation moves t_{10}, t_{12} right. 0 = positive sign. Increase of PWM modulation moves t_{10}, t_{12} left.
[1:0]	Reserved	R	Reserved.

Table 146. Register 0xFE1D—ADT_CONFIG

Bits	Bit Name	R/W	Description			
7	Averaging period	R/W	1 = 9-bit averaging (327 µs). 0 = 12-bit averaging (2.6 ms).			
6	ADT reference	R/W	0 = CS1 as reference. 1 = CS2 as reference.			
[5:3]	Update rate	R/W	The ADT algorithm adjusts the dead time in steps of 5 ns. These bits are used to program the number of PWM switching cycles between each step. The number is calculated as $2^N + 1$, where N is the 3-bit value specified by these bits. If N = 6 (110), each PWM edge is adjusted by 5 ns every $2^6 + 1 = 65$ switching cycles.			
[2:0]	Multiplier	R/W	These bits specify the programming step for Register 0xFE1F to Register 0xFE22, Bits[6:4] and Bits[2:0].			
			Bit 2	**Bit 1**	**Bit 0**	**Multiplier**
			0	0	0	5
			0	0	1	10
			0	1	0	15
			0	1	1	20
			1	0	0	25
			1	0	1	30
			1	1	0	35
			1	1	1	40

Table 147. Register 0xFE1E—ADT_THRESHOLD

Bits	Bit Name	R/W	Description
[7:0]	Adaptive dead time threshold	R/W	This register sets the ADT threshold. This 8-bit number is compared to the eight MSBs of the CS1/CS2 value register. When the current level measured on CS1/CS2 falls below this threshold, the edges of the PWM signals are affected as a linear function of the CS1/CS2 current, as programmed in Register 0xFE1F to Register 0xFE24. When this register is programmed to 0x00, the ADT function is disabled. When CS1 is used as the reference, each LSB in this register corresponds to $1.6\ V/2^8 = 6.25$ mV. When CS2 is used as the reference, each LSB in this register corresponds to 26.25 mV, 52.5 mV, or 420 mV]/2^8 = 102.539 µV, 205.078 µV, or 1640.625 µV. Also note that when CS2 is used as the reference, the maximum allowed value in this register is 224 (0xE0).

Table 148. Register 0xFE1F, Register 0xFE20, Register 0xFE21, Register 0xFE22—OUTA_DEAD_TIME, OUTB_DEAD_TIME, OUTC_DEAD_TIME, OUTD_DEAD_TIME (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description			
7	t_1, t_3, t_5, t_7, t_9, t_{11} polarity	R/W	0 = positive polarity. 1 = negative polarity.			
[6:4]	t_1, t_3, t_5, t_7, t_9, t_{11} offset	R/W	This value multiplied by Register 0xFE1D[2:0] determines the offset for t_1, t_3, t_5, t_7, t_9, t_{11} from nominal timing at no load.			
			Bit 6	**Bit 5**	**Bit 4**	**Offset (ns)**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	7
3	t_2, t_4, t_6, t_8, t_{10}, t_{12} polarity	R/W	0 = positive polarity. 1 = negative polarity.			

Bits	Bit Name	R/W	Description			
[2:0]	t_2, t_4, t_6, t_8, t_{10}, t_{12} offset	R/W	This value multiplied by Register 0xFE1D[2:0] determines the offset for t_2, t_4, t_6, t_8, t_{10}, t_{12} from nominal timing at no load.			
			Bit 2	**Bit 1**	**Bit 0**	**Offset (ns)**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	7

Table 149. Register 0xFE23, Register 0xFE24—SR1_DEAD_TIME, SR2_DEAD_TIME (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description			
7	t_9, t_{11} polarity	R/W	0 = positive polarity. 1 = negative polarity.			
[6:4]	t_9, t_{11} offset	R/W	This value multiplied by Register 0xFE1D[2:0] determines the offset for t_1, t_3, t_5, t_7, t_9, t_{11} from nominal timing at no load.			
			Bit 6	**Bit 5**	**Bit 4**	**Offset (ns)**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	7
3	t_{10}, t_{12} polarity	R/W	0 = positive polarity. 1 = negative polarity.			
[2:0]	t_{10}, t_{12} offset	R/W	This value multiplied by Register 0xFE1D[2:0] determines the offset for t_2, t_4, t_6, t_8, t_{10}, t_{12} from nominal timing at no load.			
			Bit 2	**Bit 1**	**Bit 0**	**Offset (ns)**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	7

Table 150. Register 0xFE25—VSBAL_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
7	Reserved	R	Reserved.
6	Volt-second balance enable	R/W	Setting this bit enables volt-second balance for the main transformer (used for full-bridge configurations).
5	Reserved	R	Set to 0 for proper operation.
4	Volt-second disable during soft start	R/W	0 = do not blank volt-second balance control during soft start (recommended). 1 = blank volt-second balance control during soft start.
3	Reserved	R	Reserved.
2	Reserved	R	Reserved.

Bits	Bit Name	R/W	Description		
[1:0]	Volt-second balance gain setting	R/W	These bits set the gain of the volt-second balance circuit. The gain can be changed by a factor of 64. When these bits are set to 00, it takes approximately 700 ms to achieve volt-second balance. When these bits are set to 11, it takes approximately 10 ms to achieve volt-second balance.		
			Bit 1	**Bit 0**	**Volt-Second Balance Gain**
			0	0	1
			0	1	4
			1	0	16
			1	1	64

Table 151. Register 0xFE26—VSBAL_OUTA_B

Bits	Bit Name	R/W	Description
7	Modulate enable, t_1	R/W	Setting this bit enables modulation from balance control on the OUTA rising edge, t_1.
6	t_1 sign	R/W	0 = positive sign. Increase of balance control modulation moves t_1 right. 1 = negative sign. Increase of balance control modulation moves t_1 left.
5	Modulate enable, t_2	R/W	Setting this bit enables modulation from balance control on the OUTA falling edge, t_2.
4	t_2 sign	R/W	0 = positive sign. Increase of balance control modulation moves t_2 right. 1 = negative sign. Increase of balance control modulation moves t_2 left.
3	Modulate enable, t_3	R/W	Setting this bit enables modulation from balance control on the OUTB rising edge, t_3.
2	t_3 sign	R/W	0 = positive sign. Increase of balance control modulation moves t_3 right. 1 = negative sign. Increase of balance control modulation moves t_3 left.
1	Modulate enable, t_4	R/W	Setting this bit enables modulation from balance control on the OUTB falling edge, t_4.
0	t_4 sign	R/W	0 = positive sign. Increase of balance control modulation moves t_4 right. 1 = negative sign. Increase of balance control modulation moves t_4 left.

Table 152. Register 0xFE27—VSBAL_OUTC_D

Bits	Bit Name	R/W	Description
7	Modulate enable, t_5	R/W	Setting this bit enables modulation from balance control on the OUTC rising edge, t_5.
6	t_5 sign	R/W	0 = positive sign. Increase of balance control modulation moves t_5 right. 1 = negative sign. Increase of balance control modulation moves t_5 left.
5	Modulate enable, t_6	R/W	Setting this bit enables modulation from balance control on the OUTC falling edge, t_6.
4	t_6 sign	R/W	0 = positive sign. Increase of balance control modulation moves t_6 right. 1 = negative sign. Increase of balance control modulation moves t_6 left.
3	Modulate enable, t_7	R/W	Setting this bit enables modulation from balance control on the OUTD rising edge, t_7.
2	t_7 sign	R/W	0 = positive sign. Increase of balance control modulation moves t_7 right. 1 = negative sign. Increase of balance control modulation moves t_7 left.
1	Modulate enable, t_8	R/W	Setting this bit enables modulation from balance control on the OUTD falling edge, t_8.
0	t_8 sign	R/W	0 = positive sign. Increase of balance control modulation moves t_8 right. 1 = negative sign. Increase of balance control modulation moves t_8 left.

Table 153. Register 0xFE28—VSBAL_SR1_2

Bits	Bit Name	R/W	Description
7	Modulate enable, t_9	R/W	Setting this bit enables modulation from balance control on the SR1 rising edge, t_9.
6	t_9 sign	R/W	0 = positive sign. Increase of balance control modulation moves t_9 right. 1 = negative sign. Increase of balance control modulation moves t_9 left.
5	Modulate enable, t_{10}	R/W	Setting this bit enables modulation from balance control on the SR1 falling edge, t_{10}.
4	t_{10} sign	R/W	0 = positive sign. Increase of balance control modulation moves t_{10} right. 1 = negative sign. Increase of balance control modulation moves t_{10} left.
3	Modulate enable, t_{11}	R/W	Setting this bit enables modulation from balance control on the SR2 rising edge, t_{11}.
2	t_{11} sign	R/W	0 = positive sign. Increase of balance control modulation moves t_{11} right. 1 = negative sign. Increase of balance control modulation moves t_{11} left.
1	Modulate enable, t_{12}	R/W	Setting this bit enables modulation from balance control on the SR2 falling edge, t_{12}.
0	t_{12} sign	R/W	0 = positive sign. Increase of balance control modulation moves t_{12} right. 1 = negative sign. Increase of balance control modulation moves t_{12} left.

Table 154. Register 0xFE29—FFWD_SETTING (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:4]	Reserved	R/W	Reserved.
3	Disable feedforward during soft start	R/W	If voltage line feedforward is enabled, this bit disables it during the soft start process. This operation is gated by the filter GO bit (Register 0xFE00). 0 = feedforward enabled during soft start (recommended setting). 1 = feedforward disabled during soft start.
2	Feedforward enable	R/W	This bit enables the voltage line feedforward loop. This operation is gated by the filter GO bit (Register 0xFE00]). 0 = feedforward disabled. 1 = feedforward enabled.
1	LF 8× gain increase	R/W	0 = default. 1 = 8× LF gain.
0	Global bit for nonlinear gain	R/W	0 = 1×/1.25×/1.5×/2× gain. 1 = 1×/2×/3×/4× gain.

Table 155. Register 0xFE2A—ISHARE_SETTING

Bits	Bit Name	R/W	Description
[7:4]	Number of bits dropped by master	R/W	These bits determine how much a master device reduces its output voltage to maintain current sharing. Each LSB corresponds to 1.6 V/2^{16} = 24 µV (at the VS± pins). This LSB is multiplied or divided by the setting in the share bus bandwidth register.
[3:0]	Bit difference between master and slave	R/W	These bits determine how closely a slave tries to match the current of the master device. The higher the setting, the larger the voltage difference that satisfies the current sharing criteria.

Table 156. Register 0xFE2B—ISHARE_BANDWIDTH

Bits	Bit Name	R/W	Description
[7:5]	Reserved	R	Reserved.
4	Bitstream	R/W	1 = the current sense ADC reading is output on the ISHARE pin. This bit stream can be used for analog current sharing. (recommended setting for standalone power supplies). 0 = the digital share bus signal is output on the ISHARE pin. This signal can be used for digital current sharing.
3	Current share select	R/W	1 = CS1 reading used for current share. 0 = CS2 reading used for current share.
[2:0]	Share bus bandwidth	R/W	These bits determine the amount of bandwidth dedicated to the share bus. The value 000 is the lowest possible bandwidth, and the value 111 is the highest possible bandwidth. The slave moves up 1 LSB for every share bus transaction (that is, eight data bits plus the start and stop bits). The master moves down x LSBs per share bus transaction, where x is the share bus register setting (Register 0xFE2A[7:4]). 0 = divide LSB by 16 (1 LSB = 24 µV/16). 1 = divide LSB by 8. 2 = divide LSB by 4. 3 = divide LSB by 2. 4 = nominal. 5 = multiply LSB by 2. 6 = multiply LSB by 4. 7 = multiply LSB by 8. 8 = multiply LSB by 16.

Table 157. Register 0xFE2C—IIN_OC_FAST_SETTING

Bits	Bit Name	R/W	Description		
[7:3]	Reserved	R	Reserved.		
2	Threshold	R/W	0 = 1.2 V range. 1 = 250 mV range.		
[1:0]	Debounce	R/W	**Bit 1**	**Bit 0**	**Debounce Time**
			0	0	0 ns
			0	1	40 ns
			1	0	80 ns
			1	1	120 ns

Table 158. Register 0xFE2D—IOUT_OC_FAST_SETTING

Bits	Bit Name	R/W	Description		
[7:2]	Threshold	R/W	When the ADC range is 480 mV, LSB = 600/63 = 9.52 mV. When the ADC range is 30 mV or 60 mV, LSB = 60/63 = 0.952 mV. Threshold = LSB × Register 0xFE2D[7:2].		
[1:0]	Debounce	R/W	**Bit 1**	**Bit 0**	**Debounce Time**
			0	0	0 ns
			0	1	40 ns
			1	0	200 ns
			1	1	400 ns

Table 159. Register 0xFE2E—IOUT_UC_FAST_SETTING

Bits	Bit Name	R/W	Description
[7:2]	Threshold	R/W	|LSB| = 30/63 = 0.476 mV. Range is +30 mV to −30 mV in 64 steps. Polarity = 0: Threshold = − 0.477 mV × Register 0xFE2E[7:2]. Polarity = 1: Threshold = + 0.472 mV × Register 0xFE2E [7:2]. Note that the IOUT_UC_FAST fault is set when the CS2 reverse comparator is asserted for the minimum debounce programmed time. Once set, the IOUT_UC_FAST fault is cleared from 327 μs to 656 μs following the deassertion of the CS2 reverse comparator.
1	Polarity	R/W	1 = 0 to +30 mV range. 0 = 0 to −30 mV range.
0	Debounce	R/W	The debounce setting is set by Register 0xFE2D[1:0]. For example, if Register 0xFE2D[1:0] = 10, the IOUT_OC_FAST_SETTING is 200 ns and the IOUT_UC_FAST_SETTING is 800 ns. 00 = 40 ns. 01 = 200 ns. 10 = 800 ns. 11 = 1200 ns.

Table 160. Register 0xFE2F—VOUT_OV_FAST_SETTING

Bits	Bit Name	R/W	Description		
[7:2]	Threshold	R/W	64 steps: Threshold = 0.8 + (Register 0xFE2F[7:2]) × 0.8/63.		
[1:0]	Debounce	R/W	These bits set the debounce time.		
			Bit 1	**Bit 0**	**Typical Debounce Time**
			0	0	40 ns
			0	1	2 μs + 1 μs
			1	0	5 μs + 1 μs
			1	1	10 μs + 1 μs

Table 161. Register 0xFE30—DEBOUNCE_SETTING_1

Bits	Bit Name	R/W	Description				
[15:14]	IOUT_OC_LV_DEB	R/W	These bits set the debounce time for the IOUT_OC_LV fault.				
			Bit 15	**Bit 14**	**Debounce**		
			0	0	0		
			0	1	1 ms + 10 μs		
			1	0	10 ms + 100 μs		
			1	1	100 ms + 1 ms		
[13:11]	VIN_UV_DEB	R/W	These bits set the debounce time for the VIN_UV fault.				
			Bit 13	**Bit 12**	**Bit 11**	**Debounce**	
			0	0	0	0	
			0	0	1	1 ms + 10 μs	
			0	1	0	2.5 ms + 10 μs	
			0	1	1	5 ms + 10 μs	
			1	0	0	10 ms + 100 μs	
			1	0	1	50 ms + 100 μs	
			1	1	0	100 ms + 1 ms	
			1	1	1	250 ms + 1 ms	
[10:8]	VOUT_UV_DEB	R/W	These bits set the debounce time for the VOUT_UV fault.				
			Bit 10	**Bit 9**	**Bit 8**	**Debounce**	
			0	0	0	0	
			0	0	1	1 ms + 10 μs	
			0	1	0	2.5 ms + 10 μs	
			0	1	1	5 ms + 10 μs	
			1	0	0	10 ms + 100 μs	
			1	0	1	50 ms + 100 μs	
			1	1	0	100 ms + 1 ms	
			1	1	1	250 ms + 1 ms	
[7:4]	VIN_OV_DEB	R/W	These bits set the debounce time for the VIN_OV fault.				
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Debounce**
			0	0	0	0	0
			0	0	0	1	100 μs + 1 μs
			0	0	1	0	250 μs + 1 μs
			0	0	1	1	500 μs + 1 μs
			0	1	0	0	750 μs + 10 μs
			0	1	0	1	1 ms + 10 μs
			0	1	1	0	2.5 ms + 10 μs
			0	1	1	1	5 ms + 10 μs
			1	0	0	0	7.5 ms + 100 μs
			1	0	0	1	10 ms + 100 μs
			1	0	1	0	25 ms + 100 μs
			1	0	1	1	50 ms + 100 μs
			1	1	0	0	75 ms + 1 ms
			1	1	0	1	100 ms + 1 ms
			1	1	1	0	250 ms + 1 ms
			1	1	1	1	500 ms + 1 ms

Bits	Bit Name	R/W	Description				
[3:0]	VOUT_OV_DEB	R/W	These bits set the debounce time for the VOUT_OV fault.				
			Bit 3	Bit 2	Bit 1	Bit 0	Debounce
			0	0	0	0	0
			0	0	0	1	100 µs + 1 µs
			0	0	1	0	250 µs + 1 µs
			0	0	1	1	500 µs + 1 µs
			0	1	0	0	750 µs + 10 µs
			0	1	0	1	1 ms + 10 µs
			0	1	1	0	2.5 ms + 10 µs
			0	1	1	1	5 ms + 10 µs
			1	0	0	0	7.5 ms + 100 µs
			1	0	0	1	10 ms + 100 µs
			1	0	1	0	25 ms + 100 µs
			1	0	1	1	50 ms + 100 µs
			1	1	0	0	75 ms + 1 ms
			1	1	0	1	100 ms + 1 ms
			1	1	1	0	250 ms + 1 ms
			1	1	1	1	500 ms + 1 ms

Table 162. Register 0xFE31—DEBOUNCE_SETTING_2

Bits	Bit Name	R/W	Description				
[15:12]	ISHARE_DEB	R/W	These bits set the debounce time for the ISHARE fault.				
			Bit 15	Bit 14	Bit 13	Bit 12	Debounce
			0	0	0	0	0
			0	0	0	1	1 ms + 10 µs
			0	0	1	0	2.5 ms + 10 µs
			0	0	1	1	5 ms + 10 µs
			0	1	0	0	7.5 ms + 100 µs
			0	1	0	1	10 ms + 100 µs
			0	1	1	0	25 ms + 100 µs
			0	1	1	1	50 ms + 100 µs
			1	0	0	0	75 ms + 1 ms
			1	0	0	1	100 ms + 1 ms
			1	0	1	0	250 ms + 1 ms
			1	0	1	1	500 ms + 1 ms
			1	1	0	0	750 ms + 10 ms
			1	1	0	1	1 sec + 10 ms
			1	1	1	0	2.5 sec + 10 ms
			1	1	1	1	5 sec + 10 ms

Bits	Bit Name	R/W	Description				
[11:8]	IIN_OC_DEB	R/W	These bits set the debounce time for the IIN_OC fault.				
			Bit 11	**Bit 10**	**Bit 9**	**Bit 8**	**Debounce**
			0	0	0	0	0
			0	0	0	1	1 ms + 10 μs
			0	0	1	0	2.5 ms + 10 μs
			0	0	1	1	5 ms + 10 μs
			0	1	0	0	7.5 ms + 100 μs
			0	1	0	1	10 ms + 100 μs
			0	1	1	0	25 ms + 100 μs
			0	1	1	1	50 ms + 100 μs
			1	0	0	0	75 ms + 1 ms
			1	0	0	1	100 ms + 1 ms
			1	0	1	0	250 ms + 1 ms
			1	0	1	1	500 ms + 1 ms
			1	1	0	0	750 ms + 10 ms
			1	1	0	1	1 sec + 10 ms
			1	1	1	0	2.5 sec + 10 ms
			1	1	1	1	5 sec + 10 ms
[7:4]	IOUT_UC_DEB	R/W	These bits set the debounce time for the IOUT_UC fault.				
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Debounce**
			0	0	0	0	0
			0	0	0	1	1 ms + 10 μs
			0	0	1	0	2.5 ms + 10 μs
			0	0	1	1	5 ms + 10 μs
			0	1	0	0	7.5 ms + 100 μs
			0	1	0	1	10 ms + 100 μs
			0	1	1	0	25 ms + 100 μs
			0	1	1	1	50 ms + 100 μs
			1	0	0	0	75 ms + 1 ms
			1	0	0	1	100 ms + 1 ms
			1	0	1	0	250 ms + 1 ms
			1	0	1	1	500 ms + 1 ms
			1	1	0	0	750 ms + 10 ms
			1	1	0	1	1 sec + 10 ms
			1	1	1	0	2.5 sec + 10 ms
			1	1	1	1	5 sec + 10 ms

Bits	Bit Name	R/W	Description				
[3:0]	IOUT_OC_DEB	R/W	These bits set the debounce time for the IOUT_OC fault.				
			Bit 3	Bit 2	Bit 1	Bit 0	Debounce
			0	0	0	0	0
			0	0	0	1	1 ms + 10 µs
			0	0	1	0	2.5 ms + 10 µs
			0	0	1	1	5 ms + 10 µs
			0	1	0	0	7.5 ms + 100 µs
			0	1	0	1	10 ms + 100 µs
			0	1	1	0	25 ms + 100 µs
			0	1	1	1	50 ms + 100 µs
			1	0	0	0	75 ms + 1 ms
			1	0	0	1	100 ms + 1 ms
			1	0	1	0	250 ms + 1 ms
			1	0	1	1	500 ms + 1 ms
			1	1	0	0	750 ms + 10 ms
			1	1	0	1	1 sec + 10 ms
			1	1	1	0	2.5 sec + 10 ms
			1	1	1	1	5 sec + 10 ms

Table 163. Register 0xFE32—DEBOUNCE_SETTING_3

Bits	Bit Name	R/W	Description				
[15:12]	Reserved	R	Reserved.				
[11:8]	POUT_OP_DEB	R/W	These bits set the debounce time for the POUT_OP fault.				
			Bit 11	Bit 10	Bit 9	Bit 8	Debounce
			0	0	0	0	0
			0	0	0	1	100 µs + 1 µs
			0	0	1	0	250 µs + 1 µs
			0	0	1	1	500 µs + 1 µs
			0	1	0	0	750 µs + 10 µs
			0	1	0	1	1 ms + 10 µs
			0	1	1	0	2.5 ms + 10 µs
			0	1	1	1	5 ms + 10 µs
			1	0	0	0	7.5 ms + 100 µs
			1	0	0	1	10 ms + 100 µs
			1	0	1	0	25 ms + 100 µs
			1	0	1	1	50 ms + 100 µs
			1	1	0	0	75 ms + 1 ms
			1	1	0	1	100 ms + 1 ms
			1	1	1	0	250 ms + 1 ms
			1	1	1	1	500 ms + 1 ms

Bits	Bit Name	R/W	Description				
[7:4]	TON_MAX_DEB	R/W	These bits set the debounce time for the TON_MAX fault.				
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Debounce**
			0	0	0	0	0
			0	0	0	1	100 µs + 1 µs
			0	0	1	0	250 µs + 1 µs
			0	0	1	1	500 µs + 1 µs
			0	1	0	0	750 µs + 10 µs
			0	1	0	1	1 ms + 10 µs
			0	1	1	0	2.5 ms + 10 µs
			0	1	1	1	5 ms + 10 µs
			1	0	0	0	7.5 ms + 100 µs
			1	0	0	1	10 ms + 100 µs
			1	0	1	0	25 ms + 100 µs
			1	0	1	1	50 ms + 100 µs
			1	1	0	0	75 ms + 1 ms
			1	1	0	1	100 ms + 1 ms
			1	1	1	0	250 ms + 1 ms
			1	1	1	1	500 ms + 1 ms
[3:0]	OT_DEB	R/W	These bits set the debounce time for the overtemperature fault.				
			Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Debounce**
			0	0	0	0	0
			0	0	0	1	1 ms + 10 µs
			0	0	1	0	2.5 ms + 10 µs
			0	0	1	1	5 ms + 10 µs
			0	1	0	0	7.5 ms + 100 µs
			0	1	0	1	10 ms + 100 µs
			0	1	1	0	25 ms + 100 µs
			0	1	1	1	50 ms + 100 µs
			1	0	0	0	75 ms + 1 ms
			1	0	0	1	100 ms + 1 ms
			1	0	1	0	250 ms + 1 ms
			1	0	1	1	500 ms + 1 ms
			1	1	0	0	750 ms + 10 ms
			1	1	0	1	1 sec + 10 ms
			1	1	1	0	2.5 sec + 10 ms
			1	1	1	1	5 sec + 10 ms

Table 164. Register 0xFE33—DEBOUNCE_SETTING_4

Bits	Bit Name	R/W	Description				
[15:12]	GPIO4_DEB	R/W	These bits set the debounce time for the GPIO4 fault.				
			Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Debounce**
			0	0	0	0	0
			0	0	0	1	80 ns
			0	0	1	0	1 µs + 1 µs
			0	0	1	1	100 µs + 1 µs
			0	1	0	0	500 µs + 1 µs
			0	1	0	1	1 ms + 10 µs
			0	1	1	0	2.5 ms + 10 µs
			0	1	1	1	5 ms + 10 µs
			1	0	0	0	7.5 ms + 100 µs
			1	0	0	1	10 ms + 100 µs
			1	0	1	0	25 ms + 100 µs
			1	0	1	1	50 ms + 100 µs
			1	1	0	0	75 ms + 1 ms
			1	1	0	1	100 ms + 1 ms
			1	1	1	0	250 ms + 1 ms
			1	1	1	1	500 ms + 1 ms
[11:8]	GPIO3_DEB	R/W	These bits set the debounce time for the GPIO3 fault.				
			Bit 11	**Bit 10**	**Bit 9**	**Bit 8**	**Debounce**
			0	0	0	0	0
			0	0	0	1	80 ns
			0	0	1	0	1 µs + 1 µs
			0	0	1	1	100 µs + 1 µs
			0	1	0	0	500 µs + 1 µs
			0	1	0	1	1 ms + 10 µs
			0	1	1	0	2.5 ms + 10 µs
			0	1	1	1	5 ms + 10 µs
			1	0	0	0	7.5 ms + 100 µs
			1	0	0	1	10 ms + 100 µs
			1	0	1	0	25 ms + 100 µs
			1	0	1	1	50 ms + 100 µs
			1	1	0	0	75 ms + 1 ms
			1	1	0	1	100 ms + 1 ms
			1	1	1	0	250 ms + 1 ms
			1	1	1	1	500 ms + 1 ms

Bits	Bit Name	R/W	Description				
[7:4]	GPIO2_DEB	R/W	These bits set the debounce time for the GPIO2 fault.				
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Debounce**
			0	0	0	0	0
			0	0	0	1	80 ns
			0	0	1	0	1 µs + 1 µs
			0	0	1	1	100 µs + 1 µs
			0	1	0	0	500 µs + 1 µs
			0	1	0	1	1 ms + 10 µs
			0	1	1	0	2.5 ms + 10 µs
			0	1	1	1	5 ms + 10 µs
			1	0	0	0	7.5 ms + 100 µs
			1	0	0	1	10 ms + 100 µs
			1	0	1	0	25 ms + 100 µs
			1	0	1	1	50 ms + 100 µs
			1	1	0	0	75 ms + 1 ms
			1	1	0	1	100 ms + 1 ms
			1	1	1	0	250 ms + 1 ms
			1	1	1	1	500 ms + 1 ms
[3:0]	GPIO1_DEB	R/W	These bits set the debounce time for the GPIO1 fault.				
			Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Debounce**
			0	0	0	0	0
			0	0	0	1	80 ns
			0	0	1	0	1 µs + 1 µs
			0	0	1	1	100 µs + 1 µs
			0	1	0	0	500 µs + 1 µs
			0	1	0	1	1 ms + 10 µs
			0	1	1	0	2.5 ms + 10 µs
			0	1	1	1	5 ms + 10 µs
			1	0	0	0	7.5 ms + 100 µs
			1	0	0	1	10 ms + 100 µs
			1	0	1	0	25 ms + 100 µs
			1	0	1	1	50 ms + 100 µs
			1	1	0	0	75 ms + 1 ms
			1	1	0	1	100 ms + 1 ms
			1	1	1	0	250 ms + 1 ms
			1	1	1	1	500 ms + 1 ms

The VOUT_OV_FAST_FAULT_RESPONSE command instructs the device on the actions to take due to an output fast overvoltage fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the VOUT_OV_FAST_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 165. Register 0xFE34—VOUT_OV_FAST_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to a fast overvoltage fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Do nothing.	
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].	
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).	
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay time	R/W	Number of delay time units (see Register 0xFE3E).			

The IOUT_OC_FAST_FAULT_RESPONSE command instructs the device on the actions to take due to an output fast overcurrent fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the IOUT_OC_FAST_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 166. Register 0xFE35—IOUT_OC_FAST_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to a fast overcurrent fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT.	
			0	1	Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT. If V_{OUT} falls below the IOUT_OC_LV_FAULT_LIMIT, respond as programmed by the retry setting (Bits[5:3]).	
			1	0	Continue operation in current limiting mode for the delay time (Bits[2:0]). If the device is still in current limiting mode, respond as programmed by the retry setting (Bits[5:3]).	
			1	1	Shut down, disable the output, and respond as programmed by the retry setting (Bits[5:3]).	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).			

The IOUT_UC_FAST_FAULT_RESPONSE command instructs the device on the actions to take due to an output fast undercurrent fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the IOUT_UC_FAST_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 167. Register 0xFE36—IOUT_UC_FAST_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to a fast undercurrent fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT.	
			0	1	Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT. If V_{OUT} falls below the IOUT_OC_LV_FAULT_LIMIT, respond as programmed by the retry setting (Bits[5:3]).	
			1	0	Continue operation in current limiting mode for the delay time (Bits[2:0]). If the device is still in current limiting mode, respond as programmed by the retry setting (Bits[5:3]).	
			1	1	Shut down, disable the output, and respond as programmed by the retry setting (Bits[5:3]).	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).			

The IIN_OC_FAST_FAULT_RESPONSE command instructs the device on the actions to take due to an input fast overcurrent fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the IIN_OC_FAST_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 168. Register 0xFE37—IIN_OC_FAST_FAULT_RESPONSE

Bits	Bit Name	R/W	Description		
[7:6]	Response	R/W	Determines the device response to a fast input overcurrent fault condition.		
			Bit 7	**Bit 6**	**Response**
			0	0	Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT.
			0	1	Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT. If V_{OUT} falls below the IOUT_OC_LV_FAULT_LIMIT, respond as programmed by the retry setting (Bits[5:3]).
			1	0	Continue operation in current limiting mode for the delay time (Bits[2:0]). If the device is still in current limiting mode, respond as programmed by the retry setting (Bits[5:3]).
			1	1	Shut down, disable the output, and respond as programmed by the retry setting (Bits[5:3]).

Bits	Bit Name	R/W	Description			
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).			

The ISHARE_FAULT_RESPONSE command instructs the device on the actions to take due to a current sharing fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the IOUT bit in STATUS_WORD register, and the ISHARE_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 169. Register 0xFE38—ISHARE_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to a current sharing fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT.	
			0	1	Operate in current limiting mode, maintaining the output current at IOUT_OC_FAULT_LIMIT. If V_{OUT} falls below the IOUT_OC_LV_FAULT_LIMIT, respond as programmed by the retry setting (Bits[5:3]).	
			1	0	Continue operation in current limiting mode for the delay time (Bits[2:0]). If the device is still in current limiting mode, respond as programmed by the retry setting (Bits[5:3]).	
			1	1	Shut down, disable the output, and respond as programmed by the retry setting (Bits[5:3]).	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay times	R/W	Number of delay time units (see Register 0xFE3E).			

The GPIO1_FAULT_RESPONSE command instructs the device on the actions to take due to a GPIO1 fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the GPIO1_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 170. Register 0xFE39—GPIO1_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to a GPIO1 fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Do nothing.	
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].	
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).	
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay time	R/W	Number of delay time units (see Register 0xFE3E).			

The GPIO2_FAULT_RESPONSE command instructs the device on the actions to take due to a GPIO2 fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the GPIO2_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 171. Register 0xFE3A—GPIO2_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to a GPIO2 fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Do nothing.	
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].	
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).	
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay time	R/W	Number of delay time units (see Register 0xFE3E).			

The GPIO3_FAULT_RESPONSE command instructs the device on the actions to take due to a GPIO3 fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the GPIO3_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 172. Register 0xFE3B—GPIO3_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to a GPIO3 fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Do nothing.	
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].	
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).	
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay time	R/W	Number of delay time units (see Register 0xFE3E).			

The GPIO4_FAULT_RESPONSE command instructs the device on the actions to take due to a GPIO4 fault condition. The device notifies the host and sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register, the MFR_SPECIFIC bit in STATUS_WORD register, and the GPIO4_FAULT bit in STATUS_MFR_SPECIFIC register.

Table 173. Register 0xFE3C—GPIO4_FAULT_RESPONSE

Bits	Bit Name	R/W	Description			
[7:6]	Response	R/W	Determines the device response to a GPIO4 fault condition.			
			Bit 7	**Bit 6**	**Response**	
			0	0	Do nothing.	
			0	1	Continue operation for the delay time (Bits[2:0]). If the fault persists, retry the number of times specified by Bits[5:3].	
			1	0	Shut down, disable the output, and respond as programmed in the retry setting (Bits[5:3]).	
			1	1	Disable the output while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.	
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	Infinite
[2:0]	Delay time	R/W	Number of delay time units (see Register 0xFE3E).			

Register 0xFE3D masks PWM disabling when a fault condition causes the device to disable the output and wait for the fault to clear (Response[7:6] = 11). Note that this masking register applies only when the ADP1055 is servicing a fault condition that has the fault response programmed to Bits[7:6] = 11.

Table 174. Register 0xFE3D—PWM_FAULT_MASK

Bits	Bit Name	R/W	Description
[7:6]	Reserved	R	Reserved.
5	Mask SR2	R/W	0 = SR2 disabled on fault; 1 = SR2 ignores fault.
4	Mask SR1	R/W	0 = SR1 disabled on fault; 1 = SR1 ignores fault.
3	Mask OUTD	R/W	0 = OUTD disabled on fault; 1 = OUTD ignores fault.
2	Mask OUTC	R/W	0 = OUTC disabled on fault; 1 = OUTC ignores fault.
1	Mask OUTB	R/W	0 = OUTB disabled on fault; 1 = OUTB ignores fault.
0	Mask OUTA	R/W	0 = OUTA disabled on fault; 1 = OUTA ignores fault.

Table 175. Register 0xFE3E—DELAY_TIME_UNIT

Bits	Bit Name	R/W	Description			
7	Current fault delay time unit	R/W	0 = ms. 1 = µs.			
[6:4]	Current fault delay time multiplier	R/W	**Bit 6**	**Bit 5**	**Bit 4**	**Multiplier**
			0	0	0	1
			0	0	1	4
			0	1	0	16
			0	1	1	64
			1	0	0	128
			1	0	1	256
			1	1	0	512
			1	1	1	1024
3	Voltage/other fault delay time unit	R/W	0 = ms. 1 = µs.			
[2:0]	Voltage/other fault delay time multiplier	R/W	**Bit 2**	**Bit 1**	**Bit 0**	**Multiplier**
			0	0	0	1
			0	0	1	4
			0	1	0	16
			0	1	1	64
			1	0	0	128
			1	0	1	256
			1	1	0	512
			1	1	1	1024

Table 176. Register 0xFE3F—WDT_SETTING

Bits	Bit Name	R/W	Description		
[7:2]	Reserved	R	Reserved.		
[1:0]	Watchdog timeout		**Bit 1**	**Bit 0**	**Timeout**
			0	0	Disable
			0	1	1 sec
			1	0	5 sec
			1	1	10 sec

Table 177. Register 0xFE40—GPIO_SETTING

Bits	Bit Name	R/W	Description
7	GPIO4 polarity	R/W	0 = active high; 1 = active low
6	GPIO4 direction	R/W	0 = input; 1 = output
5	GPIO3 polarity	R/W	0 = active high; 1 = active low
4	GPIO3 direction	R/W	0 = input; 1 = output
3	GPIO2 polarity	R/W	0 = active high; 1 = active low
2	GPIO2 direction	R/W	0 = input; 1 = output
1	GPIO1 polarity	R/W	0 = active high; 1 = active low
0	GPIO1 direction	R/W	0 = input; 1 = output

Table 178. Register 0xFE41—GPIO1_2_KARNAUGH_MAP

Bits	Bit Name	R/W	Description
[7:4]	GPIO2 logic function	R/W	0x0 = GND 0x1 = PGOOD1 AND PGOOD2 0x2 = PGOOD1 AND ~PGOOD2 0x3 = PGOOD1 0x4 = ~PGOOD1 AND PGOOD2 0x5 = PGOOD2 0x6 = PGOOD1 XOR PGOOD2 0x7 = PGOOD1 OR PGOOD2 0x8 = PGOOD1 NOR PGOOD2 0x9 = PGOOD1 XNOR PGOOD2 0xA = ~PGOOD2 0xB = PGOOD1 OR ~PGOOD2 0xC = ~PGOOD1 0xD = ~PGOOD1 OR PGOOD2 0xE = PGOOD1 NAND PGOOD2 0xF = VDD
[3:0]	GPIO1 logic function	R/W	0x0 = GND 0x1 = PGOOD1 AND PGOOD2 0x2 = PGOOD1 AND ~PGOOD2 0x3 = PGOOD1 0x4 = ~PGOOD1 AND PGOOD2 0x5 = PGOOD2 0x6 = PGOOD1 XOR PGOOD2 0x7 = PGOOD1 OR PGOOD2 0x8 = PGOOD1 NOR PGOOD2 0x9 = PGOOD1 XNOR PGOOD2 0xA = ~PGOOD2 0xB = PGOOD1 OR ~PGOOD2 0xC = ~PGOOD1 0xD = ~PGOOD1 OR PGOOD2 0xE = PGOOD1 NAND PGOOD2 0xF = VDD

Table 179. Register 0xFE42—GPIO3_4_KARNAUGH_MAP

Bits	Bit Name	R/W	Description
[7:4]	GPIO4 logic function	R/W	0x0 = GND
			0x1 = PGOOD1 AND PGOOD2
			0x2 = PGOOD1 AND ~PGOOD2
			0x3 = PGOOD1
			0x4 = ~PGOOD1 AND PGOOD2
			0x5 = PGOOD2
			0x6 = PGOOD1 XOR PGOOD2
			0x7 = PGOOD1 OR PGOOD2
			0x8 = PGOOD1 NOR PGOOD2
			0x9 = PGOOD1 XNOR PGOOD2
			0xA = ~PGOOD2
			0xB = PGOOD1 OR ~PGOOD2
			0xC = ~PGOOD1
			0xD = ~PGOOD1 OR PGOOD2
			0xE = PGOOD1 NAND PGOOD2
			0xF = VDD
[3:0]	GPIO3 logic function	R/W	0x0 = GND
			0x1 = PGOOD1 AND PGOOD2
			0x2 = PGOOD1 AND ~PGOOD2
			0x3 = PGOOD1
			0x4 = ~PGOOD1 AND PGOOD2
			0x5 = PGOOD2
			0x6 = PGOOD1 XOR PGOOD2
			0x7 = PGOOD1 OR PGOOD2
			0x8 = PGOOD1 NOR PGOOD2
			0x9 = PGOOD1 XNOR PGOOD2
			0xA = ~PGOOD2
			0xB = PGOOD1 OR ~PGOOD2
			0xC = ~PGOOD1
			0xD = ~PGOOD1 OR PGOOD2
			0xE = PGOOD1 NAND PGOOD2
			0xF = VDD

Table 180. Register 0xFE43—PGOOD_FAULT_DEB

Bits	Bit Name	R/W	Description		
[7:6]	PGOOD2_OFF_DEB	R/W	**Bit 7**	**Bit 6**	**Debounce (ms)**
			0	0	0
			0	1	150 + 10
			1	0	350 + 10
			1	1	550 + 10
[5:4]	PGOOD2_ON_DEB	R/W	**Bit 5**	**Bit 4**	**Debounce (ms)**
			0	0	0
			0	1	150 + 10
			1	0	350 + 10
			1	1	550 + 10
[3:2]	PGOOD1_OFF_DEB	R/W	**Bit 3**	**Bit 2**	**Debounce (ms)**
			0	0	0
			0	1	150 + 10
			1	0	350 + 10
			1	1	550 + 10

Bits	Bit Name	R/W	Description		
[1:0]	PGOOD1_ON_DEB	R/W	Bit 1	Bit 0	Debounce (ms)
			0	0	0
			0	1	150 + 10
			1	0	350 + 10
			1	1	550 + 10

Table 181. Register 0xFE44—PGOOD1_FAULT_SELECT

Bits	Bit Name	R/W	Description
15	TON_MAX_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
14	IOUT_UC_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
13	POUT_OP_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
12	IIN_OC_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
11	VIN_OV_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
10	VOUT_UV_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
9	VOUT_OV_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
8	IOUT_OC_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
7	VIN_UV_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
6	IIN_OC_FAST_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
5	IOUT_OC_FAST_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
4	VOUT_OV_FAST	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
3	SOFT_START_RAMP	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
2	OT_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
1	SR_OFF	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)
0	OFF	R/W	1 = this flag, if asserted, sets the PGOOD1 flag (Bit 6 of STATUS_UNKNOWN)

Table 182. Register 0xFE45—PGOOD2_FAULT_SELECT

Bits	Bit Name	R/W	Description
15	VOUT (STATUS_WORD[15])	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
14	IOUT/POUT (STATUS_WORD[14])	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
13	INPUT (STATUS_WORD[13])	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
12	TEMPERATURE (STATUS_WORD[2])	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
11	GPIO2/GPIO4	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
10	GPIO1/GPIO3	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
9	TOFF_MAX_WARN	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
8	IOUT_UC_FAST_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
7	Constant current	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
6	IIN_OC_FAST_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
5	IOUT_OC_FAST_FAULT	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
4	VOUT_OV_FAST	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
3	SOFT_START_RAMP	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
2	SYNC_UNLOCK	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
1	Maximum black box record reached	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)
0	Soft start filter	R/W	1 = this flag, if asserted, sets the PGOOD2 flag (Bit 7 of STATUS_UNKNOWN)

Table 183. Register 0xFE46—SOFT_START_BLANKING

Bits	Bit Name	R/W	Description
15	VOUT_OV_FAULT	R/W	1 = this flag is ignored during soft start
14	GPIO3/GPIO4 snubber	R/W	1 = the GPIO3/GPIO4 snubber outputs are disabled during soft start
13	TON_MAX_FAULT	R/W	1 = this flag is ignored during soft start
12	VIN_OV_FAULT	R/W	1 = this flag is ignored during soft start
11	VIN_UV_FAULT	R/W	1 = this flag is ignored during soft start

Bits	Bit Name	R/W	Description
10	IIN_OC_FAULT	R/W	1 = this flag is ignored during soft start
9	IOUT_OC_FAULT	R/W	1 = this flag is ignored during soft start
8	IOUT_UC_FAULT and IOUT_UC_FAST_FAULT	R/W	1 = this flag is ignored during soft start
7	POUT_OP_FAULT	R/W	1 = this flag is ignored during soft start
6	IIN_OC_FAST_FAULT	R/W	1 = this flag is ignored during soft start
5	IOUT_OC_FAST_FAULT	R/W	1 = this flag is ignored during soft start
4	VOUT_OV_FAST	R/W	1 = this flag is ignored during soft start
3	IOUT_OC_LV_FAULT	R/W	1 = this flag is ignored during soft start
2	GPIO1/GPIO3	R/W	1 = this flag is ignored during soft start
1	GPIO2/GPIO4	R/W	1 = this flag is ignored during soft start
0	OT_FAULT	R/W	1 = this flag is ignored during soft start

Table 184. Register 0xFE47—SOFT_STOP_BLANKING

Bits	Bit Name	R/W	Description
15	VOUT_OV_FAULT	R/W	1 = this flag is ignored during soft stop
14	GPIO3/GPIO4 snubber	R/W	1 = the GPIO3/GPIO4 snubber outputs are disabled during soft stop
13	TOFF_MAX_WARN	R/W	1 = this flag is ignored during soft stop
12	VIN_OV_FAULT	R/W	1 = this flag is ignored during soft stop
11	VIN_UV_FAULT	R/W	1 = this flag is ignored during soft stop
10	IIN_OC_FAULT	R/W	1 = this flag is ignored during soft stop
9	IOUT_OC_FAULT	R/W	1 = this flag is ignored during soft stop
8	IOUT_UC_FAULT and IOUT_UC_FAST_FAULT	R/W	1 = this flag is ignored during soft stop
7	POUT_OP_FAULT	R/W	1 = this flag is ignored during soft stop
6	IIN_OC_FAST_FAULT	R/W	1 = this flag is ignored during soft stop
5	IOUT_OC_FAST_FAULT	R/W	1 = this flag is ignored during soft stop
4	VOUT_OV_FAST	R/W	1 = this flag is ignored during soft stop
3	IOUT_OC_LV_FAULT	R/W	1 = this flag is ignored during soft stop
2	GPIO1/GPIO3	R/W	1 = this flag is ignored during soft stop
1	GPIO2/GPIO4	R/W	1 = this flag is ignored during soft stop
0	OT_FAULT	R/W	1 = this flag is ignored during soft stop

Table 185. Register 0xFE48—BLACKBOX_SETTING

<table>
<tr><th>Bits</th><th>Bit Name</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td>[7:3]</td><td>Reserved</td><td>R</td><td colspan="3">Reserved.</td></tr>
<tr><td>[2]</td><td>Maximum record number</td><td>R/W</td><td colspan="3">Sets the maximum record number at which the black box recording feature is disabled.
0 = 150,000. Recommended when operating at <85°C.
1 = 16,000. Recommended when operating at 125°C.</td></tr>
<tr><td rowspan="6">[1:0]</td><td rowspan="6">Recording options</td><td rowspan="6">R/W</td><td colspan="3">Sets black box recording options before shutting down the power supply. The minimum time for the black box to write all the status registers into the EEPROM is approximately 1.1 ms. When black box writing is enabled for the save on every retry shutdown cycle, the minimum retry delay time must be greater than the time to write to the EEPROM (1.1 ms).</td></tr>
<tr><td>Bit 1</td><td>Bit 0</td><td>Options</td></tr>
<tr><td>0</td><td>0</td><td>No recording.</td></tr>
<tr><td>0</td><td>1</td><td>Record only telemetry just before the final shutdown.</td></tr>
<tr><td>1</td><td>0</td><td>Record telemetry of final shutdown and all retry attempts.</td></tr>
<tr><td>1</td><td>1</td><td>Record telemetry of final shutdown, all retry attempts, and normal unit-off per the CTRL pin and the OPERATION command.</td></tr>
</table>

Table 186. Register 0xFE49—PWM_DISABLE_SETTING

Bits	Bit Name	R/W	Description
[7:6]	Reserved	R	Reserved.
5	SR2 disable	R/W	Setting this bit disables the SR2 output.
4	SR1 disable	R/W	Setting this bit disables the SR1 output.
3	OUTD disable	R/W	Setting this bit disables the OUTD output.
2	OUTC disable	R/W	Setting this bit disables the OUTC output.
1	OUTB disable	R/W	Setting this bit disables the OUTB output.
0	OUTA disable	R/W	Setting this bit disables the OUTA output.

Table 187. Register 0xFE4A—FILTER_TRANSITION (Requires Use of the GO Bit in Register 0xFE00)

<table>
<tr><th>Bits</th><th>Bit Name</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td>7</td><td>Overshoot protection</td><td>R/W</td><td colspan="3">0 = disable setpoint reference tracking.
1 = enable setpoint reference tracking (see the Integrator Windup and Output Voltage Regulation Loss (Overshoot Protection) section).</td></tr>
<tr><td>6</td><td>Overshoot speed</td><td>R/W</td><td colspan="3">0 = if V_{OUT} is out of regulation for 96 out of 128 switching cycles, the reference moves to the last known value of V_{OUT} (9-bit precision) and tries to return to regulation at a controlled rate given by the VOUT_TRANSITION_RATE command.
1 = if V_{OUT} is out of regulation for 48 out of 64 switching cycles, V_{REF} tracks V_{OUT} (9-bit precision).
Double update rate affects this register.</td></tr>
<tr><td>[5:3]</td><td>HF ADC configuration</td><td>R/W</td><td colspan="3">000 = autocorrection loop disabled.
001 = autocorrection loop bandwidth set to approximately 9 Hz.
010 = autocorrection loop bandwidth set to approximately 19 Hz.
011 = autocorrection loop bandwidth set to approximately 37 Hz.
100 = autocorrection loop bandwidth set to approximately 75 Hz.
101 = autocorrection loop bandwidth set to approximately 150 Hz.
110 = autocorrection loop bandwidth set to approximately 300 Hz.
111 = autocorrection loop bandwidth set to approximately 600 Hz.</td></tr>
<tr><td>2</td><td>Enable soft transition</td><td>R/W</td><td colspan="3">Enables soft transition between filter settings to minimize output transients. All four parameters of each filter are linearly transitioned to the new value.</td></tr>
<tr><td rowspan="6">[1:0]</td><td rowspan="6">Transition speed</td><td rowspan="6">R/W</td><td colspan="3">The filter changes in 32 steps, with one step applied at the interval specified by these bits.</td></tr>
<tr><td>Bit 1</td><td>Bit 0</td><td>Speed</td></tr>
<tr><td>0</td><td>0</td><td>$32 \times t_{SW}$ (total transition time = $32 \times 32 \times t_{SW} = 1024 \times t_{SW}$)</td></tr>
<tr><td>0</td><td>1</td><td>$8 \times t_{SW}$ (total transition time = $8 \times 32 = 256 \times t_{SW}$)</td></tr>
<tr><td>1</td><td>0</td><td>$2 \times t_{SW}$ (total = $64 \times t_{SW}$)</td></tr>
<tr><td>1</td><td>1</td><td>$1 \times t_{SW}$ (total = $32 \times t_{SW}$)</td></tr>
</table>

Table 188. Register 0xFE4B—DEEP_LLM_SETTING

<table>
<tr><th>Bits</th><th>Bit Name</th><th>R/W</th><th colspan="4">Description</th></tr>
<tr><td rowspan="10">[7:5]</td><td rowspan="10">Deep LLM thresholds</td><td rowspan="10">R/W</td><td colspan="4">These bits set the load current limit on the CS2 ADC below which SR1 and SR2 enter deep light load mode. The averaging time, debounce, and hysteresis are programmed in Register 0xFE4B. SR outputs are always off in pulse skip mode.</td></tr>
<tr><td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Thresholds (LSBs)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>12</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>20</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>24</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>28</td></tr>
</table>

Bits	Bit Name	R/W	Description
[4:3]	Deep light load mode averaging speed	R/W	Sets the averaging speed and resolution used for the deep light load mode thresholds. Faster speed corresponds to lower resolution, and therefore to smaller accuracy of the threshold. **Bit 4 / Bit 3 / Speed (μs)** 0 / 0 / 37.5 (six bits) 0 / 1 / 82 (seven bits) 1 / 0 / 163 (eight bits) 1 / 1 / 327 (nine bits)
[2:1]	Deep light load mode hysteresis	R/W	Sets the amount of hysteresis applied to the deep light load mode thresholds. The size of the LSB is affected by the speed and resolution selected in Bits[4:3]. For example, if the ADC range of 30 mV is used with 8-bit resolution, the LSB size is 30 mV/2^8 = 117.187 μV. **Bit 2 / Bit 1 / LSBs** 0 / 0 / 3 0 / 1 / 8 1 / 0 / 12 1 / 1 / 16
0	Fast phase-in	R/W	0 = SR transition speed is always the value programmed during all transitions, as set by Register 0xFE5F[7:4]. 1 = the SR transition speed is the value programmed in Register 0xFE5F[7:4] for the first transition process (whenever that occurs after PSON according to the settings), but for every subsequent transition, the SR outputs transition at the fastest speed, that is, 5 ns/t_{SW}.

Table 189. Register 0xFE4C—DEEP_LLM_DISABLE_SETTING

Bits	Bit Name	R/W	Description
7	SR phase-in enable	R/W	0 = disable SR phase-in. 1 = enable SR phase-in.
6	OUTD disable	R/W	Setting this bit means that OUTD is disabled if the load current drops below the deep light load threshold.
5	OUTC disable	R/W	Setting this bit means that OUTC is disabled if the load current drops below the deep light load threshold.
4	OUTB disable	R/W	Setting this bit means that OUTB is disabled if the load current drops below the deep light load threshold.
3	OUTA disable	R/W	Setting this bit means that OUTA is disabled if the load current drops below the deep light load threshold.
2	SR2 disable	R/W	Setting this bit means that SR2 are disabled if the load current drops below the deep light load threshold.
1	SRs enable during soft stop	R/W	Setting this bit means that SR2 are disabled if the load current drops below the deep light load threshold.
0	SRs enable during soft stop	R/W	Setting this bit reenables the SRs during soft stop to facilitate discharging the load. The recommended setting is 1.

Table 190. Register 0xFE4D—OVP_FAULT_CONFIG

Bits	Bit Name	R/W	Description
7	VDD/VCORE OV fault ignore	R/W	0 = VDD OV and VCORE OV flags are not ignored 1 = VDD OV and VCORE OV flags are ignored
6	VDD/VCORE OV restart	R/W	0 = do not download EEPROM again following a fault shutdown 1 = download EEPROM following a fault shutdown
5	VDD/VCORE OV debounce	R/W	0 = 2 μs + 1 μs debounce 1 = 500 μs + 10 μs debounce
4	VDD UV debounce	R/W	0 = no debounce 1 = 120 ns debounce

Bits	Bit Name	R/W	Description		
[3:2]	VOUT_OV sampling	R/W	**Bit 3**	**Bit 2**	**Sampling**
			0	0	One sample sets the VOUT_OV flag (80 µs sampling period)
			0	1	Two consecutive samples that read a value greater than the one set in VOUT_OV_FAULT_LIMIT set the VOUT_OV flag (160 µs sampling period)
			1	0	Three consecutive samples that read a value greater than the one set in VOUT_OV_FAULT_LIMIT set the VOUT_OV flag (240 µs sampling period)
			1	1	Four consecutive samples that read a value greater than the one set in VOUT_OV_FAULT_LIMIT set the VOUT_OV flag (320 µs sampling period)
[1:0]	Reserved		Reserved		

Table 191. Register 0xFE4E—CS1_SETTING

Bits	Bit Name	R/W	Description
7	Reserved	R	Reserved.
[6:4]	CS1 fast OCP blanking	R/W	Set the CS1 fast OCP blanking time to 0 ns, 40 ns, 80 ns, 120 ns, 200 ns, 400 ns, 600 ns, or 800 ns.
3	CS1 fast OCP bypass	R/W	Setting this bit means that the GPIO1 pin is used for CS1 fast OCP instead of the CS1 pin.
[2:0]	CS1 fast OCP timeout	R/W	Set the number of consecutive switching cycles with a CS1 OCP condition before the IIN_OC_FAST_FAULT flag is set: 1, 4, 16, 128, 256, 384, 512, or 1024.

Table 192. Register 0xFE4F—CS2_SETTING

Bits	Bit Name	R/W	Description		
7	CC turbo mode	R/W	Reduces the CS2 average time from 328 µs to 41 µs for CC mode.		
[6:4]	CS2 fast OCP timeout	R/W	Sets the number of consecutive switching cycles with a CS2 OCP condition before the IOUT_OC_FAST_FAULT flag is set: 1, 4, 16, 128, 256, 384, 512, or 1024.		
3	Peak constant current mode	R/W	When this bit is set, CS2 fast OCP cycle-by-cycle protection on OUTA to OUTD is disabled. The CS2 fast OCP timeout is still active.		
2	Average constant current disable	R/W	0 = average constant current mode is enabled/disabled, as defined by PMBus. Threshold = IOUT_OC_FAULT_LIMIT. ILIM = IOUT_OC_FAULT_LIMIT × (100 + percentage), where percentage and polarity are defined in Register 0xFE5D[3:0]. The current fault response is PMBus compliant. 1 = average constant current mode is always on (not PMBus compliant). Threshold = ILIM = IOUT_OC_FAULT_LIMIT × (100 ± percentage), where percentage and polarity are defined in Register 0xFE5D[3:0]. Current fault response defaults to these settings (Response Bits[7:6]). 00 = ignore fault. 01 = ignore fault. 10 = ignore fault. 11 = shut down, disable the output, and respond as programmed in retry setting (Bits[5:3]).		
[1:0]	CS2 range	R/W	Sets the CS2 ADC range.		
			Bit 1	**Bit 0**	**ADC Range (mV)**
			0	0	30 (low-side sensing)
			0	1	60 (low-side sensing)
			1	0	480 (high-side sensing)
			1	1	Reserved

Table 193. Register 0xFE50—PULSE_SKIP_AND_SHUTDOWN

Bits	Bit Name	R/W	Description		
[7:6]	Addition PS on time after end of soft stop ramp	R/W	To allow any negative current to dissipate, PWM outputs such as the SR outputs are kept active after the soft stop ramp-down.		
			Bit 7	**Bit 6**	**LSBs**
			0	0	No additional on time at the end of soft stop. All PWM outputs are shut off immediately at end of ramp. The SR PWM outputs continue to increase their modulation limit and completely turn on for the entire switching cycle after the maximum limit is reached.
			0	1	2 ms of extra on time.
			1	0	4 ms of extra on time.
			1	1	8 ms of extra on time.
5	Instant SR transition	R/W	1 = SR outputs move from LLM to normal mode instantly. 0 = SR outputs transition from one mode to another (LLM to CCM or CCM to LLM) at the phase-in speed (recommended).		
4	Pulse killer mode	R/W	Register 0xFE50[0] kills all PWM outputs that are modulated. However, this bit kills all PWM outputs whether modulated or not (useful for FBPS topology where there are two fixed duty cycle PWM outputs). 1 = kill all PWM outputs during pulse skip. 0 = do not kill all PWM outputs during pulse skip.		
3	End-of-cycle shutdown	R/W	0 = all PWM outputs are disabled immediately on a shutdown condition. 1 = all PWM outputs are disabled at the end of the switching cycle on a shutdown condition.		
2	Soft stop pulse skipping enable	R/W	If set, allow pulse skipping during soft stop (regardless of value of Bit 1). However, SR1 and SR2 never pulse skip during soft stop.		
1	Pulse skipping enable	R/W	0 = disable. 1 = enable.		
0	Pulse skipping zero PWM	R/W	0 = pulse skipping drives all modulated PWM outputs to 0 V. 1 = sets all modulated edges to t = 0.		

Table 194. Register 0xFE51—SOFT_START_SETTING

Bits	Bit Name	R/W	Description
7	Soft stop enable for current faults	R/W	0 = disable soft stop on a current fault. 1 = enable soft stop on a current fault.
6	Soft stop enable for other faults	R/W	0 = disable soft stop on a voltage fault. 1 = enable soft stop on a voltage and other fault.
[5:3]	SR phase-in speed up factor during soft stop	R/W	During the soft stop process, these bits increase the SR edge transitioning speed that is specified by Register 0xFE5F[7:4]. The speed-up factor is 2^x where x is this 3-bit number. The maximum speed of the SR edge is 40 ns per t_{SW}. For example, if Register 0xFE5F specifies 5 ns per 4 t_{SW}, setting these three bits to 2 increases the SR speed to 5 ns per t_{SW} (5 ns/4t_{SW} × 2^2). Setting these bits to 3 increases the SR speed to 10 ns per t_{SW} (5 ns/4t_{SW} × 2^3). Setting these bits to 7 increases the SR speed to 40 ns per t_{SW} (the maximum rate). A smaller value means slower SR transitioning.
2	Force soft start filter	R/W	1 = soft start filter is used regardless of whether the low temperature filter is active or not.
1	Disable light load filter during soft start	R/W	0 = allow switching to DCM filter during soft start. 1 = never switch to DCM filter during soft start.
0	Soft start from precharge	R/W	Setting this bit to 1 enables the soft start from precharge function. When this function is enabled, the soft start ramp starts from the last known value of the voltage detected on VS±.

Table 195. Register 0xFE52—SR_DELAY

<table>
<tr><th>Bits</th><th>Bit Name</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td rowspan="6">[7:6]</td><td rowspan="6">SR blanking</td><td rowspan="6">R/W</td><td colspan="3">These bits add blanking to the reverse current comparator from the falling edges of the SR LLM edges. Adding dead time to the SR edges effectively gives additional blanking. When the SR outputs are disabled upon a negative going zero crossing transition, they remain disabled for a period of 327 μs to 754 μs to ensure that the comparator is not falsely triggered.</td></tr>
<tr><td>Bit 7</td><td>Bit 6</td><td>Blanking (ns)</td></tr>
<tr><td>0</td><td>0</td><td>40</td></tr>
<tr><td>0</td><td>1</td><td>80</td></tr>
<tr><td>1</td><td>0</td><td>120</td></tr>
<tr><td>1</td><td>1</td><td>160</td></tr>
<tr><td>[5:0]</td><td>SR driver delay</td><td>R/W</td><td colspan="3">These bits specify the 6-bit representation of the SR delay in steps of 5 ns.
000000 = 0 ns.
000001 = 5 ns.
000010 = 10 ns.
…
111111 = 63 × 5 ns = 315 ns.</td></tr>
</table>

Table 196. Register 0xFE53—MODULATION_LIMIT

<table>
<tr><th>Bits</th><th>Bit Name</th><th>R/W</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td>Full bridge mode</td><td>R/W</td><td colspan="2">Enable this bit when operating in full bridge mode. It affects the modulation high limit.</td></tr>
<tr><td rowspan="7">[6:0]</td><td rowspan="7">Modulation limits</td><td rowspan="7">R/W</td><td colspan="2">This value sets the minimum/maximum modulation limits relative to the nominal edge value. The resolution depends on the switching frequency range.</td></tr>
<tr><td>Switching Frequency Range (kHz)</td><td>Resolution Corresponding to LSB</td></tr>
<tr><td>48.8 to 97.7</td><td>Register 0xFE53[6:0] × 32 × 5 ns</td></tr>
<tr><td>97.7 to 195.3</td><td>Register 0xFE53[6:0] × 16 × 5 ns</td></tr>
<tr><td>195.3 to 390.6</td><td>Register 0xFE53[6:0] × 8 × 5 ns</td></tr>
<tr><td>390.6 to 781</td><td>Register 0xFE53[6:0] × 4 × 5 ns</td></tr>
<tr><td>f_{SW} > 781</td><td>Register 0xFE53[6:0] × 2 × 5 ns</td></tr>
</table>

Table 197. Register 0xFE55—SYNC (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
7	Reserved	R	Reserved.
6	PLL disable	R/W	0 = enable SYNC function. 1 = disable SYNC function.
[5:2]	Reserved	R	Reserved.
1	Jitter enable	R/W	1 = enable jitter on clock (to randomize frequency components).
0	5 ns resolution enable	R/W	0 = t_{SW} varies in multiples of 10 ns (50% point is synchronized with 5 ns; see the External Frequency Synchronization section). 1 = t_{SW} varies in multiples of 5 ns.

Table 198. Register 0xFE56—DUTY_BAL_EDGESEL

Bits	Bit Name	R/W	Description
[7:4]	Positive integration of PWM outputs	R/W	1 = selects the PWM outputs to be AND'ed together for positive integration Bit 7 = OUTA Bit 6 = OUTB Bit 5 = OUTC Bit 4 = OUTD
[3:0]	Negative integration of PWM outputs	R/W	1 = selects the PWM outputs to be AND'ed together for negative integration Bit 3 = OUTA Bit 2 = OUTB Bit 1 = OUTC Bit 0 = OUTD

Table 199. Register 0xFE57—DOUBLE_UPD_RATE (Requires Use of the GO Bit in Register 0xFE00)

<table>
<tr><th>Bits</th><th>Bit Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>Enable duty balance</td><td>R/W</td><td>0 = disable.
1 = enable.</td></tr>
<tr><td>6</td><td>Enable OCP duty equalization</td><td>R/W</td><td>1 = enable OCP duty equalization. When OCP occurs, shut down any OUTx that is high and generate an equalizing OCP to balance the complementary output. Refer to Register 0xFE56 for the selection of PWM outputs.</td></tr>
<tr><td>[5:4]</td><td>Duty balance averaging time</td><td>R/W</td><td>These bits control how rapidly the misbalance information is used to correct for imbalance.
<table>
<tr><th>Bit 5</th><th>Bit 4</th><th>Time</th></tr>
<tr><td>0</td><td>0</td><td>Normal value: cycle-by-cycle integral is divided by 8 and applied to OUTx.</td></tr>
<tr><td>0</td><td>1</td><td>2× faster: cycle-by-cycle integral is divided by 4 and applied to OUTx.</td></tr>
<tr><td>1</td><td>0</td><td>4× faster: cycle-by-cycle integral is divided by 2 and applied to OUTx.</td></tr>
<tr><td>1</td><td>1</td><td>8× faster: no averaging; cycle-by-cycle integral is applied on the next cycle to OUTx.</td></tr>
</table></td></tr>
<tr><td>3</td><td>Reserved</td><td>R/W</td><td>Set to 0 for proper operation.</td></tr>
<tr><td>[2:1]</td><td>Duty balance and VS balance limit</td><td>R/W</td><td>To balance OUTA and OUTB, time is added to or subtracted from OUTA and OUTB and added to or subtracted from OUTC and OUTD, as in VS balance. These bits set the maximum balance value.
<table>
<tr><th>Bit 2</th><th>Bit 1</th><th>Limit (ns)</th></tr>
<tr><td>0</td><td>0</td><td>±160</td></tr>
<tr><td>0</td><td>1</td><td>±80</td></tr>
<tr><td>1</td><td>0</td><td>±40</td></tr>
<tr><td>1</td><td>1</td><td>±20</td></tr>
</table></td></tr>
<tr><td>0</td><td>Enable double update rate</td><td>R/W</td><td>0 = disable.
1 = enable.</td></tr>
</table>

The VIN_SCALE_MONITOR command sets the gain (K_{VIN}) by which the input sensed voltage at the DUT (V_{IN_DUT}) is scaled to generate the reading for the READ_VIN command. READ_VIN = $V_{IN\_DUT} \times K_{VIN}$, where $K_{VIN} = Y \times 2^N$.

Table 200. Register 0xFE58—VIN_SCALE_MONITOR

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

The IIN_CAL_GAIN command sets the ratio of the voltage at the input current sense pins to the sensed current (in ohms).

Table 201. Register 0xFE59—IIN_CAL_GAIN

Bits	Bit Name	R/W	Description
[15:11]	Exponent-N	R/W	Twos complement N-exponent used in linear data format ($X = Y \times 2^N$).
[10:0]	Mantissa-Y	R/W	Twos complement Y-mantissa used in linear data format ($X = Y \times 2^N$).

The TSNS_SETTING command is the temperature sensor current select.

Table 202. Register 0xFE5A—TSNS_SETTING

Bits	Bit Name	R/W	Description
7	Enable reverse diode	R/W	1 = enable external reverse temperature sensor
[6:5]	Resolution	R/W	11 = 11 bit 10 = 12 bit 01 = 13 bit 00 = 14 bit
4	Reserved	R/W	Set this bit to 0 for proper operation.
3	Temperature sense level shift disable	R/W	0 = enable internal diode level shifter during external T_J sense. This setting is recommended for a single-ended (PN) diode connected between JTD and AGND. 1 = disable internal diode level shifter during external T_J sense. This setting is recommended for differential sensing.
[2:0]	Temperature sense current select	R/W	Set these bits to 0x04 for proper operation (10 µA).

Table 203. Register 0xFE5B—AUTO_GO_CMD

Bits	Bit Name	R/W	Description
[7:2]	Reserved	R	Reserved.
1	Frequency auto-go enable	R/W	0 = GO_CMD, Bit 2 (Register 0xFE00) is required to latch the programmed frequency in FREQUENCY_SWITCH into the internal loop frequency. 1 = write to FREQUENCY_SWITCH is automatically latched into the internal loop switching frequency.
0	V_{REF} auto-go enable	R/W	0 = GO_CMD, Bit 0 (Register 0xFE00) is required to latch the programmed reference voltage in VOUT_COMMAND into the internal loop frequency. 1 = write to any commands affecting the reference voltage is automatically latched into the internal loop reference voltage. Commands that affect the reference voltage include VOUT_COMMAND, VOUT_MODE, VOUT_MAX, VOUT_TRIM, VOUT_CAL_OFFSET, VOUT_SCALE_LOOP, and VOUT_DROOP.

Table 204. Register 0xFE5C—DIODE_EMULATION

<table>
<tr><th>Bits</th><th>Bit Name</th><th>R/W</th><th colspan="4">Description</th></tr>
<tr><td rowspan="10">[7:5]</td><td rowspan="10">SR debounce</td><td rowspan="10">R/W</td><td colspan="4">These bits delay the onset of LLM or CCM when the light load mode or deep light load mode threshold is crossed. The device transitions from CCM to LLM based on the debounce time specified using these bits and the light load mode threshold. The same is true when the device transitions from LLM to CCM and is also valid for deep light load mode.
For example, if the device is in CCM and the load current step places the device in LLM, the device physically enters LLM, that is, the SR outputs start phasing after the debounce time set by these bits. The same debounce time delays the entry to DCM.
Entering deep light load mode is possible only if the ADP1055 is already in DCM (that is, the device is already below the DCM threshold) and SR transitioning is finished.</td></tr>
<tr><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Debounce Time (t_{SW})</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>64</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>128</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>256</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>512</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>768</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1152</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>2048</td></tr>
<tr><td>[4:2]</td><td>Reserved</td><td>R</td><td colspan="4">Reserved.</td></tr>
<tr><td>1</td><td>Diode emulation mode</td><td>R/W</td><td colspan="4">0 = disable diode emulation mode (SR LLM and deep LLM are active if the thresholds are correctly set).
1 = enable diode emulation mode (SR LLM setting is disabled. Only deep LLM is active if the threshold is correctly set). Once the SR outputs are disabled upon a negative going zero crossing transition, they are disabled for a period of 327 μs to 754 μs to ensure that the comparator is not falsely triggered.</td></tr>
<tr><td>0</td><td>SR toggle rate in diode emulation mode</td><td>R/W</td><td colspan="4">0 = SR outputs toggle once in one t_{SW}.
1 = SR outputs toggle twice in one t_{SW} (recommended setting).</td></tr>
</table>

Table 205. Register 0xFE5D—CS2_CONST_CUR_MODE

Bits	Bit Name	R/W	Description
[7:6]	Reserved	R	Reserved.
[5:4]	Slew rate during CC mode (turbo mode only)	R/W	00 = Nominal slew rate of (8 × 1.18) V/sec Setting 00 provides 2x nominal at VS± pins in CC turbo mode 01 = 16× 10 = 24× 11 = 32×
3	CC mode thresholds polarity	R/W	0 = positive (% above OCP limit) 1 = negative (% below OCP limit)

[2:0]	CC mode thresholds	R/W	Percentage above or below OCP limit (IOUT_OC_FAULT_LIMIT) 00 = 0% 001 = 3.125% 010 = 6.25% 011 = 12.5% 100 = 25% 101 = 50% 11x = 100%

The NL_ERR_GAIN_FACTOR register applies nonlinear gain. Bits[7:6] apply nonlinear gain to the ±1% to 2% range, where the total ADC range is 5% of 1 V, that is, ±50 mV. Bits[5:4] apply nonlinear gain to the ±2% to 3.2% range, where the total ADC range is 5% of 1 V, that is, ±50 mV. Bits[3:2] apply nonlinear gain to the ±3.2% to 3.9% range, where the total ADC range is 5% of 1 V, that is, ±50 mV. Bits[1:0] apply nonlinear gain to the ±3.9% and greater range, where the total ADC range is 5% of 1 V, that is, ±50 mV.

Table 206. Register 0xFE5E—NL_ERR_GAIN_FACTOR (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description		
[7:6]	Nonlinear gain, 1% to 2% range	R/W	**Bit 7**	**Bit 6**	**Gain**
			0	0	1× gain
			0	1	2× gain or 1.25× (see Register 0xFE29[0])
			1	0	4× gain or 1.5× (see Register 0xFE29[0])
			1	1	8× gain or 2× (see Register 0xFE29[0])
[5:4]	Nonlinear gain, 2% to 3.2% range	R/W	**Bit 5**	**Bit 4**	**Gain**
			0	0	1× gain
			0	1	2× gain or 1.25× (see Register 0xFE29[0])
			1	0	4× gain or 1.5× (see Register 0xFE29[0])
			1	1	8× gain or 2× (see Register 0xFE29[0])
[3:2]	Nonlinear gain, 3.2% to 3.9% range	R/W	**Bit 3**	**Bit 2**	**Gain**
			0	0	1× gain
			0	1	2× gain or 1.25× (see Register 0xFE29[0])
			1	0	4× gain or 1.5× (see Register 0xFE29[0])
			1	1	8× gain or 2× (see Register 0xFE29[0])
[1:0]	Nonlinear gain, 3.9% or greater range	R/W	**Bit 1**	**Bit 0**	**Gain**
			0	0	1× gain
			0	1	2× gain or 1.25× (see Register 0xFE29[0])
			1	0	4× gain or 1.5× (see Register 0xFE29[0])
			1	1	8× gain or 2× (see Register 0xFE29[0])

Table 207. Register 0xFE5F—SR_SETTING

Bits	Bit Name	R/W	Description
[7:4]	SR phase-in speed	R/W	SR edges move by 5 ns every 1/2/4/8/16/32/64/128/256/384/512/640/768/832/960/1024 (total of 16). SR outputs are always phased in during soft start, soft stop, and all mode transitions; for example, if SR outputs enter pulse skip or are disabled, they turn on again at the phase-in speed selected by these bits.

Bit 7	Bit 6	Bit 5	Bit 4	Multiplier
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	16
0	1	0	1	32
0	1	1	0	64
0	1	1	1	128
1	0	0	0	256
1	0	0	1	384
1	0	1	0	512
1	0	1	1	640
1	1	0	0	768
1	1	0	1	832
1	1	1	0	960
1	1	1	1	1024

Bits	Bit Name	R/W	Description
[3:1]	SR LLM threshold	R/W	These bits set the load current limit on the CS2 ADC below which SR1 and SR2 enter the light load mode (SR on during forward conduction only). Averaging time, debounce, and hysteresis are the same values set in Register 0xFE4B.

Bit 3	Bit 2	Bit 1	Thresholds (LSBs)
0	0	0	0
0	0	1	4
0	1	0	8
0	1	1	12
1	0	0	16
1	0	1	20
1	1	0	24
1	1	1	28

Bits	Bit Name	R/W	Description
0	Blank SR during soft start	R/W	1 = blank SR during soft start.

Table 208. Register 0xFE60—NOMINAL_TEMP_POLE

Bits	Bit Name	R/W	Description
[7:0]	ADD_PZ	R/W	Additional pole/zero setting. A value of 0 disables ADD_PZ. The analog frequency (in rad/sec) is located at $w = \ln(reg\_val/256)/t_{SW}$, where t_{SW} is the switching period and reg_val is the contents of Register 0xFE60 and Register 0xFE61 in decimal format.

Table 209. Register 0xFE61—LOW_TEMP_POLE

Bits	Bit Name	R/W	Description
[7:0]	ADD_PZ	R/W	Additional pole/zero setting. A value of 0 disables ADD_PZ. The analog pole frequency in rad/sec is located at $w = \ln(0xFE61[7:0]/256)/t_{SW}$, where t_{SW} is the switching period.

Table 210. Register 0xFE62—LOW_TEMP_SETTING

Bits	Bit Name	R/W	Description
7	ADD_PZ configuration	R/W	0 = ADD_PZ is configured as a digital pole. 1 = ADD_PZ is configured as a digital zero.
[6:4]	Low temperature threshold	R/W	If non-zero, the filter switches from the NMF (normal mode filter) to the SS filter (soft start filter) in steps of ±4°C. 000 = regular filter operation independent of temperature unless the sensing point (configured in Bits[1:0]) is set to GPIO2 (the filter then changes based on the GPIO2 pin). 001 = below −14°C, the soft start filter is used for regulation instead of the normal mode filter. 010 = below −10°C, the soft start filter is used for regulation instead of the normal mode filter. 011 = below −6°C, the soft start filter is used for regulation instead of the normal mode filter. 100 = below −2°C, the soft start filter is used for regulation instead of the normal mode filter. 101 = below +2°C, the soft start filter is used for regulation instead of the normal mode filter. 110 = below +6°C, the soft start filter is used for regulation instead of the normal mode filter. 111 = below +10°C, the soft start filter is used for regulation instead of the normal mode filter.
[3:2]	Low temperature hysteresis	R/W	Each bit is 5°C of hysteresis. 00 = 5°C. 01 = 10°C. 10 = 15°C. 11 = 20°C.
[1:0]	Low temperature sensing point	R/W	00 = reserved. 01 = external FWD temperature sensing. 10 = external REV temperature sensing. 11 = rising edge of GPIO2.

Table 211. Register 0xFE63—GPIO3_4_SNUBBER_ON_TIME

Bits	Bit Name	R/W	Description
[7:0]	Snubber on time	R/W	Maximum on time of GPIO3/GPIO4 (if SR/OUTC/OUTD goes high, then the GPIO3/GPIO4 output goes low/high) in units of 20 ns 0x00 = 0 ns 0x01 = 20 ns … 0xFE = 5.08 µs 0xFF = on until SRx goes high or OUTC or OUTD goes low

Table 212. Register 0xFE64—GPIO3_4_SNUBBER_DELAY

Bits	Bit Name	R/W	Description
[7:6]	GPIO4 snubber enable	R/W	00 = disable active snubber on GPIO3/GPIO4. 01 = only GPIO3 is active snubber. GPIO3 goes high after the snubber delay time in Register 0xFE64[5:0]. 10 = only GPIO4 is active snubber. GPIO4 goes high after the snubber delay time in Register 0xFE64[5:0]. 11 = GPIO3 and GPIO4 are active snubber outputs. GPIO3 is the inverse of SR1 or OUTC; GPIO4 is the inverse of SR2 or OUTC, depending on Register 0xFE65[7].
[5:0]	Snubber delay	R/W	Dead time delay from fall of SR to rise of GPIO3/GPIO4, in units of 5 ns, regardless of the polarity of GPIO3/GPIO4. 0x00 = 0 ns. 0x01 = 5 ns. 0x3F = 315 ns.

Table 213. Register 0xFE65—VOUT_DROOP_SETTING

Bits	Bit Name	R/W	Description
7	Snubber selection	R/W	0 = falling edge of SRx is used to activate the snubber. 1 = falling edge of OUTC or OUTD is used to activate the snubber.
[6:3]	Reserved	R	Reserved.
2	Disable VOUT_ TRANSITION_RATE	R/W	1 = disable. The voltage reference immediately jumps to the value set by VOUT_COMMAND. 0 = enable. The output voltage changes from one value to another as programmed by the VOUT_TRANSITION_RATE command.
[1:0]	VOUT_DROOP sampling rate	R/W	For the purposes of VOUT_DROOP, IOUT is sampled at the following intervals: 00 = 7 bits = 82 μs. 01 = 8 bits = 164 μs. 10 = 9 bits = 327 μs. 11 = 10 bits = 655 μs.

Table 214. Register 0xFE66—NC_BURST_MODE (Requires Use of the GO Bit in Register 0xFE00)

Bits	Bit Name	R/W	Description
[7:6]	ADC threshold	R/W	Burst occurs if the ADC error exceeds the specified threshold. 00 = error threshold > |±1%| of 1 V (that is, 10 mV) 01 = error threshold > |±2%| of 1 V (that is, 20 mV) 10 = error threshold > |±3%| of 1 V (that is, 30 mV) 11 = error threshold > |±4%| of 1 V (that is, 40 mV)
[5:3]	Number of burst cycles	R/W	Set to 0 for no burst
2	Enable burst in LLM/DEM only	R/W	1 = burst in light load mode and diode emulation mode only (not in CCM) 0 = burst in any mode
[1:0]	Burst magnitude	R/W	Magnitude of burst in percentage of duty cycle that is added to the present duty cycle 00 = 6.25% 01 = 12.5% 10 = 25% 11 = 50%

Table 215. Register 0xFE67—HF_ADC_CONFIG

Bits	Bit Name	R/W	Description		
[7:4]	HF ADC samples	R/W	These bits specify the number of samples taken by the flash ADC for loop regulation. The number of samples ranges from 1 (Bits[7:4] = 0000) to 16 (Bits[7:4] = 1111). Following are suggested values depending on the frequency range and whether double update rate is enabled.		
			Frequency Range (kHz)	**Double Update Rate Enabled**	**Double Update Rate Disabled**
			f_{SW} ≤ 250	1111 (16 samples)	1111 (16 samples)
			250 < f_{SW} ≤ 300	0111 (8 samples)	1111 (16 samples)
			300 < f_{SW} ≤ 724.638	0011 (4 samples)	1111 (16 samples)
			724.638 < f_{SW} ≤ 1000	0001 (2 samples)	0111 (8 samples)
[3:0]	Reserved	R/W	Set these bits to 000 for proper operation.		

Table 216. Register 0xFE80—VS_TRIM

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	Gain trim	R/W	These bits set the amount of gain trim that is applied to the VS ADC reading. This register trims the voltage at the VS± pins for external resistor tolerances. The VS trim must be performed before the load OVP and load UVP trims are performed. The total range for these bits is ±6.25%. The LSB = (6.25%)/128.

Table 217. Register 0xFE81—VFF_GAIN_TRIM

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	Gain trim	R/W	These bits set the gain trim for the VFF ADC. Total range is ±12.5% with 128 steps in the positive direction and 127 steps in the negative direction, and the LSB = 12.5%/128.

Table 218. Register 0xFE82—CS1_GAIN_TRIM

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	Gain trim	R/W	These bits set the gain trim for the primary side current gain. Total range is ±12.5% with 128 steps in the positive direction and 127 steps in the negative direction, and the LSB = 12.5%/128.

Table 219. Register 0xFE86—TSNS_EXTFWD_GAIN_TRIM

Bits	Bit Name	R/W	Description
[7:0]	Gain trim	R/W	Gain trim in twos complement added to scaling factor (977 for 10-bit resolution set) for external forward diode temperature measurement. For example, Register 0xFE5A[6:5] = 00 corresponds to an increase in gain by 1/489% Register 0xFE86 = 0x01 corresponds to an increase in gain by 1/977% Register 0xFE86 = 0x02 corresponds to an increase in gain by 2/977%

Table 220. Register 0xFE87—TSNS_EXTFWD_OFFSET_TRIM

Bits	Bit Name	R/W	Description
[7:0]	Offset trim	R/W	Offset trim added to the acquisition result of the forward diode temperature measurement; 1 LSB corresponds to 0.0156°C, in twos complement format. Maximum correction is 2°C.

Table 221. Register 0xFE88—TSNS_EXTREV_GAIN_TRIM

Bits	Bit Name	R/W	Description
[7:0]	Gain trim	R/W	Gain trim in twos complement added to scaling factor (977 for 10-bit resolution set) for external reverse diode temperature measurement. For example, Register 0xFE88 = 0x01 corresponds to an increase in gain by 1/977% Register 0xFE88 = 0x02 corresponds to an increase in gain by 2/977%

Table 222. Register 0xFE89—TSNS_EXTREV_OFFSET_TRIM

Bits	Bit Name	R/W	Description
[7:0]	Offset trim	R/W	Offset trim added to the acquisition result of the reverse diode temperature measurement; 1 LSB corresponds to 0.0156°C, in twos complement format. Maximum correction is 2°C.

Table 223. Register 0xFE8C—FAULT_VOUT

Bits	Bit Name	R/W	Description
[7:0]	FAULT_VOUT	R	Unlatched fault conditions after debounce (see STATUS_VOUT for latched version)

Table 224. Register 0xFE8D—FAULT_IOUT

Bits	Bit Name	R/W	Description
[7:0]	FAULT_IOUT	R	Unlatched fault conditions after debounce (see STATUS_IOUT for latched version)

Table 225. Register 0xFE8E—FAULT_INPUT

Bits	Bit Name	R/W	Description
[7:0]	FAULT_INPUT	R	Unlatched fault conditions after debounce (see STATUS_INPUT for latched version)

Table 226. Register 0xFE8F—FAULT_TEMPERATURE

Bits	Bit Name	R/W	Description
[7:0]	FAULT_TEMPERATURE	R	Unlatched fault conditions after debounce (see STATUS_TEMPERATURE for latched version)

Table 227. Register 0xFE90—FAULT_CML

Bits	Bit Name	R/W	Description
[7:0]	FAULT_CML	R	Unlatched fault conditions after debounce (see STATUS_CML for latched version)

Table 228. Register 0xFE91—FAULT_OTHER

Bits	Bit Name	R/W	Description
[7:0]	FAULT_OTHER	R	Unlatched fault conditions after debounce (see STATUS_OTHER for latched version)

Table 229. Register 0xFE92—FAULT_MFR_SPECIFIC

Bits	Bit Name	R/W	Description
[7:0]	FAULT_MFR_SPECIFIC	R	Unlatched fault conditions after debounce (see STATUS_MFR_SPECIFIC for latched version)

Table 230. Register 0xFE93—FAULT_UNKNOWN

Bits	Bit Name	R/W	Description
[15:0]	FAULT_UNKNOWN	R	Unlatched fault conditions after debounce (see STATUS_UNKNOWN for latched version)

Table 231. Register 0xFE94—STATUS_UNKNOWN

Bits	Bit Name	R/W	Description
15	EEPROM unlocked	R/W	The EEPROM is unlocked.
14	Adaptive dead time	R/W	Adaptive dead time threshold has been crossed.
13	Soft start filter	R/W	The soft start filter is in use.
12	Soft start ramp or soft stop ramp	R/W	The reference is being ramped up (soft start) or ramped down (soft stop).
11	Modulation limit	R/W	Modulation is at its minimum or maximum limit.
10	Volt-second and duty balance limit	R/W	Volt-second balance or duty balance at is the maximum/minimum limit.
9	Light load mode	R/W	The device is in light load mode.
8	Constant current	R/W	Power supply is operating in constant current mode (constant current mode is enabled).
7	PGOOD2 fault	R/W	PGOOD2 fault. At least one of the flags listed in Register 0xFE45 has been set (see Table 182).
6	PGOOD1 fault	R/W	PGOOD1 fault. At least one of the flags listed in Register 0xFE44 has been set (see Table 181).
5	Sync unlock	R/W	Sync mode is enabled, but unit not locked to sync input frequency.
4	SR off	R/W	Synchronous rectifiers SR1 and SR2 are disabled. This flag is set when one of the following cases is true: SR1 and SR2 are disabled by the user; the load current has fallen below the threshold in Register 0xFE4B[7:5]; a fault has been set that was configured to disable the synchronous rectifiers; or SR outputs are blanked during soft start and during a pulse skip condition.
3	Address warning	R/W	I^2C/PMBus address warning. ADD resistor value out-of-range.
2	VCORE OV	R/W	2.5 V VCORE is above limit. Action is set to immediate shutdown.
1	VDD OV	R/W	VDD is above limit. The I^2C interface stays functional, but a unit power-off/power-on sequence is required to restart the power supply. The response to a VDD overvoltage is programmable in Register 0xFE4D[6].
0	VDD UV	R/W	VDD is below limit. The response to a VDD undervoltage immediate shutdown.

Table 232. Register 0xFE95—FIRST_FAULT_ID

Bits	Bit Name	R/W	Description
[7:0]	First-fault ID (in hex)	R	0x00 = no fault 0x01 = VOUT_OV 0x02 = VOUT_OV_FAST 0x03 = VOUT_UV 0x04 = IOUT_OC_LV 0x05 = VIN_OV 0x06 = VIN_UV 0x07 = OT 0x08 = TON_MAX 0x09 = POUT_OP 0x0A = GPIO1 0x0B = GPIO2 0x0C = GPIO3 0x0D = GPIO4 0x0E = IOUT_OC 0x0F = IOUT_OC_FAST 0x10 = IOUT_UC 0x11 = IOUT_UC_FAST 0x12 = IIN_OC 0x13 = IIN_OC_FAST 0x14 = ISHARE

Table 233. Register 0xFE96—VFF_VALUE

Bits	Bit Name	R/W	Description
[15:0]	VFF value	R	This register contains the feedforward information. This value has 12 bits of resolution from Bit 13 to Bit 2.

Table 234. Register 0xFE97—VS_VALUE

Bits	Bit Name	R/W	Description
[15:0]	VS value (output voltage)	R	This register contains the output voltage information. This value has 12 bits of resolution from Bit 13 to Bit 2.

Table 235. Register 0xFE98—CS1_VALUE

Bits	Bit Name	R/W	Description
[15:0]	CS1 value (input current)	R	This register contains the input current information. This value has 12 bits of resolution from Bit 13 to Bit 2.

Table 236. Register 0xFE99—CS2_VALUE

Bits	Bit Name	R/W	Description
[15:0]	CS2 value (output current)	R	This register contains the 12-bit output current information. This value is the voltage drop across the sense resistor. To obtain the current value, divide the value of this register by the sense resistor value. The CS2± pins have a full-scale input range of 30 mV, 60 mV, or 480 mV (set in Register 0xFE4F[1:0]). When the CS2 input range is set to 30 mV, the LSB step size is 7.32 µV. For example, at a 15 mV input signal on CS2, the value in this register is 15 mV/7.32 µV = 1000 0000 0000.

Table 237. Register 0xFE9A—POUT_VALUE

Bits	Bit Name	R/W	Description
[15:0]	CS2 × VS value (output power)	R	This register contains the 16-bit output power information. This value is the product of the remote output voltage value (VS) and the output current reading (CS2).

Table 238. Register 0xFE9B—Reserved

Bits	Bit Name	R/W	Description
[15:0]	Reserved	R	Reserved.

Table 239. Register 0xFE9C—TSNS_EXTFWD_VALUE

Bits	Bit Name	R/W	Description
[15:7]	Integer	R	Twos complement integer in the range of −256 to +255
[6:0]	Decimal	R	Decimal component of the temperature reading

Table 240. Register 0xFE9D—TSNS_EXTREV_VALUE

Bits	Bit Name	R/W	Description
[15:7]	Integer	R	Twos complement integer in the range of −256 to +255
[6:0]	Decimal	R	Decimal component of the temperature reading

Table 241. Register 0xFE9F—MODULATION_VALUE

Bits	Bit Name	R/W	Description
[7:0]	Modulation value	R	This register contains the 8-bit modulation information. It outputs the amount of modulation from 0% to 100% that is being placed on the modulating edges.

Table 242. Register 0xFEA0—ISHARE_VALUE

Bits	Bit Name	R/W	Description
[7:0]	Share bus value	R	This register contains the 8-bit share bus voltage information. If the power supply is the master, this register outputs 0.

Table 243. Register 0xFEA3—ADD_ADC_VALUE

Bits	Bit Name	R/W	Description
[7:0]	ADD ADC value	R	This register contains the address information. This value has eight bits of resolution. LSB = $1.6/2^8$ = 6.25 mV. At 1 V input, the value in this register is 160 (0xA0). It is used in conjunction with Register 0xD0[5:4].

SUPPORTED SWITCHING FREQUENCIES

Table 244 lists switching frequencies supported by the ADP1055. For information about setting the switching frequency, see the FREQUENCY_SWITCH section. For entries with the same exponent and mantissa values, the entry with the lower period value is valid.

Table 244. Supported Switching Frequencies

Period (ns)	Frequency (kHz)	Exponent	Mantissa
20,470	48.85197851	−4	782
20,460	48.87585533	−4	782
20,430	48.94762604	−4	783
20,400	49.01960784	−4	784
20,380	49.06771344	−4	785
20,350	49.14004914	−4	786
20,330	49.18839154	−4	787
20,300	49.26108374	−4	788
20,270	49.33399112	−4	789
20,250	49.38271605	−4	790
20,220	49.45598417	−4	791
20,200	49.5049505	−4	792
20,170	49.57858205	−4	793
20,150	49.62779156	−4	794
20,120	49.70178926	−4	795
20,100	49.75124378	−4	796
20,070	49.82561036	−4	797
20,050	49.87531172	−4	798
20,020	49.95004995	−4	799
20,000	50	−4	800
19,970	50.07511267	−4	801
19,950	50.12531328	−4	802
19,920	50.20080321	−4	803
19,900	50.25125628	−4	804
19,870	50.32712632	−4	805
19,850	50.37783375	−4	806
19,820	50.45408678	−4	807
19,800	50.50505051	−4	808
19,770	50.58168943	−4	809
19,750	50.63291139	−4	810
19,720	50.70993915	−4	811
19,700	50.76142132	−4	812
19,680	50.81300813	−4	813
19,650	50.89058524	−4	814
19,630	50.94243505	−4	815
19,600	51.02040816	−4	816
19,580	51.07252298	−4	817
19,550	51.15089514	−4	818
19,530	51.20327701	−4	819
19,510	51.25576627	−4	820
19,480	51.33470226	−4	821
19,460	51.38746146	−4	822
19,440	51.44032922	−4	823
19,410	51.51983514	−4	824
19,390	51.57297576	−4	825
19,370	51.62622612	−4	826
19,340	51.70630817	−4	827
19,320	51.75983437	−4	828
19,300	51.8134715	−4	829
19,270	51.89413596	−4	830
19,250	51.94805195	−4	831
19,230	52.00208008	−4	832
19,200	52.08333333	−4	833
19,180	52.13764338	−4	834
19,160	52.19206681	−4	835
19,130	52.27391532	−4	836
19,110	52.32862376	−4	837
19,090	52.38344683	−4	838
19,070	52.4383849	−4	839
19,040	52.5210084	−4	840
19,020	52.57623554	−4	841
19,000	52.63157895	−4	842
18,970	52.71481286	−4	843
18,950	52.77044855	−4	844
18,930	52.8262018	−4	845
18,910	52.88207298	−4	846
18,890	52.93806247	−4	847
18,860	53.02226935	−4	848
18,840	53.07855626	−4	849
18,820	53.13496281	−4	850
18,800	53.19148936	−4	851
18,770	53.27650506	−4	852
18,750	53.33333333	−4	853
18,730	53.39028297	−4	854
18,710	53.44735436	−4	855
18,690	53.50454789	−4	856
18,660	53.59056806	−4	857
18,640	53.64806867	−4	858
18,620	53.7056928	−4	859
18,600	53.76344086	−4	860
18,580	53.82131324	−4	861
18,560	53.87931034	−4	862
18,530	53.96654074	−4	863
18,510	54.02485143	−4	864
18,490	54.08328826	−4	865
18,470	54.14185165	−4	866
18,450	54.20054201	−4	867
18,430	54.25935974	−4	868
18,410	54.31830527	−4	869
18,390	54.37737901	−4	870
18,360	54.46623094	−4	871
18,340	54.52562704	−4	872
18,320	54.58515284	−4	873
18,300	54.64480874	−4	874

Period (ns)	Frequency (kHz)	Exponent	Mantissa
18,280	54.70459519	−4	875
18,260	54.7645126	−4	876
18,240	54.8245614	−4	877
18,220	54.88474204	−4	878
18,200	54.94505495	−4	879
18,180	55.00550055	−4	880
18,160	55.0660793	−4	881
18,140	55.12679162	−4	882
18,120	55.18763797	−4	883
18,090	55.27915976	−4	884
18,070	55.34034311	−4	885
18,050	55.40166205	−4	886
18,030	55.46311703	−4	887
18,010	55.5247085	−4	888
17,990	55.58643691	−4	889
17,970	55.64830273	−4	890
17,950	55.71030641	−4	891
17,930	55.77244841	−4	892
17,910	55.8347292	−4	893
17,890	55.89714925	−4	894
17,870	55.95970901	−4	895
17,850	56.02240896	−4	896
17,830	56.08524958	−4	897
17,810	56.14823133	−4	898
17,790	56.21135469	−4	899
17,770	56.27462015	−4	900
17,750	56.33802817	−4	901
17,730	56.40157924	−4	902
17,710	56.46527386	−4	903
17,690	56.52911249	−4	904
17,670	56.59309564	−4	905
17,660	56.62514156	−4	906
17,640	56.6893424	−4	907
17,620	56.75368899	−4	908
17,600	56.81818182	−4	909
17,580	56.88282139	−4	910
17,560	56.9476082	−4	911
17,540	57.01254276	−4	912
17,520	57.07762557	−4	913
17,500	57.14285714	−4	914
17,480	57.20823799	−4	915
17,460	57.27376861	−4	916
17,440	57.33944954	−4	917
17,420	57.40528129	−4	918
17,410	57.43825388	−4	919
17,390	57.50431282	−4	920
17,370	57.57052389	−4	921
17,350	57.63688761	−4	922
17,330	57.7034045	−4	923
17,310	57.7700751	−4	924
17,290	57.83689994	−4	925
17,270	57.90387956	−4	926
17,250	57.97101449	−4	928

Period (ns)	Frequency (kHz)	Exponent	Mantissa
17,240	58.00464037	−4	928
17,220	58.07200929	−4	929
17,200	58.13953488	−4	930
17,180	58.20721769	−4	931
17,160	58.27505828	−4	932
17,140	58.34305718	−4	933
17,130	58.37711617	−4	934
17,110	58.44535359	−4	935
17,090	58.51375073	−4	936
17,070	58.58230814	−4	937
17,050	58.65102639	−4	938
17,030	58.71990605	−4	940
17,020	58.75440658	−4	940
17,000	58.82352941	−4	941
16,980	58.89281508	−4	942
16,960	58.96226415	−4	943
16,940	59.03187721	−4	945
16,930	59.06674542	−4	945
16,910	59.13660556	−4	946
16,890	59.20663114	−4	947
16,870	59.27682276	−4	948
16,850	59.34718101	−4	950
16,840	59.3824228	−4	950
16,820	59.4530321	−4	951
16,800	59.52380952	−4	952
16,780	59.59475566	−4	954
16,770	59.63029219	−4	954
16,750	59.70149254	−4	955
16,730	59.77286312	−4	956
16,710	59.84440455	−4	958
16,700	59.88023952	−4	958
16,680	59.95203837	−4	959
16,660	60.0240096	−4	960
16,640	60.09615385	−4	962
16,630	60.13229104	−4	962
16,610	60.20469597	−4	963
16,590	60.27727547	−4	964
16,580	60.31363088	−4	965
16,560	60.38647343	−4	966
16,540	60.45949214	−4	967
16,520	60.53268765	−4	969
16,510	60.56935191	−4	969
16,490	60.64281383	−4	970
16,470	60.71645416	−4	971
16,460	60.75334143	−4	972
16,440	60.82725061	−4	973
16,420	60.90133983	−4	974
16,410	60.93845216	−4	975
16,390	61.01281269	−4	976
16,370	61.08735492	−4	977
16,350	61.16207951	−4	979
16,340	61.1995104	−4	979
16,320	61.2745098	−4	980

Period (ns)	Frequency (kHz)	Exponent	Mantissa
16,300	61.34969325	−4	982
16,290	61.38735421	−4	982
16,270	61.462815	−4	983
16,260	61.50061501	−4	984
16,240	61.57635468	−4	985
16,220	61.65228113	−4	986
16,210	61.69031462	−4	987
16,190	61.76652254	−4	988
16,170	61.84291899	−4	989
16,160	61.88118812	−4	990
16,140	61.95786865	−4	991
16,120	62.03473945	−4	993
16,110	62.07324643	−4	993
16,090	62.15040398	−4	994
16,080	62.18905473	−4	995
16,060	62.26650062	−4	996
16,040	62.34413965	−4	998
16,030	62.38303182	−4	998
16,010	62.4609619	−4	999
16,000	62.5	−4	1000
15,980	62.57822278	−4	1001
15,960	62.6566416	−4	1003
15,950	62.69592476	−4	1003
15,930	62.77463905	−4	1004
15,920	62.81407035	−4	1005
15,900	62.89308176	−4	1006
15,880	62.97229219	−4	1008
15,870	63.01197227	−4	1008
15,850	63.09148265	−4	1009
15,840	63.13131313	−4	1010
15,820	63.21112516	−4	1011
15,810	63.25110689	−4	1012
15,790	63.33122229	−4	1013
15,770	63.4115409	−4	1015
15,760	63.45177665	−4	1015
15,740	63.53240152	−4	1017
15,730	63.57279085	−4	1017
15,710	63.65372374	−4	1018
15,700	63.69426752	−4	1019
15,680	63.7755102	−4	1020
15,670	63.81620932	−4	1021
15,650	63.89776358	−4	1022
15,640	63.93861893	−4	1023
15,620	64.02048656	−3	512
15,590	64.14368185	−3	513
15,560	64.26735219	−3	514
15,530	64.39150032	−3	515
15,500	64.51612903	−3	516
15,470	64.64124111	−3	517
15,440	64.76683938	−3	518
15,410	64.89292667	−3	519
15,380	65.01950585	−3	520
15,350	65.1465798	−3	521
15,320	65.27415144	−3	522
15,290	65.40222368	−3	523
15,260	65.53079948	−3	524
15,230	65.65988181	−3	525
15,200	65.78947368	−3	526
15,180	65.87615283	−3	527
15,150	66.00660066	−3	528
15,120	66.13756614	−3	529
15,090	66.26905235	−3	530
15,060	66.40106242	−3	531
15,030	66.53359947	−3	532
15,000	66.66666667	−3	533
14,980	66.75567423	−3	534
14,950	66.88963211	−3	535
14,920	67.02412869	−3	536
14,890	67.15916723	−3	537
14,860	67.29475101	−3	538
14,840	67.38544474	−3	539
14,810	67.52194463	−3	540
14,780	67.65899865	−3	541
14,760	67.75067751	−3	542
14,730	67.88866259	−3	543
14,700	68.02721088	−3	544
14,670	68.16632584	−3	545
14,650	68.25938567	−3	546
14,620	68.3994528	−3	547
14,590	68.54009596	−3	548
14,570	68.63417982	−3	549
14,540	68.77579092	−3	550
14,510	68.91798759	−3	551
14,490	69.01311249	−3	552
14,460	69.15629322	−3	553
14,440	69.25207756	−3	554
14,410	69.3962526	−3	555
14,380	69.54102921	−3	556
14,360	69.63788301	−3	557
14,330	69.78367062	−3	558
14,310	69.88120196	−3	559
14,280	70.0280112	−3	560
14,260	70.12622721	−3	561
14,230	70.27406887	−3	562
14,200	70.42253521	−3	563
14,180	70.52186178	−3	564
14,150	70.67137809	−3	565
14,130	70.77140835	−3	566
14,100	70.92198582	−3	567
14,080	71.02272727	−3	568
14,050	71.17437722	−3	569
14,030	71.27583749	−3	570
14,010	71.37758744	−3	571
13,980	71.53075823	−3	572
13,960	71.63323782	−3	573
13,930	71.78750897	−3	574

Period (ns)	Frequency (kHz)	Exponent	Mantissa
13,910	71.8907261	−3	575
13,880	72.04610951	−3	576
13,860	72.15007215	−3	577
13,840	72.25433526	−3	578
13,810	72.41129616	−3	579
13,790	72.51631617	−3	580
13,760	72.6744186	−3	581
13,740	72.78020378	−3	582
13,720	72.88629738	−3	583
13,690	73.04601899	−3	584
13,670	73.15288954	−3	585
13,650	73.26007326	−3	586
13,620	73.42143906	−3	587
13,600	73.52941176	−3	588
13,580	73.6377025	−3	589
13,550	73.80073801	−3	590
13,530	73.90983001	−3	591
13,510	74.019245	−3	592
13,490	74.12898443	−3	593
13,460	74.29420505	−3	594
13,440	74.4047619	−3	595
13,420	74.51564829	−3	596
13,400	74.62686567	−3	597
13,370	74.79431563	−3	598
13,350	74.90636704	−3	599
13,330	75.01875469	−3	600
13,310	75.13148009	−3	601
13,280	75.30120482	−3	602
13,260	75.4147813	−3	603
13,240	75.52870091	−3	604
13,220	75.6429652	−3	605
13,200	75.75757576	−3	606
13,170	75.93014427	−3	607
13,150	76.04562738	−3	608
13,130	76.1614623	−3	609
13,110	76.27765065	−3	610
13,090	76.39419404	−3	611
13,070	76.51109411	−3	612
13,050	76.62835249	−3	613
13,020	76.80491551	−3	614
13,000	76.92307692	−3	615
12,980	77.04160247	−3	616
12,960	77.16049383	−3	617
12,940	77.2797527	−3	618
12,920	77.3993808	−3	619
12,900	77.51937984	−3	620
12,880	77.63975155	−3	621
12,860	77.76049767	−3	622
12,840	77.88161994	−3	623
12,820	78.00312012	−3	624
12,800	78.125	−3	625
12,770	78.30853563	−3	626
12,750	78.43137255	−3	627

Period (ns)	Frequency (kHz)	Exponent	Mantissa
12,730	78.55459544	−3	628
12,710	78.67820614	−3	629
12,690	78.80220646	−3	630
12,670	78.92659826	−3	631
12,650	79.0513834	−3	632
12,630	79.17656374	−3	633
12,610	79.30214116	−3	634
12,590	79.42811755	−3	635
12,570	79.55449483	−3	636
12,550	79.6812749	−3	637
12,530	79.8084597	−3	638
12,510	79.93605116	−3	639
12,500	80	−3	640
12,480	80.12820513	−3	641
12,460	80.25682183	−3	642
12,440	80.38585209	−3	643
12,420	80.51529791	−3	644
12,400	80.64516129	−3	645
12,380	80.77544426	−3	646
12,360	80.90614887	−3	647
12,340	81.03727715	−3	648
12,320	81.16883117	−3	649
12,300	81.30081301	−3	650
12,280	81.43322476	−3	651
12,260	81.56606852	−3	653
12,250	81.63265306	−3	653
12,230	81.76614881	−3	654
12,210	81.9000819	−3	655
12,190	82.03445447	−3	656
12,170	82.16926869	−3	657
12,150	82.30452675	−3	658
12,130	82.44023083	−3	660
12,120	82.50825083	−3	660
12,100	82.6446281	−3	661
12,080	82.78145695	−3	662
12,060	82.91873964	−3	663
12,040	83.05647841	−3	664
12,030	83.12551953	−3	665
12,010	83.26394671	−3	666
11,990	83.4028357	−3	667
11,970	83.54218881	−3	668
11,950	83.68200837	−3	669
11,940	83.7520938	−3	670
11,920	83.89261745	−3	671
11,900	84.03361345	−3	672
11,880	84.17508418	−3	673
11,860	84.31703204	−3	675
11,850	84.38818565	−3	675
11,830	84.53085376	−3	676
11,810	84.67400508	−3	677
11,790	84.81764207	−3	679
11,780	84.88964346	−3	679
11,760	85.03401361	−3	680

Period (ns)	Frequency (kHz)	Exponent	Mantissa
11,740	85.17887564	−3	681
11,730	85.2514919	−3	682
11,710	85.3970965	−3	683
11,690	85.54319932	−3	684
11,670	85.68980291	−3	686
11,660	85.76329331	−3	686
11,640	85.91065292	−3	687
11,620	86.05851979	−3	688
11,610	86.13264427	−3	689
11,590	86.28127696	−3	690
11,570	86.43042351	−3	691
11,560	86.50519031	−3	692
11,540	86.65511265	−3	693
11,520	86.80555556	−3	694
11,510	86.88097307	−3	695
11,490	87.03220191	−3	696
11,470	87.18395815	−3	697
11,460	87.2600349	−3	698
11,440	87.41258741	−3	699
11,420	87.56567426	−3	701
11,410	87.64241893	−3	701
11,390	87.79631255	−3	702
11,370	87.95074758	−3	704
11,360	88.02816901	−3	704
11,340	88.18342152	−3	705
11,330	88.26125331	−3	706
11,310	88.4173298	−3	707
11,290	88.57395926	−3	709
11,280	88.65248227	−3	709
11,260	88.80994671	−3	710
11,250	88.88888889	−3	711
11,230	89.04719501	−3	712
11,220	89.12655971	−3	713
11,200	89.28571429	−3	714
11,180	89.44543828	−3	716
11,170	89.52551477	−3	716
11,150	89.68609865	−3	717
11,140	89.76660682	−3	718
11,120	89.92805755	−3	719
11,110	90.0090009	−3	720
11,090	90.17132552	−3	721
11,080	90.25270758	−3	722
11,060	90.4159132	−3	723
11,040	90.57971014	−3	725
11,030	90.66183137	−3	725
11,010	90.82652134	−3	727
11,000	90.90909091	−3	727
10,980	91.07468124	−3	729
10,970	91.15770283	−3	729
10,950	91.32420091	−3	731
10,940	91.40767824	−3	731
10,920	91.57509158	−3	733
10,910	91.65902841	−3	733

Period (ns)	Frequency (kHz)	Exponent	Mantissa
10,890	91.82736455	−3	735
10,880	91.91176471	−3	735
10,860	92.08103131	−3	737
10,850	92.16589862	−3	737
10,840	92.25092251	−3	738
10,820	92.42144177	−3	739
10,810	92.50693802	−3	740
10,790	92.67840593	−3	741
10,780	92.76437848	−3	742
10,760	92.93680297	−3	743
10,750	93.02325581	−3	744
10,730	93.19664492	−3	746
10,720	93.28358209	−3	746
10,700	93.45794393	−3	748
10,690	93.5453695	−3	748
10,680	93.6329588	−3	749
10,660	93.80863039	−3	750
10,650	93.89671362	−3	751
10,630	94.07337723	−3	753
10,620	94.16195857	−3	753
10,610	94.25070688	−3	754
10,590	94.42870633	−3	755
10,580	94.51795841	−3	756
10,560	94.6969697	−3	758
10,550	94.78672986	−3	758
10,540	94.87666034	−3	759
10,520	95.05703422	−3	760
10,510	95.14747859	−3	761
10,490	95.32888465	−3	763
10,480	95.41984733	−3	763
10,470	95.51098376	−3	764
10,450	95.6937799	−3	766
10,440	95.78544061	−3	766
10,430	95.87727709	−3	767
10,410	96.06147935	−3	768
10,400	96.15384615	−3	769
10,380	96.33911368	−3	771
10,370	96.43201543	−3	771
10,360	96.52509653	−3	772
10,340	96.71179884	−3	774
10,330	96.8054211	−3	774
10,320	96.89922481	−3	775
10,300	97.08737864	−3	777
10,290	97.18172983	−3	777
10,280	97.27626459	−3	778
10,260	97.46588694	−3	780
10,250	97.56097561	−3	780
10,240	97.65625	−3	781
10,230	97.75171065	−3	782
10,210	97.94319295	−3	784
10,200	98.03921569	−3	784
10,190	98.13542689	−3	785
10,170	98.32841691	−3	787

Period (ns)	Frequency (kHz)	Exponent	Mantissa
10,160	98.42519685	−3	787
10,150	98.52216749	−3	788
10,130	98.71668312	−3	790
10,120	98.81422925	−3	791
10,110	98.91196835	−3	791
10,100	99.00990099	−3	792
10,080	99.20634921	−3	794
10,070	99.30486594	−3	794
10,060	99.40357853	−3	795
10,050	99.50248756	−3	796
10,030	99.70089731	−3	798
10,020	99.8003992	−3	798
10,010	99.9000999	−3	799
10,000	100	−3	800
9980	100.2004008	−3	802
9970	100.3009027	−3	802
9960	100.4016064	−3	803
9950	100.5025126	−3	804
9930	100.7049345	−3	806
9920	100.8064516	−3	806
9910	100.9081736	−3	807
9900	101.010101	−3	808
9880	101.2145749	−3	810
9870	101.3171226	−3	811
9860	101.4198783	−3	811
9850	101.5228426	−3	812
9840	101.6260163	−3	813
9820	101.8329939	−3	815
9810	101.9367992	−3	815
9800	102.0408163	−3	816
9790	102.145046	−3	817
9770	102.3541453	−3	819
9760	102.4590164	−3	820
9750	102.5641026	−3	821
9740	102.6694045	−3	821
9730	102.7749229	−3	822
9720	102.8806584	−3	823
9700	103.0927835	−3	825
9690	103.1991744	−3	826
9680	103.3057851	−3	826
9670	103.4126163	−3	827
9660	103.5196687	−3	828
9650	103.626943	−3	829
9630	103.8421599	−3	831
9620	103.950104	−3	832
9610	104.0582726	−3	832
9600	104.1666667	−3	833
9590	104.2752868	−3	834
9580	104.3841336	−3	835
9560	104.6025105	−3	837
9550	104.7120419	−3	838
9540	104.8218029	−3	839
9530	104.9317943	−3	839
9520	105.0420168	−3	840
9510	105.1524711	−3	841
9500	105.2631579	−3	842
9480	105.4852321	−3	844
9470	105.5966209	−3	845
9460	105.7082452	−3	846
9450	105.8201058	−3	847
9440	105.9322034	−3	847
9430	106.0445387	−3	848
9420	106.1571125	−3	849
9410	106.2699256	−3	850
9400	106.3829787	−3	851
9380	106.6098081	−3	853
9370	106.7235859	−3	854
9360	106.8376068	−3	855
9350	106.9518717	−3	856
9340	107.0663812	−3	857
9330	107.1811361	−3	857
9320	107.2961373	−3	858
9310	107.4113856	−3	859
9300	107.5268817	−3	860
9290	107.6426265	−3	861
9280	107.7586207	−3	862
9260	107.9913607	−3	864
9250	108.1081081	−3	865
9240	108.2251082	−3	866
9230	108.3423619	−3	867
9220	108.4598698	−3	868
9210	108.577633	−3	869
9200	108.6956522	−3	870
9190	108.8139282	−3	871
9180	108.9324619	−3	871
9170	109.0512541	−3	872
9160	109.1703057	−3	873
9150	109.2896175	−3	874
9140	109.4091904	−3	875
9130	109.5290252	−3	876
9120	109.6491228	−3	877
9110	109.7694841	−3	878
9100	109.8901099	−3	879
9090	110.0110011	−3	880
9080	110.1321586	−3	881
9070	110.2535832	−3	882
9060	110.3752759	−3	883
9040	110.619469	−3	885
9030	110.7419712	−3	886
9020	110.864745	−3	887
9010	110.9877913	−3	888
9000	111.1111111	−3	889
8990	111.2347052	−3	890
8980	111.3585746	−3	891
8970	111.4827202	−3	892
8960	111.6071429	−3	893

Period (ns)	Frequency (kHz)	Exponent	Mantissa
8950	111.7318436	−3	894
8940	111.8568233	−3	895
8930	111.9820829	−3	896
8920	112.1076233	−3	897
8910	112.2334456	−3	898
8900	112.3595506	−3	899
8890	112.4859393	−3	900
8880	112.6126126	−3	901
8870	112.7395716	−3	902
8860	112.8668172	−3	903
8850	112.9943503	−3	904
8840	113.1221719	−3	905
8830	113.2502831	−3	906
8820	113.3786848	−3	907
8810	113.507378	−3	908
8800	113.6363636	−3	909
8790	113.7656428	−3	910
8780	113.8952164	−3	911
8770	114.0250855	−3	912
8760	114.1552511	−3	913
8750	114.2857143	−3	914
8740	114.416476	−3	915
8730	114.5475372	−3	916
8720	114.6788991	−3	917
8710	114.8105626	−3	918
8700	114.9425287	−3	920
8690	115.0747986	−3	921
8680	115.2073733	−3	922
8670	115.3402537	−3	923
8660	115.4734411	−3	924
8650	115.6069364	−3	925
8640	115.7407407	−3	926
8630	115.8748552	−3	927
8620	116.0092807	−3	928
8610	116.1440186	−3	929
8600	116.2790698	−3	930
8590	116.4144354	−3	931
8580	116.5501166	−3	932
8570	116.6861144	−3	933
8560	116.8224299	−3	935
8550	116.9590643	−3	936
8540	117.0960187	−3	937
8530	117.2332943	−3	938
8520	117.370892	−3	939
8510	117.5088132	−3	940
8500	117.6470588	−3	941
8490	117.7856302	−3	942
8480	117.9245283	−3	943
8470	118.0637544	−3	945
8460	118.2033097	−3	946
8450	118.3431953	−3	947
8440	118.4834123	−3	948
8430	118.623962	−3	949

Period (ns)	Frequency (kHz)	Exponent	Mantissa
8420	118.7648456	−3	950
8410	118.9060642	−3	951
8400	119.047619	−3	952
8390	119.1895113	−3	954
8380	119.3317422	−3	955
8370	119.474313	−3	956
8360	119.6172249	−3	957
8350	119.760479	−3	958
8340	119.9040767	−3	959
8330	120.0480192	−3	960
8320	120.1923077	−3	962
8310	120.3369434	−3	963
8300	120.4819277	−3	964
8290	120.6272618	−3	965
8280	120.7729469	−3	966
8270	120.9189843	−3	967
8260	121.0653753	−3	969
8250	121.2121212	−3	970
8240	121.3592233	−3	971
8230	121.5066829	−3	972
8220	121.6545012	−3	973
8210	121.8026797	−3	974
8200	121.9512195	−3	976
8190	122.1001221	−3	977
8180	122.2493888	−3	978
8170	122.3990208	−3	979
8160	122.5490196	−3	980
8150	122.6993865	−3	982
8140	122.8501229	−3	983
8130	123.00123	−3	984
8120	123.1527094	−3	985
8110	123.3045623	−3	986
8100	123.4567901	−3	988
8090	123.6093943	−3	989
8080	123.7623762	−3	990
8070	123.9157373	−3	991
8060	124.0694789	−3	993
8050	124.2236025	−3	994
8040	124.3781095	−3	995
8030	124.5330012	−3	996
8020	124.6882793	−3	998
8010	124.8439451	−3	999
8000	125	−3	1000
7990	125.1564456	−3	1001
7980	125.3132832	−3	1003
7970	125.4705144	−3	1004
7960	125.6281407	−3	1005
7950	125.7861635	−3	1006
7940	125.9445844	−3	1008
7930	126.1034048	−3	1009
7920	126.2626263	−3	1010
7910	126.4222503	−3	1011
7900	126.5822785	−3	1013

Period (ns)	Frequency (kHz)	Exponent	Mantissa
7890	126.7427123	−3	1014
7880	126.9035533	−3	1015
7870	127.064803	−3	1017
7860	127.2264631	−3	1018
7850	127.388535	−3	1019
7840	127.5510204	−3	1020
7830	127.7139208	−3	1022
7820	127.8772379	−3	1023
7810	128.0409731	−2	512
7790	128.3697047	−2	513
7780	128.5347044	−2	514
7760	128.8659794	−2	515
7750	129.0322581	−2	516
7730	129.3661061	−2	517
7720	129.5336788	−2	518
7700	129.8701299	−2	519
7690	130.0390117	−2	520
7670	130.3780965	−2	522
7660	130.5483029	−2	522
7640	130.8900524	−2	524
7630	131.061599	−2	524
7610	131.4060447	−2	526
7600	131.5789474	−2	526
7590	131.7523057	−2	527
7570	132.1003963	−2	528
7560	132.2751323	−2	529
7540	132.6259947	−2	531
7530	132.8021248	−2	531
7510	133.1557923	−2	533
7500	133.3333333	−2	533
7490	133.5113485	−2	534
7470	133.8688086	−2	535
7460	134.0482574	−2	536
7440	134.4086022	−2	538
7430	134.589502	−2	538
7420	134.7708895	−2	539
7400	135.1351351	−2	541
7390	135.3179973	−2	541
7380	135.501355	−2	542
7360	135.8695652	−2	543
7350	136.0544218	−2	544
7330	136.425648	−2	546
7320	136.6120219	−2	546
7310	136.7989056	−2	547
7290	137.1742112	−2	549
7280	137.3626374	−2	549
7270	137.5515818	−2	550
7250	137.9310345	−2	552
7240	138.121547	−2	552
7230	138.3125864	−2	553
7220	138.5041551	−2	554
7200	138.8888889	−2	556
7190	139.0820584	−2	556

Period (ns)	Frequency (kHz)	Exponent	Mantissa
7180	139.275766	−2	557
7160	139.6648045	−2	559
7150	139.8601399	−2	559
7140	140.0560224	−2	560
7130	140.2524544	−2	561
7110	140.6469761	−2	563
7100	140.8450704	−2	563
7090	141.0437236	−2	564
7070	141.4427157	−2	566
7060	141.6430595	−2	567
7050	141.8439716	−2	567
7040	142.0454545	−2	568
7020	142.4501425	−2	570
7010	142.6533524	−2	571
7000	142.8571429	−2	571
6990	143.0615165	−2	572
6980	143.2664756	−2	573
6960	143.6781609	−2	575
6950	143.8848921	−2	576
6940	144.092219	−2	576
6930	144.3001443	−2	577
6920	144.5086705	−2	578
6900	144.9275362	−2	580
6890	145.137881	−2	581
6880	145.3488372	−2	581
6870	145.5604076	−2	582
6860	145.7725948	−2	583
6840	146.1988304	−2	585
6830	146.4128843	−2	586
6820	146.627566	−2	587
6810	146.8428781	−2	587
6800	147.0588235	−2	588
6790	147.275405	−2	589
6770	147.7104874	−2	591
6760	147.9289941	−2	592
6750	148.1481481	−2	593
6740	148.3679525	−2	593
6730	148.5884101	−2	594
6720	148.8095238	−2	595
6710	149.0312966	−2	596
6700	149.2537313	−2	597
6680	149.7005988	−2	599
6670	149.9250375	−2	600
6660	150.1501502	−2	601
6650	150.3759398	−2	602
6640	150.6024096	−2	602
6630	150.8295626	−2	603
6620	151.0574018	−2	604
6610	151.2859304	−2	605
6600	151.5151515	−2	606
6580	151.9756839	−2	608
6570	152.2070015	−2	609
6560	152.4390244	−2	610

Period (ns)	Frequency (kHz)	Exponent	Mantissa
6550	152.6717557	−2	611
6540	152.9051988	−2	612
6530	153.1393568	−2	613
6520	153.3742331	−2	613
6510	153.609831	−2	614
6500	153.8461538	−2	615
6490	154.0832049	−2	616
6480	154.3209877	−2	617
6470	154.5595054	−2	618
6460	154.7987616	−2	619
6450	155.0387597	−2	620
6440	155.2795031	−2	621
6430	155.5209953	−2	622
6420	155.7632399	−2	623
6410	156.0062402	−2	624
6400	156.25	−2	625
6380	156.7398119	−2	627
6370	156.9858713	−2	628
6360	157.2327044	−2	629
6350	157.480315	−2	630
6340	157.7287066	−2	631
6330	157.9778831	−2	632
6320	158.2278481	−2	633
6310	158.4786054	−2	634
6300	158.7301587	−2	635
6290	158.9825119	−2	636
6280	159.2356688	−2	637
6270	159.4896332	−2	638
6260	159.7444089	−2	639
6250	160	−2	640
6240	160.2564103	−2	641
6230	160.5136437	−2	642
6220	160.7717042	−2	643
6210	161.0305958	−2	644
6200	161.2903226	−2	645
6190	161.5508885	−2	646
6180	161.8122977	−2	647
6170	162.0745543	−2	648
6160	162.3376623	−2	649
6150	162.601626	−2	650
6140	162.8664495	−2	651
6130	163.132137	−2	653
6120	163.3986928	−2	654
6110	163.6661211	−2	655
6100	163.9344262	−2	656
6090	164.2036125	−2	657
6080	164.4736842	−2	658
6070	164.7446458	−2	659
6060	165.0165017	−2	660
6050	165.2892562	−2	661
6040	165.5629139	−2	662
6030	165.8374793	−2	663
6020	166.1129568	−2	664

Period (ns)	Frequency (kHz)	Exponent	Mantissa
6010	166.3893511	−2	666
6000	166.6666667	−2	667
5990	166.9449082	−2	668
5980	167.2240803	−2	669
5970	167.5041876	−2	670
5960	167.7852349	−2	671
5950	168.0672269	−2	672
5940	168.3501684	−2	673
5930	168.6340641	−2	675
5920	168.9189189	−2	676
5910	169.2047377	−2	677
5900	169.4915254	−2	678
5890	169.7792869	−2	679
5880	170.0680272	−2	680
5870	170.3577513	−2	681
5860	170.6484642	−2	683
5850	170.9401709	−2	684
5840	171.2328767	−2	685
5830	171.5265866	−2	686
5820	171.8213058	−2	687
5810	172.1170396	−2	688
5800	172.4137931	−2	690
5790	172.7115717	−2	691
5780	173.0103806	−2	692
5770	173.3102253	−2	693
5760	173.6111111	−2	694
5750	173.9130435	−2	696
5740	174.2160279	−2	697
5730	174.5200698	−2	698
5720	174.8251748	−2	699
5710	175.1313485	−2	701
5700	175.4385965	−2	702
5690	175.7469244	−2	703
5680	176.056338	−2	704
5670	176.366843	−2	705
5660	176.6784452	−2	707
5650	176.9911504	−2	708
5640	177.3049645	−2	709
5630	177.6198934	−2	710
5620	177.9359431	−2	712
5610	178.2531194	−2	713
5600	178.5714286	−2	714
5590	178.8908766	−2	716
5580	179.2114695	−2	717
5570	179.5332136	−2	718
5560	179.8561151	−2	719
5550	180.1801802	−2	721
5540	180.5054152	−2	722
5530	180.8318264	−2	723
5520	181.1594203	−2	725
5510	181.4882033	−2	726
5500	181.8181818	−2	727
5490	182.1493625	−2	729

Period (ns)	Frequency (kHz)	Exponent	Mantissa
5480	182.4817518	−2	730
5470	182.8153565	−2	731
5460	183.1501832	−2	733
5450	183.4862385	−2	734
5440	183.8235294	−2	735
5430	184.1620626	−2	737
5420	184.501845	−2	738
5410	184.8428835	−2	739
5400	185.1851852	−2	741
5390	185.528757	−2	742
5380	185.8736059	−2	743
5370	186.2197393	−2	745
5360	186.5671642	−2	746
5350	186.9158879	−2	748
5340	187.2659176	−2	749
5330	187.6172608	−2	750
5320	187.9699248	−2	752
5310	188.3239171	−2	753
5300	188.6792453	−2	755
5290	189.0359168	−2	756
5280	189.3939394	−2	758
5270	189.7533207	−2	759
5260	190.1140684	−2	760
5250	190.4761905	−2	762
5240	190.8396947	−2	763
5230	191.2045889	−2	765
5220	191.5708812	−2	766
5210	191.9385797	−2	768
5200	192.3076923	−2	769
5190	192.6782274	−2	771
5180	193.0501931	−2	772
5170	193.4235977	−2	774
5160	193.7984496	−2	775
5150	194.1747573	−2	777
5140	194.5525292	−2	778
5130	194.9317739	−2	780
5120	195.3125	−2	781
5110	195.6947162	−2	783
5100	196.0784314	−2	784
5090	196.4636542	−2	786
5080	196.8503937	−2	787
5070	197.2386588	−2	789
5060	197.6284585	−2	791
5050	198.019802	−2	792
5040	198.4126984	−2	794
5030	198.8071571	−2	795
5020	199.2031873	−2	797
5010	199.6007984	−2	798
5000	200	−2	800
4990	200.4008016	−2	802
4980	200.8032129	−2	803
4970	201.2072435	−2	805
4960	201.6129032	−2	806

Period (ns)	Frequency (kHz)	Exponent	Mantissa
4950	202.020202	−2	808
4940	202.4291498	−2	810
4930	202.8397566	−2	811
4920	203.2520325	−2	813
4910	203.6659878	−2	815
4900	204.0816327	−2	816
4890	204.4989775	−2	818
4880	204.9180328	−2	820
4870	205.338809	−2	821
4860	205.7613169	−2	823
4850	206.185567	−2	825
4840	206.6115702	−2	826
4830	207.0393375	−2	828
4820	207.4688797	−2	830
4810	207.9002079	−2	832
4800	208.3333333	−2	833
4790	208.7682672	−2	835
4780	209.2050209	−2	837
4770	209.6436059	−2	839
4760	210.0840336	−2	840
4750	210.5263158	−2	842
4740	210.9704641	−2	844
4730	211.4164905	−2	846
4720	211.8644068	−2	847
4710	212.3142251	−2	849
4700	212.7659574	−2	851
4690	213.2196162	−2	853
4680	213.6752137	−2	855
4670	214.1327623	−2	857
4660	214.5922747	−2	858
4650	215.0537634	−2	860
4640	215.5172414	−2	862
4630	215.9827214	−2	864
4620	216.4502165	−2	866
4610	216.9197397	−2	868
4600	217.3913043	−2	870
4590	217.8649237	−2	871
4580	218.3406114	−2	873
4570	218.8183807	−2	875
4560	219.2982456	−2	877
4550	219.7802198	−2	879
4540	220.2643172	−2	881
4530	220.7505519	−2	883
4520	221.2389381	−2	885
4510	221.72949	−2	887
4500	222.2222222	−2	889
4490	222.7171492	−2	891
4480	223.2142857	−2	893
4470	223.7136465	−2	895
4460	224.2152466	−2	897
4450	224.7191011	−2	899
4440	225.2252252	−2	901
4430	225.7336343	−2	903

Period (ns)	Frequency (kHz)	Exponent	Mantissa
4420	226.2443439	−2	905
4410	226.7573696	−2	907
4400	227.2727273	−2	909
4390	227.7904328	−2	911
4380	228.3105023	−2	913
4370	228.8329519	−2	915
4360	229.3577982	−2	917
4350	229.8850575	−2	920
4340	230.4147465	−2	922
4330	230.9468822	−2	924
4320	231.4814815	−2	926
4310	232.0185615	−2	928
4300	232.5581395	−2	930
4290	233.1002331	−2	932
4280	233.6448598	−2	935
4270	234.1920375	−2	937
4260	234.741784	−2	939
4250	235.2941176	−2	941
4240	235.8490566	−2	943
4230	236.4066194	−2	946
4220	236.9668246	−2	948
4210	237.5296912	−2	950
4200	238.0952381	−2	952
4190	238.6634845	−2	955
4180	239.2344498	−2	957
4170	239.8081535	−2	959
4160	240.3846154	−2	962
4150	240.9638554	−2	964
4140	241.5458937	−2	966
4130	242.1307506	−2	969
4120	242.7184466	−2	971
4110	243.3090024	−2	973
4100	243.902439	−2	976
4090	244.4987775	−2	978
4080	245.0980392	−2	980
4070	245.7002457	−2	983
4060	246.3054187	−2	985
4050	246.9135802	−2	988
4040	247.5247525	−2	990
4030	248.1389578	−2	993
4020	248.7562189	−2	995
4010	249.3765586	−2	998
4000	250	−2	1000
3990	250.6265664	−2	1003
3980	251.2562814	−2	1005
3970	251.8891688	−2	1008
3960	252.5252525	−2	1010
3950	253.164557	−2	1013
3940	253.8071066	−2	1015
3930	254.4529262	−2	1018
3920	255.1020408	−2	1020
3910	255.7544757	−2	1023
3900	256.4102564	−1	513

Period (ns)	Frequency (kHz)	Exponent	Mantissa
3890	257.0694087	−1	514
3880	257.7319588	−1	515
3870	258.3979328	−1	517
3860	259.0673575	−1	518
3850	259.7402597	−1	519
3840	260.4166667	−1	521
3830	261.0966057	−1	522
3820	261.7801047	−1	524
3810	262.4671916	−1	525
3800	263.1578947	−1	526
3790	263.8522427	−1	528
3780	264.5502646	−1	529
3770	265.2519894	−1	531
3760	265.9574468	−1	532
3750	266.6666667	−1	533
3740	267.3796791	−1	535
3730	268.0965147	−1	536
3720	268.8172043	−1	538
3710	269.541779	−1	539
3700	270.2702703	−1	541
3690	271.00271	−1	542
3680	271.7391304	−1	543
3670	272.479564	−1	545
3660	273.2240437	−1	546
3650	273.9726027	−1	548
3640	274.7252747	−1	549
3630	275.4820937	−1	551
3620	276.2430939	−1	552
3610	277.0083102	−1	554
3600	277.7777778	−1	556
3590	278.551532	−1	557
3580	279.3296089	−1	559
3570	280.1120448	−1	560
3560	280.8988764	−1	562
3550	281.6901408	−1	563
3540	282.4858757	−1	565
3530	283.286119	−1	567
3520	284.0909091	−1	568
3510	284.9002849	−1	570
3500	285.7142857	−1	571
3490	286.5329513	−1	573
3480	287.3563218	−1	575
3470	288.184438	−1	576
3460	289.017341	−1	578
3450	289.8550725	−1	580
3440	290.6976744	−1	581
3430	291.5451895	−1	583
3420	292.3976608	−1	585
3410	293.255132	−1	587
3400	294.1176471	−1	588
3390	294.9852507	−1	590
3380	295.8579882	−1	592
3370	296.735905	−1	593

Period (ns)	Frequency (kHz)	Exponent	Mantissa
3360	297.6190476	−1	595
3350	298.5074627	−1	597
3340	299.4011976	−1	599
3330	300.3003003	−1	601
3320	301.2048193	−1	602
3310	302.1148036	−1	604
3300	303.030303	−1	606
3290	303.9513678	−1	608
3280	304.8780488	−1	610
3270	305.8103976	−1	612
3260	306.7484663	−1	613
3250	307.6923077	−1	615
3240	308.6419753	−1	617
3230	309.5975232	−1	619
3220	310.5590062	−1	621
3210	311.5264798	−1	623
3200	312.5	−1	625
3190	313.4796238	−1	627
3180	314.4654088	−1	629
3170	315.4574132	−1	631
3160	316.4556962	−1	633
3150	317.4603175	−1	635
3140	318.4713376	−1	637
3130	319.4888179	−1	639
3120	320.5128205	−1	641
3110	321.5434084	−1	643
3100	322.5806452	−1	645
3090	323.6245955	−1	647
3080	324.6753247	−1	649
3070	325.732899	−1	651
3060	326.7973856	−1	654
3050	327.8688525	−1	656
3040	328.9473684	−1	658
3030	330.0330033	−1	660
3020	331.1258278	−1	662
3010	332.2259136	−1	664
3000	333.3333333	−1	667
2990	334.4481605	−1	669
2980	335.5704698	−1	671
2970	336.7003367	−1	673
2960	337.8378378	−1	676
2950	338.9830508	−1	678
2940	340.1360544	−1	680
2930	341.2969283	−1	683
2920	342.4657534	−1	685
2910	343.6426117	−1	687
2900	344.8275862	−1	690
2890	346.0207612	−1	692
2880	347.2222222	−1	694
2870	348.4320557	−1	697
2860	349.6503497	−1	699
2850	350.877193	−1	702
2840	352.1126761	−1	704
2830	353.3568905	−1	707
2820	354.6099291	−1	709
2810	355.8718861	−1	712
2800	357.1428571	−1	714
2790	358.4229391	−1	717
2780	359.7122302	−1	719
2770	361.0108303	−1	722
2760	362.3188406	−1	725
2750	363.6363636	−1	727
2740	364.9635036	−1	730
2730	366.3003663	−1	733
2720	367.6470588	−1	735
2710	369.00369	−1	738
2700	370.3703704	−1	741
2690	371.7472119	−1	743
2680	373.1343284	−1	746
2670	374.5318352	−1	749
2660	375.9398496	−1	752
2650	377.3584906	−1	755
2640	378.7878788	−1	758
2630	380.2281369	−1	760
2620	381.6793893	−1	763
2610	383.1417625	−1	766
2600	384.6153846	−1	769
2590	386.1003861	−1	772
2580	387.5968992	−1	775
2570	389.1050584	−1	778
2560	390.625	−1	781
2550	392.1568627	−1	784
2540	393.7007874	−1	787
2530	395.256917	−1	791
2520	396.8253968	−1	794
2510	398.4063745	−1	797
2500	400	−1	800
2490	401.6064257	−1	803
2480	403.2258065	−1	806
2470	404.8582996	−1	810
2460	406.504065	−1	813
2450	408.1632653	−1	816
2440	409.8360656	−1	820
2430	411.5226337	−1	823
2420	413.2231405	−1	826
2410	414.9377593	−1	830
2400	416.6666667	−1	833
2390	418.4100418	−1	837
2380	420.1680672	−1	840
2370	421.9409283	−1	844
2360	423.7288136	−1	847
2350	425.5319149	−1	851
2340	427.3504274	−1	855
2330	429.1845494	−1	858
2320	431.0344828	−1	862
2310	432.9004329	−1	866

Period (ns)	Frequency (kHz)	Exponent	Mantissa
2300	434.7826087	−1	870
2290	436.6812227	−1	873
2280	438.5964912	−1	877
2270	440.5286344	−1	881
2260	442.4778761	−1	885
2250	444.4444444	−1	889
2240	446.4285714	−1	893
2230	448.4304933	−1	897
2220	450.4504505	−1	901
2210	452.4886878	−1	905
2200	454.5454545	−1	909
2190	456.6210046	−1	913
2180	458.7155963	−1	917
2170	460.8294931	−1	922
2160	462.962963	−1	926
2150	465.1162791	−1	930
2140	467.2897196	−1	935
2130	469.4835681	−1	939
2120	471.6981132	−1	943
2110	473.9336493	−1	948
2100	476.1904762	−1	952
2090	478.4688995	−1	957
2080	480.7692308	−1	962
2070	483.0917874	−1	966
2060	485.4368932	−1	971
2050	487.804878	−1	976
2040	490.1960784	−1	980
2030	492.6108374	−1	985
2020	495.049505	−1	990
2010	497.5124378	−1	995
2000	500	−1	1000
1990	502.5125628	−1	1005
1980	505.0505051	−1	1010
1970	507.6142132	−1	1015
1960	510.2040816	−1	1020
1950	512.8205128	0	513
1940	515.4639175	0	515
1930	518.134715	0	518
1920	520.8333333	0	521
1910	523.5602094	0	524
1900	526.3157895	0	526
1890	529.1005291	0	529
1880	531.9148936	0	532
1870	534.7593583	0	535
1860	537.6344086	0	538
1850	540.5405405	0	541
1840	543.4782609	0	543
1830	546.4480874	0	546
1820	549.4505495	0	549
1810	552.4861878	0	552
1800	555.5555556	0	556
1790	558.6592179	0	559
1780	561.7977528	0	562

Period (ns)	Frequency (kHz)	Exponent	Mantissa
1770	564.9717514	0	565
1760	568.1818182	0	568
1750	571.4285714	0	571
1740	574.7126437	0	575
1730	578.0346821	0	578
1720	581.3953488	0	581
1710	584.7953216	0	585
1700	588.2352941	0	588
1690	591.7159763	0	592
1680	595.2380952	0	595
1670	598.8023952	0	599
1660	602.4096386	0	602
1650	606.0606061	0	606
1640	609.7560976	0	610
1630	613.4969325	0	613
1620	617.2839506	0	617
1610	621.1180124	0	621
1600	625	0	625
1590	628.9308176	0	629
1580	632.9113924	0	633
1570	636.9426752	0	637
1560	641.025641	0	641
1550	645.1612903	0	645
1540	649.3506494	0	649
1530	653.5947712	0	654
1520	657.8947368	0	658
1510	662.2516556	0	662
1500	666.6666667	0	667
1490	671.1409396	0	671
1480	675.6756757	0	676
1470	680.2721088	0	680
1460	684.9315068	0	685
1450	689.6551724	0	690
1440	694.4444444	0	694
1430	699.3006993	0	699
1420	704.2253521	0	704
1410	709.2198582	0	709
1400	714.2857143	0	714
1390	719.4244604	0	719
1380	724.6376812	0	725
1370	729.9270073	0	730
1360	735.2941176	0	735
1350	740.7407407	0	741
1340	746.2686567	0	746
1330	751.8796992	0	752
1320	757.5757576	0	758
1310	763.3587786	0	763
1300	769.2307692	0	769
1290	775.1937984	0	775
1280	781.25	0	781
1270	787.4015748	0	787
1260	793.6507937	0	794
1250	800	0	800

Period (ns)	Frequency (kHz)	Exponent	Mantissa
1240	806.4516129	0	806
1230	813.0081301	0	813
1220	819.6721311	0	820
1210	826.446281	0	826
1200	833.3333333	0	833
1190	840.3361345	0	840
1180	847.4576271	0	847
1170	854.7008547	0	855
1160	862.0689655	0	862
1150	869.5652174	0	870
1140	877.1929825	0	877
1130	884.9557522	0	885
1120	892.8571429	0	893

Period (ns)	Frequency (kHz)	Exponent	Mantissa
1110	900.9009009	0	901
1100	909.0909091	0	909
1090	917.4311927	0	917
1080	925.9259259	0	926
1070	934.5794393	0	935
1060	943.3962264	0	943
1050	952.3809524	0	952
1040	961.5384615	0	962
1030	970.8737864	0	971
1020	980.3921569	0	980
1010	990.0990099	0	990
1000	1000	0	1000

OUTLINE DIMENSIONS

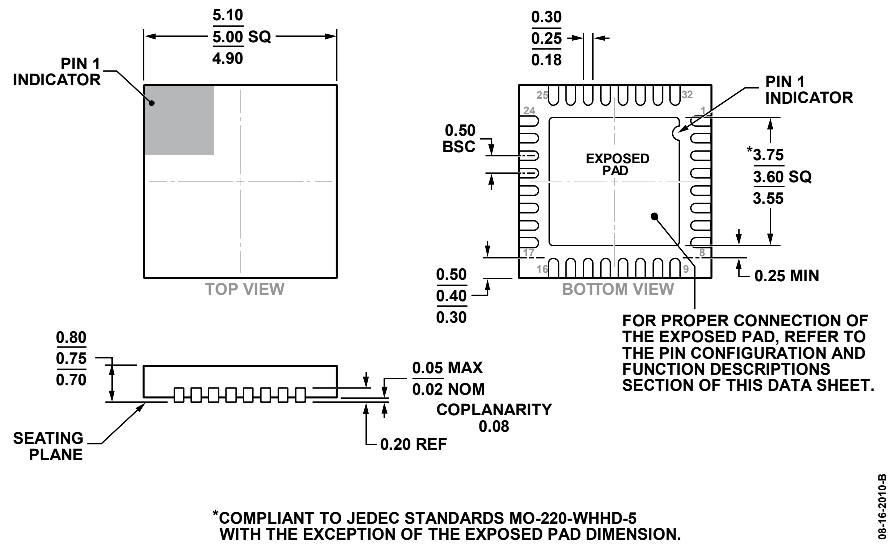


Figure 86. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1055ACPZ-RL	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADP1055ACPZ-R7	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADP1055-EVALZ		ADP1055 Evaluation Board	
ADP1055DC1-EVALZ		ADP1055 Daughter Card	
ADP-I2C-USB-Z		USB to I^2C Adapter	

[1] Z = RoHS Compliant Part.

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D12004-0-3/15(A)