

FEATURES

- Operates with 3.3 V supply
- EIA RS-422 and RS-485 compliant over full CM range
- 19 k Ω input impedance
- Up to 50 transceivers on bus
- 20 Mbps data rate
- Short-circuit protection
- Specified over full temperature range
- Thermal shutdown
- Interoperable with 5 V logic
- 840 μ A supply current
- 2 nA shutdown current
- Available in PDIP, SOIC, and TSSOP
- Meets IEC1000-4-4 (>1 kV)
- 8 ns skew
- Upgrade for MAX3491, SN75ALS180

APPLICATIONS

- Telecommunications
- DTE–DCE interface
- Packet switching
- Local area networks
- Data concentration
- Data multiplexers
- Integrated services digital network (ISDN)
- AppleTalk
- Industrial controls

GENERAL DESCRIPTION

The **ADM3491-1** is a low power, differential line transceiver designed to operate using a single 3.3 V power supply. Low power consumption, coupled with a shutdown mode, makes it ideal for power-sensitive applications. It is suitable for communication on multipoint bus transmission lines.

The **ADM3491-1** is intended for balanced data transmission and complies with both Electronic Industries Association (EIA) Standards RS-485 and RS-422. It contains a differential line driver and a differential line receiver, making it suitable for full-duplex data transfer.

FUNCTIONAL BLOCK DIAGRAM

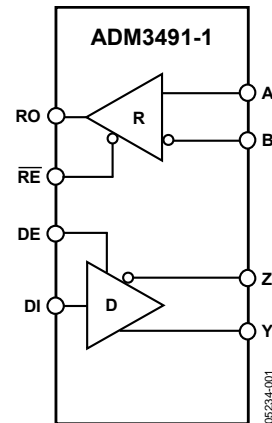


Figure 1.

The input impedance is 19 k Ω , allowing up to 50 transceivers to be connected on the bus. A thermal shutdown circuit prevents excessive power dissipation caused by bus contention or by output shorting. This feature forces the driver output into a high impedance state if a significant temperature increase is detected in the internal driver circuitry during fault conditions.

If the inputs are unconnected (floating), the receiver contains a fail-safe feature that results in a logic high output state.

The **ADM3491-1** is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology.

Rev. C

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REVISION HISTORY

6/14—Rev. B to Rev. C

Changes to Ordering Guide	13
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10/06—Rev. A to Rev. B

Changes to Part Number	Universal
Updated Format.....	Universal
Changes to Features.....	1
Changes to General Description	1
Changes to Table 2.....	4
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11/04—Rev. 0 to Rev. A

Format Updated.....	Universal
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1/98—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}	2.0			V	$R_L = 100 \Omega$, $V_{CC} > 3.1 \text{ V}$, see Figure 14
	1.5			V	$R_L = 54 \Omega$, see Figure 14
	1.5			V	$R_L = 60 \Omega$, $-7 \text{ V} < V_{TST} < +12 \text{ V}$, see Figure 15
$\Delta V_{OD} $ for Complementary Output States			0.2	V	$R = 54 \Omega$ or 100Ω , see Figure 14
Common-Mode Output Voltage, V_{OC}			3	V	$R = 54 \Omega$ or 100Ω , see Figure 14
$\Delta V_{OC} $ for Complementary Output States			0.2	V	$R = 54 \Omega$ or 100Ω , see Figure 14
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0			V	
Logic Input Current (DE, DI, \overline{RE})			± 1.0	μA	
Output Leakage (Y, Z) Current			± 3	μA	$V_O = -7 \text{ V}$ or $+12 \text{ V}$, $V_{CC} = 0 \text{ V}$ or 3.6 V
Output Short-Circuit Current			± 250	mA	$V_O = -7 \text{ V}$ or $+12 \text{ V}$
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	-0.2		+0.2	V	$-7 \text{ V} < V_{CM} < +12 \text{ V}$
Input Voltage Hysteresis, ΔV_{TH}		50		mV	$V_{CM} = 0 \text{ V}$
Input Resistance	12	19		k Ω	$-7 \text{ V} < V_{CM} < +12 \text{ V}$
Input Current (A, B)			1	mA	$V_{IN} = 12 \text{ V}$
			-0.8	mA	$V_{IN} = -7 \text{ V}$
Logic Enable Input Current (\overline{RE})			± 1	μA	
Output Voltage Low, V_{OL}			0.4	V	$I_{OUT} = +2.5 \text{ mA}$
Output Voltage High, V_{OH}	$V_{CC} - 0.4 \text{ V}$			V	$I_{OUT} = -1.5 \text{ mA}$
Short-Circuit Output Current			± 60	mA	$V_{OUT} = \text{GND}$ or V_{CC}
Three-State Output Leakage Current			± 1.0	μA	$V_{CC} = 3.6 \text{ V}$, $0 \text{ V} < V_{OUT} < V_{CC}$
POWER SUPPLY CURRENT					
I_{CC}		0.84	1.5	mA	Outputs unloaded
		0.84	1.5	mA	DE = V_{CC} , $\overline{RE} = 0 \text{ V}$
		0.84	1.5	mA	DE = 0 V , $\overline{RE} = 0 \text{ V}$
Supply Current in Shutdown		0.002	1	μA	DE = 0 V , $\overline{RE} = V_{CC}$

TIMING SPECIFICATIONS

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/ Comments
DRIVER					
Differential Output Delay, T_{DD}	1		35	ns	$R_L = 60\ \Omega$, $C_{L1} = C_{L2} = 15\text{ pF}$, see Figure 18
Differential Output Transition Time	1	8	15	ns	$R_L = 60\ \Omega$, $C_{L1} = C_{L2} = 15\text{ pF}$, see Figure 18
Propagation Delay Input to Output, T_{PLH} , T_{PHL}	7	22	35	ns	$R_L = 27\ \Omega$, $C_{L1} = C_{L2} = 15\text{ pF}$, see Figure 19
Driver Output to Output, T_{SKEW}			8	ns	$R_L = 54\ \Omega$, $C_{L1} = C_{L2} = 15\text{ pF}$, see Figure 19
ENABLE/DISABLE					
Driver Enable to Output Valid		45	90	ns	$R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 16
Driver Disable Timing		40	80	ns	$R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 16
Driver Enable from Shutdown		65	110	ns	$R_L = 110\ \Omega$, $C_L = 15\text{ pF}$, see Figure 16
RECEIVER					
Time to Shutdown	80	190	300	ns	
Propagation Delay Input to Output, T_{PLH} , T_{PHL}	25	65	90	ns	$C_L = 15\text{ pF}$, see Figure 21
Skew, $T_{PLH} - T_{PHL}$			10	ns	$C_L = 15\text{ pF}$, see Figure 21
Receiver Enable, T_{EN}		25	50	ns	$C_L = 15\text{ pF}$, see Figure 17
Receiver Disable, T_{DEN}		25	45	ns	$C_L = 15\text{ pF}$, see Figure 17
Receiver Enable from Shutdown			500	ns	$C_L = 15\text{ pF}$, see Figure 17

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Output Delay, T_{DD}	1		70	ns	$R_L = 60\ \Omega$, $C_{L1} = C_{L2} = 15\text{ pF}$, see Figure 18
Differential Output Transition Time	2	8	15	ns	$R_L = 60\ \Omega$, $C_{L1} = C_{L2} = 15\text{ pF}$, see Figure 18
Propagation Delay Input to Output, T_{PLH} , T_{PHL}	7	22	70	ns	$R_L = 27\ \Omega$, $C_{L1} = C_{L2} = 15\text{ pF}$, see Figure 19
Driver Output to Output, T_{SKEW}			10	ns	$R_L = 54\ \Omega$, $C_{L1} = C_{L2} = 15\text{ pF}$, see Figure 19
ENABLE/DISABLE					
Driver Enable to Output Valid		45	110	ns	$R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 16
Driver Disable Timing		40	110	ns	$R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 16
Driver Enable from Shutdown		65	110	ns	$R_L = 110\ \Omega$, $C_L = 15\text{ pF}$, see Figure 16
RECEIVER					
Time to Shutdown	50	190	500	ns	
Propagation Delay Input to Output, T_{PLH} , T_{PHL}	25	65	115	ns	$C_L = 15\text{ pF}$, see Figure 21
Skew, $T_{PLH} - T_{PHL}$			20	ns	$C_L = 15\text{ pF}$, see Figure 21
Receiver Enable, T_{EN}		25	50	ns	$C_L = 15\text{ pF}$, see Figure 17
Receiver Disable, T_{DEN}		25	50	ns	$C_L = 15\text{ pF}$, see Figure 17
Receiver Enable from Shutdown			600	ns	$C_L = 15\text{ pF}$, see Figure 17

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{CC}	7 V
Inputs	
Driver Input (DI)	$-0.3\text{ V to }V_{CC} + 0.3\text{ V}$
Control Inputs (DE, $\overline{\text{RE}}$)	$-0.3\text{ V to }V_{CC} + 0.3\text{ V}$
Receiver Inputs (A, B)	$-7.5\text{ V to }+12.5\text{ V}$
Outputs	
Driver Outputs	$-7.5\text{ V to }+12.5\text{ V}$
Receiver Output	$-0.5\text{ V to }V_{CC} + 0.5\text{ V}$
14-Lead PDIP, Power Dissipation	800 mW
θ_{JA} , Thermal Impedance	140°C/W
14-Lead SOIC, Power Dissipation	650 mW
θ_{JA} , Thermal Impedance	115°C/W
16-Lead TSSOP, Power Dissipation	500 mW
θ_{JA} , Thermal Impedance	158°C/W
Operating Temperature Range	
Industrial (A Version)	$-40^\circ\text{C to }+85^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Rating	>2 kV
EFT Rating (IEC1000-4-4)	>1 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

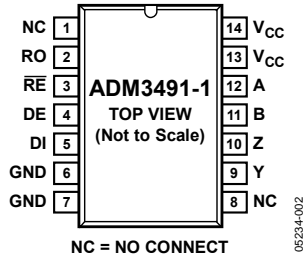


Figure 2. 14-Lead PDIP and 14-Lead SOIC Pin Configuration

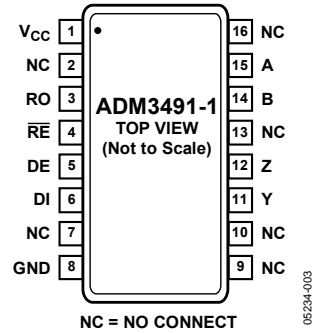


Figure 3. 16-Lead TSSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin Number		Mnemonic	Description
PDIP/SOIC	TSSOP		
1, 8	2, 7, 9, 10, 13, 16	NC	No Connect.
2	3	RO	Receiver Output. High when $A > B$ by 200 mV; low when $A < B$ by 200 mV.
3	4	\overline{RE}	Receiver Output Enable. When \overline{RE} is low, the receiver output RO is enabled. When \overline{RE} is high, the output is high impedance. If \overline{RE} is high and DE is low, the ADM3491-1 enters a shutdown state.
4	5	DE	Driver Output Enable. A high level enables the driver differential outputs, Y and Z. A low level places the part in a high impedance state.
5	6	DI	Driver Input. When the driver is enabled, a logic low on DI forces Y low and Z high; a logic high on DI forces Y high and Z low.
6, 7	8	GND	Ground Connection, 0V.
9	11	Y	Noninverting Driver Output Y.
10	12	Z	Inverting Driver Output Z.
11	14	B	Inverting Receiver Input B.
12	15	A	Noninverting Receiver Input A.
13, 14	1	V _{CC}	Power Supply, 3.3 V ± 0.3 V.

TYPICAL PERFORMANCE CHARACTERISTICS

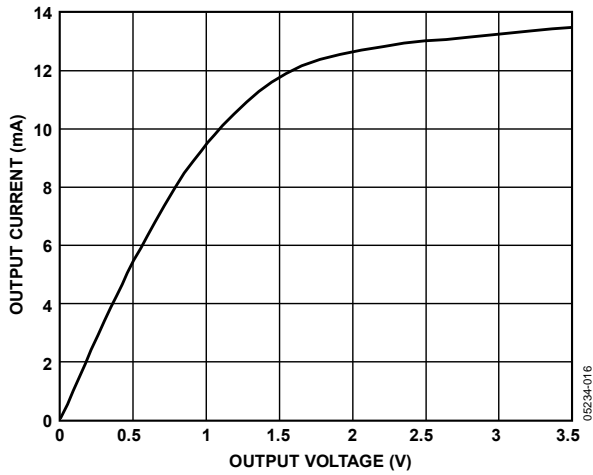


Figure 4. Output Current vs. Receiver Output Low Voltage

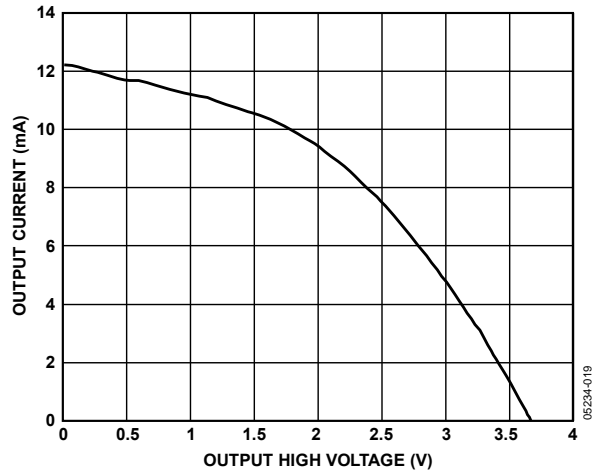


Figure 7. Output Current vs. Receiver Output High Voltage

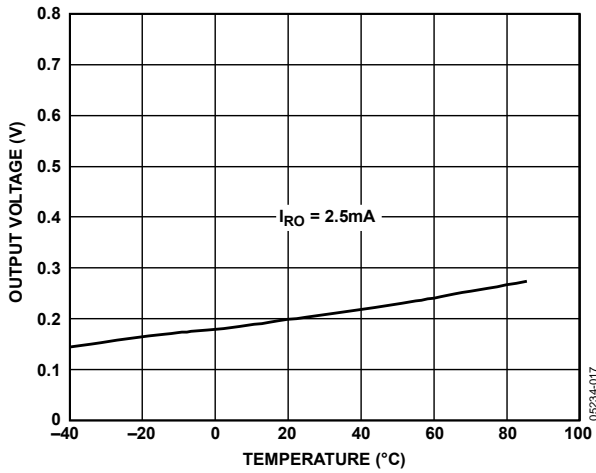


Figure 5. Receiver Output Low Voltage vs. Temperature

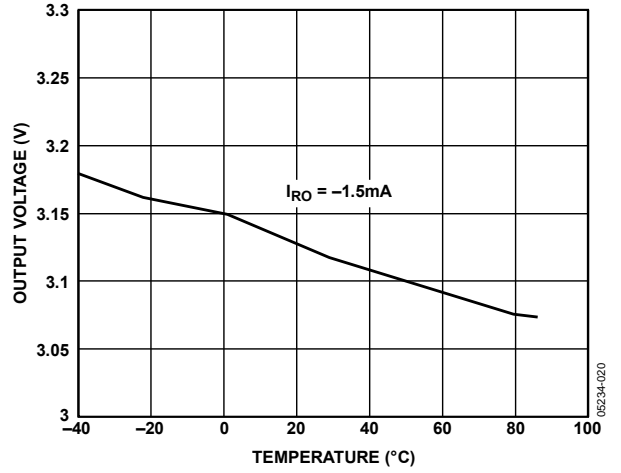


Figure 8. Receiver Output High Voltage vs. Temperature

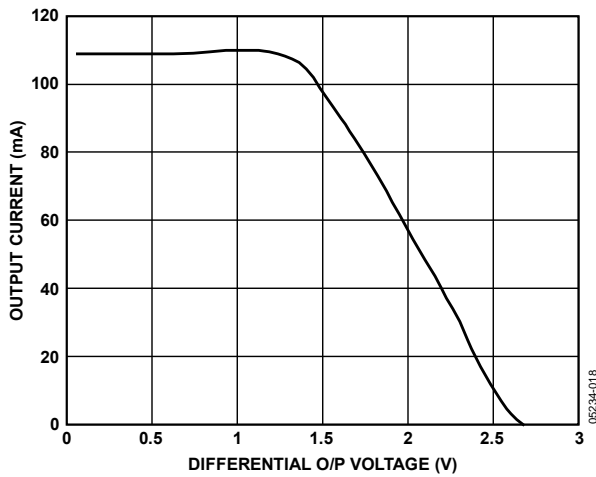


Figure 6. Output Current vs. Driver Differential Output Voltage

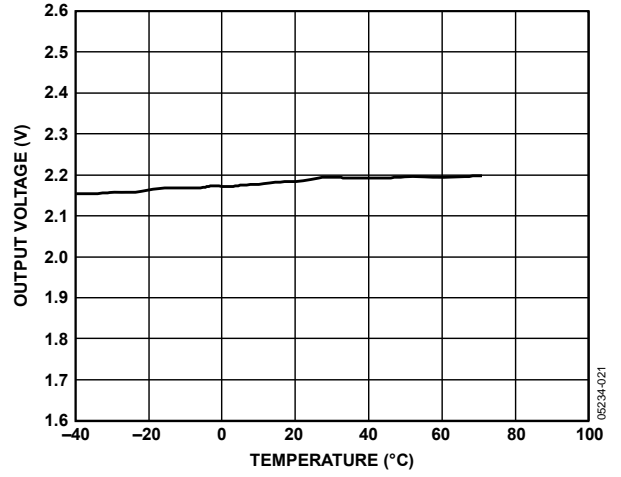


Figure 9. Driver Differential Output Voltage vs. Temperature

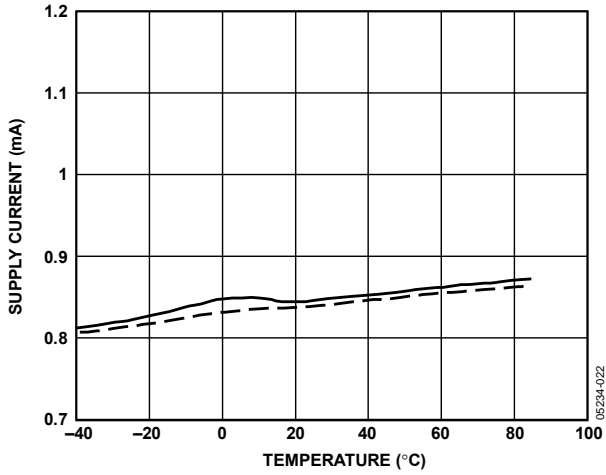


Figure 10. Supply Current vs. Temperature

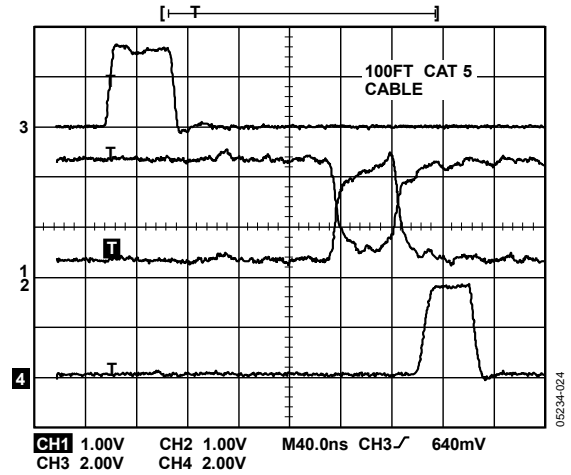


Figure 12. Driving 100 ft. Cable H-L Transition

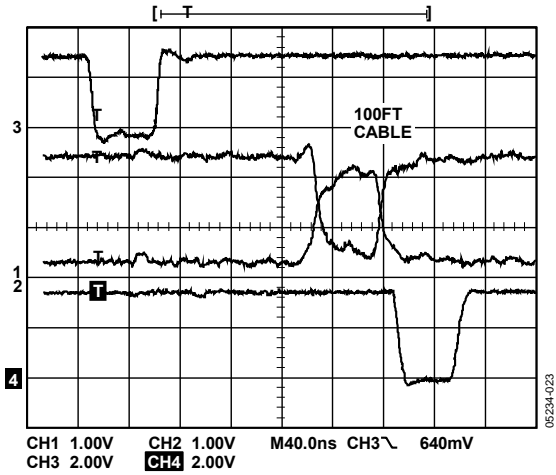


Figure 11. Driving 100 ft. Cable L-H Transition

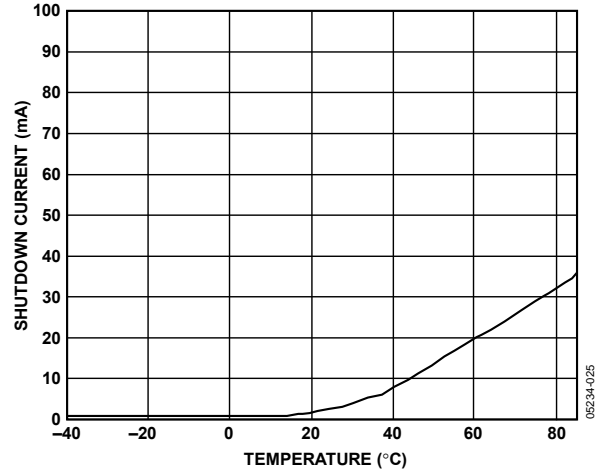


Figure 13. Shutdown Current vs. Temperature

TEST CIRCUITS

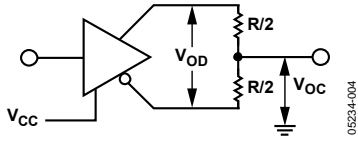


Figure 14. Driver Voltage Measurement Test Circuit

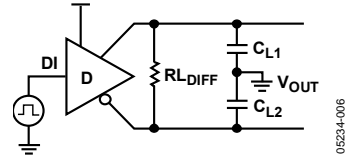


Figure 18. Driver Differential Output Delay Test Circuit

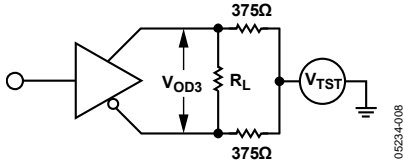


Figure 15. Driver Voltage Measurement Test Circuit 2

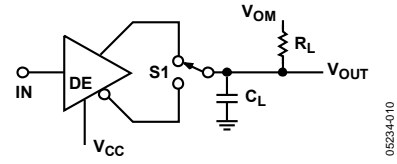


Figure 19. Driver Propagation Delay Test Circuit

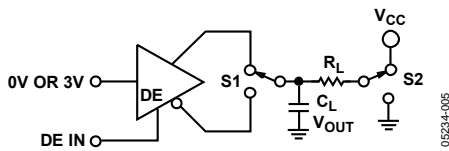


Figure 16. Driver Enable/Disable Test Circuit

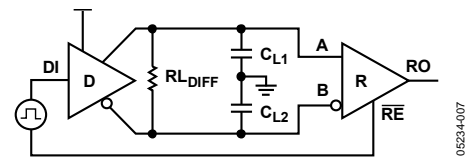


Figure 20. Driver/Receiver Propagation Delay Test Circuit

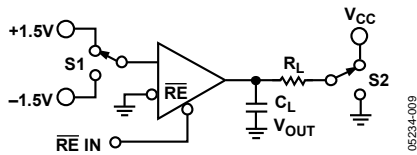


Figure 17. Receiver Enable/Disable Test Circuit

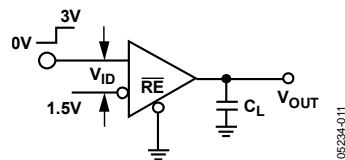


Figure 21. Receiver Propagation Delay Test Circuit

SWITCHING CHARACTERISTICS

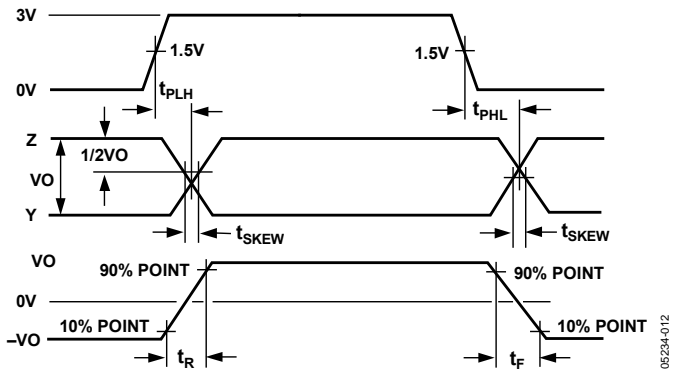


Figure 22. Driver Propagation Delay, Rise/Fall Timing

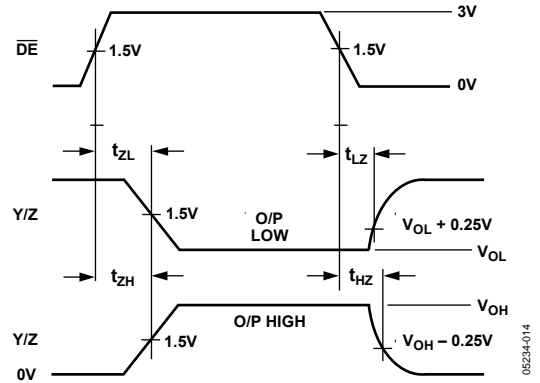


Figure 24. Driver Enable/Disable Timing

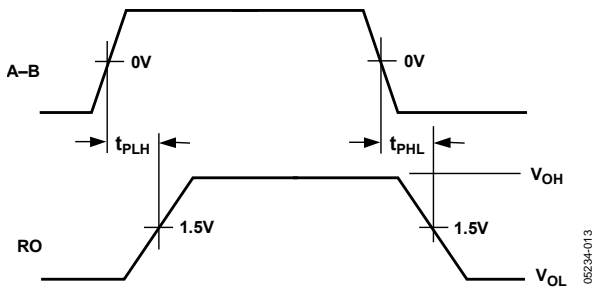


Figure 23. Receiver Propagation Delay

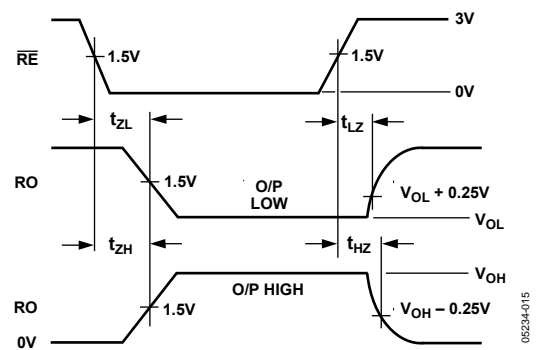


Figure 25. Receiver Enable/Disable Timing

THEORY OF OPERATION

DIFFERENTIAL DATA TRANSMISSION

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line.

The two main standards approved by the EIA specify the electrical characteristics of transceivers used in differential data transmission:

- RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.
- RS-485 standard was defined to cater to true multipoint communications. This standard meets or exceeds all the requirements of RS-422, but also allows multiple drivers and receivers to be connected to a single bus. An extended common-mode range of -7 V to $+12\text{ V}$ is defined.

The most significant differentiator of the RS-485 standard is that the drivers can be disabled, thereby allowing more than one to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

Table 6. Comparison of RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	$\pm 2\text{ V}$	$\pm 1.5\text{ V}$
Driver Load Impedance	$100\ \Omega$	$54\ \Omega$
Receiver Input Resistance	$4\text{ k}\Omega$ min	$12\text{ k}\Omega$ min
Receiver Input Sensitivity	$\pm 200\text{ mV}$	$\pm 200\text{ mV}$
Receiver Input Voltage Range	-7 V to $+7\text{ V}$	-7 V to $+12\text{ V}$

CABLE AND DATA RATE

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM3491-1 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 26. Only one driver can transmit at a particular time, but multiple receivers can be enabled simultaneously.

As with any transmission line, it is important that reflections be minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

RECEIVER OPEN-CIRCUIT FAIL-SAFE FEATURE

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.

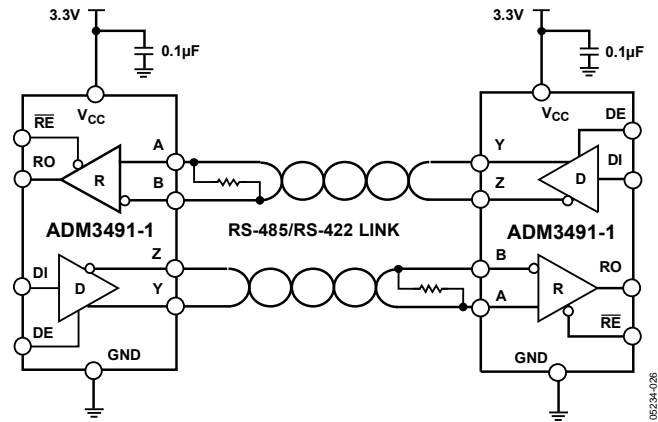


Figure 26. ADM3491-1 Full-Duplex Data Link

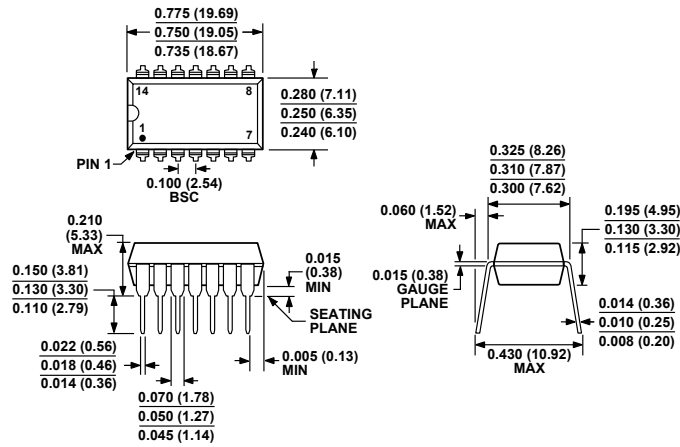
Table 7. Transmitting Truth Table

Inputs			Outputs	
RE	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	Hi-Z	Hi-Z
1	0	X	Hi-Z	Hi-Z

Table 8. Receiving Truth Table

Inputs			Outputs
RE	DE	A-B	RO
0	X	$\geq +0.2\text{ V}$	0
0	X	$\leq -0.2\text{ V}$	0
0	X	Inputs O/C	1
1	X	X	Hi-Z

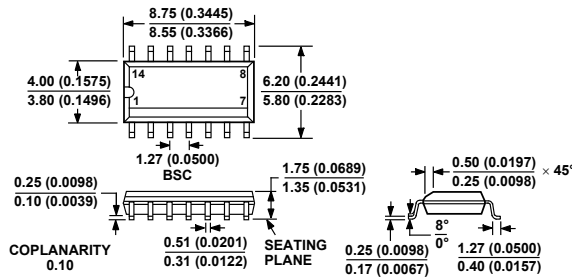
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-AA
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 27. 14-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-14)

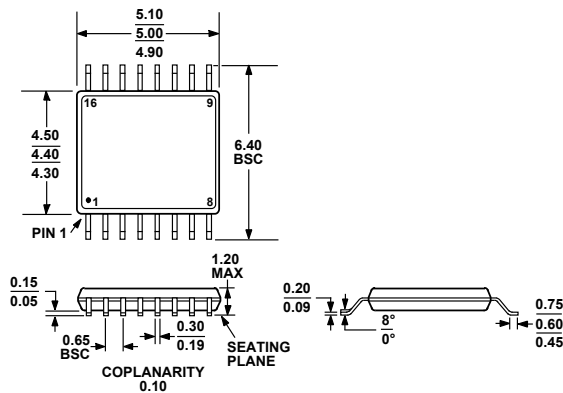
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AB
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 28. 14-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-14)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 29. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model¹	Temperature Range	Package Description	Package Option	Ordering Quantity
ADM3491ANZ-1	-40°C to +85°C	14-Lead Plastic DIP	N-14	
ADM3491AR-1	-40°C to +85°C	14-Lead Narrow Body Small Outline [SOIC]	R-14	
ADM3491ARZ-1	-40°C to +85°C	14-Lead Narrow Body Small Outline [SOIC]	R-14	
ADM3491ARZ-1REEL	-40°C to +85°C	14-Lead Narrow Body Small Outline [SOIC]	R-14	2,500
ADM3491ARZ-1REEL7	-40°C to +85°C	14-Lead Narrow Body Small Outline [SOIC]	R-14	1,000
ADM3491ARU-1	-40°C to +85°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16	
ADM3491ARU-1REEL	-40°C to +85°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16	2,500
ADM3491ARUZ-1	-40°C to +85°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16	
ADM3491ARUZ-1REEL	-40°C to +85°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16	2,500
ADM3491ARUZ-1REEL7	-40°C to +85°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16	1,000

¹ Z = RoHS Compliant Part.

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Mouser Electronics

Authorized Distributor

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