











CSD13201W10

SLPS306A-MAY 2012-REVISED SEPTEMBER 2015

CSD13201W10 N-Channel NexFET™ Power MOSFET

Features

- Ultra-Low Qa and Qad
- Small Footprint (1 mm × 1 mm)
- Low Profile 0.62-mm Height
- Pb-Free
- **RoHS Compliant**
- Halogen-Free
- Gate-Source Voltage Clamp

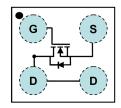
Applications

- **Battery Management**
- Load Switch
- **Battery Protection**

Description

This 12-V, 26-mΩ, N-Channel device is designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile.

Top View



Product Summary

T _A = 25°	С	TYPICAL V	UNIT	
V_{DS}	Drain-to-Source Voltage		V	
Q_g	Gate Charge Total (4.5 V)	2.3		nC
Q _{gd}	Gate Charge Gate-to-Drain	0.3	0.3	
		V _{GS} = 1.8 V	38	mΩ
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 2.5 V	29	11122
	T to olota loo	$V_{GS} = 4.5 \text{ V}$	26	mΩ
V _{GS(th)}	Threshold Voltage	0.8		V

Device Information⁽¹⁾

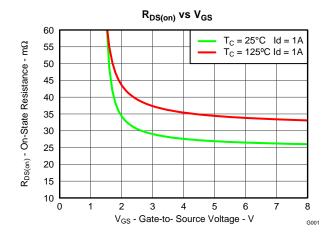
PART NUMBER	UMBER PACKAGE MEDIA		QTY	SHIP	
CSD13201W10	1 mm x 1 mm Wafer Level Package	7-inch reel	3000	Tape and Reel	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^{\circ}C$;	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±8	٧
I _D	Continuous Drain Current, T _A = 25°C ⁽¹⁾	1.6	Α
I_{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	20.2	Α
P_D	Power Dissipation ⁽¹⁾	1.2	W
T _J , T _{stg}	Operating Junction and Storage Temperature Range	-55 to 150	°C

- (1) $R_{\theta JA} = 105^{\circ}\text{C/W}$ on 1in^2 Cu (2 oz.) on 0.060" thick FR4 PCB.
- (2) Pulse width ≤ 300 µs, duty cycle ≤ 2%



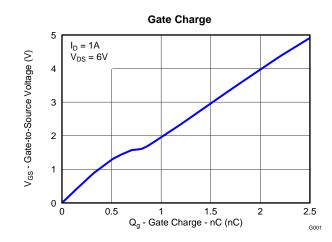




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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Cł	hanges from Original (May 2012) to Revision A	Page
•	Added part number to title	1
•	Enhanced Description	1
•	Added Device and Documentation Support section.	<mark>7</mark>

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5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC C	CHARACTERISTICS					
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	12			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 9.6 V			1	μΑ
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 8 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.65	0.8	1.1	V
		V _{GS} = 1.8 V, I _D = 1 A		38	53	
R _{DS(on)}	Drain-to-source on resistance	V _{GS} = 2.5 V, I _D = 1 A		29	39	$m\Omega$
-(- /		V _{GS} = 4.5 V, I _D = 1 A		26	34	
9 _{fs}	Transconductance	V _{DS} = 6 V, I _D = 1 A		23		S
DYNAMIC	CHARACTERISTICS					
C _{ISS}	Input capacitance			385	462	pF
Coss	Output capacitance	V _{GS} = 0 V, V _{DS} = 6 V, f = 1 MHz		245	294	pF
C _{RSS}	Reverse transfer capacitance			18.1	22.6	pF
R _g	Series gate resistance			3		Ω
Q _g	Gate charge total (4.5 V)			2.3	2.9	nC
Q _{gd}	Gate charge gate-to-drain	V 6V 1 4 A		0.3		nC
Q _{gs}	Gate charge gate-to-source	$V_{DS} = 6 \text{ V}, I_{D} = 1 \text{ A}$		0.5		nC
Q _{g(th)}	Gate charge at Vth			0.3		nC
Q _{OSS}	Output charge	V _{DS} = 6.0 V, V _{GS} = 0 V		1.8		nC
t _{d(on)}	Turn on delay time			3.9		ns
t _r	Rise time	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 1 A		5.9		ns
t _{d(off)}	Turn off delay time	$R_G = 20 \Omega$		14.4		ns
t _f	Fall time			9.7		ns
DIODE CI	HARACTERISTICS				*	
V _{SD}	Diode forward voltage	I _S = 1 A, V _{GS} = 0 V		0.7	1	V
Q _{rr}	Reverse recovery charge	V CV I 4.0 di/dt 400.0 ft		2.4		nC
t _{rr}	Reverse recovery time	V_{DS} = 6 V, I_{S} = 1 A, di/dt = 100 A/ μ s		11.5		ns

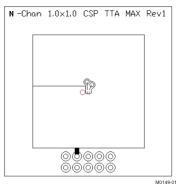
5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

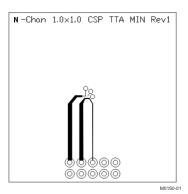
	THERMAL METRIC	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal resistance junction-to-ambient (minimum Cu area)			228.6	°C/W
$R_{\theta JA}$	Thermal resistance junction-to-ambient (1 in ² Cu area)			131.1	°C/W

Product Folder Links: CSD13201W10





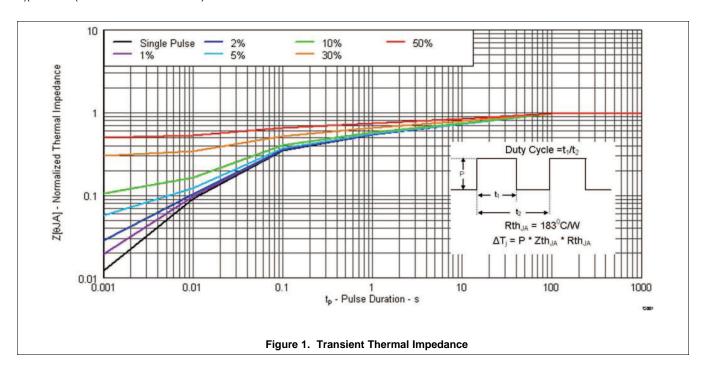
Max $R_{\theta JA} = 131.1^{\circ}$ C/W when mounted on 1 inch² of 2 oz. Cu.



Max $R_{\theta JA} = 228.6$ °C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

 $T_A = 25$ °C (unless otherwise noted)



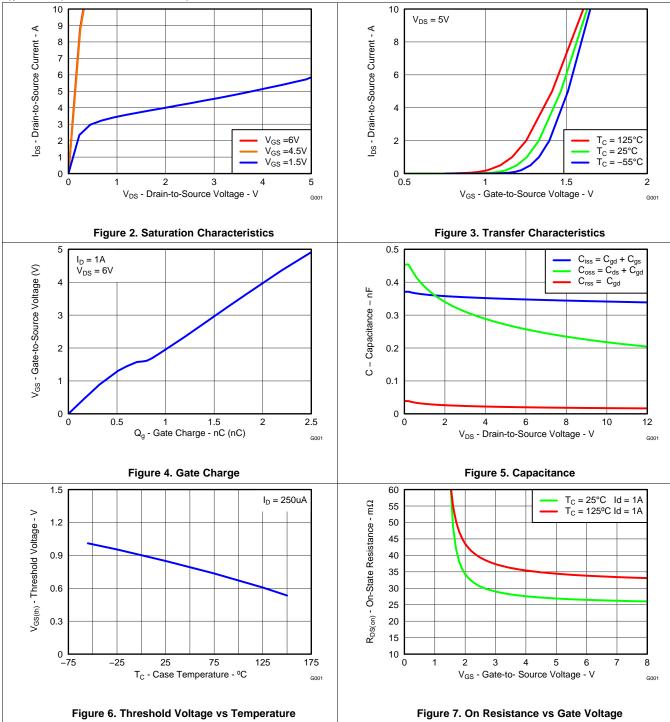
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Typical MOSFET Characteristics (continued)

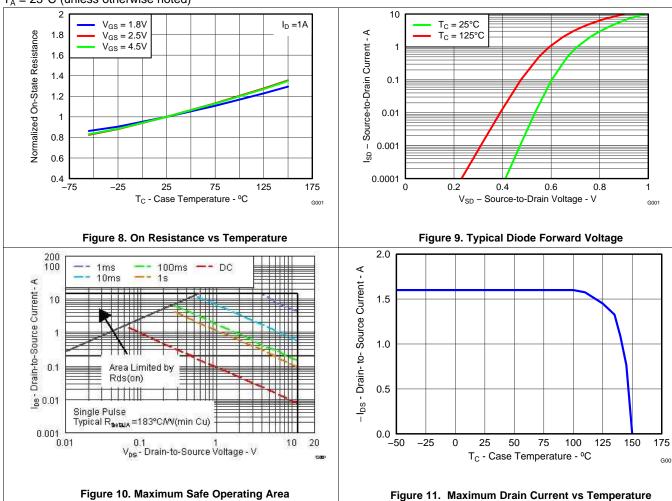
 $T_A = 25$ °C (unless otherwise noted)





Typical MOSFET Characteristics (continued)

 $T_A = 25$ °C (unless otherwise noted)





6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

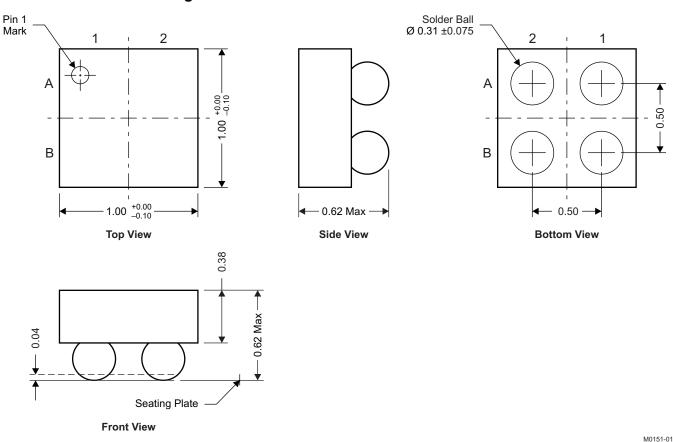
Product Folder Links: CSD13201W10



Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

CSD13201W10 Package Dimensions



NOTE: All dimensions are in mm (unless otherwise specified)

Pin Configuration Table

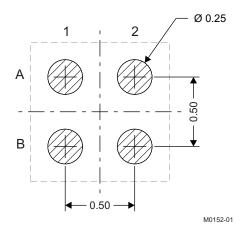
POSITION	DESIGNATION
A2	Source
A1	Gate
B1, B2	Drain

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Product Folder Links: CSD13201W10



7.2 Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

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PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
							(6)				
CSD13201W10	ACTIVE	DSBGA	YZB	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	201	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

www.ti.com 9-Aug-2020

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13201W10	DSBGA	YZB	4	3000	180.0	8.4	1.06	1.06	0.69	2.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

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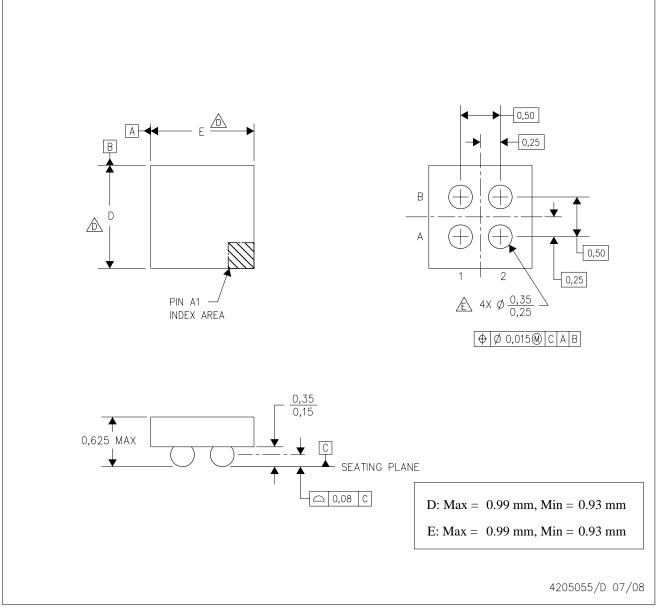


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13201W10	DSBGA	YZB	4	3000	182.0	182.0	20.0

YZB (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm.

 To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
- E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
- F. This package contains lead—free balls. Refer to YEB (Drawing #4204178) for tin—lead (SnPb) balls.



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