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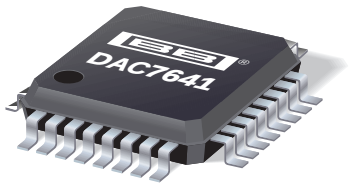


DAC7641

For most current data sheet and other product information, visit www.burr-brown.com

16-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 2.5mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10μs to 0.003%
- 15-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C
- PROGRAMMABLE RESET TO MID-SCALE OR ZERO-SCALE
- DATA READBACK
- DOUBLE-BUFFERED DATA INPUTS

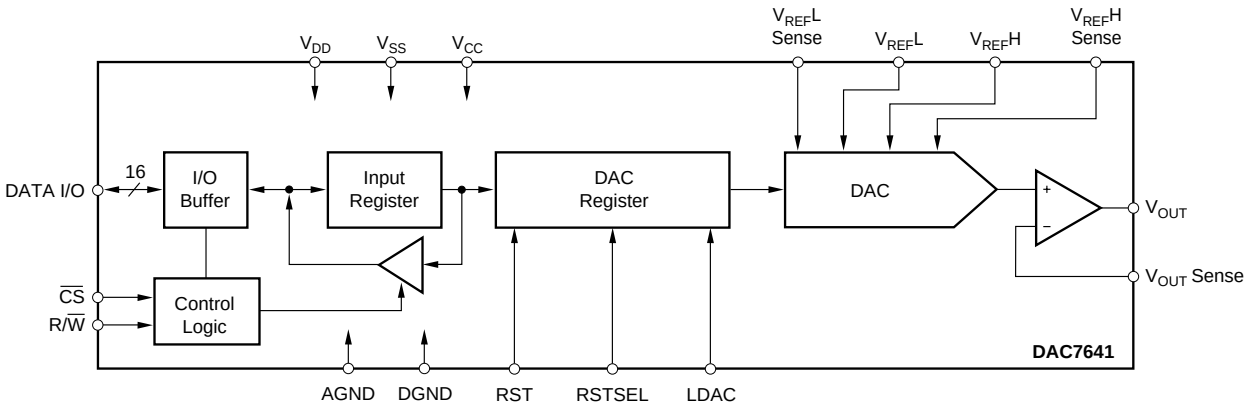
APPLICATIONS

- PROCESS CONTROL
- ATE PIN ELECTRONICS
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS
- DAC-PER-PIN PROGRAMMERS

DESCRIPTION

The DAC7641 is a 16-bit, voltage output digital-to-analog converter (DAC) with guaranteed 15-bit monotonic performance over the specified temperature range. It accepts 16-bit parallel input data, has double-buffered DAC input logic (allowing asynchronous update), and provides a readback mode of the internal input registers. Programmable asynchronous reset clears all registers to a mid-scale code of 8000_H or to a zero-scale of 0000_H. The DAC7641 can operate from a single +5V supply or from +5V and –5V supplies.

Low power and small size per DAC make the DAC7641 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7641 is available in a TQFP-32 package, and offers guaranteed specifications over the –40°C to +85°C temperature range.



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PDS-1532A
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SBAS118

SPECIFICATIONS (Dual Supply)

At $T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $V_{REF}H = +2.5V$, and $V_{REF}L = -2.5V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7641Y			DAC7641YB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error			±3	±4		±2	±3	LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Bipolar Zero Error			±1	±3		*	*	mV
Bipolar Zero Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			±1	±3		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Power Supply Rejection Ratio (PSRR)	At Full Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	$V_{REF} = -2.5V$, $R_L = 10k\Omega$, $V_{SS} = -5V$	$V_{REF}L$		$V_{REF}H$	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			–10, +30			*		mA
Short-Circuit Duration	GND or V_{CC} or V_{SS}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REF}L + 1.25$		+2.5	*		*	V
Ref Low Input Voltage Range		–2.5		$V_{REF}H - 1.25$	*		*	V
Ref High Input Current			500			*		µA
Ref Low Input Current			–500			*		µA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 5V Output Step		8	10		*	*	µs
Digital Feedthrough			2			*		nV-s
Output Noise Voltage	f = 10kHz		60			*		$nV/\sqrt{Hz}$
DAC Glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			*		nV-s
DIGITAL INPUT								
V_{IH}		$0.7 \cdot V_{DD}$			*			V
V_{IL}				$0.3 \cdot V_{DD}$			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = -0.8mA$	3.6	4.5		*	*		V
V_{OL}	$I_{OL} = 1.2mA$		0.3	0.4		*	*	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		–5.25	–5.0	–4.75	*	*	*	V
I_{CC}			0.4	0.5		*	*	mA
I_{DD}			15			*		µA
I_{SS}		–0.6	–0.5	–0.4	*	*		mA
Power			4	5.5		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as DAC7641Y.

SPECIFICATIONS (Single Supply)

At $T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REF}H = +2.5V$, and $V_{REF}L = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7641Y			DAC7641YB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error(1)			±3	±4		±2	±3	LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Zero Scale Error			±1	±3		*	*	mV
Zero Scale Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			±1	±3		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Power Supply Rejection Ratio (PSRR)	At Full Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	$V_{REF}L = 0V$, $V_{SS} = 0V$, $R_L = 10k\Omega$	0		$V_{REF}H$	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			±30			*		mA
Short-Circuit Duration	GND or V_{CC}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REF}L + 1.25$		+2.5	*		*	V
Ref Low Input Voltage Range		0		$V_{REF}H - 1.25$	*		*	V
Ref High Input Current			250			*		µA
Ref Low Input Current			–250			*		µA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 2.5V Output Step		8	10		*	*	µs
Digital Feedthrough			2			*		nV-s
Output Noise Voltage, f = 10kHz			60			*		$nV/\sqrt{Hz}$
DAC Glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			*		nV-s
DIGITAL INPUT								
V_{IH}		0.7 • V_{DD}			*			V
V_{IL}				0.3 • V_{DD}			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = –0.8mA$	3.6	4.5		*	*		V
V_{OL}	$I_{OL} = 1.2mA$		0.3	0.4		*	*	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		0	0	0	*	*	*	V
I_{CC}			0.4	0.5		*	*	mA
I_{DD}			15			*		µA
Power			1.8	2.5		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as DAC7641Y.

NOTE: (1) If $V_{SS} = 0V$ specification applies at Code 0040_H and above due to possible negative zero-scale error.

ABSOLUTE MAXIMUM RATINGS[1]

V_{SS} to V_{SS}	–0.3V to 11V
V_{DD} to GND	–0.3V to 5.5V
V_{REFL} to GND	–0.3V to (V_{SS} – V_{CC})
V_{REFH} to GND	–0.3V to (V_{SS} – V_{CC})
V_{REFH} to V_{REFL}	–0.3V to +11V
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to V_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

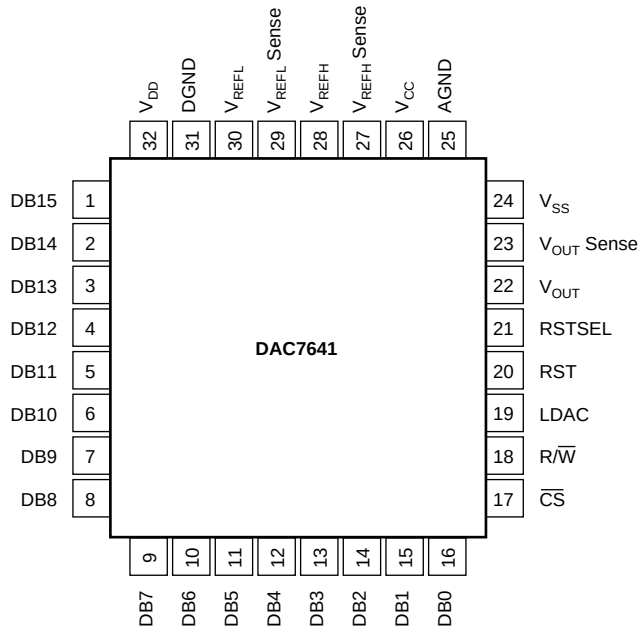
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER[1]	TRANSPORT MEDIA
DAC7641Y	±4	±3	TQFP-32	351	–40°C to +85°C	DAC7641Y/250	Tape and Reel
"	"	"	"	"	"	DAC7641Y/2K	Tape and Reel
DAC7641YB	±3	±2	TQFP-32	351	–40°C to +85°C	DAC7641YB/250	Tape and Reel
"	"	"	"	"	"	DAC7641YB/2K	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "DAC7641Y/2K" will get a single 2000-piece Tape and Reel.

PIN CONFIGURATION



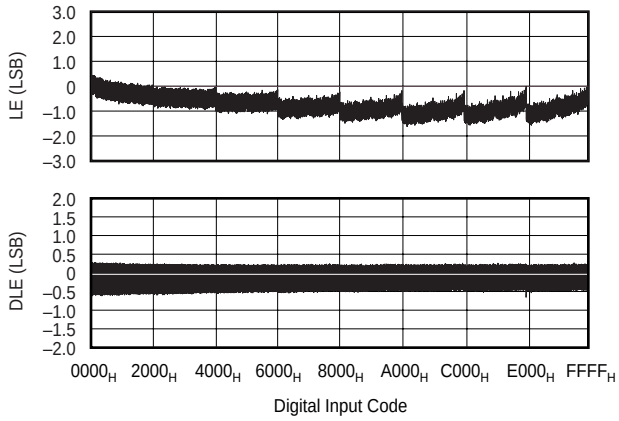
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	DB15	Data Bit 15, MSB	19	LDAC	DAC Load Strobe, rising-edge triggered.
2	DB14	Data Bit 14	20	RST	Reset, rising-edge triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.
3	DB13	Data Bit 13			
4	DB12	Data Bit 12	21	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST command will set the DAC registers to mid-scale. If LOW, a RST command will set the DAC registers to zero.
5	DB11	Data Bit 11			
6	DB10	Data Bit 10			
7	DB9	Data Bit 9			
8	DB8	Data Bit 8	22	V_{OUT}	DAC Voltage Output
9	DB7	Data Bit 7	23	V_{OUT} Sense	DAC Output Amplifier Inverting Input. Used to close the feedback loop at the load.
10	DB6	Data Bit 6			
11	DB5	Data Bit 5	24	V_{SS}	Negative Power Supply
12	DB4	Data Bit 4	25	AGND	Analog Ground
13	DB3	Data Bit 3	26	V_{CC}	Positive Power Supply
14	DB2	Data Bit 2	27	V_{REFH} Sense	DAC Reference High Sense Input
15	DB1	Data Bit 1	28	V_{REFH}	DAC Reference High Input
16	DB0	Data Bit 0, LSB	29	V_{REFL} Sense	DAC Reference Low Sense Input
17	$\overline{CS}$	Chip Select, active low.	30	V_{REFL}	DAC Reference Low Input
18	R/$\overline{W}$	Enabled by $\overline{CS}$, controls data read and write from the input register.	31	DGND	Digital Ground
			32	V_{DD}	Positive Power Supply

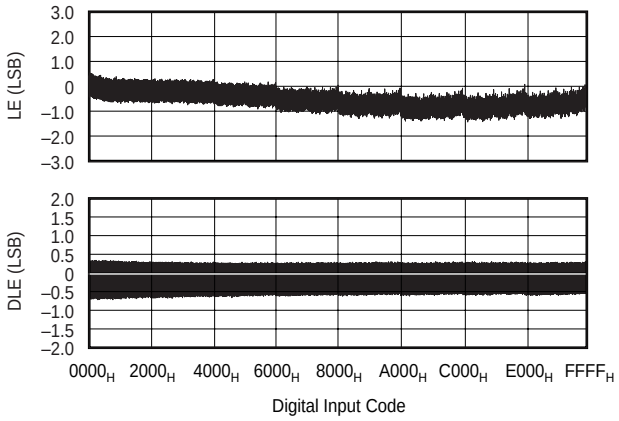
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V

At T_A = +25°C, V_{DD} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

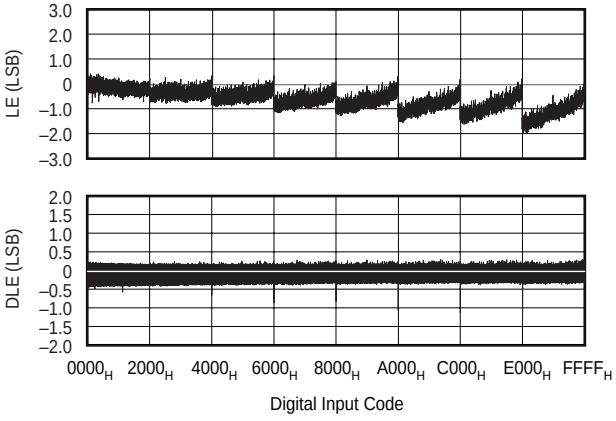
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+25°C)



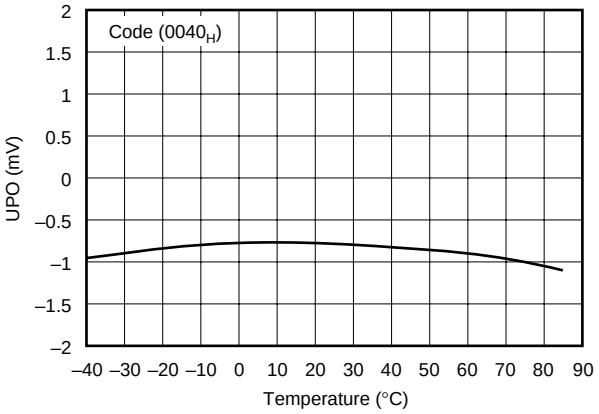
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+85°C)



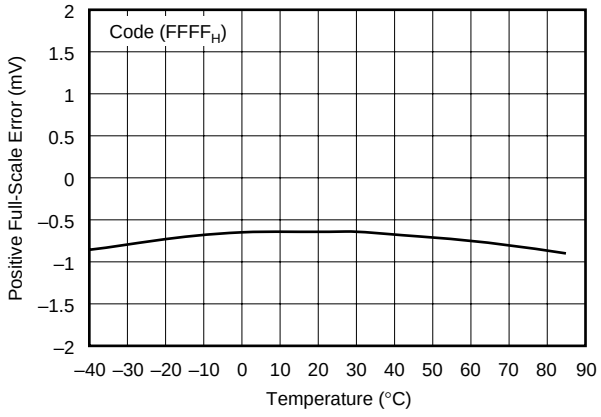
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(–40°C)



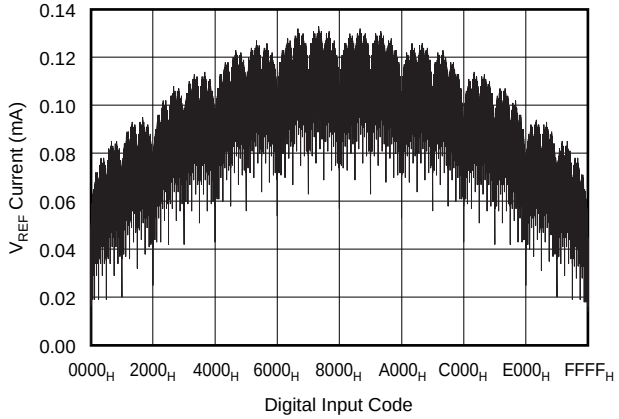
ZERO-SCALE ERROR vs TEMPERATURE



POSITIVE FULL-SCALE ERROR vs TEMPERATURE



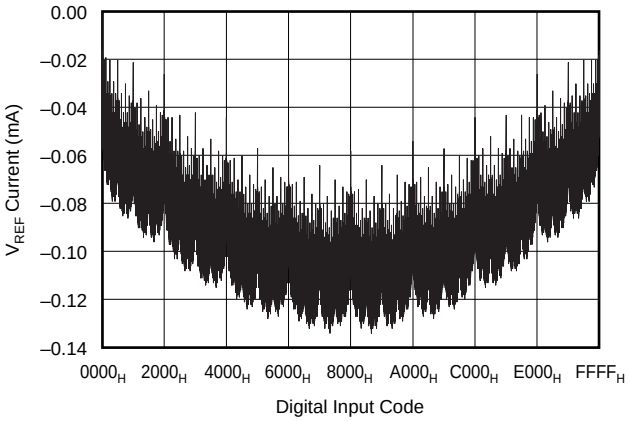
V_{REFH} CURRENT vs CODE



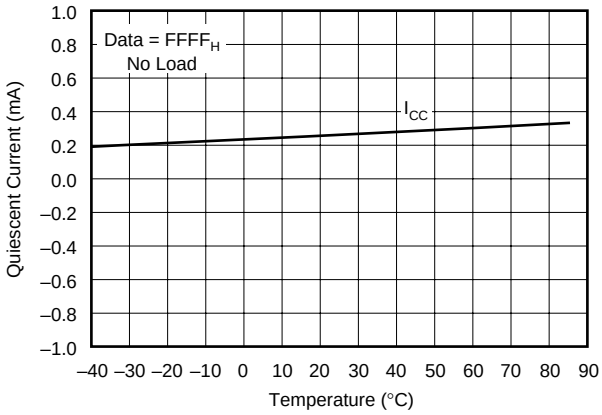
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{DD} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

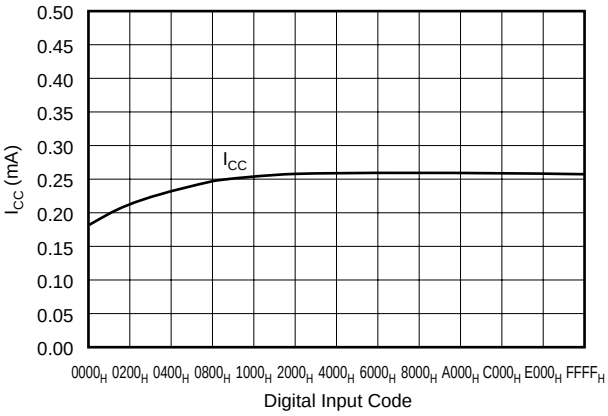
V_{REFL} CURRENT vs CODE



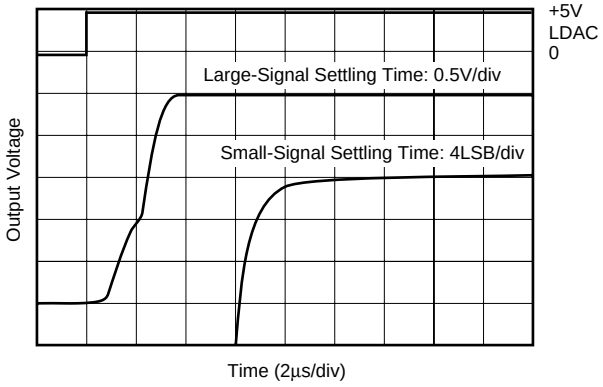
POWER SUPPLY CURRENT vs TEMPERATURE



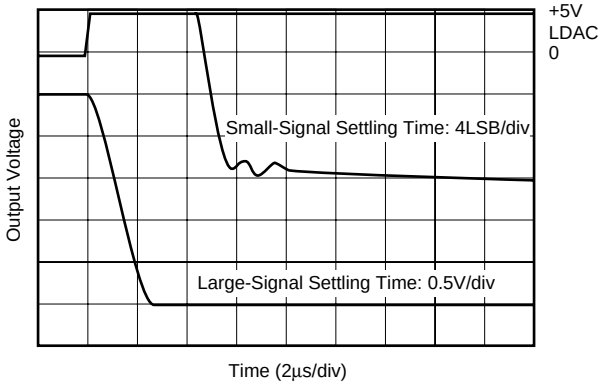
POSITIVE SUPPLY CURRENT vs DIGITAL INPUT CODE



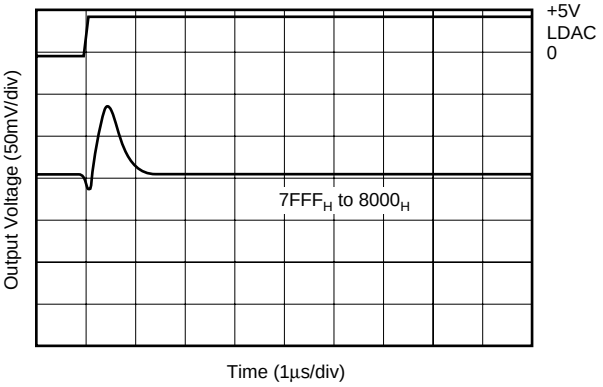
OUTPUT VOLTAGE vs SETTLING TIME (0V to +2.5V)



OUTPUT VOLTAGE vs SETTLING TIME (+2.5V to 2mV)



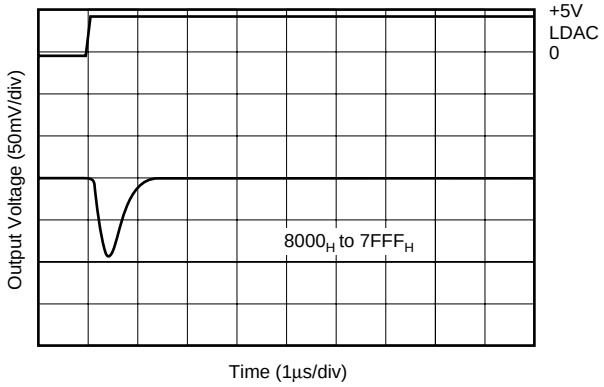
OUTPUT VOLTAGE vs MIDSCALE GLITCH PERFORMANCE



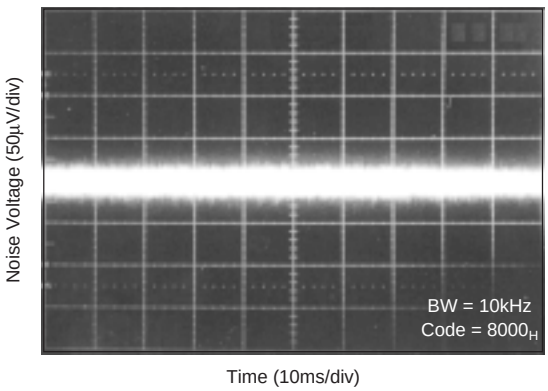
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{DD} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

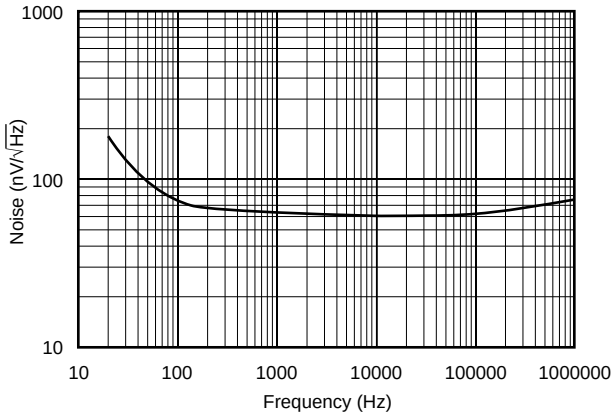
OUTPUT VOLTAGE
vs MIDSCALE GLITCH PERFORMANCE



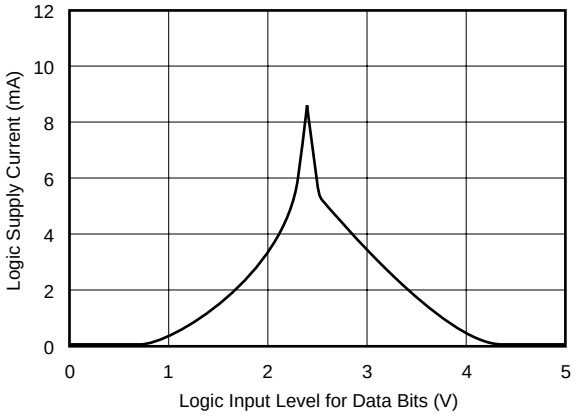
BROADBAND NOISE



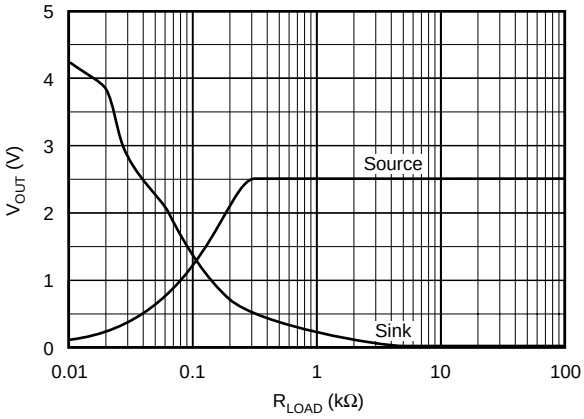
OUTPUT NOISE VOLTAGE vs FREQUENCY



LOGIC SUPPLY CURRENT
vs LOGIC INPUT LEVEL FOR DATA BITS



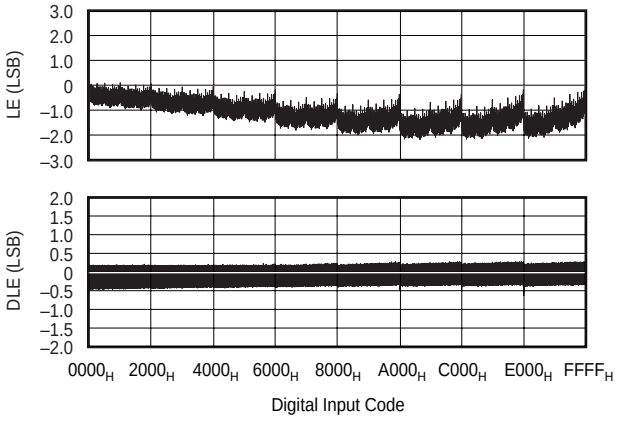
OUTPUT VOLTAGE vs R_{LOAD}



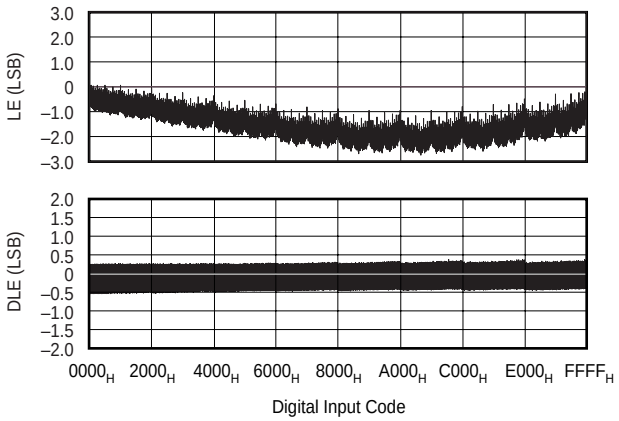
TYPICAL PERFORMANCE CURVES: V_{SS} = –5V

At T_A = +25°C, V_{DD} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.

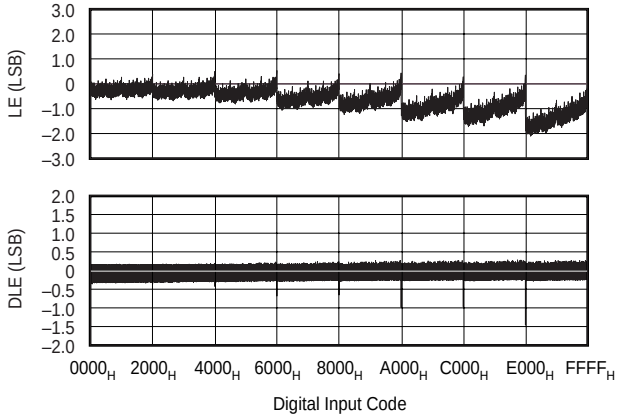
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+25°C)



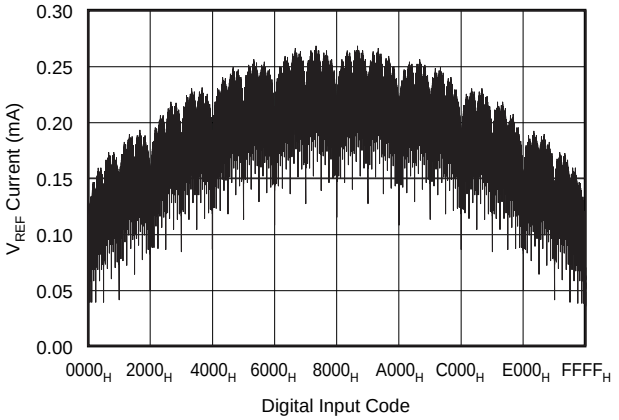
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+85°C)



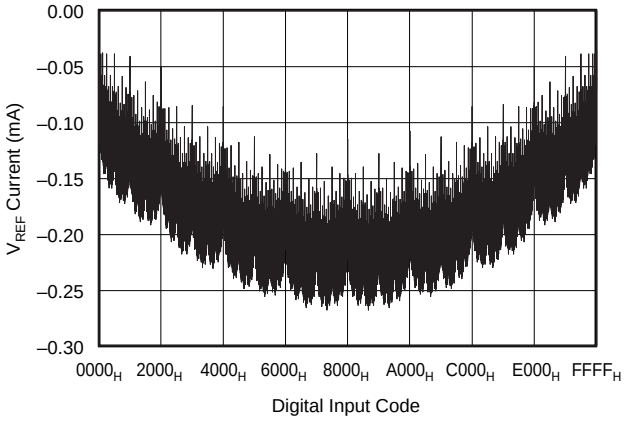
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(–40°C)



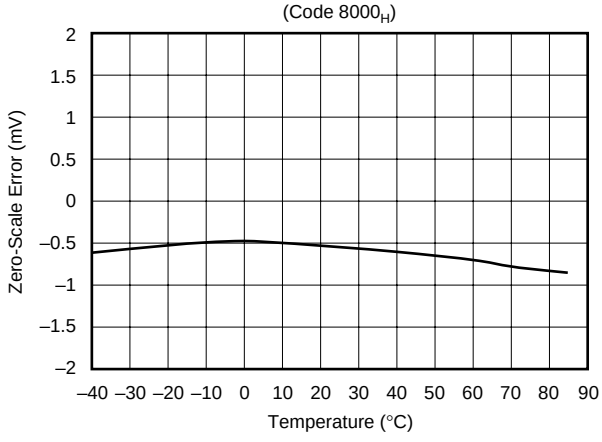
V_{REFH} CURRENT vs CODE



V_{REFL} CURRENT vs CODE



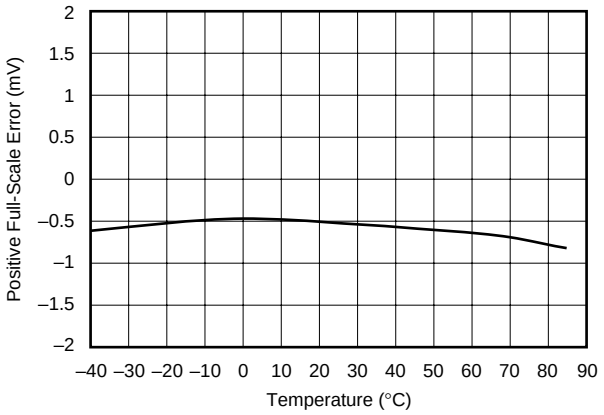
ZERO-SCALE ERROR vs TEMPERATURE
(Code 8000_H)



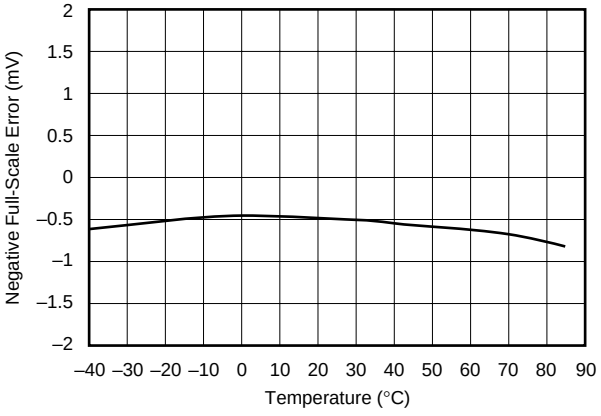
TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (Cont.)

At T_A = +25°C, V_{DD} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.

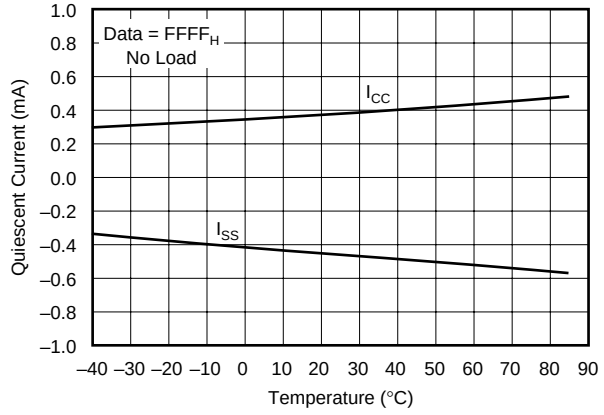
POSITIVE FULL-SCALE ERROR vs TEMPERATURE
(Code $FFFF_H$)



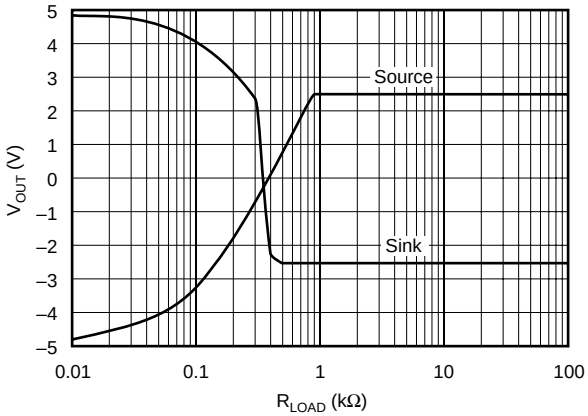
NEGATIVE FULL-SCALE ERROR vs TEMPERATURE
(Code 0000_H)



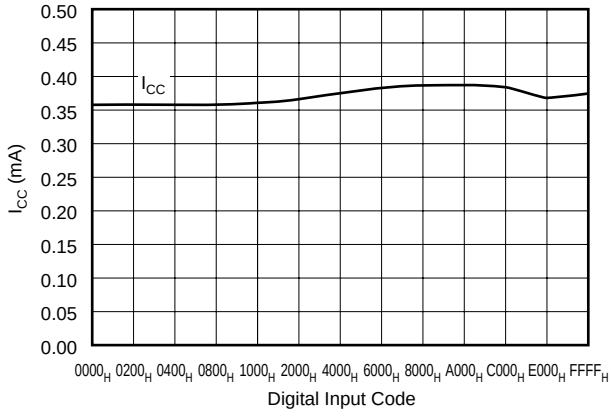
POWER SUPPLY CURRENT
vs TEMPERATURE



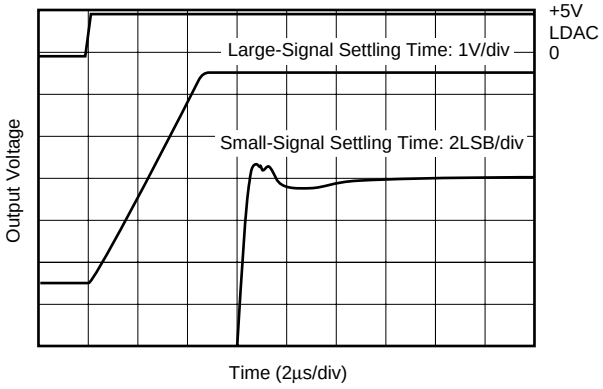
OUTPUT VOLTAGE vs R_{LOAD}



POSITIVE SUPPLY CURRENT
vs DIGITAL INPUT CODE

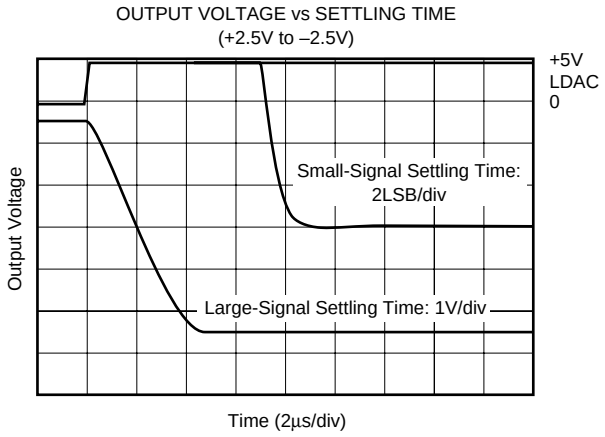


OUTPUT VOLTAGE vs SETTLING TIME
(–2.5V to +2.5V)



TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (Cont.)

At T_A = +25°C, V_{DD} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.



THEORY OF OPERATION

The DAC7641 is a voltage output, 16-bit digital-to-analog converter (DAC). The architecture is an R-2R ladder configuration with the three MSBs segmented, followed by an operational amplifier that serves as a buffer (see Figure 1). The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the external voltage references $V_{REF}L$ and $V_{REF}H$, respectively. The digital input is a 16-bit parallel word and the DAC input register offers a readback capability. The converters can be powered from either a single +5V supply or a dual ±5V supply. The device offers a reset function which immediately sets all DAC output voltages and DAC registers to mid-scale code 8000_H or to zero-scale code 0000_H. See Figures 2 and 3 for the basic operation of the DAC7641.

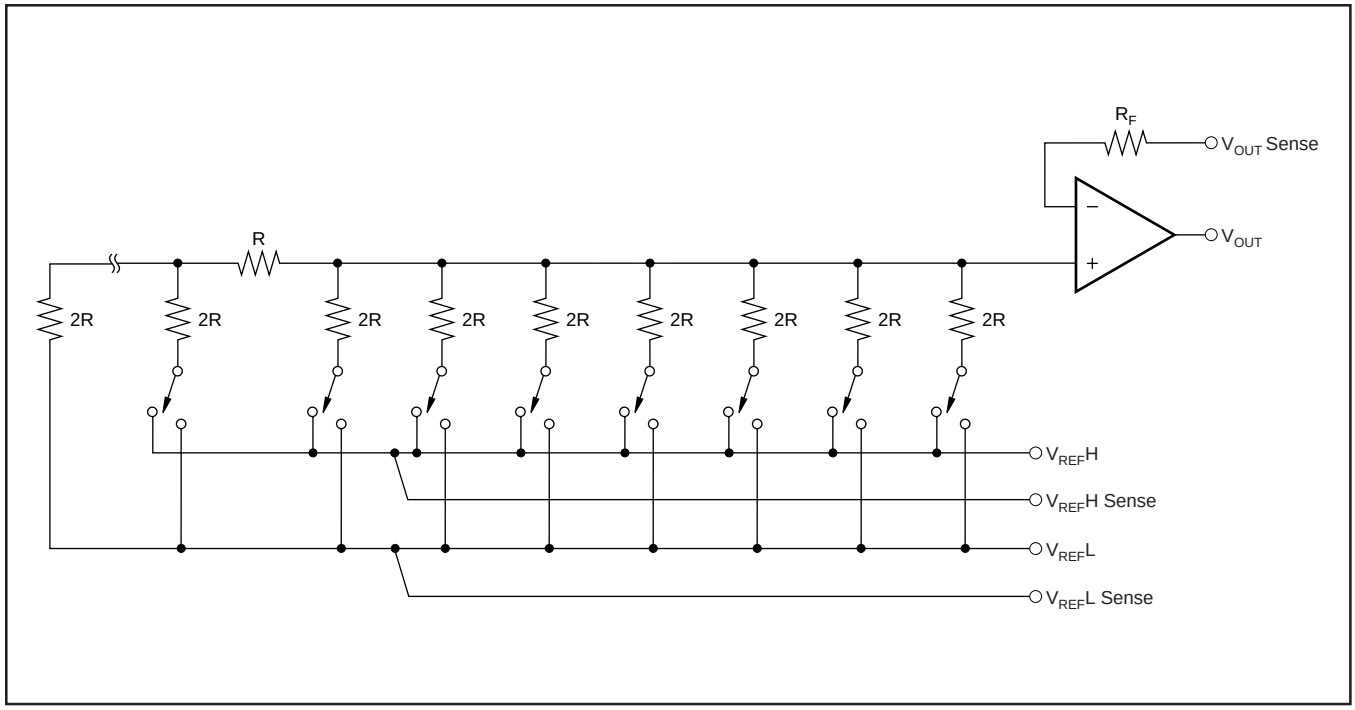


FIGURE 1. DAC7641 Architecture.

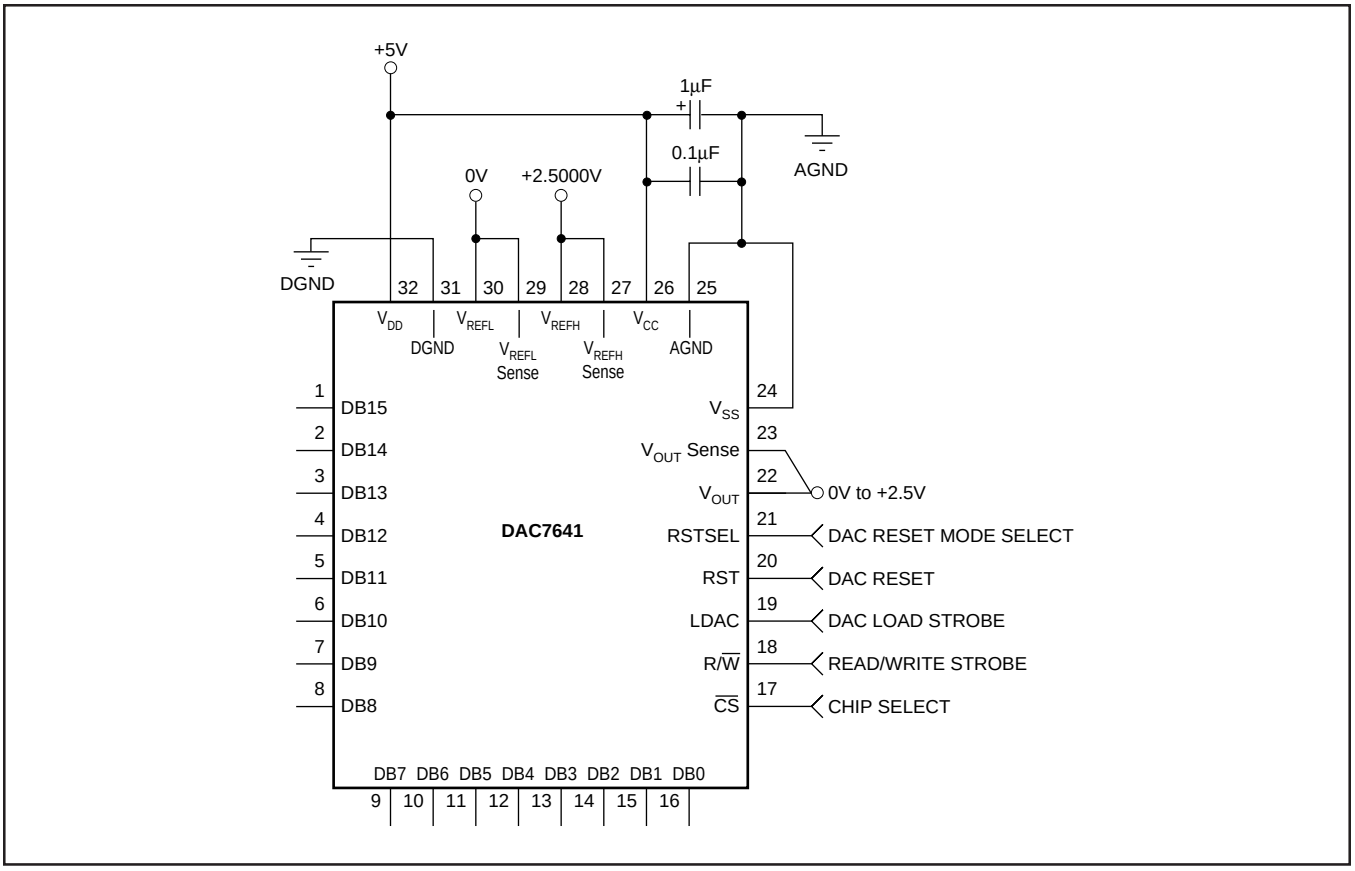


FIGURE 2. Single-Supply Operation.

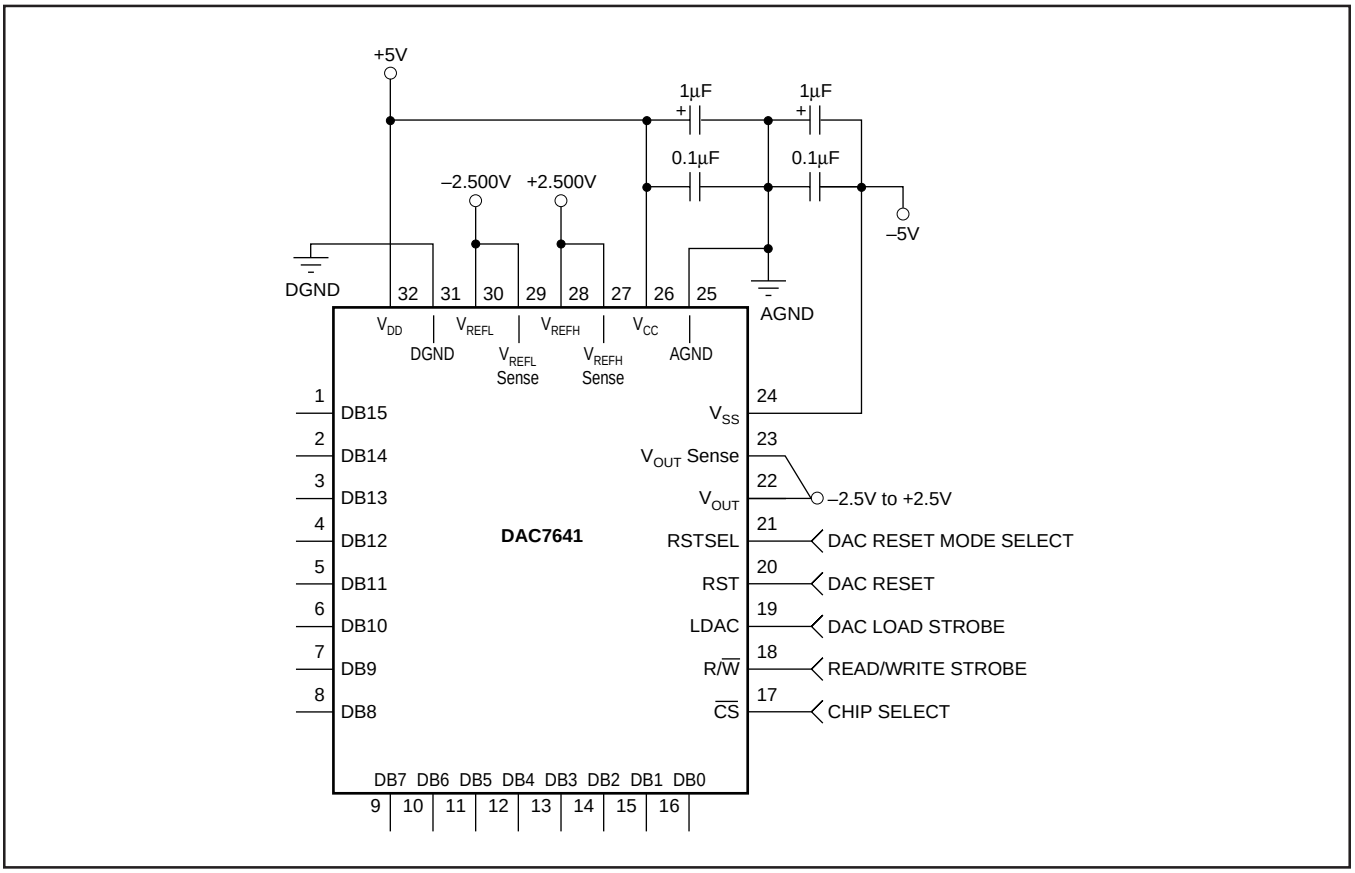


FIGURE 3. Dual-Supply Operation.

ANALOG OUTPUTS

When V_{SS} = –5V (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, guaranteed over the –40°C to +85°C temperature range. With V_{SS} = 0V (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must be taken when measuring the zero-scale error with V_{SS} = 0V. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H, 0001_H, 0002_H, etc.) if the output amplifier has a negative offset. At the negative limit of –2mV, the first specified output starts at code 0040_H.

Due to the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of 38µV. With a load current of 1mA, series wiring and connector resistance (see Figure 4) of only 40mΩ (R_{W2}) will cause a voltage drop of 40µV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 1mA load, a 10 milli-inch wide printed circuit conductor 600 milli-inches long will result in a voltage drop of 30µV.

The DAC7641 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (see Figure 4), thus ensuring an accurate output voltage.

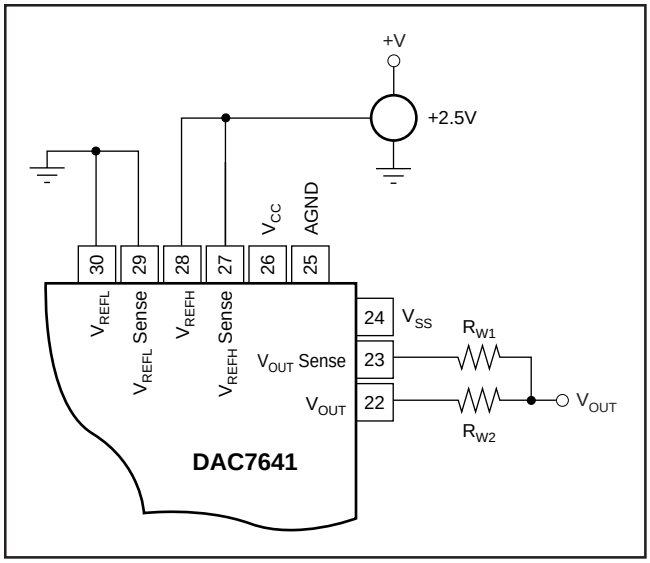


FIGURE 4. Analog Output Closed-Loop Configuration. R_W represents wiring resistances.

REFERENCE INPUTS

The reference inputs, $V_{REF}L$ and $V_{REF}H$, can be any voltage between V_{SS} + 2.5V and V_{CC} – 2.5V provided that $V_{REF}H$ is at least 1.25V greater than $V_{REF}L$. The minimum output of each DAC is equal to $V_{REF}L$ plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to $V_{REF}H$ plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –4.75V to –5.25V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the $V_{REF}H$ input and out of $V_{REF}L$ depends on the DAC output voltages and can vary from a few microamps to approximately 0.5mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC7641 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 13 show different reference configurations and the effect on the linearity and differential linearity.

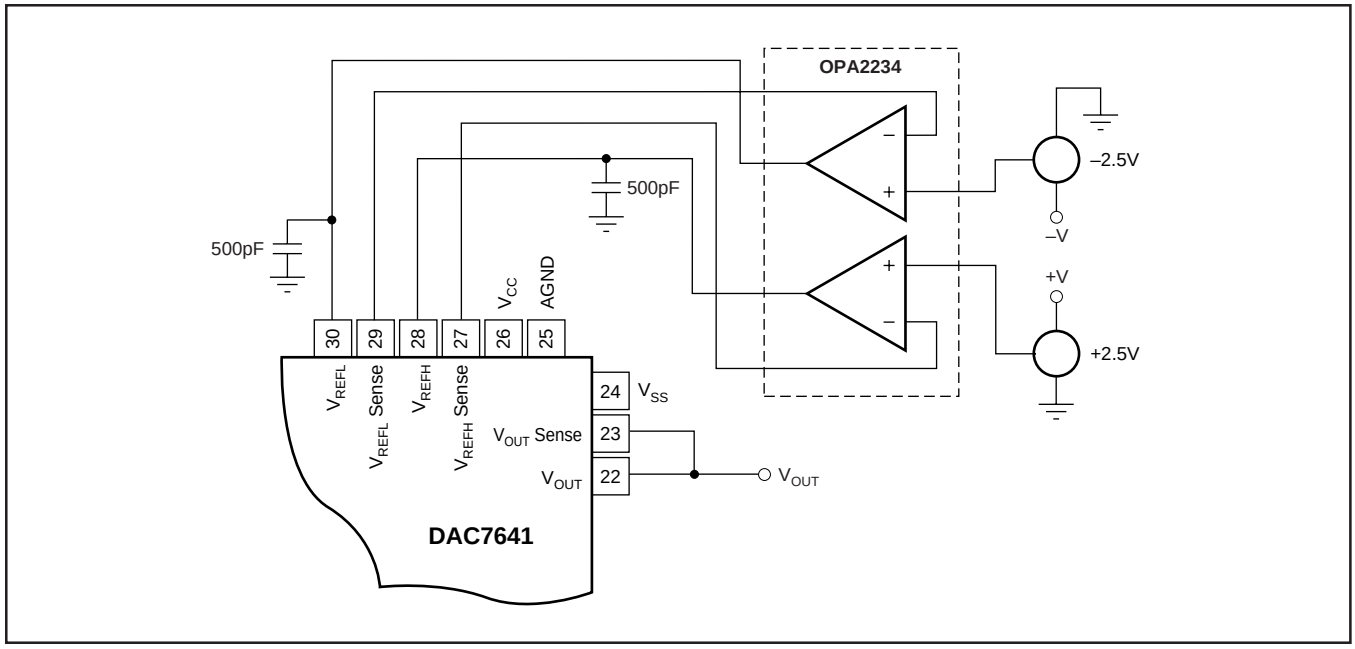
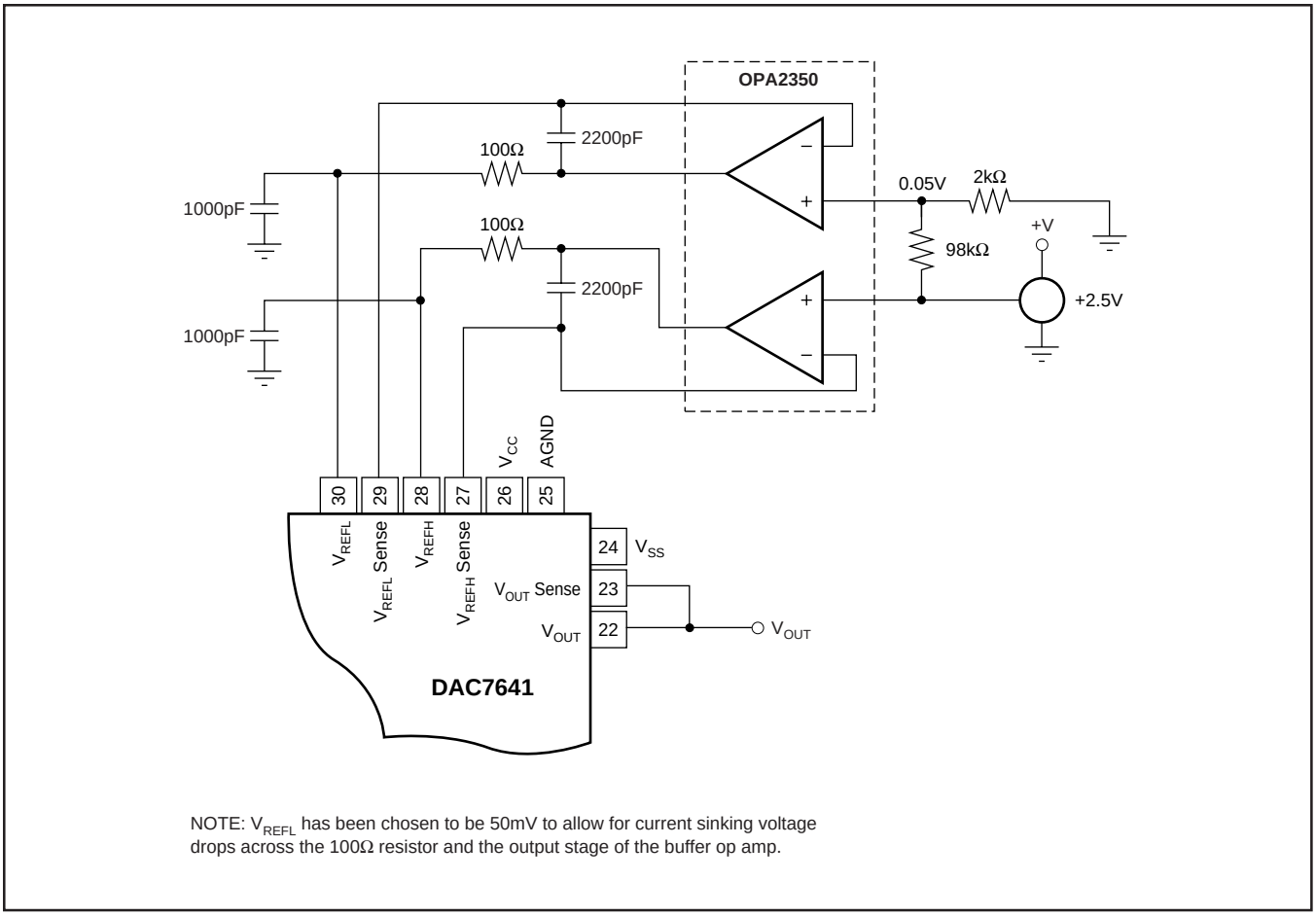


FIGURE 5. Dual Supply Configuration-Buffered References, used for Dual Supply Performance Curves.



NOTE: V_{REFL} has been chosen to be 50mV to allow for current sinking voltage drops across the 100Ω resistor and the output stage of the buffer op amp.

FIGURE 6. Single-Supply Buffered Reference with a Reference Low of 50mV.

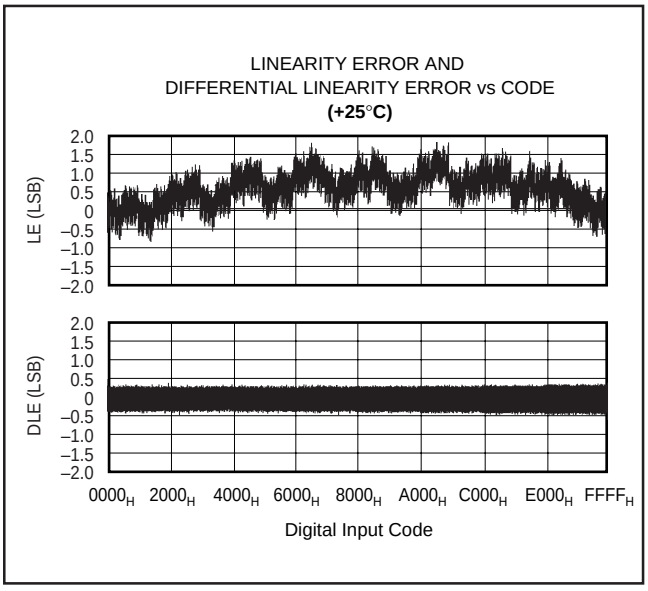


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 6.

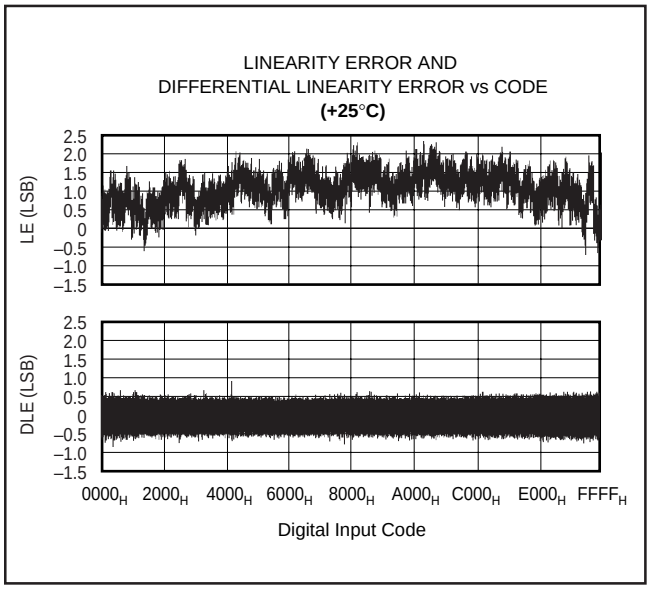


FIGURE 8. Integral Linearity and Differential Linearity Error Curves for Figure 9.

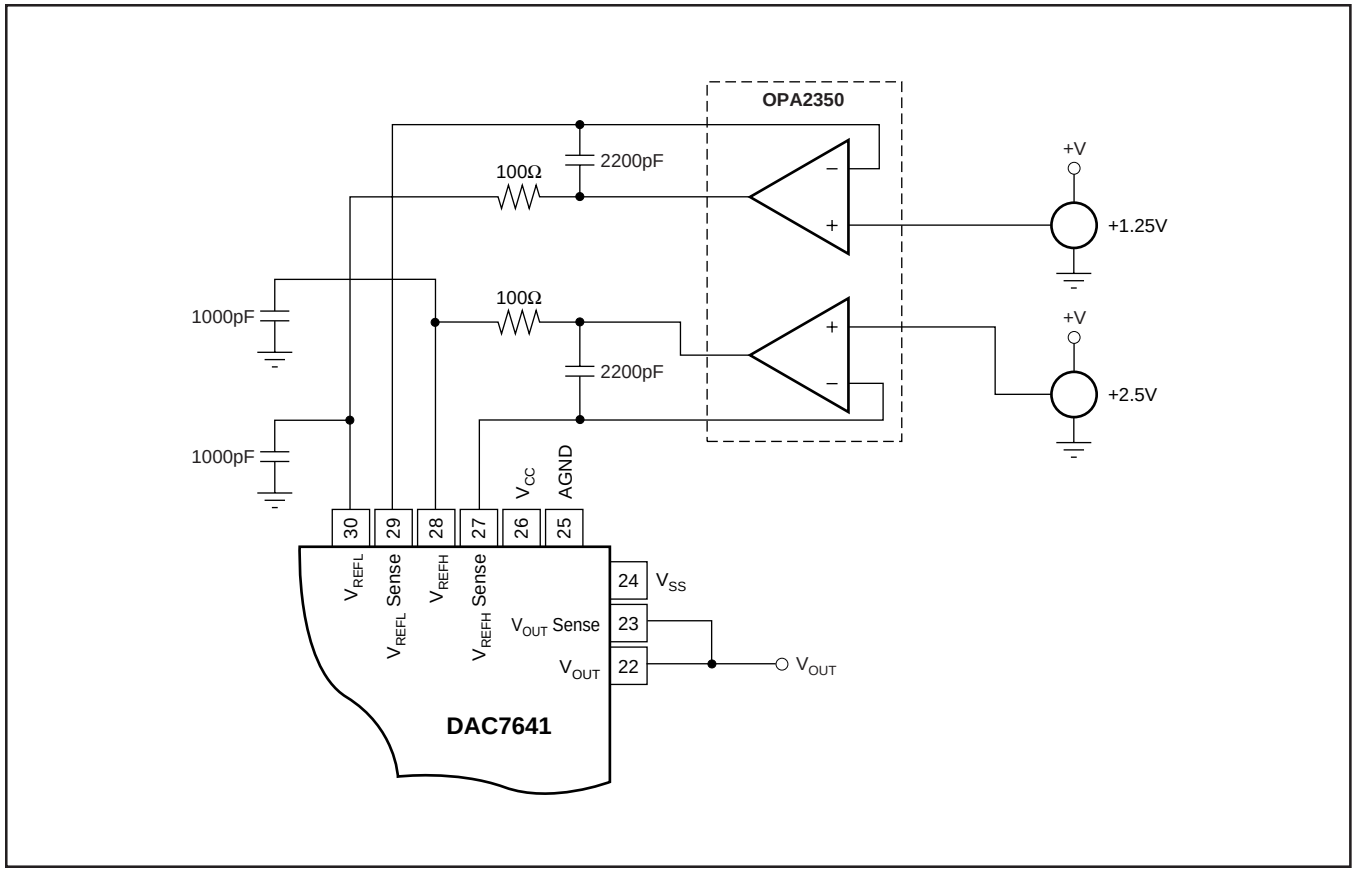


FIGURE 9. Single-Supply Buffered Reference with $V_{REF}L$ = +1.25V and $V_{REF}H$ = +2.5V.

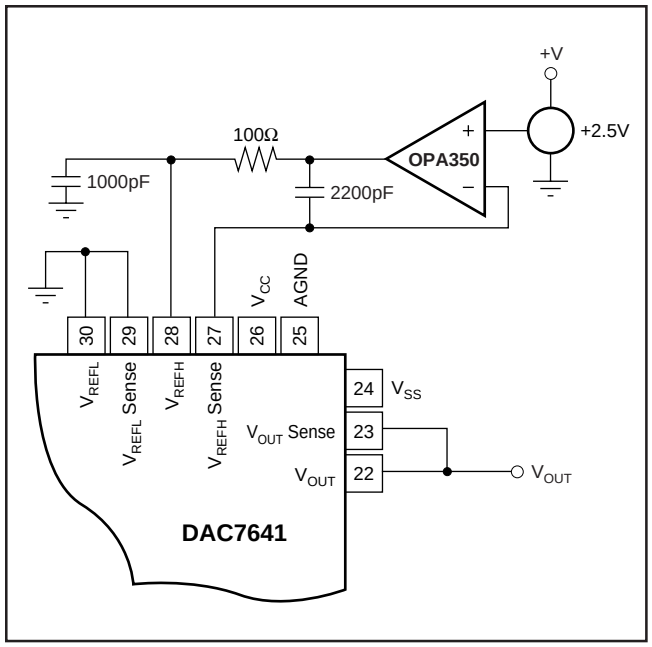


FIGURE 10. Single-Supply Buffered $V_{REF}H$.

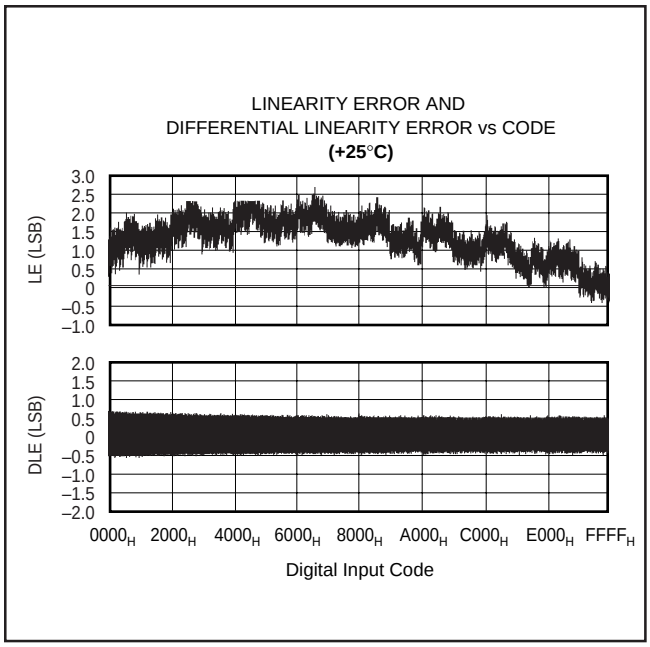


FIGURE 11. Linearity and Differential Linearity Error Curves for Figure 10.

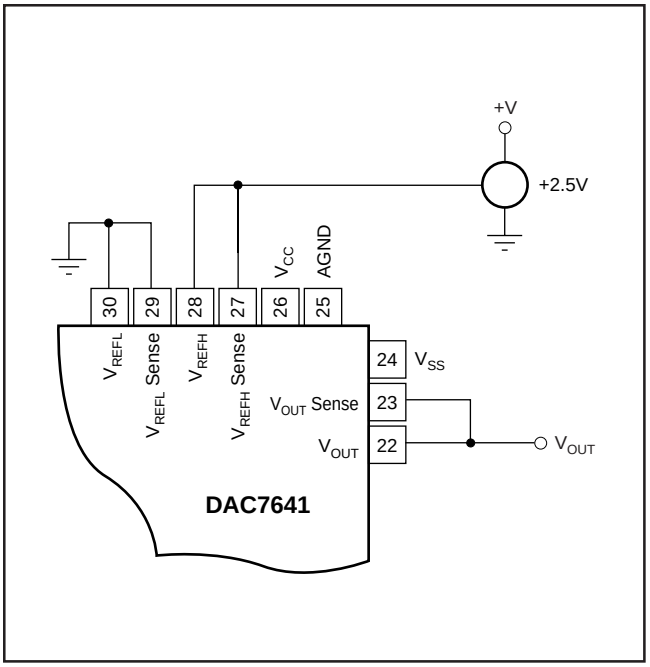


FIGURE 12. Low Cost Single-Supply Configuration.

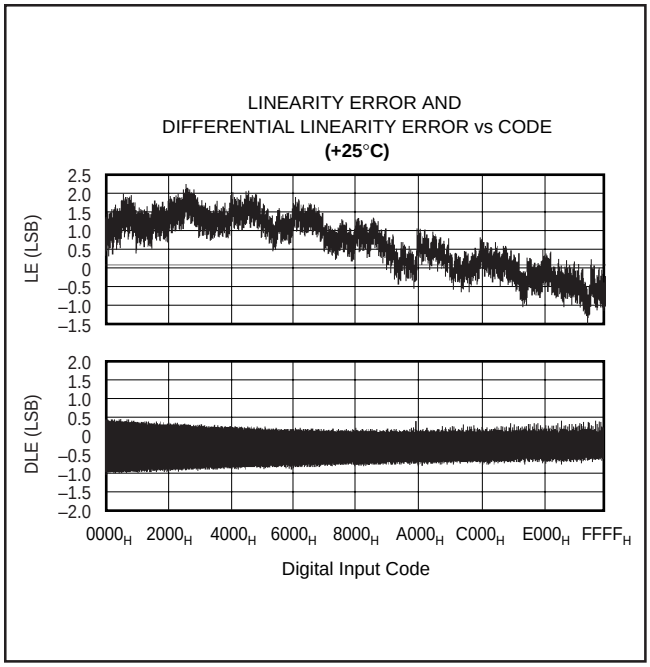


FIGURE 13. Linearity and Differential Linearity Error Curves for Figure 12.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7641. Note that the internal register is edge triggered and not level triggered. When the LDAC signal is transitioned to HIGH, the digital word currently in the register is latched.

The double-buffered architecture is designed so that the DAC input register can be written to at any time.

R/$\overline{W}$	$\overline{CS}$	RST	RSTSEL	LDAC	REGISTER	REGISTER	INPUT MODE
L	L	H	X	X	Write	Hold	Write Input
H	L	H	X	X	Read	Hold	Read Input
X	H	H	X	↑	Hold	Write	Update
X	H	H	X	H	Hold	Hold	Hold
X	X	↑	L	X		Reset to Zero	Reset to Zero
X	X	↑	H	X		Reset to Midscale	Reset to Midscale

TABLE I. DAC7641 Logic Truth Table.

DIGITAL TIMING

Figure 14 and Table II provide detailed timing for the digital interface of the DAC7641.

DIGITAL INPUT CODING

The DAC7641 input data is in Straight Binary format. The output voltage is given by Equation 1.

$$V_{OUT} = V_{REF}L + \frac{(V_{REF}H - V_{REF}L) \bullet N}{65,536} \qquad (1)$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

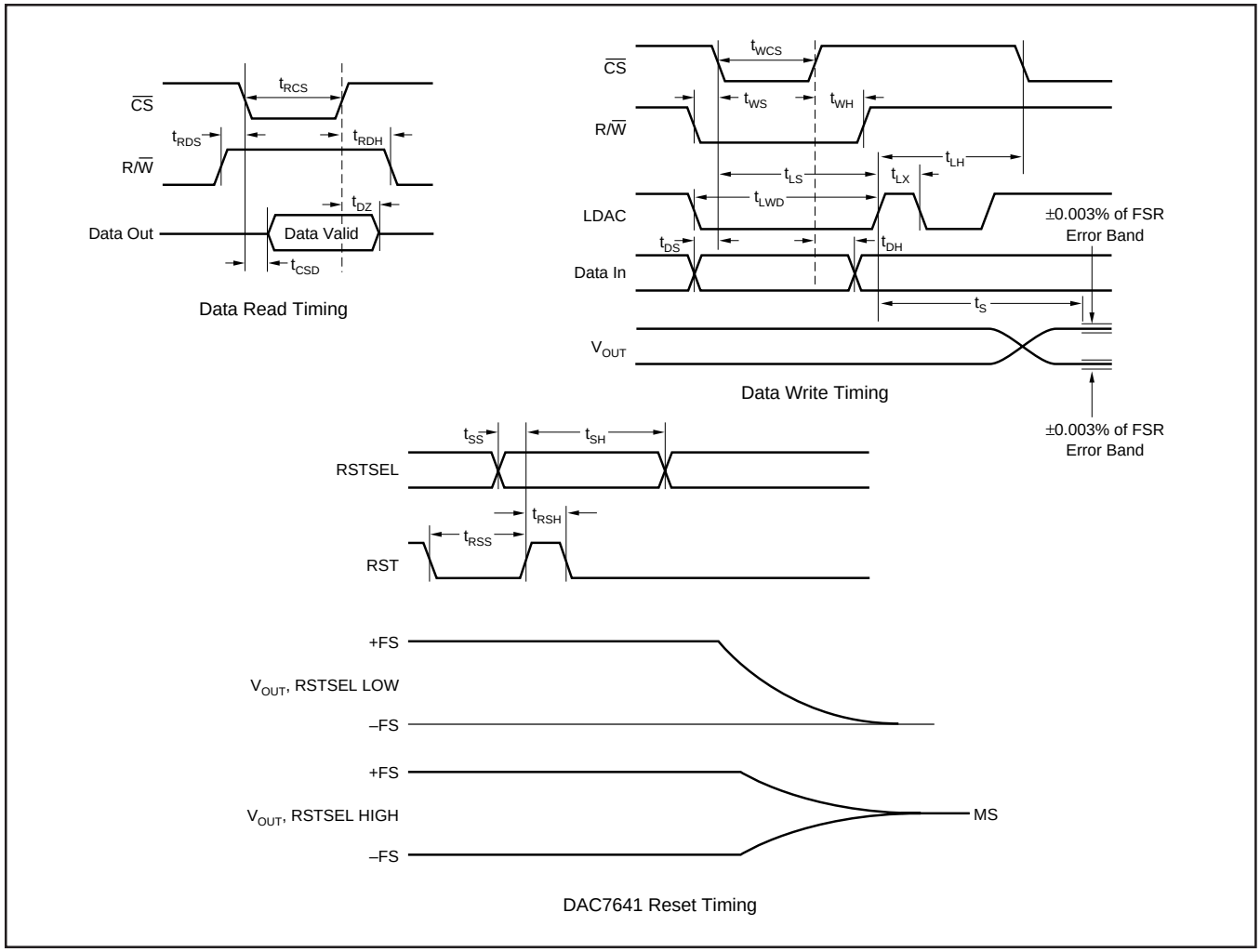


FIGURE 14. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	150			ns
t_{RDS}	R/$\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	R/$\overline{W}$ HIGH after $\overline{CS}$ HIGH	10			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus in High Impedance	10		100	ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		100	150	ns
t_{WCS}	$\overline{CS}$ LOW for Write	40			ns
t_{WS}	R/$\overline{W}$ LOW to $\overline{CS}$ LOW	0			ns
t_{WH}	R/$\overline{W}$ LOW after $\overline{CS}$ HIGH	10			ns
t_{LS}	$\overline{CS}$ LOW to LDAC HIGH	30			ns
t_{LH}	$\overline{CS}$ LOW after LDAC HIGH	100			ns
t_{LX}	LDAC HIGH	100			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	10			ns
t_{LWD}	LDAC LOW	100			ns
t_{SS}	RSTSEL Valid Before RESET HIGH	0			ns
t_{SH}	RSTSEL Valid After RESET HIGH	200			ns
t_{RSS}	RESET LOW Before RESET HIGH	10			ns
t_{RSH}	RESET LOW After RESET HIGH	10			ns
t_S	Settling Time			10	µs

TABLE II. Timing Specifications (T_A = –40°C to +85°C).

DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7641 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7641 offers both a differential reference input as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows transistor to be placed within the loop to implement a digitally-programmable, uni-directional current source. The availability of a differential reference also allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left(\left(\frac{V_{REF}H - V_{REF}L}{R_{SENSE}}\right) \bullet \left(\frac{N\ Value}{65,536}\right)\right) + \left(V_{REF}L / R_{SENSE}\right) \quad (2)$$

Figure 15 shows a DAC7641 in a 4mA to 20mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left(\left(\frac{2.5V - 0.5V}{125\Omega}\right) \bullet \left(\frac{N\ Value}{65,536}\right)\right) + \left(\frac{0.5V}{125\Omega}\right) \quad (3)$$

At full-scale, the output current is 16mA plus the 4mA for the zero current. At zero scale the output current is the offset current of 4mA (0.5V/125Ω).

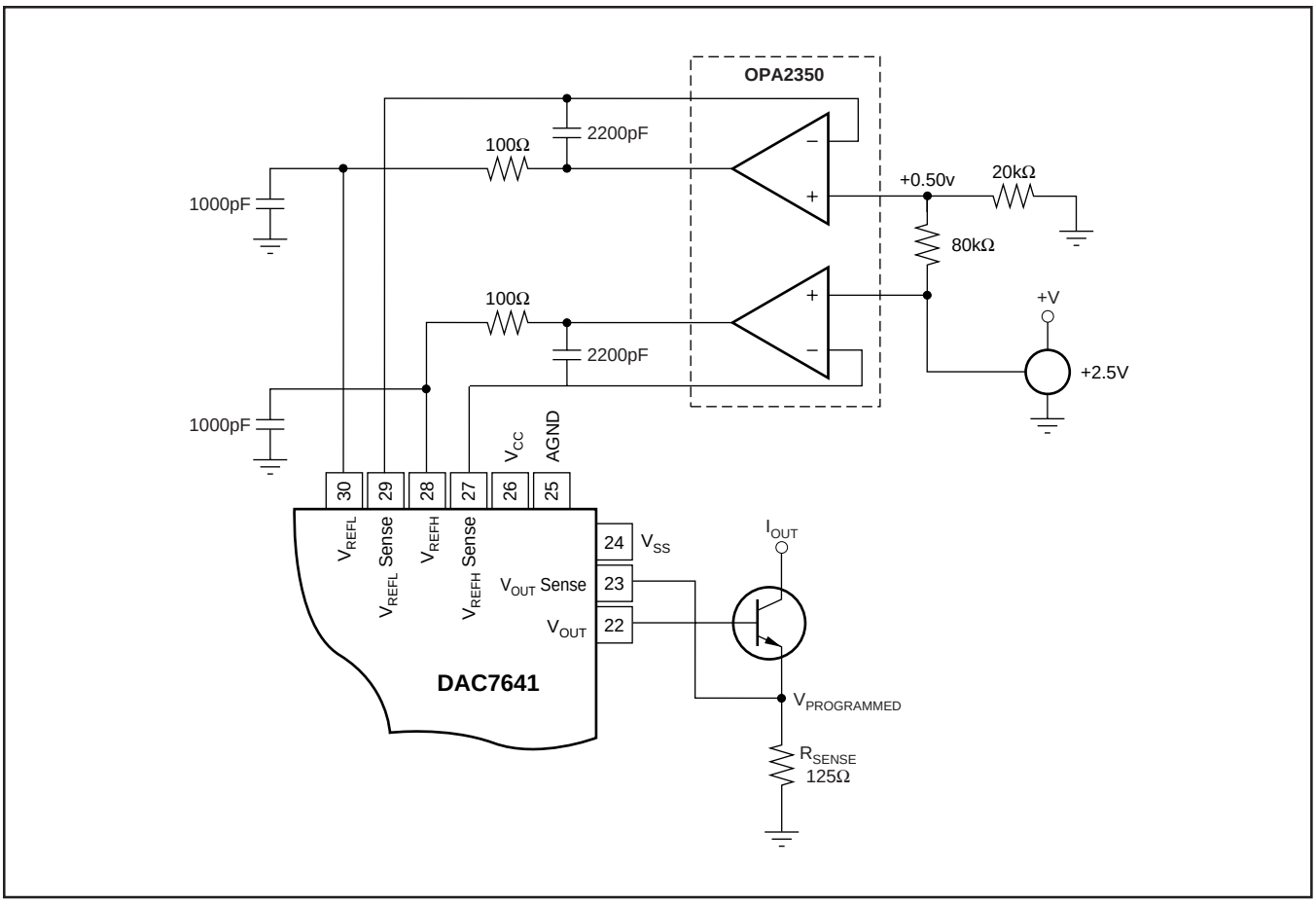


FIGURE 15. 4-to-20mA Digitally Controlled Current Source.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7641Y/250	ACTIVE	TQFP	PBS	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	7641Y	Samples
DAC7641YB/250	ACTIVE	TQFP	PBS	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	7641Y B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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