WLSC Wire-bondable vertical Low-profile Si Capacitors down to 100 μm

Rev 2.2

Key features

- Ultra low profile 100 µm.
- Low leakage current.
- High stability (temperature and voltage).
- Negligible capacitance loss through aging.
- Compatible with standard wire bonding assembly (ball and wedge).

(please refer to our Assembly Application Note for more details)

Key applications

- Any demanding applications such as radar, wireless
 infrastructure communication, data broadcasting...
- Standard wire bonding approach (top & bottom gold metallization), thanks to a perfect pad flatness.
- Decoupling / DC noise and harmonic filtering / Matching networks (e.g: GaN power amplifier, LDMOS).
- High reliability applications.
- Downsizing. Low profile applications (100 μm).
- Fully compatible with single layer ceramic capacitors and Metal Oxide Semiconductor.

The WLSC (100 µm thick) capacitors target **RF High Power applications** for wireless communication (e.g: 5G), radar and data broadcasting systems. The WLSC capacitors are suitable for **DC decoupling, matching network, and harmonic / noise filtering functions**. The unique technology of integrated passive devices in silicon developed by Murata Integrated Passive Solutions, can **solve most of the problems encountered** in demanding applications. These Si capacitors in ultra–deep trenches have been developed with a semiconductor process which enables the integration of **high capacitance density** from 1.55 nF/mm² to 250 nF/mm² (with a breakdown voltage of respectively **450 V** to 11 V).

Our SiCap technology features **high reliability** - up to 10 times better than alternative capacitors technologies - thanks to a full control of the production process with **high temperature curing** (above 900°C) generating a highly pure oxide. This technology provides **industry-leading performance** particularly in terms of capacitor stability over the full operating DC voltage & temperature range. In addition, intrinsic properties of the silicon show a low dielectric absorption and a low to zero piezo electric effect resulting **in no memory effect**. This Silicon based technology is ROHS compliant.

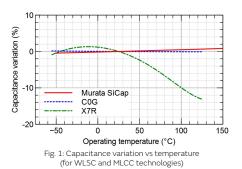


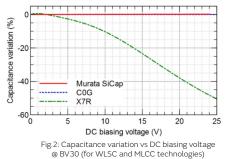


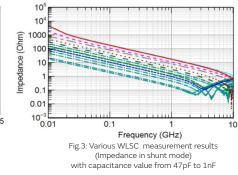
Electrical specifications

WLSC.xxx	Wire-Bondable vertical Low-profile Si Capacitors down to 100 µm from -55°C to 150°C					
Part number	Capacitance	BV	Case size	Thickness		
935146528247-xxT	47 pF	150 V	0201	100 µm		
935146522310-xxT	100 pF	150 V	0101	100 µm		
935146521310-xxT	100 pF	150 V	0202	100 µm		
935146529315-xxT	150 pF	150 V	015015	100 µm		
935146832410-xxT	1 nF	30 V	0101	100 µm		
935146632410-xxT	1 nF	50 V	0101+	100 µm		
935146521410-xxT	1 nF	150 V	0202	100 µm		
935146831510-xxT	10 nF	30 V	0202	100 µm		
935146630510-xxT	10 nF	50 V	0303	100 µm		
935146634522-xxT	22 nF	50 V	0504	100 µm		

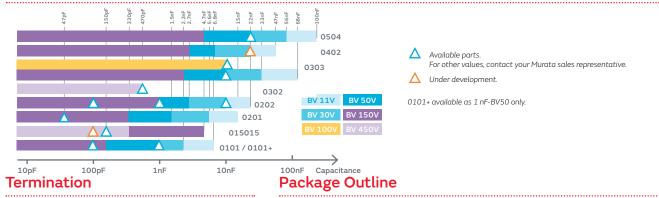
Parameter	Value		
Capacitance range	47 pF to 22 nF(*)		
Capacitance tolerances	±15 % (*)		
Operating temperature range	-55 °C to 150°C (*)		
Storage temperature range	-70°C to 165°C(**)		
Temperature coefficient	+60 ppm/K		
Breakdown Voltage (BV)	11 V, 30 V, 50 V, 100 V, 150 V, 450 V(*)		
Capacitance variation versus RVDC	0.02 %/V (from 0 to RVDC)		
Equivalent Series Inductance (ESL)	Typ 50 pH @ SRF (***)		
Equivalent Series Resistance (ESR)	Max 50 mΩ (***)		
Insulation resistance	10 GΩ @ RVDC @ 25°C t>120s for 10 nF		
Aging	Negligible, < 0.001 % / 1000 h		
Reliability	FIT<0.017 parts / billions hours		
Capacitor thickness	100 µm(*)		
(*) Other values on request (**) w/o packing (***) with wire-bonding de-embedded			





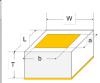


Capacitance range



Can be directly mounted on the PCB using die bonding and wire bonding(s). Bottom electrode in Ti/Ni/Au and top electrode in Gold (TiWAu). Other top finishings available on request (ex: Aluminum). Compatible with standard wire bonding assembly (ball and wedge).

	Pad dimension mm		Case size mm (typ ±0.02 mm)		
	a	b	L	W	т
0101	>0.15	>0.15	0.25	0.25	
0101+	>0.15	>0.15	0.294(*)	0.294(*)	
015015	>0.281	>0.281	0.381	0.381	
0201	>0.40	>0.15	0.50	0.25	
0202	>0.40	>0.40	0.50	0.50	0.10
0302	>0.7	>0.4	0.8	0.5	
0303	>0.70	>0.70	0.80	0.80	
0402	>0.9	>0.4	1.00	0.50	
0504	>1.15	>0.9	1.25	1.00	



(*) Only for 1nF / BV50 case size = 0.294x0.294mm





Packaging

Tape & reel (up to 0202 case size included), waffle pack, film frame carrier or raw wafer delivery.

Assembly by Soldering

The attachment techniques recommended by Murata for the WLSC capacitors on the customers substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata Silicon capacitors please download the assembly instructions on www.murata.com and read them carefully.

WB/WT/WXSC 250µm/WLSC100µm - Assembly by Wirebonding	
Rev. 1.8	
General description	
This document describes the attachment techniques recommended by Murata* for their vertical capacitors on the customer substrates. This document is non-exhaustive. Customers with specific attachment requirements or	
attachment scenarios that are not covered by this document should contact Murata.	
Murata Silicon capacitor W type	
Handling precautions and storage It is preferable to repack the remaining capacitors quantities after any process step, in the same conditions as before	
the opening (ESD bag + N2). The assembly of capacitors has to be done one year maximum after the opening date.	
Store the capacitors in a clean environment and in the manufacturer's package, without a rapid thermal change in an indoor room and with a temperature between -10 to 40 degree C	
To avoid contamination and damage like scratches and cracks, our recommendations are:	
 Die must never be handled with bare hands Avoid touching the active face Do not store and transport die outside protective bags, boxes, sawn tape 	
 Bor hot store and transport de outside protective dags, boxes, sawn tape Work only in ESD environments Plastic tweezers or a soft vacuum tool are recommended to remove the silicon die from the packing. 	
Standard packing is tape & reel for die size larger than 0201 but silicon capacitors can be provided within waffle	
pack, gelpack or sawing frame. Please contact the Murata sales contact for drawing and references (mis@murata.com).	
Pad Finishing It: • For topectode for information • A 11500 Please download the assembly instruction on www.murata.com on www.murata.com	
The proposed finishing is:	
• For top electrode(s):	
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Please download the assent on www.murata.com and read them carefully before use	
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MJ 241-	
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For the assembly instructions, pleas	se go to :
https://www.murata.com/ and follo	w the sections :
Products > Capacitor > Silicon Capa	
FIGUELS > Capacitor > Silicon Capa	

Download the pdf files called "Assembly Note WBSC / WTSC / WXSC / WLSC_V1.8_Murata "

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