36V, 1.5A Buck-Boost µModule Regulator

FEATURES

- **Complete Buck-Boost Switch Mode Power Supply**
- **Wide Input Voltage Range: 3V to 36V**
- **Wide Output Voltage Range: 1V to 36V**
- **12V/0.8A Output at $6V_{IN}$**
- **12V/1.5A Output at $12V_{IN}$**
- **12V/1.5A Output at $36V_{IN}$**
- **Integrated Three-Terminal Capacitors and Spread Spectrum for Excellent EMI Performance**
- **Compliant with CISPR25 Class 5 Limits (Refer to Figure 25)**
- 300kHz to 2MHz Fixed Switching Frequency with External Frequency Synchronization
- Adjustable Output Current Limit
- Output Current Monitoring
- RoHS Compliant Package
- 6.25mm × 6.25mm × 2.22mm BGA Package

APPLICATIONS

- Battery-Operated Devices
- Test and Measurement Equipment
- Industrial Control
- Solar Powered Voltage Regulator
- Solar Powered Battery Charging

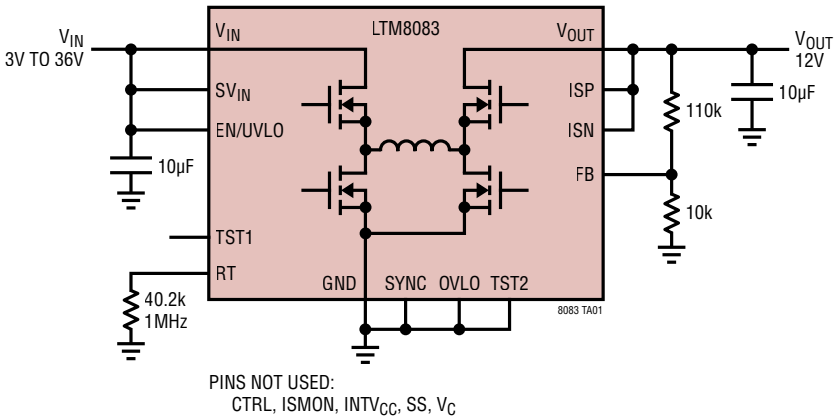
DESCRIPTION

The LTM®8083 is a $36V_{IN}$, Buck-Boost µModule® Regulator. Included in the package are the switching controller, power switches, inductor, and support components. All that is needed to complete the design is resistors for setting the output voltage and operating frequency, and input and output capacitors. Operating over an input voltage range from 3V to 36V, the LTM8083 can regulate output voltages between 1V and 36V with seamless low-noise transitions between operation regions, as well as controlling both input and output average currents through external sense resistors.

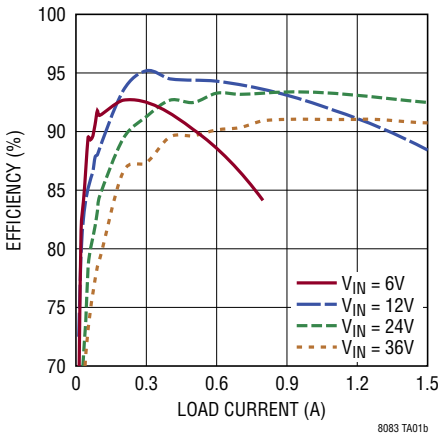
The low profile package enables utilization of unused space on the bottom of PC boards for high density point of load regulation. The LTM8083 is packaged in thermally enhanced, compact over-molded Ball Grid Array (BGA) packages suitable for automated assembly by standard surface mount equipment. The LTM8083 is RoHS compliant.

TYPICAL APPLICATION

$12V_{OUT}$ from 3-$36V_{IN}$ Buck-Boost Regulator



Efficiency at 12V Output



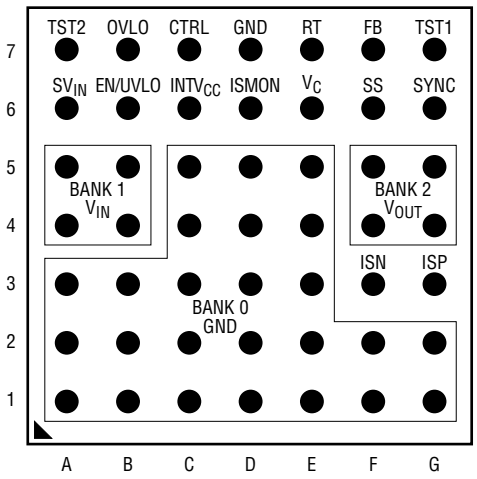
Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, SV_{IN}, EN/UVLO, ...40V
V_{OUT}, ISP, ISN 40V
OVLO, CTRL, FB, SYNC, $INTV_{CC}$ 5V
ISP-ISN .....–1V to 1V
Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 150°C
Solder Temperature ..... 260°C

PIN CONFIGURATION



BGA PACKAGE
49-LEAD (6.25mm × 6.25mm × 2.22mm)
T_{JMAX} = 125°C, θ_{JA} = 23°C/W,
θ_{JCtop} = 21.8°C/W, $\theta_{JCbottom}$ = 7.6°C/W

NOTE:
1) θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
2) θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3) REFER TO PAGE 16 FOR LAB MEASUREMENT AND DERATING INFORMATION.
4) WEIGHT = 231mg

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
		DEVICE	FINISH CODE			
LTM8083EY#PBF	SAC305 (RoHS)	8083	1	BGA	3	–40°C to 125°C
LTM8083IY#PBF						

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.

*The temperature grade is identified by a label on the shipping container.

- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = SV_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	V_{IN} = SV_{IN}	●			3	V
Output DC Voltage	R_{FBtop} = 113kΩ, $R_{FBbottom}$ open R_{FBtop} = 113kΩ, $R_{FBbottom}$ = 10kΩ R_{FBtop} = 113kΩ, $R_{FBbottom}$ = 3.24kΩ			1 12 36		V V V
Output DC Current	V_{IN} = 6V, V_{OUT} = 12V V_{IN} = 12V, V_{OUT} = 12V V_{IN} = 36V, V_{OUT} = 12V			0.8 1.5 1.5		A A A
Quiescent Current into V_{IN}	EN/UVLO = 0V (Shutdown) EN/UVLO = 1.5V, V_{OUT} = 12V, I_{OUT} = 0A			0.9 2.6		µA mA
Output Voltage Line Regulation	3V < V_{IN} < 36V, V_{OUT} = 12V, I_{OUT} = 0.1A	●		0.02	0.15	%/V
Output Voltage Load Regulation	V_{OUT} = 12V, 0.0A < I_{OUT} < 1.5A (Note 4)	●		0.5	1.5	%
Output Voltage Ripple	V_{OUT} = 12V, I_{OUT} = 0A			10		mV
Switching Frequency	RT = 178kΩ RT = 14.3kΩ			300 2000		kHz kHz
Voltage at FB pin		●	0.985	1	1.015	V
EN/UVLO Rising Threshold	Starts Switching (UVLO)			1.240		V
EN/UVLO Falling Threshold	Stops Switching (UVLO)	●	1.190	1.210	1.230	V
ENUVLO Shutdown Threshold	$INTV_{CC}$ = Disabled	●	0.3	0.6	0.9	V
EN/UVLO Pin Current	EN/UVLO = 0.3V EN/UVLO = 1.1V EN/UVLO = 1.3V		–1 2.0 –0.3	0 2.5 0	1 3.0 0.3	µA µA µA
OVLO Rising Threshold		●	1.196	1.235	1.250	V
OVLO Falling Threshold			1.055	1.120	1.140	V
ISN Pin Current	V_{ISP} = V_{ISN} = 12V V_{ISP} = V_{ISN} = 0V			23 –10		µA µA
ISP Pin Current	V_{ISP} = V_{ISN} = 12V V_{ISP} = V_{ISN} = 0V			23 –10		µA µA
ISP-ISN Current Sense Threshold	V_{CTRL} = Float V_{CTRL} = 0.75V		96 40	105 52	116 65	mV mV
ISMON Voltage	V_{ISP} = 100mV, V_{ISN} = 0V		1.20	1.25	1.30	V
SS Pull-Up Current	V_{FB} = 0.8V, V_{SS} = 0V			32		µA
SS Pull-Down Current	V_{FB} = 1V, V_{SS} = 2V			1.25		µA
SYNC input Low Threshold					0.4	V
SYNC input High Threshold			1.5			V
SYNC Pin Current			–0.1	0	0.1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

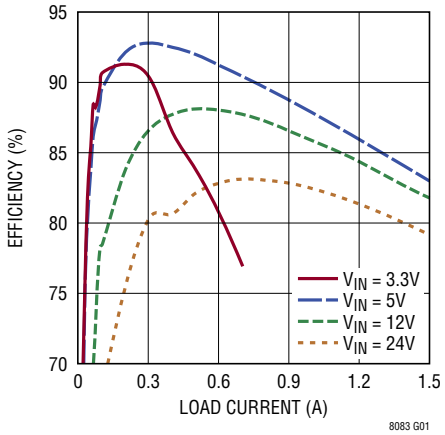
Note 2: The LTM8083E is guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8083I is guaranteed over the –40°C to 125°C operating junction temperature range.

Note 3: The LTM8083 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

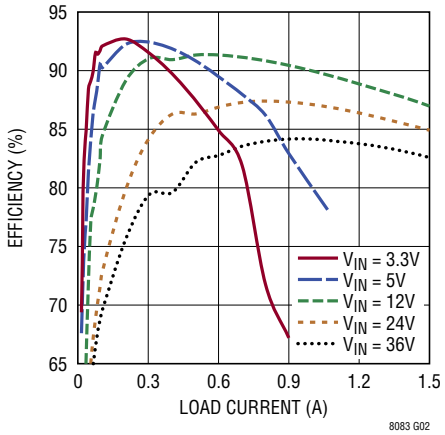
Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

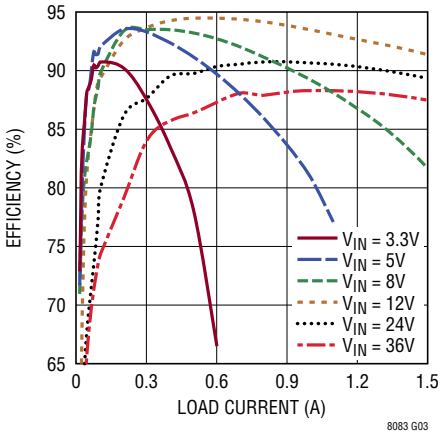
3.3V_{OUT} Efficiency



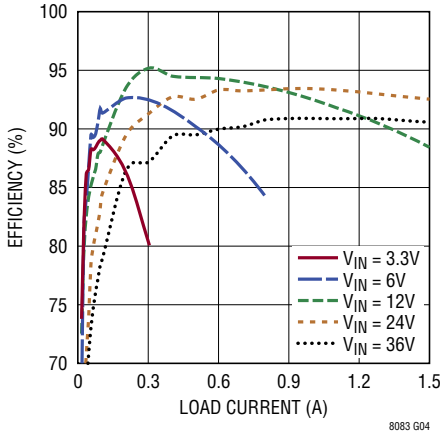
5V_{OUT} Efficiency



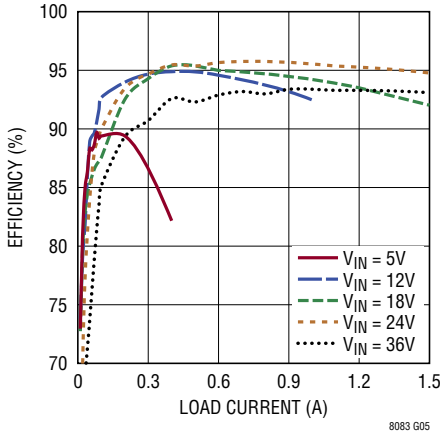
8V_{OUT} Efficiency



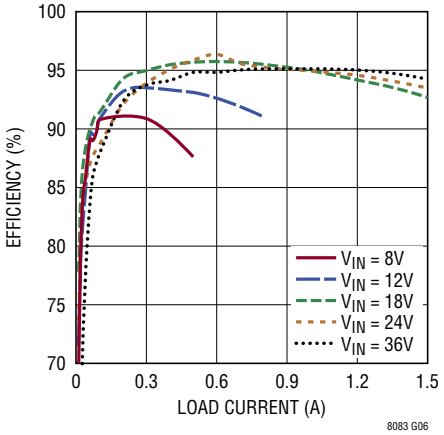
12V_{OUT} Efficiency



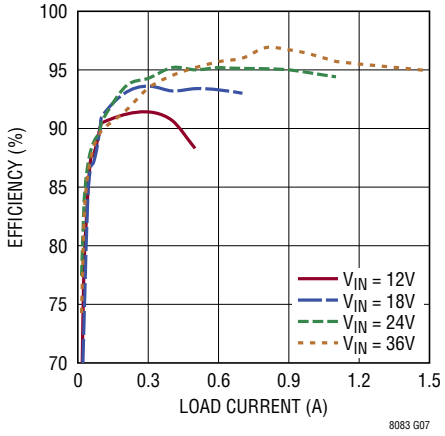
18V_{OUT} Efficiency



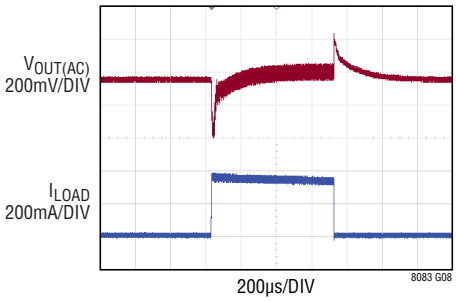
24V_{OUT} Efficiency



36V_{OUT} Efficiency

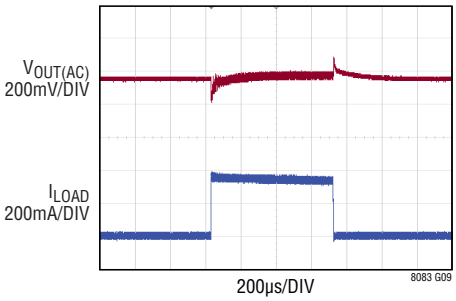


Transient Response from 3.3V_{IN} to 5V_{OUT}



V_{IN} = 3.3V, V_{OUT} = 5V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

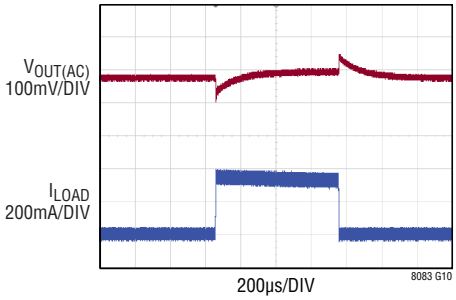
Transient Response from 5V_{IN} to 5V_{OUT}



V_{IN} = 5V, V_{OUT} = 5V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

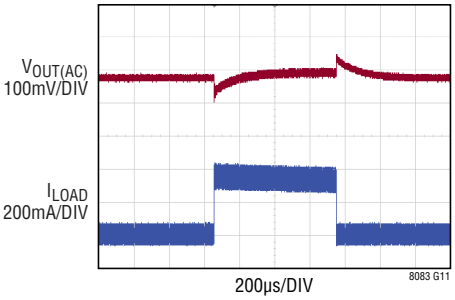
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Transient Response from $12V_{IN}$ to $5V_{OUT}$



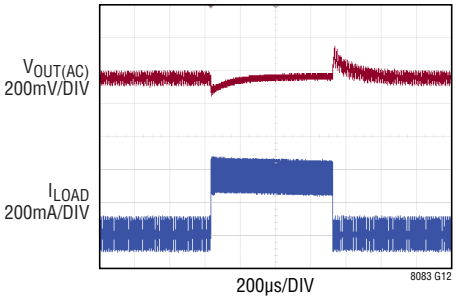
V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

Transient Response from $24V_{IN}$ to $5V_{OUT}$



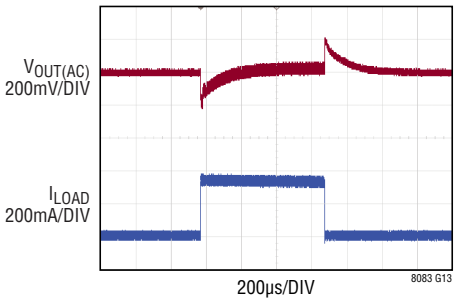
V_{IN} = 24V, V_{OUT} = 5V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

Transient Response from $36V_{IN}$ to $5V_{OUT}$



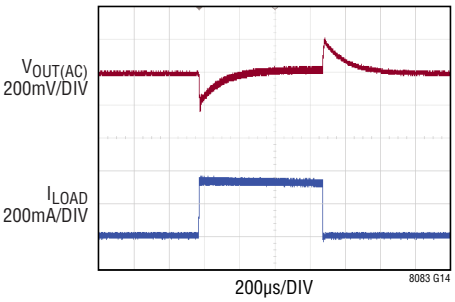
V_{IN} = 36V, V_{OUT} = 5V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

Transient Response from $6V_{IN}$ to $12V_{OUT}$



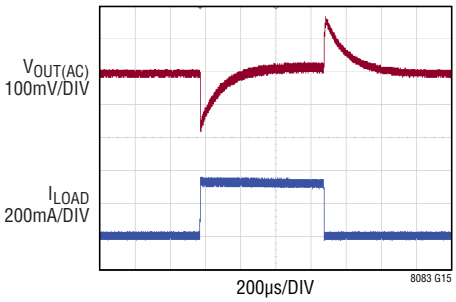
V_{IN} = 6V, V_{OUT} = 12V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

Transient Response from $12V_{IN}$ to $12V_{OUT}$



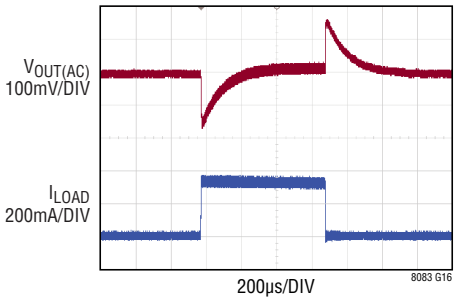
V_{IN} = 12V, V_{OUT} = 12V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

Transient Response from $24V_{IN}$ to $12V_{OUT}$



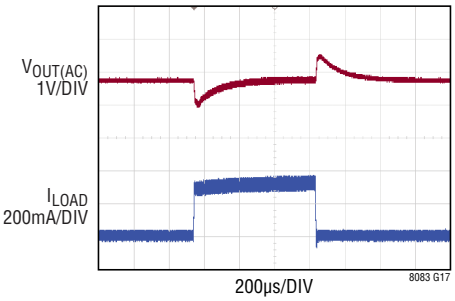
V_{IN} = 24V, V_{OUT} = 12V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

Transient Response from $36V_{IN}$ to $12V_{OUT}$



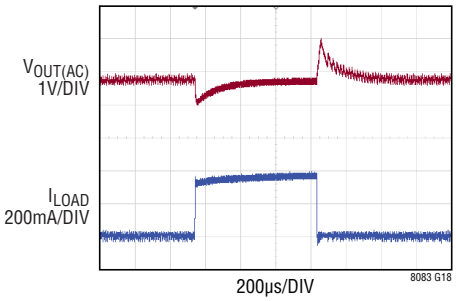
V_{IN} = 36V, V_{OUT} = 12V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

Transient Response from $18V_{IN}$ to $36V_{OUT}$



V_{IN} = 18V, V_{OUT} = 36V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

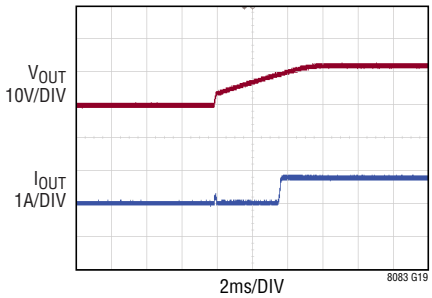
Transient Response from $36V_{IN}$ to $36V_{OUT}$



V_{IN} = 36V, V_{OUT} = 36V, f_{SW} = 1MHz,
0.375A (25%) LOAD STEP, 0.375A/µs
C_{OUT} = 10µF CERAMIC
INTERNAL COMPENSATION

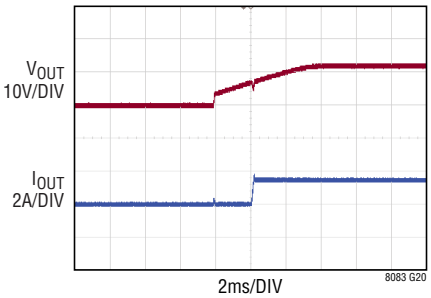
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Start-Up with $6V_{IN}$ and $12V_{OUT}$ at I_{OUT} = 0.8A



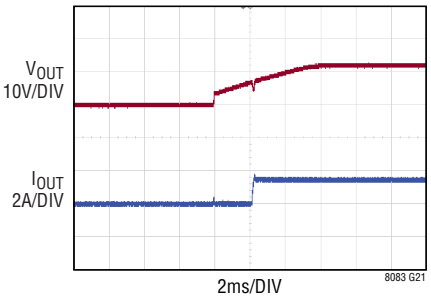
V_{IN} = 6V, V_{OUT} = 12V, f_{SW} = 1MHz, 0.8A
C_{OUT} = 10µF CERAMIC
SOFT-START CAPACITOR = 0.1µF
USE EN/UVLO PIN TO CONTROL START-UP

Start-Up with $12V_{IN}$ and $12V_{OUT}$ at I_{OUT} = 1.5A



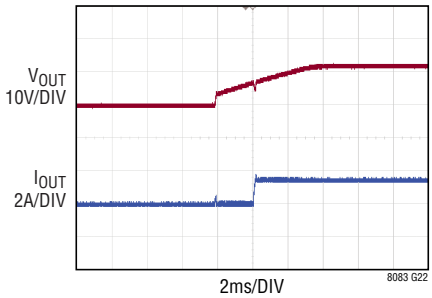
V_{IN} = 12V, V_{OUT} = 12V, f_{SW} = 1MHz, 1.5A
C_{OUT} = 10µF CERAMIC
SOFT-START CAPACITOR = 0.1µF
USE EN/UVLO PIN TO CONTROL START-UP

Start-Up with $24V_{IN}$ and $12V_{OUT}$ at I_{OUT} = 1.5A



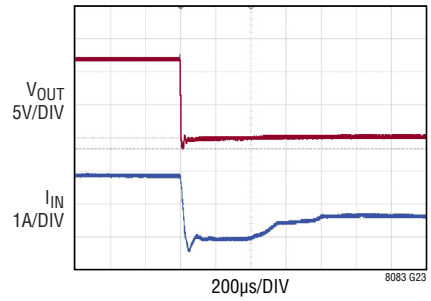
V_{IN} = 24V, V_{OUT} = 12V, f_{SW} = 1MHz, 1.5A
C_{OUT} = 10µF CERAMIC
SOFT-START CAPACITOR = 0.1µF
USE EN/UVLO PIN TO CONTROL START-UP

Start-Up with $36V_{IN}$ and $12V_{OUT}$ at I_{OUT} = 1.5A

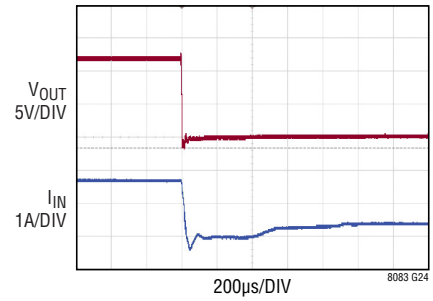


V_{IN} = 36V, V_{OUT} = 12V, f_{SW} = 1MHz, 1.5A
C_{OUT} = 10µF CERAMIC
SOFT-START CAPACITOR = 0.1µF
USE EN/UVLO PIN TO CONTROL START-UP

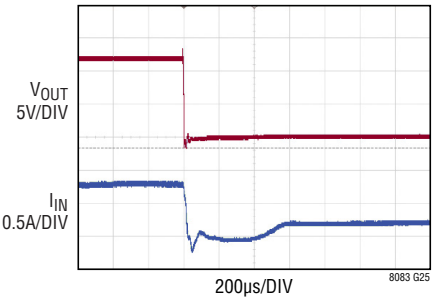
Short-Circuit with $6V_{IN}$ and $12V_{OUT}$ at I_{OUT} = 0.8A



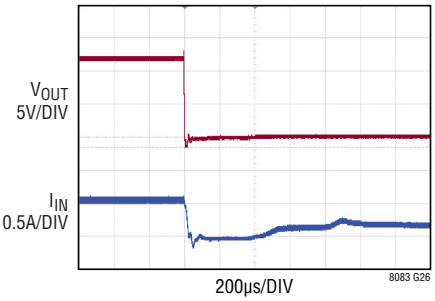
Short-Circuit with $12V_{IN}$ and $12V_{OUT}$ at I_{OUT} = 1.5A



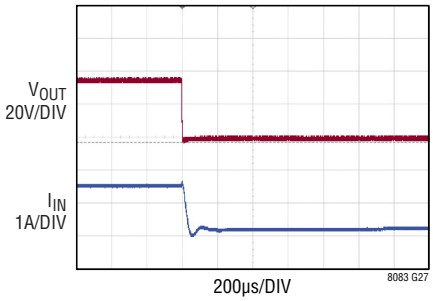
Short-Circuit with $24V_{IN}$ and $12V_{OUT}$ at I_{OUT} = 1.5A



Short-Circuit with $36V_{IN}$ and $12V_{OUT}$ at I_{OUT} = 1.5A



Short-Circuit with $24V_{IN}$ and $36V_{OUT}$ at I_{OUT} = 1A



PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (Bank 0, Pin D7): Tie these GND pins to a local ground plane below the LTM8083 and the circuit components. In most applications, the majority of the heat of the LTM8083 flows out through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider (R_{FB}) to this net.

V_{IN} (Bank 1): Input Power. The V_{IN} pin supplies current to the internal power switches. This pin must be locally bypassed with an external, low ESR ceramic capacitor.

V_{OUT} (Bank 2): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

SV_{IN} (Pin A6): Bias Supply. The SV_{IN} pin supplies the internal circuitry and the $INTV_{CC}$ linear regulator. Connect this pin to V_{IN} or another power supply. Bypass this pin to ground with a ceramic capacitor.

TST2 (Pin A7): Test Pin 2. This pin is used in production testing. Do not drive a voltage into this pin; This pin must be tied to GND.

EN/UVLO (Pin B6): Enable and Undervoltage Lockout. Force the pin below 0.3V to shut down the part and reduce V_{IN} quiescent current to 0.9µA. Force the pin above 1.240V for normal operation. The accurate 1.210V falling threshold can be used to program an undervoltage lockout (UVLO) threshold with a resistor divider from V_{IN} to ground. An accurate 2.5µA pull-down current allows the programming of V_{IN} UVLO hysteresis. If neither function is used, tie this pin directly to V_{IN}.

OVLO (Pin B7): Overvoltage Lockout. The OVLO pin is used to program an overvoltage lockout (OVLO) threshold with a resistor divider from V_{IN} to ground. Force the pin above 1.250V to pull SS pin to ground and stop switching. If not used, tie this pin to ground.

$INTV_{CC}$ (Pin C6): Internal 3.6V Linear Regulator Output. Powered from the SV_{IN} pin, the $INTV_{CC}$ supplies the internal control circuitry and gate drivers. No decoupling ceramic capacitor is required.

CTRL (Pin C7): ISP-ISN Current Sense Adjustment. The voltage on this pin determines current limit threshold voltage of ISP-ISN. The current limit threshold is 100mV when this pin is floated. Apply a voltage below 1.35V to reduce the current limit threshold of ISP-ISN across the output sense resistor. This pin is internally pulled up to 2V reference voltage with a 100k resistor. See the Applications Information section for more details.

ISMON (Pin D6): ISP-ISN Current Monitor. This pin produces a voltage that is 10 times the voltage of V_{ISP}-V_{ISN} plus 0.25V offset voltage. ISMON will equal 1.25V when $V_{ISP} – V_{ISN}$ = 100mV.

V_C (Pin E6): Error Amplifier Output. The V_C pin is normally left open in LTM8083 applications as it is already internally compensated.

RT (Pin E7): Switching Frequency Setting. Connect a resistor from this pin to ground to set the internal oscillator frequency from 300kHz to 2MHz. See Table 1 for resistor values to set common switching frequencies.

ISN (Pin F3): Negative Terminal of Current Sense Resistor. Ensure accurate current sense with Kelvin connection.

SS (Pin F6): Soft-Start. A 10nF capacitor has been integrated inside LTM8083 for start-up. To increase the built-in soft-start time, connect a capacitor from SS to GND. If no additional soft-start time is required, leave this pin floating.

FB (Pin F7): Feedback. The LTM8083 regulates its FB pin to 1V. Connect a resistor divider from this pin to the output and to ground to set the output voltage. When an output current sense resistor is connected to ISP and ISN, connect the resistor network to ISN for improved load regulation.

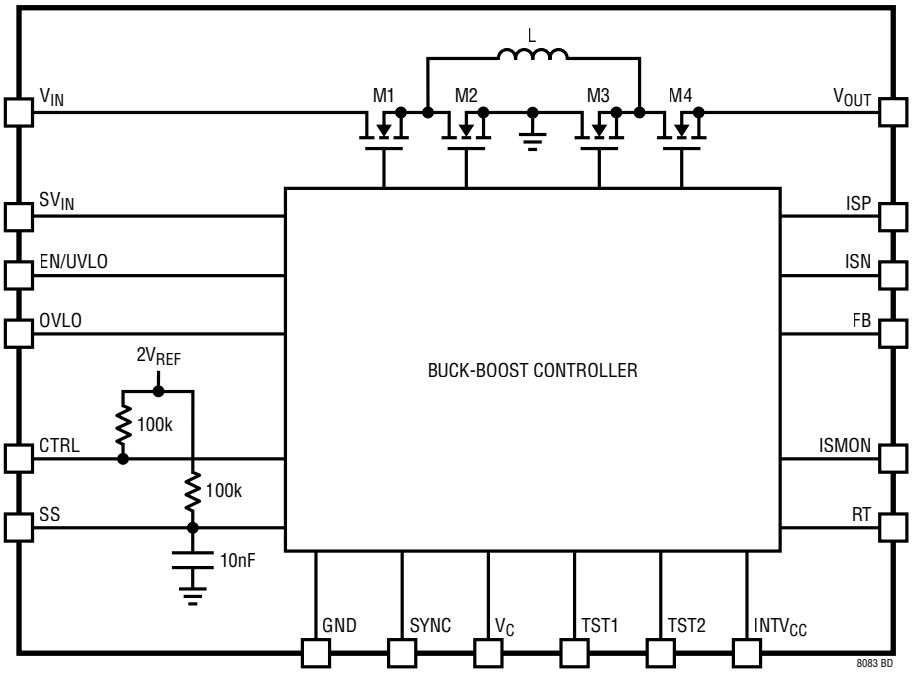
PIN FUNCTIONS

ISP (Pin G3): Positive Terminal of Current Sense Resistor. Ensure accurate current sense with Kelvin connection.

SYNC (Pin G6): Switching Frequency Synchronization or Spread Spectrum Enable. Ground this pin to switch at the internal oscillator frequency. Apply a clock signal for external frequency synchronization. Tie to $INTV_{CC}$ for 25% triangle spread spectrum above internal oscillator frequency.

TST1 (Pin G7): Test Pin 1. This pin is used in production testing. This pin must be floated. Do not drive a voltage to this pin.

BLOCK DIAGRAM



OPERATION

The LTM8083 is a standalone non-isolated buck-boost switching DC/DC power supply. The buck-boost topology allows the LTM8083 to regulate its output voltage below or above input voltage. Maximum output current is determined by the input voltage. Higher input voltages yield higher maximum output current.

The LTM8083 contains ADI's proprietary peak-buck peak-boost current mode controller with four internal low resistance N-channel DMOS switches, power inductor and a modest amount of input and output capacitors.

This control scheme directly senses the inductor current across the internal power switches and provides smooth transition between buck region, buck-boost region and boost region. A simplified block diagram is given on the previous page. A precisely regulated output voltage is programmable via an external resistor divider from 1V to 36V. The input voltage range is from 3V to 36V.

The LTM8083 is a fixed frequency PWM regulator. A resistor from RT pin to GND sets the switching frequency from 300kHz to 2MHz, allowing applications to be optimized for broad area and efficiency. Driving the SYNC pin will synchronize the LTM8083 to an external clock source.

In addition to the voltage control loop, the LTM8083 is equipped with average current control loop for the output. Add a current sense resistor between ISP and ISN to limit the output current below the maximum value set by the CTRL pin. The ISMON pin reflects the current flowing through the sense resistor.

A voltage less than 1.35V applied to the CTRL pin reduces the maximum output current. The current flowing through the sense resistor is reflected by the voltage of the ISMON pin. Drive CTRL pin below 0.2V to stop switching.

At light load, the LTM8083 typically runs at its switching frequency in discontinuous conduction mode. Both buck and boost reverse current sense thresholds are set to be zero, thus preventing any reverse current flowing from the output to the input.

As the load becomes lower and lower, the LTM8083 may run in pulse-skip mode, where the switches are held off for multiple cycles (i.e., skipping pulses) to maintain the regulation.

The LTM8083 enters shutdown mode with less than 0.9µA quiescent current when the EN/UVLO pin is below its shutdown threshold (0.3V minimum).

The LTM8083 is equipped with a thermal shutdown that inhibits operation when junction temperature is above 165°C. Prolonged or repetitive operation at junction temperature higher than 125°C may damage or impair the reliability of the device.

A low-ESL 10nF three-terminal capacitor is added on the input side as well as output side, improving noise decoupling for better EMI performance. With a small filter and Spread Spectrum function enabled, the LTM8083 module passes CISPR25 Class 5 conducted and radiated EMI standards. Refer to Figure 2 and Figure 3 for more details.

APPLICATIONS INFORMATION

The front page shows a typical LTM8083 application circuit. This Applications Information section serves as a guideline of selecting external components for typical applications. The examples and equations in this section assume continuous conduction mode unless otherwise specified.

Programming Output Voltage and Thresholds

The LTM8083 has a voltage feedback pin FB that can be used to program a constant-voltage output. The output voltage can be set by selecting the values of R5 and R6 (Figure 1) according to the following equation:

$$V_{OUT} = 1.00V \bullet \frac{R5+R6}{R6}$$

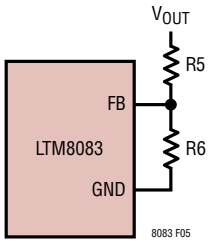


Figure 1. Feedback Resistor Connection

In addition, the FB pin also sets output overvoltage threshold. Once the FB pin hits its overvoltage threshold 1.05V, the LTM8083 stops switching by turning off all four power switches for protection. The output overvoltage threshold can be set as:

$$V_{OUT(OVP)} = 1.05V \bullet \frac{R5+R6}{R6}$$

Switching Frequency Selection

The LTM8083 uses a constant frequency control scheme between 300kHz and 2MHz. Selection of the switching frequency is a trade-off between efficiency and capacitor size to filter input and output voltage switching noise. Low frequency operation improves efficiency by reducing MOSFET switching loss but requires larger capacitor values. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band. For most applications, 1MHz switching frequency is recommended.

Switching Frequency Setting

The switching frequency of the LTM8083 can be set by the internal oscillator. With the SYNC pin pulled to ground, the switching frequency is set by a resistor from the RT pin to ground. Table 1 shows R_T resistor values for common switching frequencies.

Table 1. Switching Frequency vs R_T Value (1% Resistor)

f_{OSC} (kHz)	R_T (kΩ)
300	178
400	124
600	78.7
800	56.2
1000	40.2
1200	33.2
1400	26.1
1600	21.5
1800	17.4
2000	14.3

Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the LTM8083 implements a triangle spread spectrum frequency modulation scheme. With the SYNC pin tied to $INTV_{CC}$, the LTM8083 starts to spread its switching frequency 25% above the internal oscillator frequency. Besides, a low-ESL three-terminal capacitor is added on the input side as well as output side to further improve the EMI performance. Figure 2 and Figure 3 show the noise spectrum of the front page application with spread spectrum enabled and a small EMI filter at $12V_{IN}$, $12V_{OUT}$, and 1A load current. The detailed schematic is shown in Figure 25.

Frequency Synchronization

The LTM8083 switching frequency can be synchronized to an external clock using the SYNC pin. Driving the SYNC with a 50% duty cycle waveform is always a good choice, otherwise maintain the duty cycle between 10% and 90%. Due to the use of a phase-locked loop (PLL) inside, there is no restriction between the synchronization frequency

APPLICATIONS INFORMATION

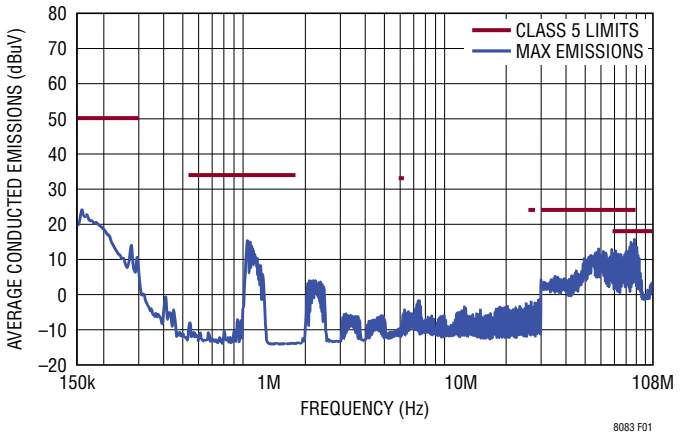


Figure 2. CISPR 25 Average Conducted EMI

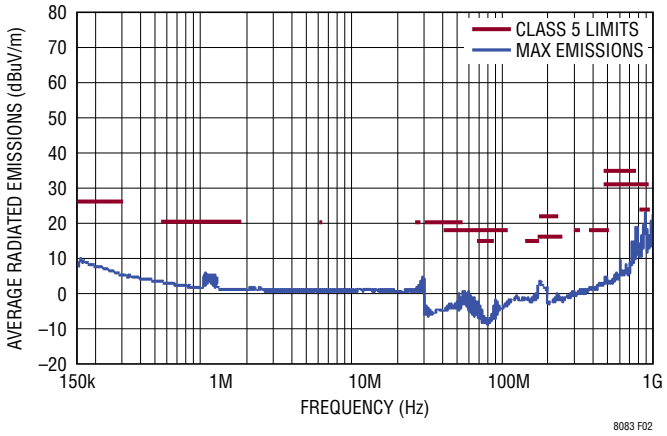


Figure 3. CISPR 25 Average Radiated EMI

and the internal oscillator frequency. The rising edge of the synchronization clock represents the beginning of a switching cycle.

C_{IN} and C_{OUT} Selection

Input and output capacitors are necessary to suppress voltage ripple caused by discontinuous current moving in or out of the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low equivalent series resistance (ESR). Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

To suppress high frequency switching spikes, ceramic capacitors of at least 1µF should be placed from V_{IN} to GND and V_{OUT} to GND as close to the LTM8083 pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R capacitors of dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage. In an application circuit, they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Input Capacitance C_{IN}:

Discontinuous input current is highest in the buck region due to the top switch M1 toggling on and off. A 10nF low-ESL three-terminal capacitor is integrated inside the module to decouple high-frequency input noise. Make sure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. In buck region, the input RMS current is given by:

$$I_{RMS} = I_{oMAX} \bullet \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{oMAX}/2$. This simple worst-case condition is commonly used for design.

Output Capacitance C_{OUT}:

Discontinuous current shifts from the input to the output in the boost region. Make sure that the C_{OUT} capacitor network is capable of reducing the output voltage ripple. The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given

APPLICATIONS INFORMATION

output ripple voltage. The maximum steady state ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{CAP(BOOST)} = \frac{I_{oMAX} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f_{SW}}$$

$$\Delta V_{CAP(BUCK)} = \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{8 \bullet L \bullet C_{OUT} \bullet V_{IN(MAX)} \bullet f_{SW}^2}$$

The maximum steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR(BOOST)} = \frac{V_{OUT} \bullet I_{oMAX}}{V_{IN(MAX)}} \bullet ESR$$

$$\Delta V_{ESR(BUCK)} = \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \bullet L \bullet f_{SW}} \bullet ESR$$

The bulk output capacitors defined as C_{OUT} are chosen with low enough ESR to meet the output voltage ripple and transient requirements. C_{OUT} can be the low ESR tantalum capacitor, the low ESR polymer capacitor or the ceramic capacitor. Multiple capacitors can be placed in parallel to meet the ESR and RMS current handling requirements. The typical capacitance is 10µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required. A 10nF low-ESL three-terminal capacitor is integrated inside the module to decouple high-frequency output noise. Table 6 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot at a current transient.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 3.6V at the $INTV_{CC}$ pin from the SV_{IN} supply pin. The $INTV_{CC}$ powers internal circuitry and gate drivers in the LTM8083. No bypassing capacitor is required.

Programming V_{IN} UVLO and OVLO

A resistor divider from V_{IN} to the EN/UVLO pin implements V_{IN} undervoltage lockout (UVLO). The EN/UVLO enable falling threshold is set at 1.21V with 30mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage on the pin is below 1.21V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are:

$$V_{IN(UVLO+)} = 1.24V \bullet \frac{R1+R2}{R2} + 2.5\mu A \bullet R1$$

$$V_{IN(UVLO-)} = 1.21V \bullet \frac{R1+R2}{R2}$$

Figure 4 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the LTM8083 in shutdown with 0.9µA quiescent current.

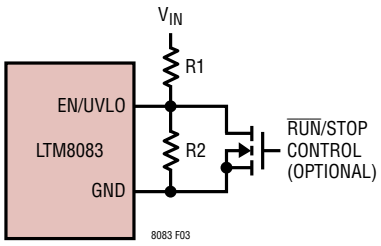


Figure 4. V_{IN} Undervoltage Lockout (UVLO)

A resistor divider from V_{IN} to the OVLO pin implements V_{IN} overvoltage lockout (OVLO). The OVLO rising threshold is set at 1.235V with 115mV falling hysteresis. Figure 5 shows the implementation of V_{IN} OVLO function. The programmable OVLO thresholds are:

$$V_{IN(OVLO+)} = 1.235V \bullet \frac{R3+R4}{R4}$$

$$V_{IN(OVLO-)} = 1.120V \bullet \frac{R3+R4}{R4}$$

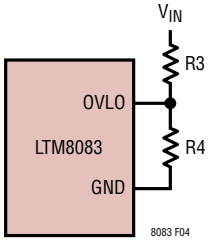


Figure 5. V_{IN} Overvoltage Lockout (OVLO)

APPLICATIONS INFORMATION

Programming Current Limit Threshold

The ISP-ISN current is programmed by placing a current sensing resistor, R_{CS}, in series with the output. The voltage drop across R_{CS} is (Kelvin) sensed by the ISP and ISN pins. The voltage on CTRL pin determines current limit threshold voltage of ISP-ISN. The default setting of the current limit threshold is full-scale 100mV. The CTRL pin is pulled up to 2V reference voltage with a 100k resistor internally. A resistor can be added between CTRL and GND to form a voltage divider or an external voltage below 1.3V can be applied to the CTRL pin to reduce the current limit threshold of ISP-ISN across the output sense resistor. When the CTRL pin voltage, V_{CTRL}, is less than 1.15V, the current limit threshold is:

$$I_{CL} = \frac{V_{CTRL} - 250mV}{10 \bullet R_{CS}}$$

When V_{CTRL} is between 1.15V and 1.35V, the current limit threshold varies with V_{CTRL}, but departs from the equation above by an increasing amount as V_{CTRL} increases. Ultimately, when V_{CTRL} > 1.35V the output current threshold is 100mV and no longer varies. The typical $V_{(ISP-ISN)}$ threshold vs V_{CTRL} is listed in Table 2.

Table 2. $V_{(ISP-ISN)}$ Threshold vs V_{CTRL}

V_{CTRL} (V)	$V_{(ISP-ISN)}$ (mV)
1.15	90
1.20	94.5
1.25	98
1.30	99.5
1.35	100

When V_{CTRL} is higher than 1.35V, the output current limit threshold is:

$$I_{CL} = \frac{100mV}{R_{CS}}$$

The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the output load, or with a resistor divider to V_{IN} to reduce output power and switching current when V_{IN} is low. The presence of a time varying differential voltage ripple signal across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by higher load current, lower switching frequency, or smaller value output filter capacitor. Some level of ripple signal is acceptable, and the compensation capacitor on the V_C pin filters the signal so the average difference between ISP and ISN is regulated to the user-programmed value. The ripple voltage amplitude (peak-to-peak) in excess of 20mV should not cause misoperation, but may lead to noticeable offset between the average value and the user-programmed value.

Monitoring Sensed Current

The ISMON pin provides a linear indication of the current flowing through the sensing resistor on the output. It outputs a buffered and amplified monitor of the voltage difference between ISP and ISN pins. The equation for V_{ISMON} is:

$$V_{ISMON} = 10 \bullet V_{(ISP-ISN)} + 250mV$$

Soft-Start

The SS pin can be used to program soft-start by connecting an external capacitor C_{SS} from the SS pin to ground. A 10nF capacitor has been integrated inside the module. The internal 32µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage rises smoothly and transitions into output voltage regulation. The soft-start range is defined to be the voltage range from 0V to the FB voltage, which is 1V when output is regulated. The soft-start time can be approximately calculated as:

$$t_{SS} = 1V \bullet \frac{C_{SS} + 10nF}{32\mu A}$$

Make sure the C_{SS} is at least five to ten times larger than the optional compensation capacitor on the V_C pin.

Loop Compensation

The LTM8083 has already been internally compensated and should be stable for all output voltages and capacitor combinations including all ceramic capacitor applications. If more switching noise attenuation is required, an optional capacitor can be added on V_C pin to ground outside of the module. Furthermore, to further increase

APPLICATIONS INFORMATION

the bandwidth and phase margin of the circuit, a feedforward capacitor (C_{FF}) could be added by connecting from V_{OUT} to FB pin which is in parallel with R5 in Figure 1.

The LTpowerCAD design tool is available to download online to perform specific control loop optimization and analyze the control stability and load transient performance.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD 51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD 51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives three thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a 95mm × 76mm PCB with four layers.
2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

   A graphical representation of the aforementioned thermal resistances is given in Figure 6; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

   As a practical matter, it should be clear to the reader that no individual or sub-group of the three thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

APPLICATIONS INFORMATION

Within the LTM8083, be aware that there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM8083 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM8083 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due diligence yields the set of derating curves shown in this data sheet. After these laboratory tests have been performed and correlated to the LTM8083 model, then the θ_{JA} is provided assuming approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

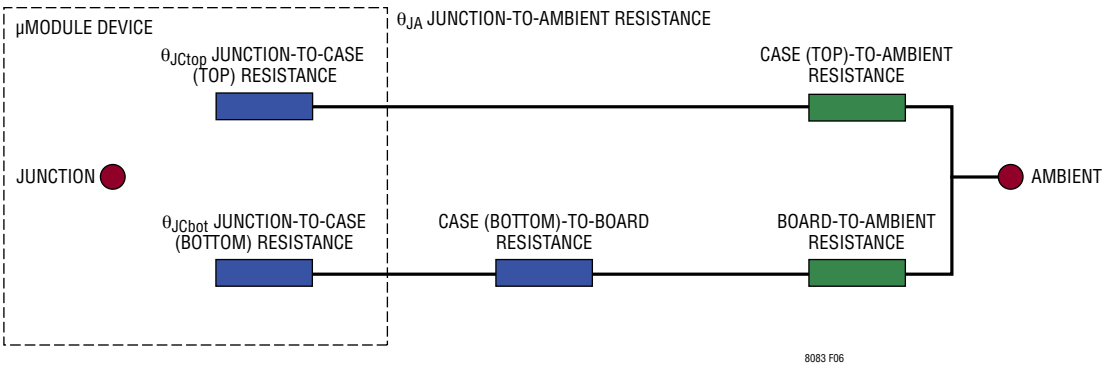


Figure 6. Graphical Approximation of the Thermal Coefficients, Including JESD 51-12 Terms

APPLICATIONS INFORMATION

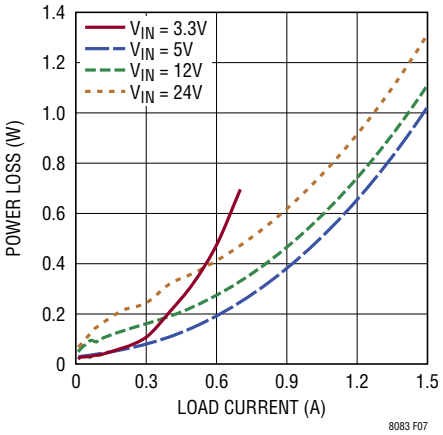


Figure 7. Power Loss at $3.3V_{OUT}$

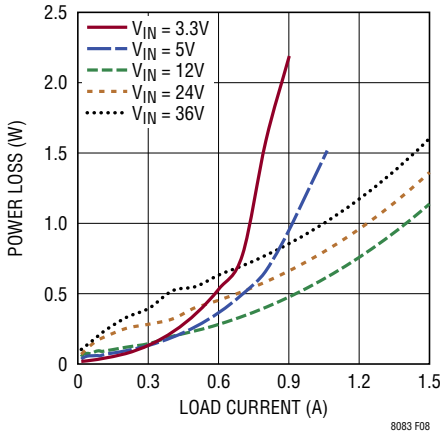


Figure 8. Power Loss at $5V_{OUT}$

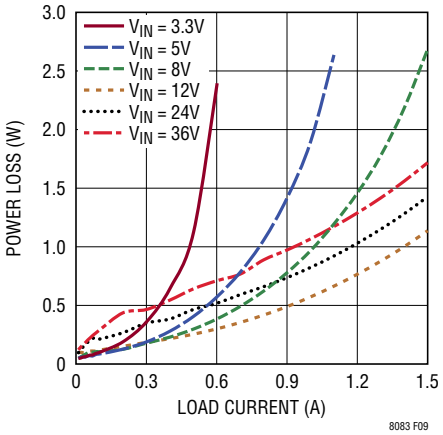


Figure 9. Power Loss at $8V_{OUT}$

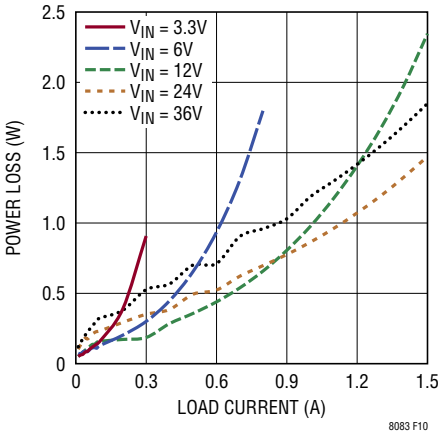


Figure 10. Power Loss at $12V_{OUT}$

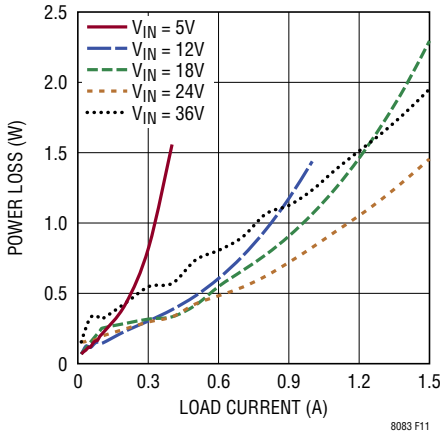


Figure 11. Power Loss at $18V_{OUT}$

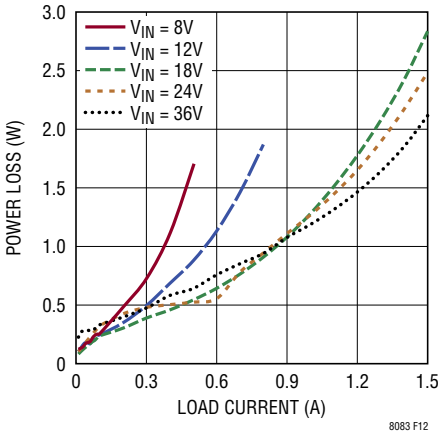


Figure 12. Power Loss at $24V_{OUT}$

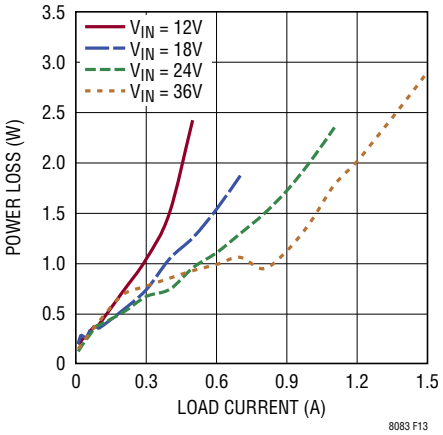


Figure 13. Power Loss at $36V_{OUT}$

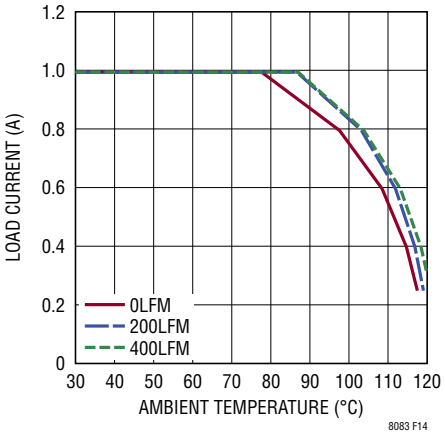


Figure 14. 5V to 5V Derating Curve, No Heat Sink

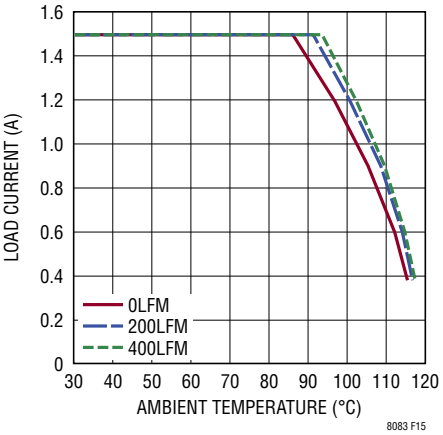


Figure 15. 12V to 5V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

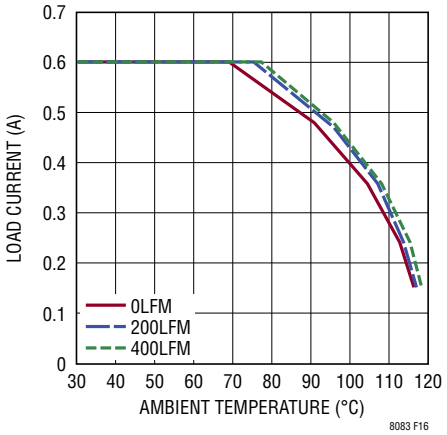


Figure 16. 5V to 12V Derating Curve, No Heat Sink

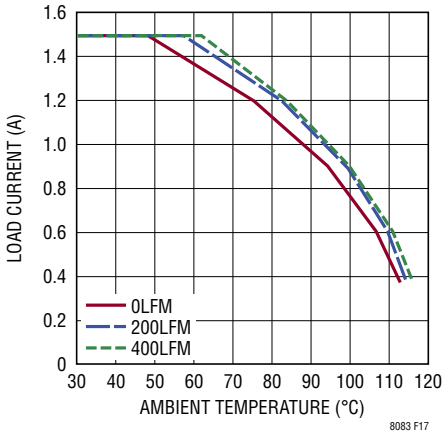


Figure 17. 12V to 12V Derating Curve, No Heat Sink

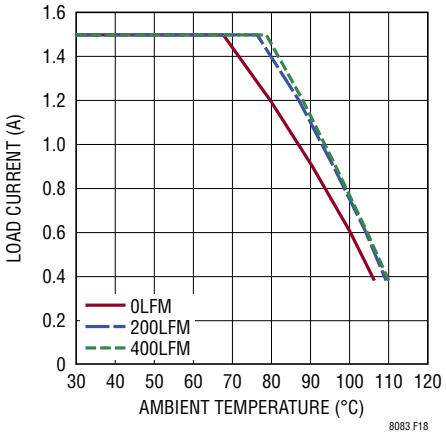


Figure 18. 36V to 12V Derating Curve, No Heat Sink

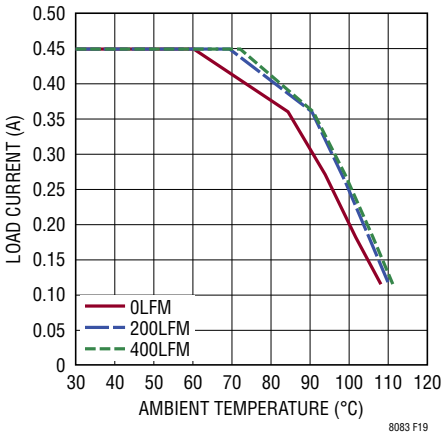


Figure 19. 12V to 36V Derating Curve, No Heat Sink

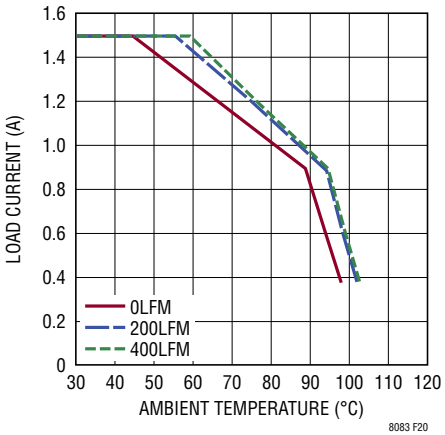


Figure 20. 36V to 36V Derating Curve, No Heat Sink

Table 3. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 14 and 15	5, 12	Figure 8	0	None	23
Figures 14 and 15	5, 12	Figure 8	200	None	18
Figures 14 and 15	5, 12	Figure 8	400	None	16

Table 4. 12V Output

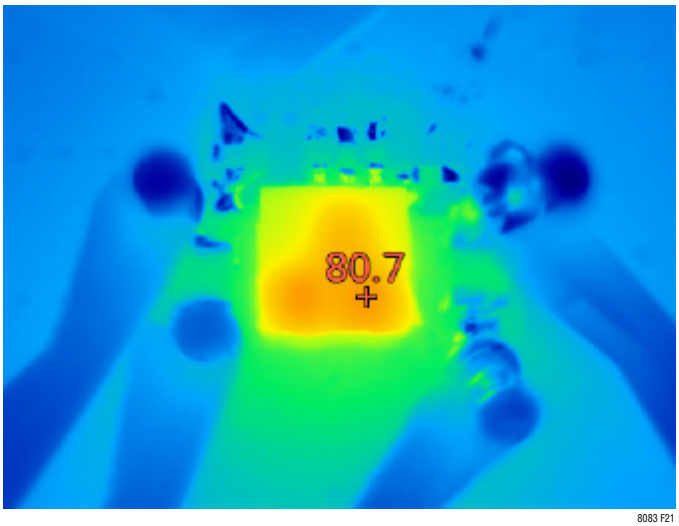
DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 16, 17 and 18	5, 12, 36	Figure 10	0	None	23
Figures 16, 17 and 18	5, 12, 36	Figure 10	200	None	18
Figures 16, 17 and 18	5, 12, 36	Figure 10	400	None	16

APPLICATIONS INFORMATION

Table 5. 36V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 19 and 20	12, 36	Figure 13	0	None	23
Figures 19 and 20	12, 36	Figure 13	200	None	18
Figures 19 and 20	12, 36	Figure 13	400	None	16

The 3.3V, 5V, 8V, 12V, 18V, 24V and 36V power loss curves in Figure 7 to Figure 13 can be used in coordination with the load current derating curves in Figure 14 to Figure 20 for calculating an approximate θ_{JA} thermal resistance for the LTM8083 with various airflow conditions. The power loss curves are taken at room temperature, and are increased with a multiplicative factor according to the ambient temperature. This approximate factor is: 1.2 for 120°C at junction temperature. Maximum load current is achievable while increasing ambient temperature as long as the junction temperature is less than 120°C, which is a 5°C guard band from maximum junction temperature of 125°C. When the ambient temperature reaches a point where the junction temperature is 120°C, then the load current is lowered to maintain the junction at 120°C while increasing ambient temperature up to 120°C. The derating curves are plotted with the output current starting at 1.5A and the ambient temperature at 30°C. The output voltages are 5V, 12V, and 36V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 18 the load current is derated to 0.6A at ~100°C with no air flow or heat sink and the power loss for the 36V to 12V at 0.6A output is about 0.84W. The 0.84W loss is calculated with the 0.7W room temperature loss from the 36V to 12V power loss curve at 0.6A, and the 1.2 multiplying factor at 120°C junction temperature. If the 100°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 20°C divided by 0.84W equals a 23.8°C/W θ_{JA} thermal resistance. Table 4 specifies a 23°C/W value which is very close. Table 3, Table 4, Table 5, provide equivalent thermal resistances for 5V, 12V, and 36V outputs with and without airflow and heat sinking. The derived thermal resistances in Table 3, Table 4 and Table 5, for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick 4-layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 64mm × 64mm. A Typical thermal image based on this PCB is shown in Figure 21.



8083 F21

Figure 21. Thermal Image of LTM8083 Running from 24V Input and 36V Output with 1A Load at 25°C Ambient without Airflow or Heat Sink

APPLICATIONS INFORMATION

PC Board Layout Checklist/Examples

The high integration of LTM8083 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- The ground plane layer should not have any traces.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of module. Connect the copper areas to GND
- Keep separation between SYNC and RT pin traces to minimize noise due to crosstalk between these signals.
- Route ISP and ISN traces together with minimum PCB trace spacing. Avoid sense lines passing through noisy areas, such as switch nodes. Ensure accurate current sensing with Kelvin connections at the current sense resistor.
- Connect the optional V_C pin compensation capacitor close to the module, between V_C and the signal ground. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.

  Figure 22 gives a good example of the recommended layout.

Table 6. Output Voltage Response vs Component Matrix (Refer to Figure 23)

C_{OUT}					PART NUMBER		VALUE	
MURATA					GCM32EC71H106KA03		10µF, 50V, 1210, X7S	
V_{IN} (V)	V_{OUT} (V)	f_{SW} (MHz)	C_{OUT} (CER CAP)	COMPENSATION	LOAD STEP (A)	LOAD STEP RISING AND FALLING TIME (µs)	PK-PK DEVIATION (mV)	RECOVERY TIME (µs)
3.3	5	1, See Note	10µF	Internal	0 – 0.375	1	640	150
5	5	1	10µF	Internal	0 – 0.375	1	280	75
12	5	1	10µF	Internal	0 – 0.375	1	150	100
36	5	1	10µF	Internal	0 – 0.375	1	320	150
6	12	1	10µF	Internal	0 – 0.375	1	440	170
12	12	1	10µF	Internal	0 – 0.375	1	440	230
24	12	1	10µF	Internal	0 – 0.375	1	350	200
36	12	1	10µF	Internal	0 – 0.375	1	340	200
18	36	1	10µF	Internal	0 – 0.375	1	1600	200
36	36	1	10µF	Internal	0 – 0.375	1	2000	220

Note: Use 40.2kΩ R_T resistor to set switching frequency at 1MHz.

APPLICATIONS INFORMATION

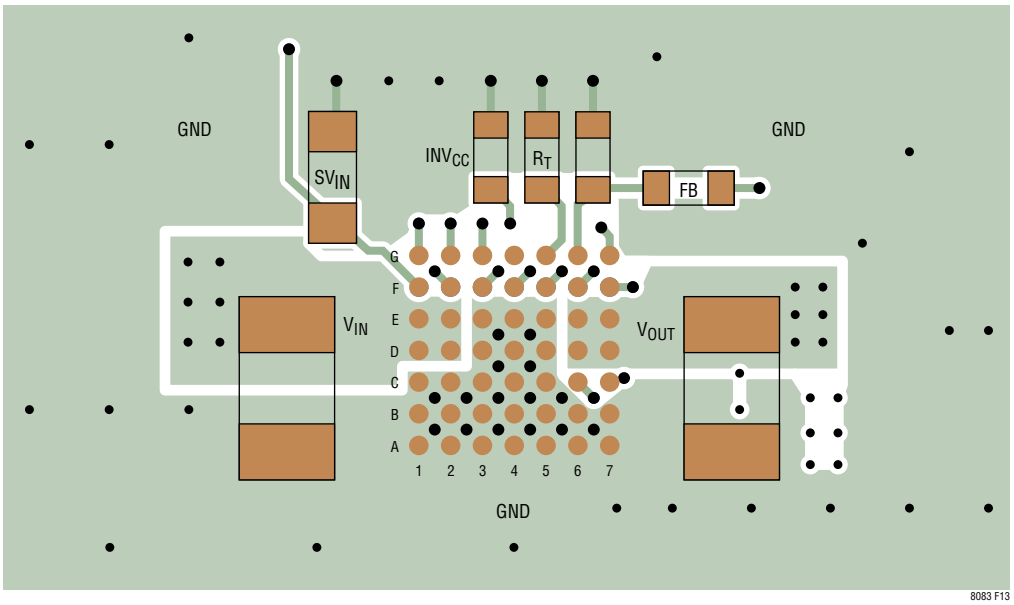


Figure 22. Recommended PCB Layout

TYPICAL APPLICATIONS

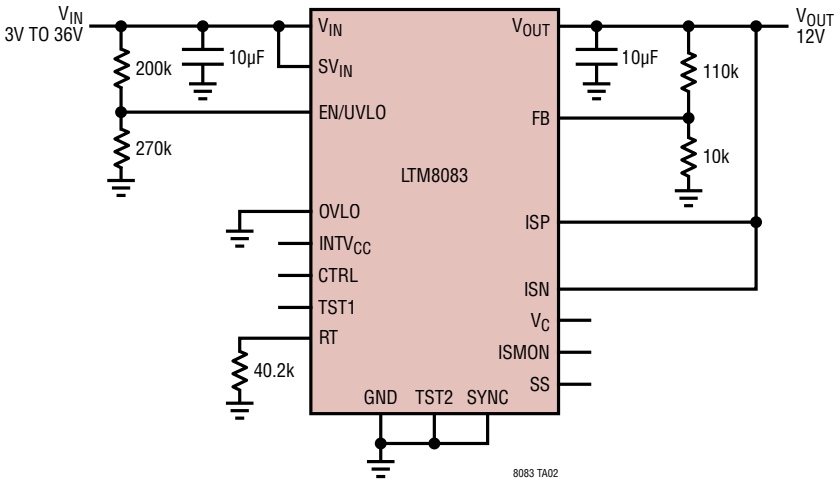


Figure 23. 18W (12V, 1.5A) 1MHz Buck-Boost Voltage Regulator

TYPICAL APPLICATIONS

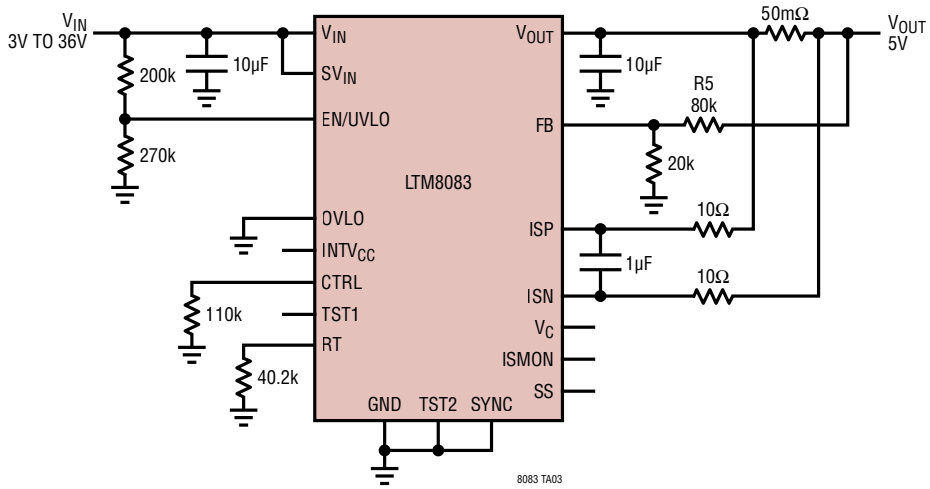


Figure 24. 7.5W (5V, 1.5A) 1MHz Buck-Boost Voltage Regulator with Output Current Monitor

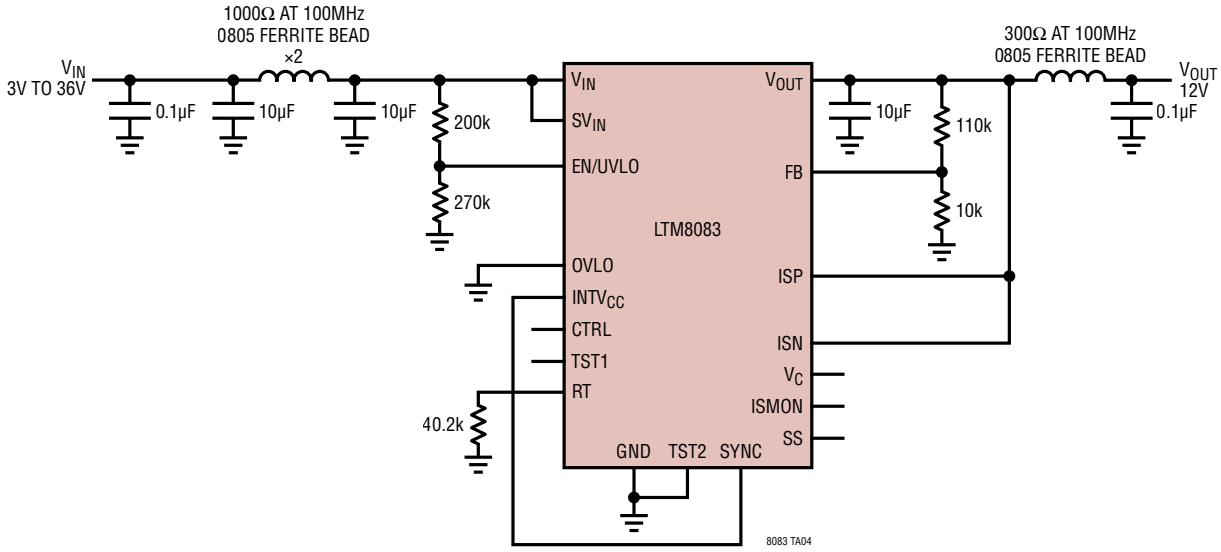


Figure 25. 18W (12V, 1.5A) 1MHz Buck-Boost Voltage Regulator Compliant with CISPR25 Class 5 Limits

PACKAGE DESCRIPTION

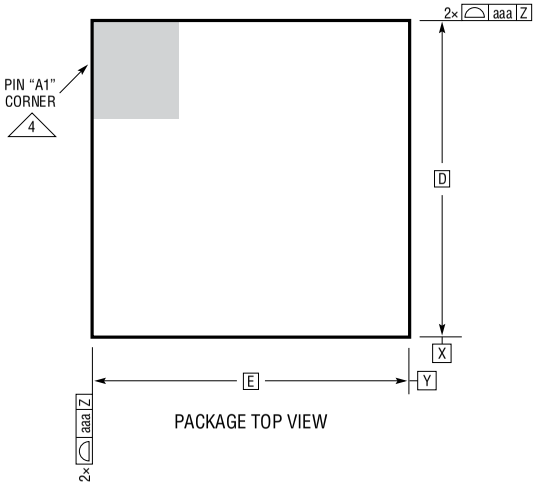
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

LTM8083 Component BGA Pinout

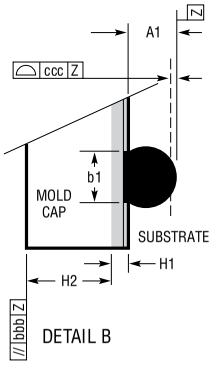
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	A2	GND	A3	GND	A4	V_{IN}	A5	V_{IN}	A6	SV_{IN}	A7	TST2
B1	GND	B2	GND	B3	GND	B4	V_{IN}	B5	V_{IN}	B6	EN/UVLO	B7	OVLO
C1	GND	C2	GND	C3	GND	C4	GND	C5	GND	C6	$INTV_{CC}$	C7	CTRL
D1	GND	D2	GND	D3	GND	D4	GND	D5	GND	D6	ISMON	D7	GND
E1	GND	E2	GND	E3	GND	E4	GND	E5	GND	E6	V_C	E7	RT
F1	GND	F2	GND	F3	ISN	F4	V_{OUT}	F5	V_{OUT}	F6	SS	F7	FB
G1	GND	G2	GND	G3	ISP	G4	V_{OUT}	G5	V_{OUT}	G6	SYNC	G7	TST1

PACKAGE DESCRIPTION

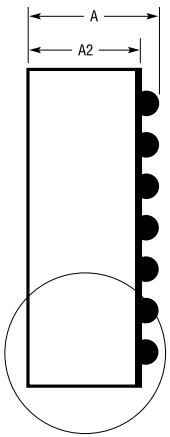
BGA Package
49-Lead (6.25mm × 6.25mm × 2.22mm)
(Reference LTC DWG# 05-08-1518 Rev B)



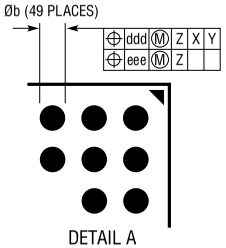
PACKAGE TOP VIEW



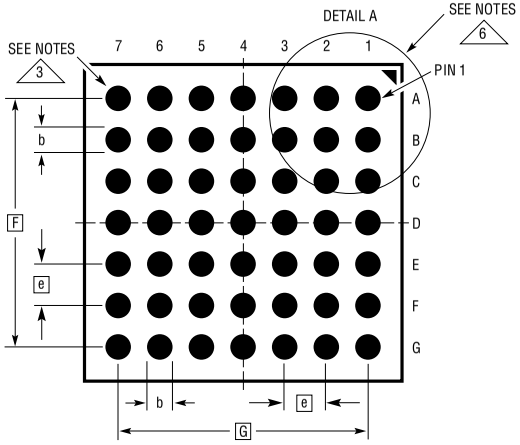
DETAIL B



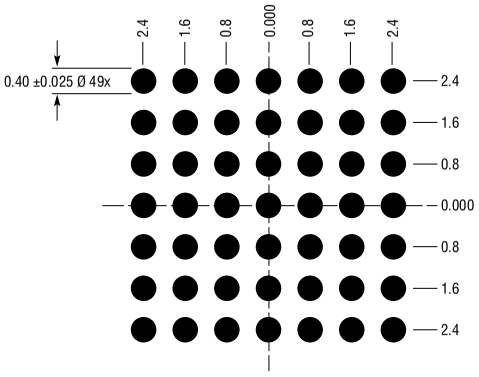
DETAIL B
PACKAGE SIDE VIEW



DETAIL A



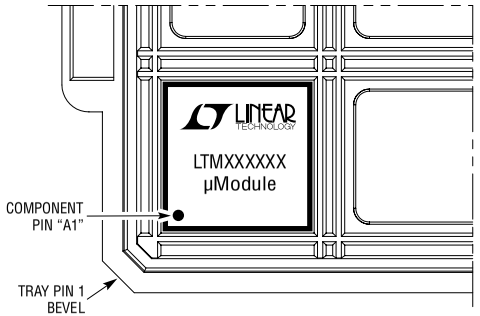
PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

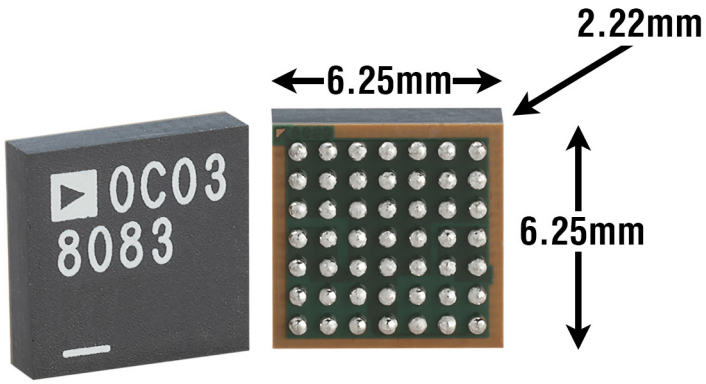
DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	2.02	2.22	2.42	
A1	0.30	0.40	0.50	BALL HT
A2	1.72	1.82	1.92	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		6.25		
E		6.25		
e		0.80		
F		4.80		
G		4.80		
H1		0.32 REF		SUBSTRATE THK
H2		1.50 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 49				



PACKAGE IN TRAY LOADING ORIENTATION

BGA 49 0418 REV B

PACKAGE PHOTO



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8054	$36V_{IN}$, $36V_{OUT}$, 5.4A Buck-Boost µModule Regulator	$5V \le V_{IN} \le 36V$, $1.2V \le V_{OUT} \le 36V$, 11.25mm × 15mm × 3.42mm BGA
LTM8055	$36V_{IN}$, $36V_{OUT}$, 8.5A Buck-Boost µModule Regulator	$5V \le V_{IN} \le 36V$, $1.2V \le V_{OUT} \le 36V$, 15mm × 15mm × 4.92mm BGA
LTM8056	$58V_{IN}$, $48V_{OUT}$, 5.5A Buck-Boost µModule Regulator	$5V \le V_{IN} \le 58V$, $1.2V \le V_{OUT} \le 48V$, 15mm × 15mm × 4.92mm BGA
LTM8045	Single, Inverting or SEPIC µModule DC/DC Convertor	$2.8V \le V_{IN} \le 18V$. $\pm 2.5V \le V_{OUT} \le \pm 15V$, 6.25mm × 11.25mm × 4.92mm BGA
LTM8049	Dual Outputs, SEPIC and/or Inverting µModule Regulator	$2.6V \le V_{IN} \le 20V$. $\pm 2.5V \le V_{OUT} \le \pm 25V$, 9mm × 15mm × 2.42mm BGA