

# 74LVC2G74

Single D-type flip-flop with set and reset;  
positive edge trigger

Rev. 14 — 27 August 2021

Product data sheet

## 1. General description

The 74LVC2G74 is a single positive edge triggered D-type flip-flop with individual data (D), clock (CP), set ( $\overline{SD}$ ) and reset ( $\overline{RD}$ ) inputs, and complementary Q and  $\overline{Q}$  outputs. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2G74DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G74DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G74GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC2G74GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74LVC2G74GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

### 4. Marking

Table 2. Marking codes

Type number	Marking code [1]
74LVC2G74DP	V74
74LVC2G74DC	V74
74LVC2G74GT	V74
74LVC2G74GN	Y4
74LVC2G74GS	Y4

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram

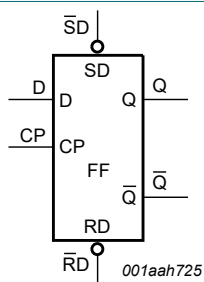


Fig. 1. Logic symbol

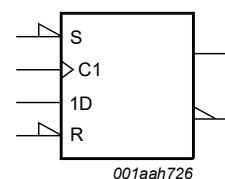


Fig. 2. IEC logic symbol

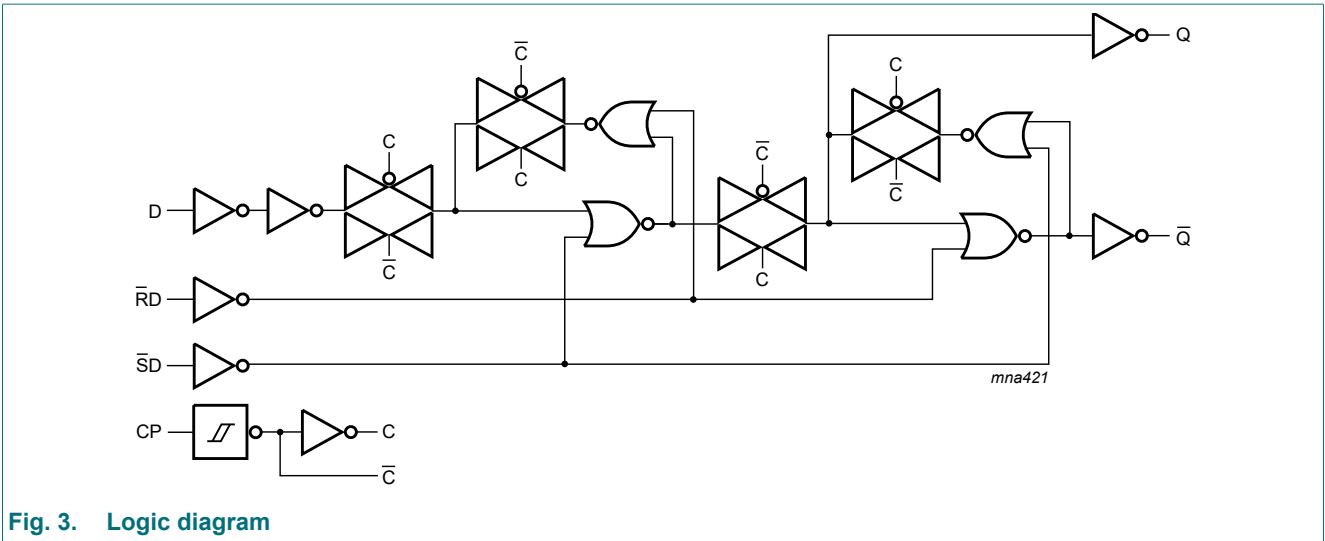


Fig. 3. Logic diagram

## 6. Pinning information

### 6.1. Pinning

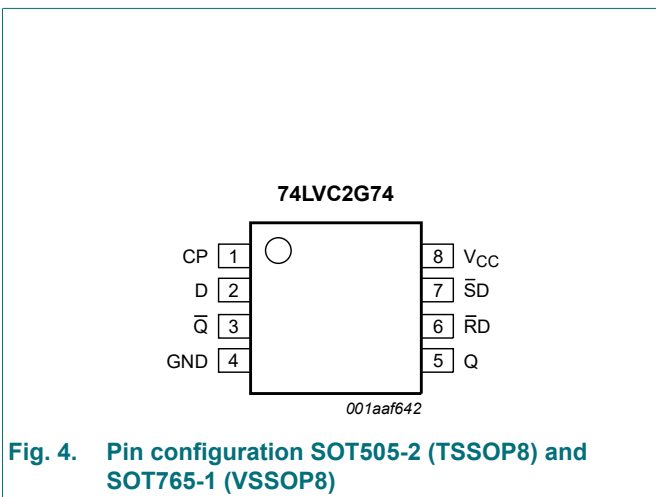


Fig. 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

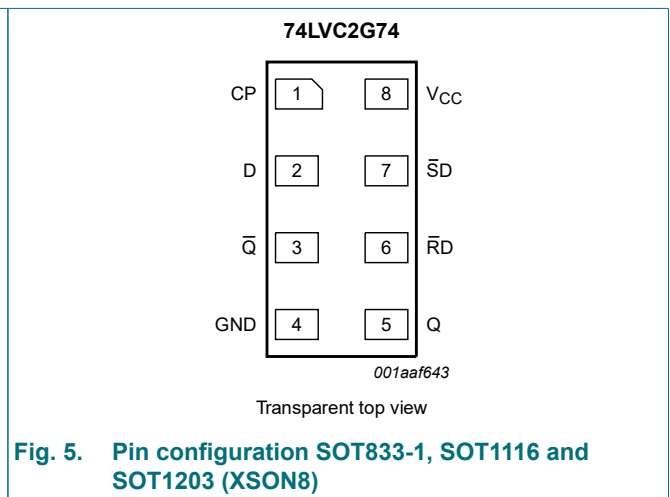


Fig. 5. Pin configuration SOT833-1, SOT1116 and SOT1203 (XSON8)

### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
D	2	data input
$\bar{Q}$	3	complement output
GND	4	ground (0 V)
Q	5	true output
$\bar{R}D$	6	asynchronous reset-direct input (active LOW)
$\bar{S}D$	7	asynchronous set-direct input (active LOW)
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

**Table 4. Function table for asynchronous operation**

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Output	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

**Table 5. Function table for synchronous operation**

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH CP transition;  
 $Q_{n+1}$  = state after the next LOW-to-HIGH CP transition.

Input				Output	
SD	RD	CP	D	$Q_{n+1}$	$\bar{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

## 8. Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	Active mode	[1] -0.5	$V_{CC} + 0.5$	V
		Power-down mode; $V_{CC} = 0$ V	[1] -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to $+125$ °C	[2] -	250	mW
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) package:  $P_{tot}$  derates linearly with 4.6 mW/K above 96 °C.  
 For SOT765-1 (VSSOP8) package:  $P_{tot}$  derates linearly with 4.9 mW/K above 99 °C.  
 For SOT833-1 (XSON8) package:  $P_{tot}$  derates linearly with 3.1 mW/K above 68 °C.  
 For SOT1116 (XSON8) package:  $P_{tot}$  derates linearly with 4.2 mW/K above 90 °C.  
 For SOT1203 (XSON8) package:  $P_{tot}$  derates linearly with 3.6 mW/K above 81 °C.

## 9. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	Active mode	0	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	10	ns/V

## 10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65V_{CC}$	-	-	$0.65V_{CC}$	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = -100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	$V_{CC} - 0.1$	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	1.2	1.54	-	0.95	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.9	2.15	-	1.7	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	2.50	-	1.9	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.3	2.62	-	2.0	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.10	-	0.10	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	0.07	0.45	-	0.70	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	0.12	0.30	-	0.45	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.17	0.40	-	0.60	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	0.33	0.55	-	0.80	V
		$I_O = 32$ mA; $V_{CC} = 4.5$ V	-	0.39	0.55	-	0.80	V

## Single D-type flip-flop with set and reset; positive edge trigger

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	$\pm 0.1$	$\pm 1$	-	$\pm 1$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5 \text{ V}$ ; $V_{CC} = 0 \text{ V}$	-	$\pm 0.1$	$\pm 2$	-	$\pm 2$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V}$ to 5.5 V; $I_O = 0 \text{ A}$	-	0.1	4	-	4	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0 \text{ A}$ ; $V_{CC} = 2.3 \text{ V}$ to 5.5 V	-	5	500	-	500	$\mu\text{A}$
$C_I$	input capacitance		-	4.0	-	-	-	pF

[1] All typical values are measured at  $T_{amb} = 25 \text{ °C}$ .

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{pd}$	propagation delay	CP to Q, $\bar{Q}$ ; see Fig. 6 [2]						
		$V_{CC} = 1.65 \text{ V}$ to 1.95 V	1.5	6.0	13.4	1.5	13.4	ns
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	1.0	3.5	7.1	1.0	7.1	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.5	7.1	1.0	7.1	ns
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	1.0	3.5	5.9	1.0	5.9	ns
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	1.0	2.5	4.1	1.0	4.1	ns
		$\bar{S}D$ to Q, $\bar{Q}$ ; see Fig. 7 [2]						
		$V_{CC} = 1.65 \text{ V}$ to 1.95 V	1.5	6.0	12.9	1.5	12.9	ns
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	1.0	3.0	5.9	1.0	5.9	ns
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	1.0	2.5	4.1	1.0	4.1	ns
		$\bar{R}D$ to Q, $\bar{Q}$ ; see Fig. 7 [2]						
		$V_{CC} = 1.65 \text{ V}$ to 1.95 V	1.5	5.0	12.9	1.5	12.9	ns
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	1.0	3.5	7.0	1.0	7.0	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.5	7.0	1.0	7.0	ns
$V_{CC} = 3.0 \text{ V}$ to 3.6 V	1.0	3.0	5.9	1.0	5.9	ns		
$V_{CC} = 4.5 \text{ V}$ to 5.5 V	1.0	2.5	4.1	1.0	4.1	ns		

## Single D-type flip-flop with set and reset; positive edge trigger

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t <sub>w</sub>	pulse width	CP HIGH or LOW; see Fig. 6						
		V <sub>CC</sub> = 1.65 V to 1.95 V	6.2	-	-	6.2	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.7	-	-	2.7	-	ns
		V <sub>CC</sub> = 2.7 V	2.7	-	-	2.7	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.7	1.3	-	2.7	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	ns
		SD and RD LOW; see Fig. 7						
		V <sub>CC</sub> = 1.65 V to 1.95 V	6.2	-	-	6.2	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.7	-	-	2.7	-	ns
		V <sub>CC</sub> = 2.7 V	2.7	-	-	2.7	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.7	1.6	-	2.7	-	ns
V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	ns		
t <sub>rec</sub>	recovery time	SD or RD; see Fig. 7						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.9	-	-	1.9	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.4	-	-	1.4	-	ns
		V <sub>CC</sub> = 2.7 V	1.3	-	-	1.3	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	+1.2	-3.0	-	+1.2	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns
t <sub>su</sub>	set-up time	D to CP; see Fig. 6						
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.9	-	-	2.9	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	ns
		V <sub>CC</sub> = 2.7 V	1.7	-	-	1.7	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.3	0.5	-	1.3	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.1	-	-	1.1	-	ns
t <sub>h</sub>	hold time	D to CP; see Fig. 6						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	-	-	1.5	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	-	-	1.0	-	ns
		V <sub>CC</sub> = 2.7 V	1.0	-	-	1.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	0.6	-	1.0	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns
f <sub>max</sub>	maximum frequency	CP; see Fig. 6						
		V <sub>CC</sub> = 1.65 V to 1.95 V	80	-	-	80	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	175	-	-	175	-	MHz
		V <sub>CC</sub> = 2.7 V	175	-	-	175	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	175	280	-	175	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V	200	-	-	200	-	MHz
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V [3]	-	15	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

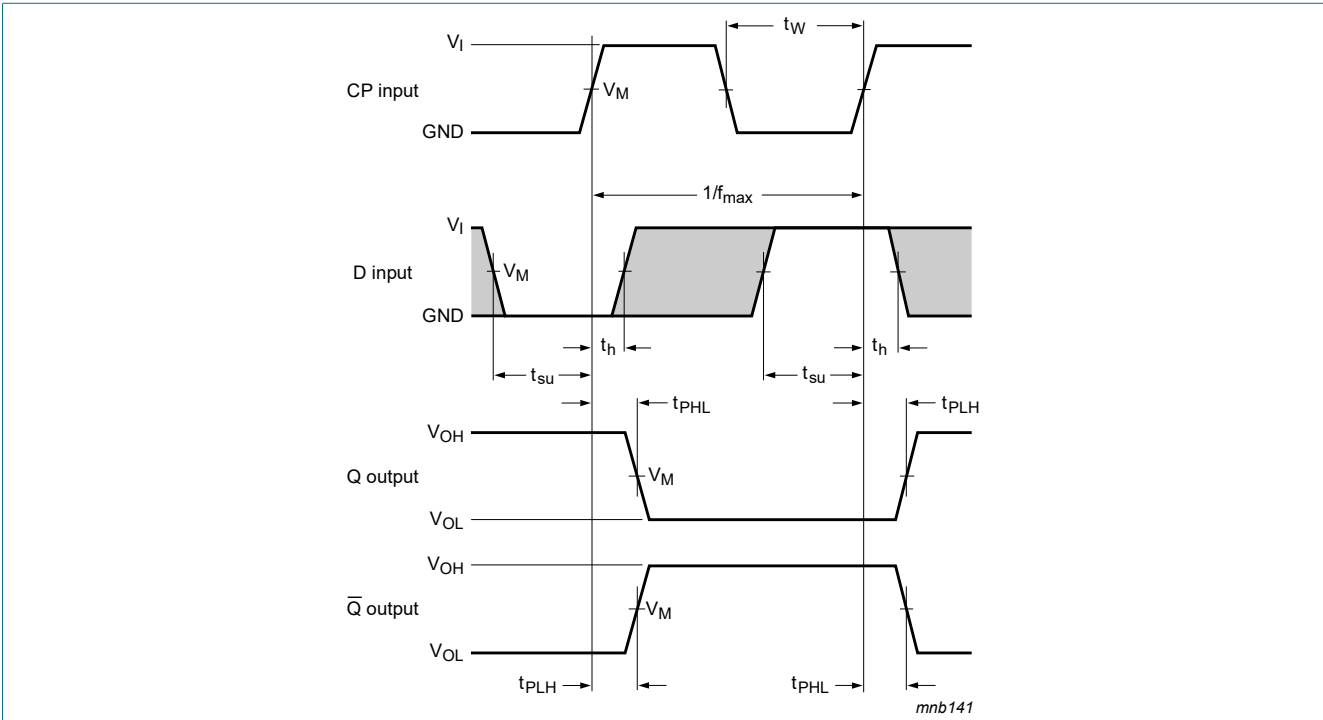
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF; V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;  $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

11.1. Waveforms and test circuit



Measurement points are given in [Table 10](#).

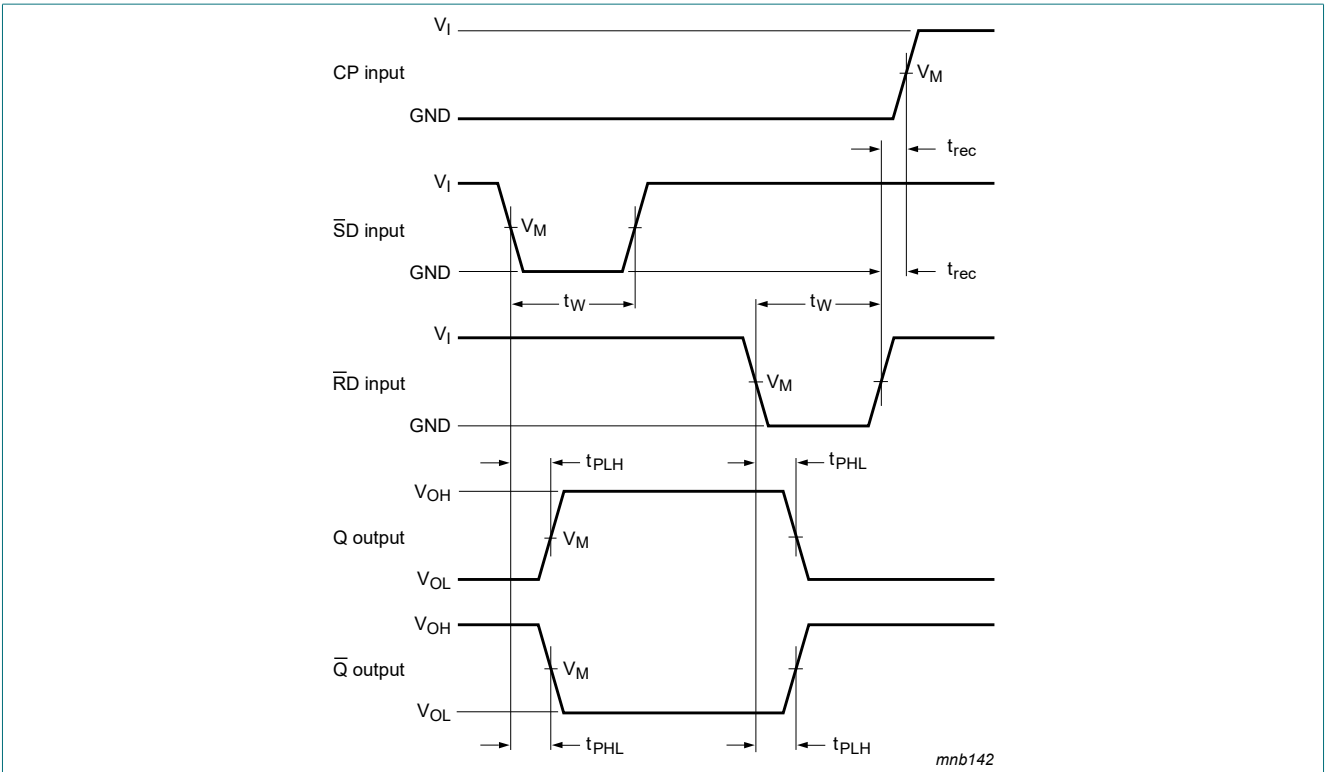
The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 6.** The clock input (CP) to output (Q,  $\bar{Q}$ ) propagation delays, the clock pulse width, the D to CP set-up time, the CP to D hold time and the CP maximum frequency



Single D-type flip-flop with set and reset; positive edge trigger



Measurement points are given in [Table 10](#).

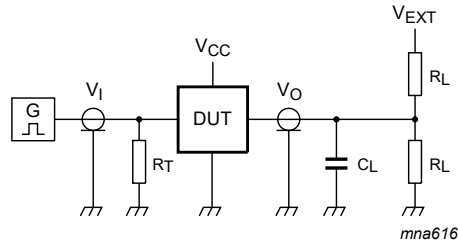
V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load.

**Fig. 7. The set ( $\overline{SD}$ ) and reset ( $\overline{RD}$ ) input to output (Q,  $\overline{Q}$ ) propagation delays, the set and reset pulse widths and the  $\overline{RD}$  to CP recovery time**

**Table 10. Measurement points**

Supply voltage	Input	Output
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>
1.65 V to 1.95 V	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>

## Single D-type flip-flop with set and reset; positive edge trigger



Test data is given in [Table 11](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 8. Test circuit for measuring switching times**

**Table 11. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open	GND	$2V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	GND	$2V_{CC}$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	6 V
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	6 V
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	$2V_{CC}$

## 12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

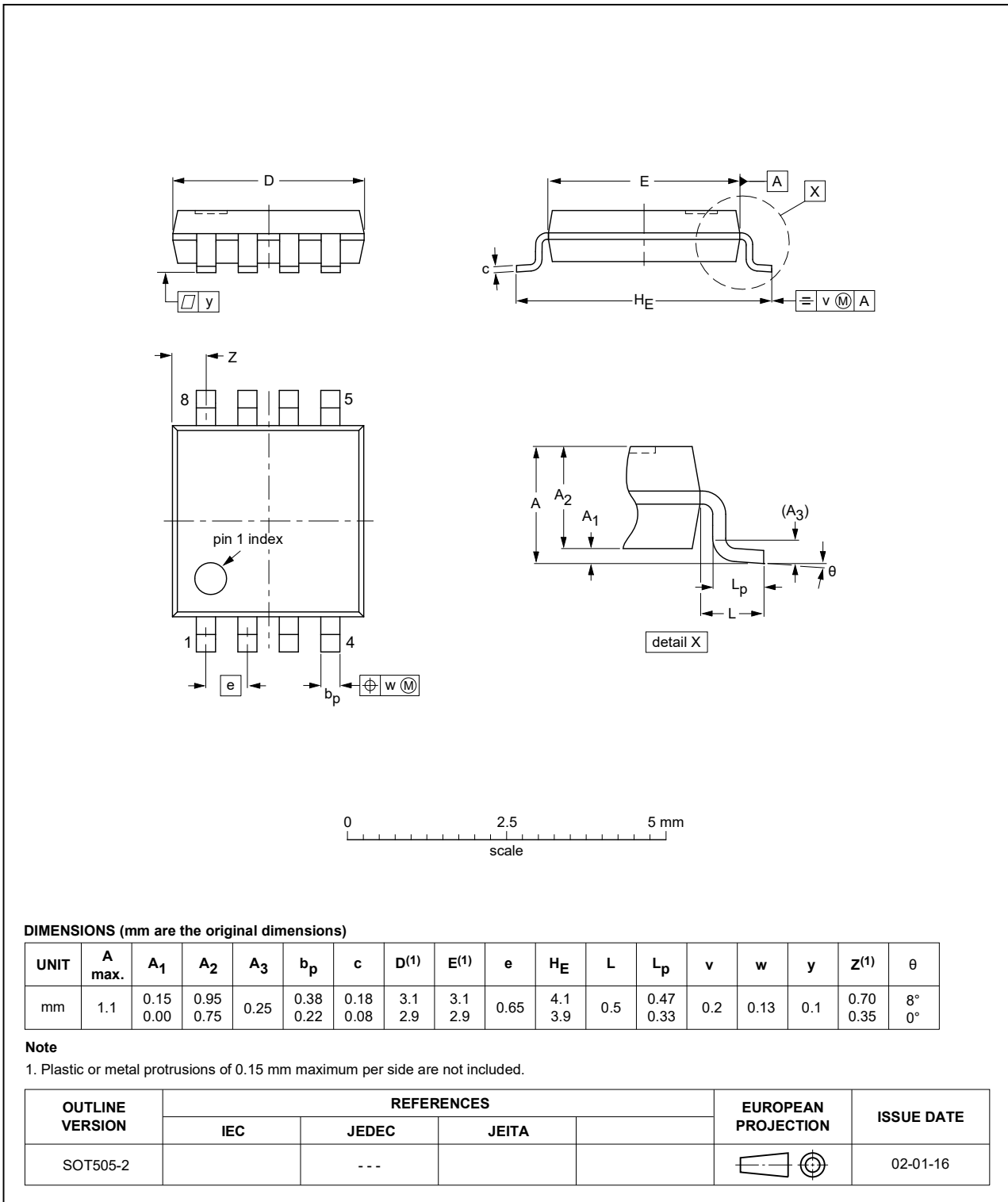


Fig. 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

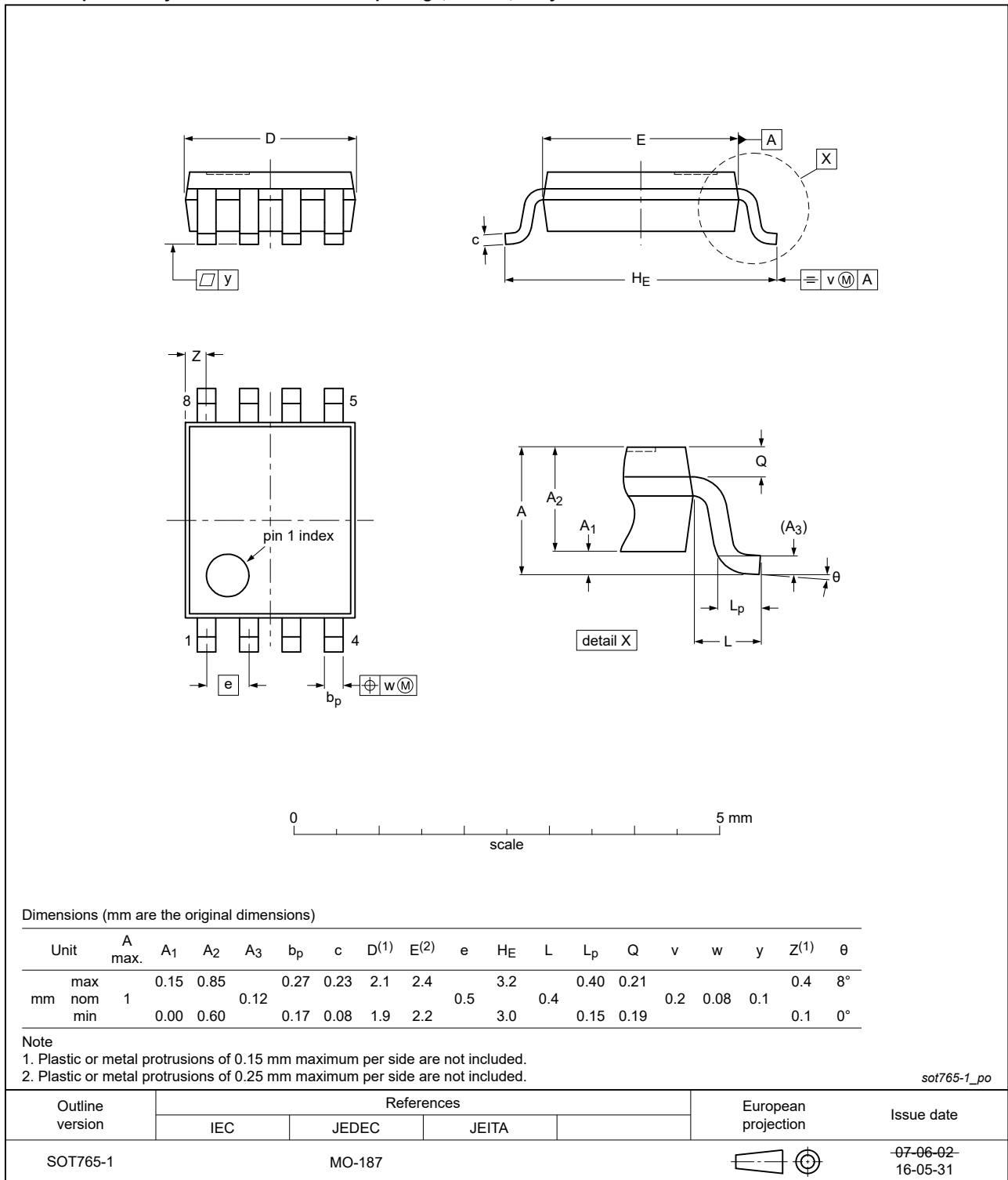


Fig. 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

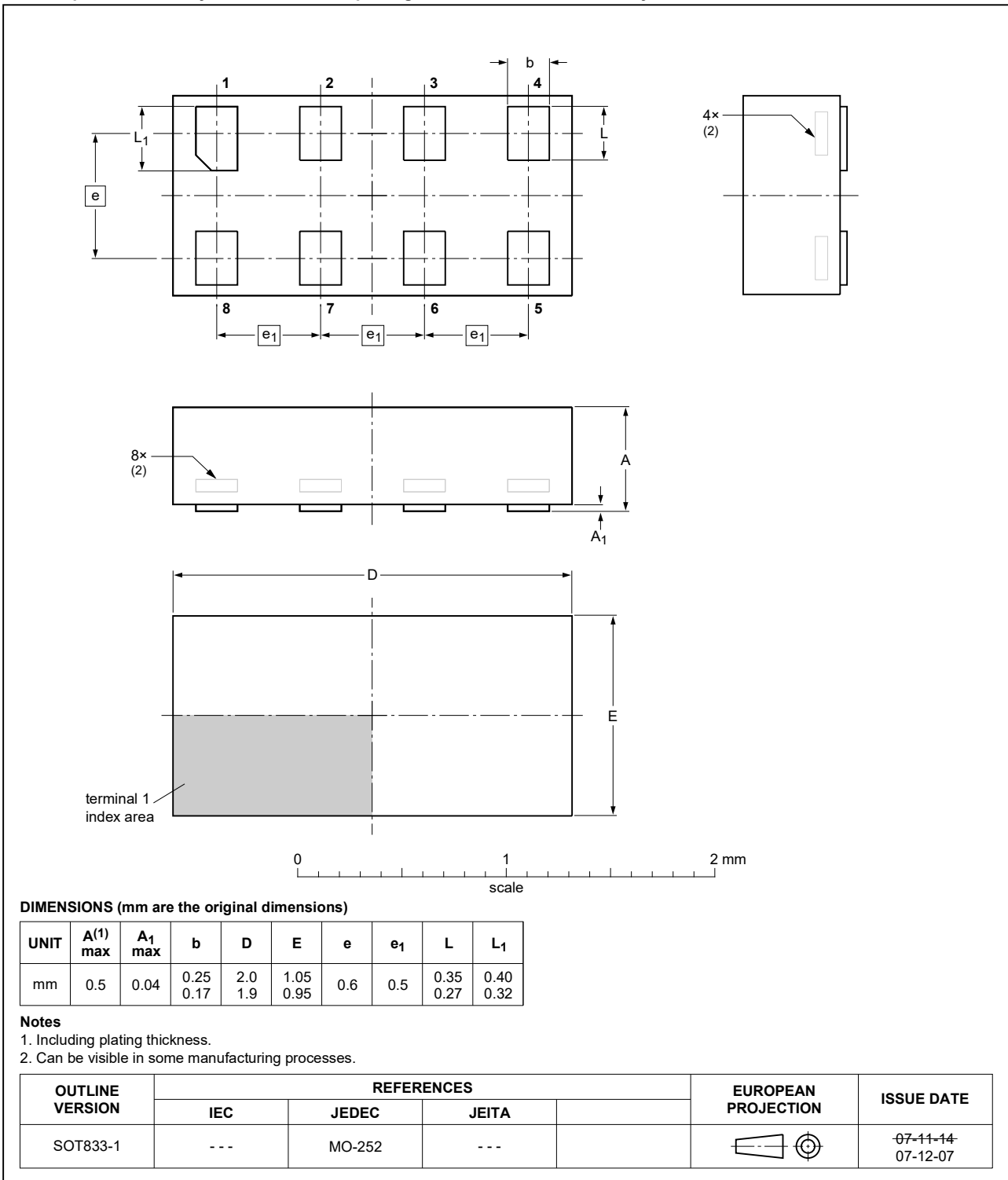


Fig. 11. Package outline SOT833-1 (XSON8)

Single D-type flip-flop with set and reset; positive edge trigger

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116

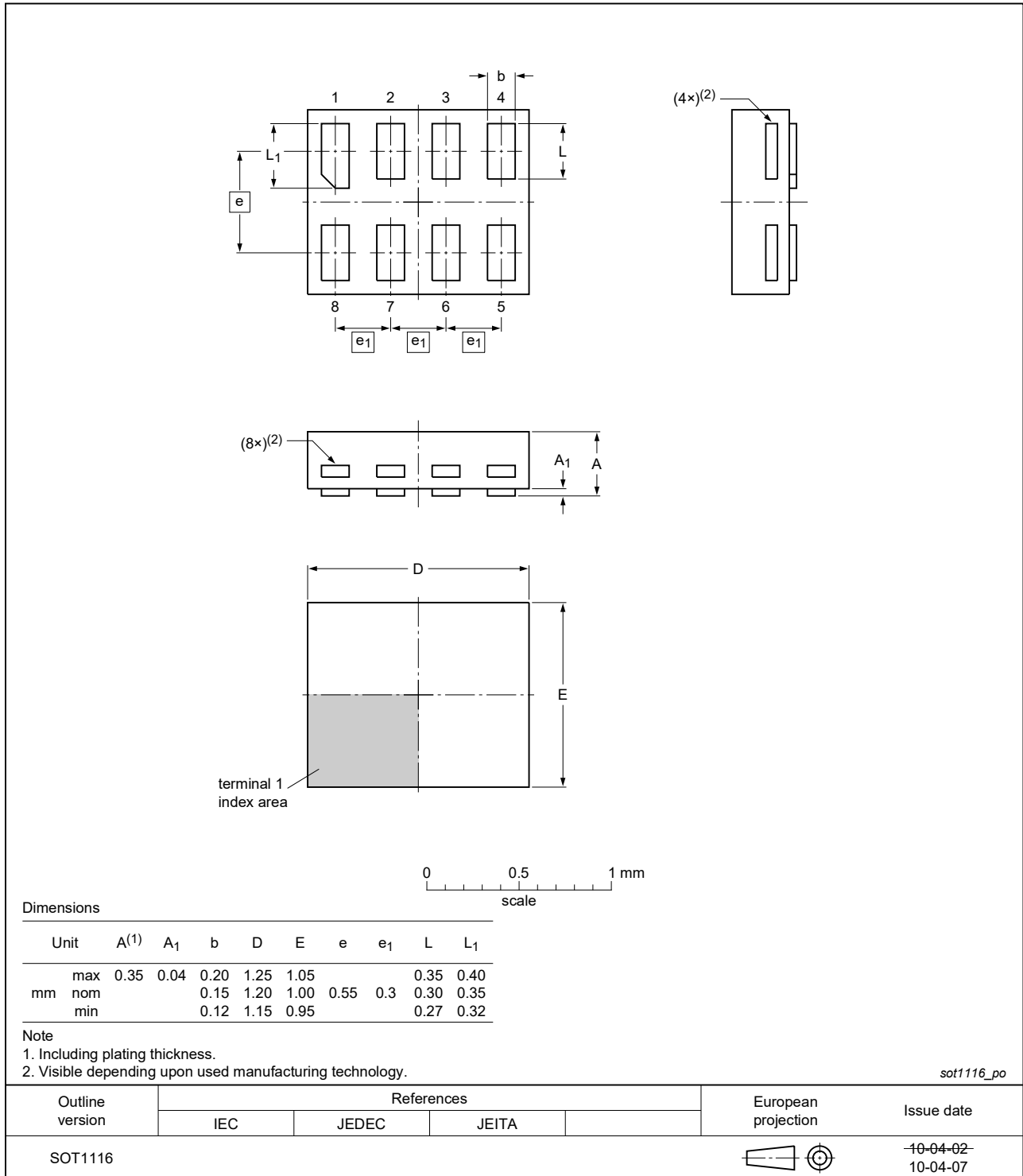


Fig. 12. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203

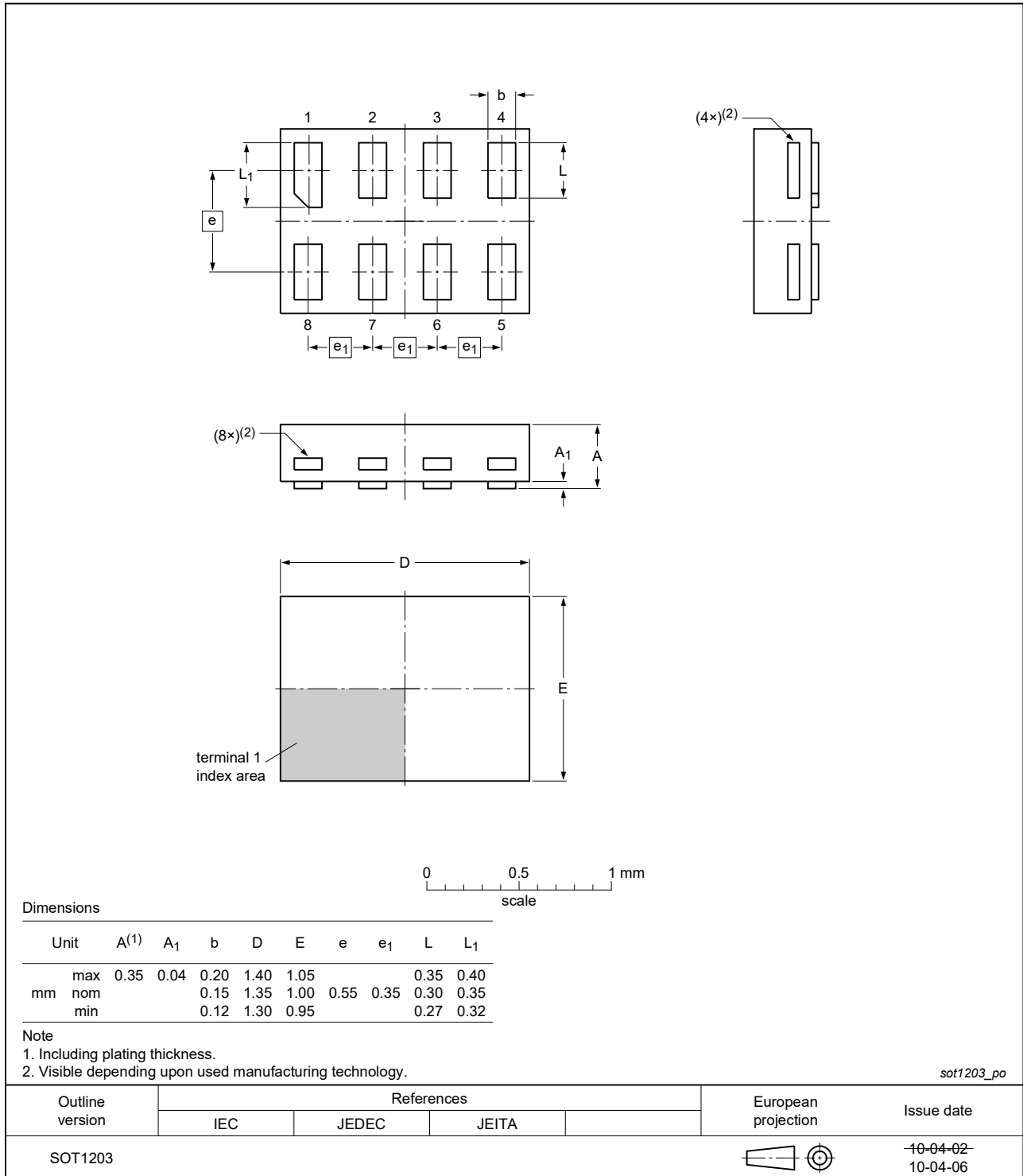


Fig. 13. Package outline SOT1203 (XSON8)

## 13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G74 v.14	20210827	Product data sheet	-	74LVC2G74 v.13
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVC2G74GM (SOT902-2/XQFN8) removed.</li> </ul>			
74LVC2G74 v.13	20210421	Product data sheet	-	74LVC2G74 v.12
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVC2G74GF (SOT1089 / XSON8) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Section 8</a>: P<sub>tot</sub> total power dissipation and it's derating values updated.</li> </ul>			
74LVC2G74 v.12	20181003	Product data sheet	-	74LVC2G74 v.11
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74LVC2G74GD (SOT996-2) removed.</li> </ul>			
74LVC2G74 v.11	20161215	Product data sheet	-	74LVC2G74 v.10
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 8</a>: The maximum limits for leakage current and supply current have changed.</li> </ul>			
74LVC2G74 v.10	20130402	Product data sheet	-	74LVC2G74 v.9
Modifications:	<ul style="list-style-type: none"> <li>For type number 74LVC2G74GD XSON8U has changed to XSON8.</li> </ul>			
74LVC2G74 v.9	20120522	Product data sheet	-	74LVC2G74 v.8
Modifications:	<ul style="list-style-type: none"> <li>For type number 74LVC2G74GM the sot code has changed to SOT902-2.</li> </ul>			
74LVC2G74 v.8	20111128	Product data sheet	-	74LVC2G74 v.7
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74LVC2G74 v.7	20101011	Product data sheet	-	74LVC2G74 v.6
74LVC2G74 v.6	20091223	Product data sheet	-	74LVC2G74 v.5
74LVC2G74 v.5	20080630	Product data sheet	-	74LVC2G74 v.4
74LVC2G74 v.4	20080207	Product data sheet	-	74LVC2G74 v.3
74LVC2G74 v.3	20070809	Product data sheet	-	74LVC2G74 v.2
74LVC2G74 v.2	20061214	Product data sheet	-	74LVC2G74 v.1
74LVC2G74 v.1	20051103	Product data sheet	-	-



## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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