

---

---

## 4 Mbit SPI Serial Flash

---

---

### Features

- Single Voltage Read and Write Operations
  - 2.7-3.6V
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- High Speed Clock Frequency
  - Up to 50 MHz
- Superior Reliability
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- Low Power Consumption:
  - Active Read Current: 10 mA (typical)
  - Standby Current: 5  $\mu$ A (typical)
- Flexible Erase Capability
  - Uniform 4 KByte sectors
  - Uniform 32 KByte overlay blocks
  - Uniform 64 KByte overlay blocks
- Fast Erase and Byte-Program:
  - Chip-Erase Time: 35 ms (typical)
  - Sector-/Block-Erase Time: 18 ms (typical)
  - Byte-Program Time: 7  $\mu$ s (typical)
- Auto Address Increment (AAI) Programming
  - Decrease total chip programming time over Byte-Program operations
- End-of-Write Detection
  - Software polling the BUSY bit in Status Register
  - Busy Status readout on SO pin in AAI Mode
- Hold Pin (HOLD#)
  - Suspends a serial sequence to the memory without deselecting the device
- Write Protection (WP#)
  - Enables/Disables the Lock-Down function of the status register
- Software Write Protection
  - Write protection through Block-Protection bits in status register
- Temperature Range
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
- Packages Available
  - 8-lead SOIC (200 mils)
  - 8-lead SOIC (150 mils)
  - 8-contact WSON (6mm x 5mm)
- All devices are RoHS compliant

### Product Description

The 25 series Serial Flash family features a four-wire, SPI-compatible interface that allows for a low pin-count package which occupies less board space and ultimately lowers total system costs. The SST25VF040B devices are enhanced with improved operating frequency and even lower power consumption. SST25VF040B SPI serial flash memories are manufactured with proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

SST25VF040B devices significantly improve performance and reliability, while lowering power consumption. The devices write (Program or Erase) with a single power supply of 2.7-3.6V for SST25VF040B. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

The SST25VF040B device is offered in an 8-lead SOIC (200 mils), 8-lead SOIC (150 mils), and 8-contact WSON (6mm x 5mm) packages. See [Figure 2-1](#) for pin assignments.

## TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at [docerrors@microchip.com](mailto:docerrors@microchip.com). We welcome your feedback.

### Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

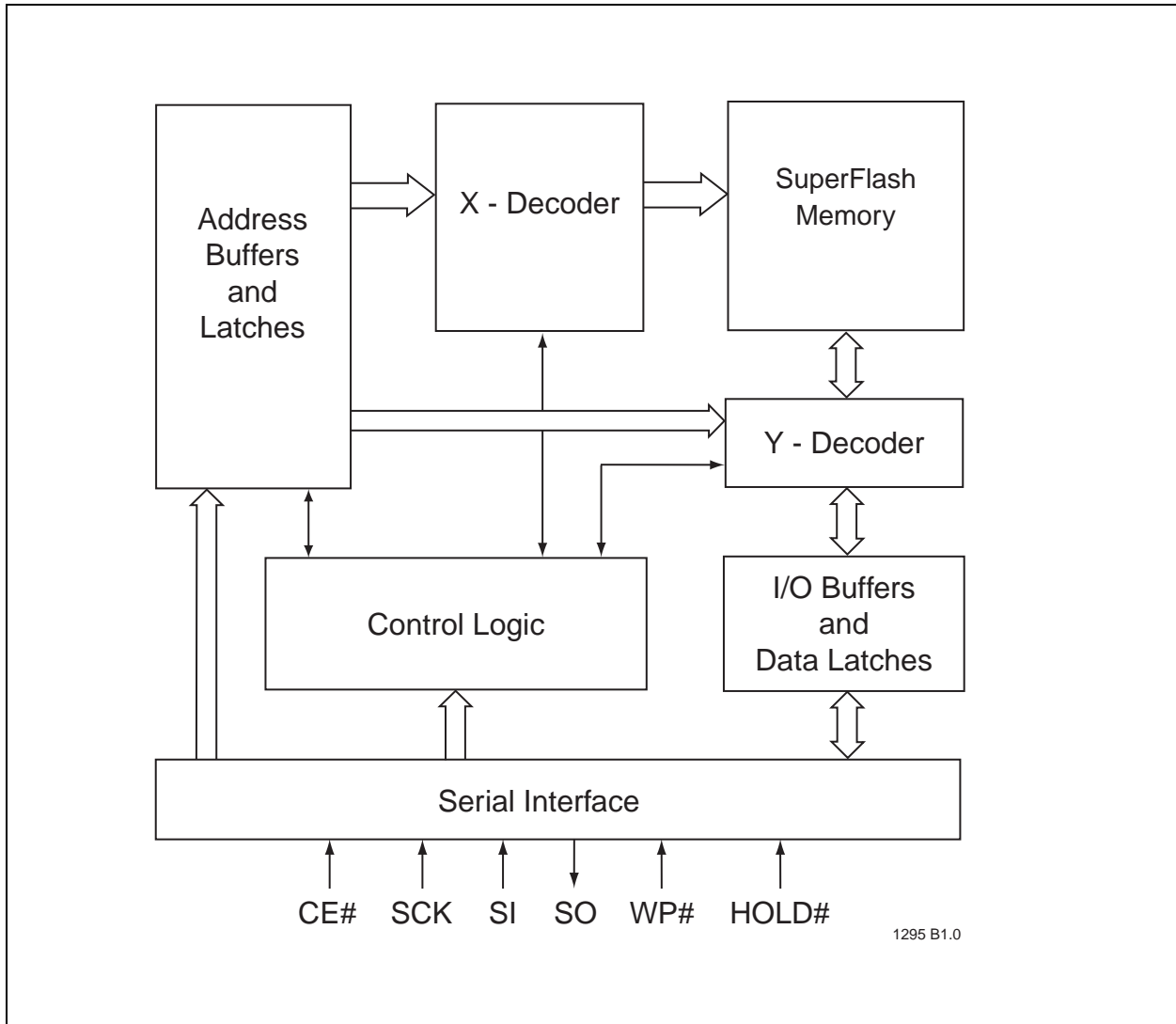
When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

### Customer Notification System

Register on our web site at [www.microchip.com](http://www.microchip.com) to receive the most current information on all of our products.

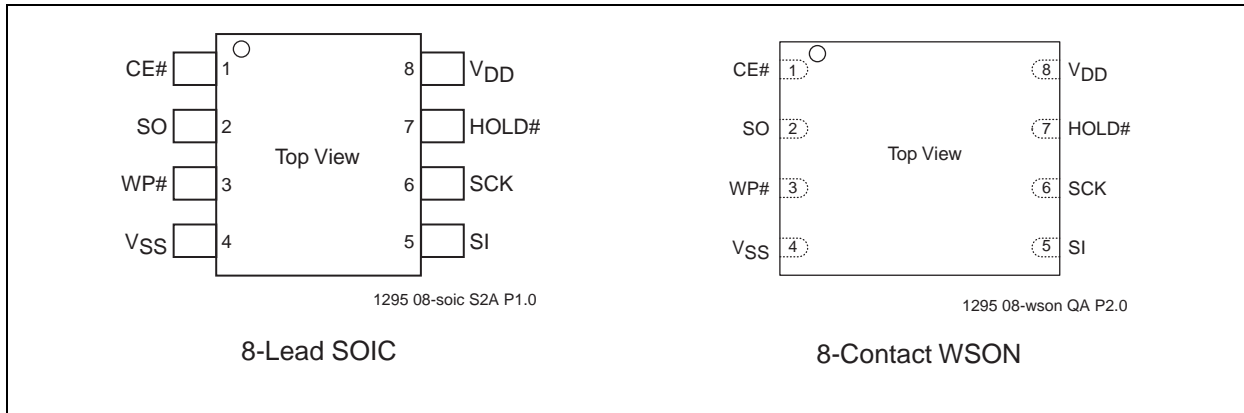
## 1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



## 2.0 PIN DESCRIPTION

**FIGURE 2-1: PIN ASSIGNMENTS**



**TABLE 2-1: PIN DESCRIPTION**

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. Outputs Flash busy status during AAI Programming when reconfigured as RY/BY# pin. See <a href="#">“Hardware End-of-Write Detection” on page 11</a> for details.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable/disable BPL bit in the status register.
HOLD#	Hold	To temporarily stop serial communication with SPI flash memory without resetting the device.
V <sub>DD</sub>	Power Supply	To provide power supply voltage: 2.7-3.6V for SST25VF040B
V <sub>SS</sub>	Ground	

### 3.0 MEMORY ORGANIZATION

The SST25VF040B SuperFlash memory array is organized in uniform 4 KByte erasable sectors with 32 KByte overlay blocks and 64 KByte overlay erasable blocks.

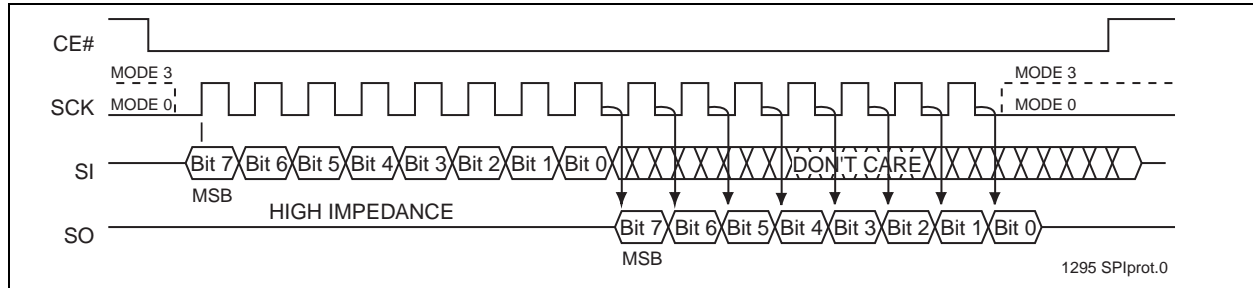
### 4.0 DEVICE OPERATION

The SST25VF040B is accessed through the SPI (Serial Peripheral Interface) bus compatible protocol. The SPI bus consist of four control lines; Chip Enable (CE#) is

used to select the device, and data is accessed through the Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK).

The SST25VF040B supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 4-1, is the state of the SCK signal when the bus master is in Stand-by mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

FIGURE 4-1: SPI PROTOCOL



#### 4.1 Hold Operation

The HOLD# pin is used to pause a serial sequence underway with the SPI flash memory without resetting the clocking sequence. To activate the HOLD# mode, CE# must be in active low state. The HOLD# mode begins when the SCK active low state coincides with the falling edge of the HOLD# signal. The HOLD mode ends when the HOLD# signal's rising edge coincides with the SCK active low state.

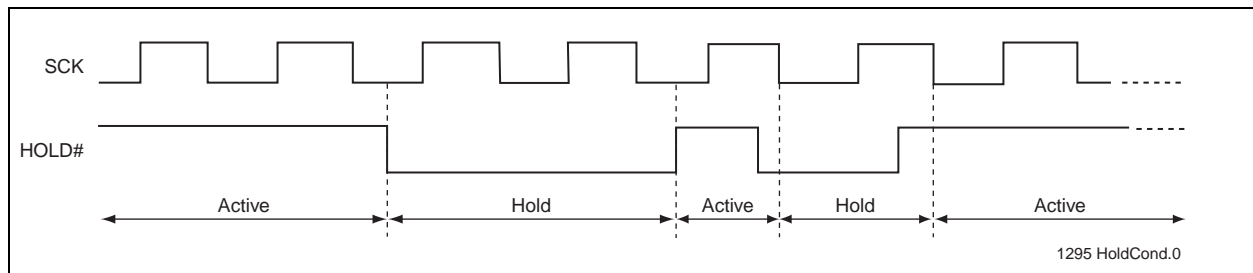
If the falling edge of the HOLD# signal does not coincide with the SCK active low state, then the device enters Hold mode when the SCK next reaches the active low state. Similarly, if the rising edge of the

HOLD# signal does not coincide with the SCK active low state, then the device exits in Hold mode when the SCK next reaches the active low state. See Figure 4-2 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be  $V_{IL}$  or  $V_{IH}$ .

If CE# is driven active high during a Hold condition, it resets the internal logic of the device. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active high, and CE# must be driven active low. See Figure 5-3 for Hold timing.

FIGURE 4-2: HOLD CONDITION WAVEFORM



## 4.2 Write Protection

SST25VF040B provides software Write protection. The Write Protect pin (WP#) enables or disables the lock-down function of the status register. The Block-Protection bits (BP3, BP2, BP1, BP0, and BPL) in the status register provide Write protection to the memory array and the status register. See [Table 4-3](#) for the Block-Protection description.

### 4.2.1 WRITE PROTECT PIN (WP#)

The Write Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the status register. When WP# is driven low, the execution of the Write-Status-Register (WRSR) instruction is determined by the value of the BPL bit (see [Table 4-1](#)). When WP# is high, the lock-down function of the BPL bit is disabled.

**TABLE 4-1: CONDITIONS TO EXECUTE WRITE-STATUS-REGISTER (WRSR) INSTRUCTION**

WP#	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

## 4.3 Status Register

The software status register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the Memory Write protection.

During an internal Erase or Program operation, the status register may be read only to determine the completion of an operation in progress. [Table 4-2](#) describes the function of each bit in the software status register.

**TABLE 4-2: SOFTWARE STATUS REGISTER**

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See <a href="#">Table 4-3</a> )	1	R/W
3	BP1	Indicate current level of block write protection (See <a href="#">Table 4-3</a> )	1	R/W
4	BP2	Indicate current level of block write protection (See <a href="#">Table 4-3</a> )	1	R/W
5	BP3	Indicate current level of block write protection (See <a href="#">Table 4-3</a> )	0	R/W
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte-Program mode	0	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are read/writable	0	R/W

### 4.3.1 BUSY

The Busy bit determines whether there is an internal Erase or Program operation in progress. A “1” for the Busy bit indicates the device is busy with an operation in progress. A “0” indicates the device is ready for the next valid operation.

any memory Write (Program/Erase) commands. The Write-Enable-Latch bit is automatically reset under the following conditions:

- Power-up
- Write-Disable (WRDI) instruction completion
- Byte-Program instruction completion
- Auto Address Increment (AAI) programming is completed or reached its highest unprotected memory address
- Sector-Erase instruction completion
- Block-Erase instruction completion
- Chip-Erase instruction completion
- Write-Status-Register instructions

### 4.3.2 WRITE ENABLE LATCH (WEL)

The Write-Enable-Latch bit indicates the status of the internal memory Write Enable Latch. If the Write-Enable-Latch bit is set to “1”, it indicates the device is Write enabled. If the bit is set to “0” (reset), it indicates the device is not Write enabled and does not accept

4.3.3 AUTO ADDRESS INCREMENT (AAI)

The Auto Address Increment Programming-Status bit provides status on whether the device is in AAI programming mode or Byte-Program mode. The default at power up is Byte-Program mode.

4.3.4 BLOCK PROTECTION (BP3,BP2, BP1, BP0)

The Block-Protection (BP3, BP2, BP1, BP0) bits define the size of the memory area, as defined in Table 4-3, to be software protected against any memory Write (Program or Erase) operation. The Write-Status-Register (WRSR) instruction is used to program the BP3, BP2,

BP1 and BP0 bits as long as WP# is high or the Block-Protect-Lock (BPL) bit is 0. Chip-Erase can only be executed if Block-Protection bits are all 0. After power-up, BP3, BP2, BP1 and BP0 are set to 1.

4.3.5 BLOCK PROTECTION LOCK-DOWN (BPL)

WP# pin driven low ( $V_{IL}$ ), enables the Block-Protection-Lock-Down (BPL) bit. When BPL is set to 1, it prevents any further alteration of the BPL, BP3, BP2, BP1, and BP0 bits. When the WP# pin is driven high ( $V_{IH}$ ), the BPL bit has no effect and its value is "Don't Care". After power-up, the BPL bit is reset to 0.

TABLE 4-3: SOFTWARE STATUS REGISTER BLOCK PROTECTION FOR SST25VF040B<sup>1</sup>

Protection Level	Status Register Bit <sup>2</sup>				Protected Memory Address
	BP3	BP2	BP1	BP0	4 Mbit
None	X	0	0	0	None
Upper 1/8	X	0	0	1	70000H-7FFFFH
Upper 1/4	X	0	1	0	60000H-7FFFFH
Upper 1/2	X	0	1	1	40000H-7FFFFH
All Blocks	X	1	0	0	00000H-7FFFFH
All Blocks	X	1	0	1	00000H-7FFFFH
All Blocks	X	1	1	0	00000H-7FFFFH
All Blocks	X	1	1	1	00000H-7FFFFH

1. X = Don't Care (RESERVED) default is "0"
2. Default at power-up for BP2, BP1, and BP0 is '111'. (All Blocks Protected)

## 4.4 Instructions

Instructions are used to read, write (Erase and Program), and configure the SST25VF040B. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. Prior to executing any Byte-Program, Auto Address Increment (AAI) programming, Sector-Erase, Block-Erase, Write-Status-Register, or Chip-Erase instructions, the Write-Enable (WREN) instruction must be executed first. The complete list of instructions is provided in [Table 4-4](#). All instructions are synchronized off a high to low transition

of CE#. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID, and Read-Status-Register instructions). Any low to high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to standby mode. Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

**TABLE 4-4: DEVICE OPERATION INSTRUCTIONS**

Instruction	Description	Op Code Cycle <sup>1</sup>	Address Cycle(s) <sup>2</sup>	Dummy Cycle(s)	Data Cycle(s)
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞
High-Speed Read	Read Memory at higher speed	0000 1011b (0BH)	3	1	1 to ∞
4 KByte Sector-Erase <sup>3</sup>	Erase 4 KByte of memory array	0010 0000b (20H)	3	0	0
32 KByte Block-Erase <sup>4</sup>	Erase 32 KByte block of memory array	0101 0010b (52H)	3	0	0
64 KByte Block-Erase <sup>5</sup>	Erase 64 KByte block of memory array	1101 1000b (D8H)	3	0	0
Chip-Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0
Byte-Program	To Program One Data Byte	0000 0010b (02H)	3	0	1
AAI-Word-Program <sup>6</sup>	Auto Address Increment Programming	1010 1101b (ADH)	3	0	2 to ∞
RDSR <sup>7</sup>	Read-Status-Register	0000 0101b (05H)	0	0	1 to ∞
EWSR	Enable-Write-Status-Register	0101b 0000b (50H)	0	0	0
WRSR	Write-Status-Register	0000 0001b (01H)	0	0	1
WREN	Write-Enable	0000 0110b (06H)	0	0	0
WRDI	Write-Disable	0000 0100b (04H)	0	0	0
RDID <sup>8</sup>	Read-ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞
JEDEC-ID	JEDEC ID read	1001 1111b (9FH)	0	0	3 to ∞
EBSY	Enable SO to output RY/BY# status during AAI programming	0111 0000b (70H)	0	0	0
DBSY	Disable SO as RY/BY# status during AAI programming	1000 0000b (80H)	0	0	0

- One bus cycle is eight clock periods.
- Address bits above the most significant bit of each density can be V<sub>IL</sub> or V<sub>IH</sub>.
- 4KByte Sector Erase addresses: use A<sub>MS</sub>-A<sub>12</sub>, remaining addresses are don't care but must be set either at V<sub>IL</sub> or V<sub>IH</sub>.
- 32KByte Block Erase addresses: use A<sub>MS</sub>-A<sub>15</sub>, remaining addresses are don't care but must be set either at V<sub>IL</sub> or V<sub>IH</sub>.
- 64KByte Block Erase addresses: use A<sub>MS</sub>-A<sub>16</sub>, remaining addresses are don't care but must be set either at V<sub>IL</sub> or V<sub>IH</sub>.
- To continue programming to the next sequential address location, enter the 8-bit command, ADH, followed by 2 bytes of data to be programmed. Data Byte 0 will be programmed into the initial address [A<sub>23</sub>-A<sub>1</sub>] with A<sub>0</sub>=0, Data Byte 1 will be programmed into the initial address [A<sub>23</sub>-A<sub>1</sub>] with A<sub>0</sub>=1.
- The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.
- Manufacturer's ID is read with A<sub>0</sub>=0, and Device ID is read with A<sub>0</sub>=1. All other address bits are 00H. The Manufacturer's ID and device ID output stream is continuous until terminated by a low-to-high transition on CE#.



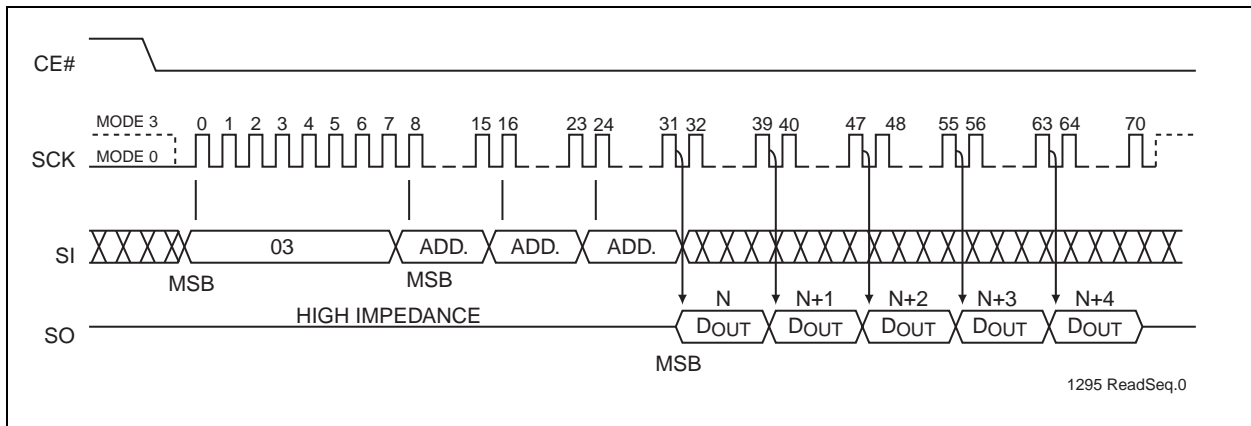
4.4.1 READ (25 MHZ)

The Read instruction, 03H, supports up to 25 MHz Read. The device outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automati-

cally increment to the beginning (wrap-around) of the address space. Once the data from address location 1FFFFFFH has been read, the next output will be from address location 000000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits [A<sub>23</sub>-A<sub>0</sub>]. CE# must remain active low for the duration of the Read cycle. See Figure 4-3 for the Read sequence.

FIGURE 4-3: READ SEQUENCE



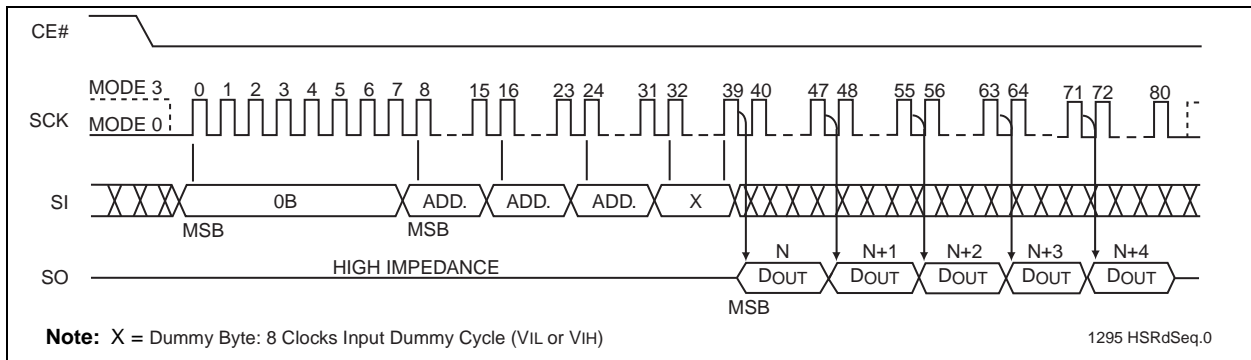
4.4.2 HIGH-SPEED-READ (50 MHZ)

The High-Speed-Read instruction supporting up to 50 MHz Read is initiated by executing an 8-bit command, 0BH, followed by address bits [A<sub>23</sub>-A<sub>0</sub>] and a dummy byte. CE# must remain active low for the duration of the High-Speed-Read cycle. See Figure 4-4 for the High-Speed-Read sequence.

Following a dummy cycle, the High-Speed-Read instruction outputs the data starting from the specified address location. The data output stream is continuous

through all addresses until terminated by a low to high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. Once the data from address location 7FFFFFFH has been read, the next output will be from address location 000000H.

FIGURE 4-4: HIGH-SPEED-READ SEQUENCE



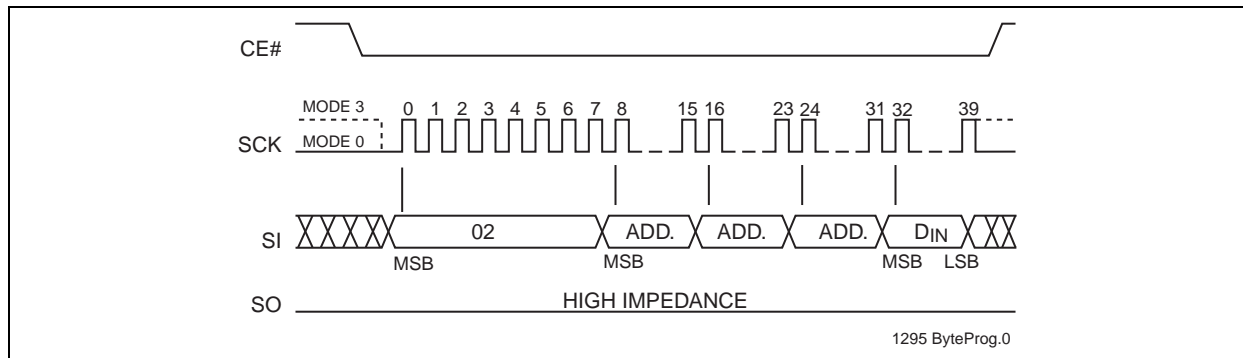
## 4.4.3 BYTE-PROGRAM

The Byte-Program instruction programs the bits in the selected byte to the desired data. The selected byte must be in the erased state (FFH) when initiating a Program operation. A Byte-Program instruction applied to a protected memory area will be ignored.

Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of the Byte-Program instruction.

The Byte-Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits [A<sub>23</sub>-A<sub>0</sub>]. Following the address, the data is input in order from MSB (bit 7) to LSB (bit 0). CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait T<sub>BP</sub> for the completion of the internal self-timed Byte-Program operation. See Figure 4-5 for the Byte-Program sequence.

**FIGURE 4-5: BYTE-PROGRAM SEQUENCE**



## 4.4.4 AUTO ADDRESS INCREMENT (AAI) WORD-PROGRAM

The AAI program instruction allows multiple bytes of data to be programmed without re-issuing the next sequential address location. This feature decreases total programming time when multiple bytes or entire memory array is to be programmed. An AAI Word program instruction pointing to a protected memory area will be ignored. The selected address range must be in the erased state (FFH) when initiating an AAI Word Program operation. While within AAI Word Programming sequence, only the following instructions are valid: for software end-of-write detection—AAI Word (ADH), WRDI (04H), and RDSR (05H); for hardware end-of-write detection—AAI Word (ADH) and WRDI (04H). There are three options to determine the completion of each AAI Word program cycle: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the software status register, or wait T<sub>BP</sub>. Refer to “End-of-Write Detection” for details.

Prior to any write operation, the Write-Enable (WREN) instruction must be executed. Initiate the AAI Word Program instruction by executing an 8-bit command, ADH, followed by address bits [A<sub>23</sub>-A<sub>0</sub>]. Following the addresses, two bytes of data are input sequentially, each one from MSB (Bit 7) to LSB (Bit 0). The first byte of data (D0) is programmed into the initial address [A<sub>23</sub>-A<sub>1</sub>] with A<sub>0</sub>=0, the second byte of Data (D1) is programmed into the initial address [A<sub>23</sub>-A<sub>1</sub>] with A<sub>0</sub>=1. CE# must be driven high before executing the AAI Word Program instruction. Check the BUSY status before entering the next valid command. Once the

device indicates it is no longer busy, data for the next two sequential addresses may be programmed, followed by the next two, and so on.

When programming the last desired word, or the highest unprotected memory address, check the busy status using either the hardware or software (RDSR instruction) method to check for program completion. Once programming is complete, use the applicable method to terminate AAI. If the device is in Software End-of-Write Detection mode, execute the Write-Disable (WRDI) instruction, 04H. If the device is in AAI Hardware End-of-Write Detection mode, execute the Write-Disable (WRDI) instruction, 04H, followed by the 8-bit DBSY command, 80H. There is no wrap mode during AAI programming once the highest unprotected memory address is reached. See Figures 4-8 and 4-9 for the AAI Word programming sequence.

## 4.4.5 END-OF-WRITE DETECTION

There are three methods to determine completion of a program cycle during AAI Word programming: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the Software Status Register, or wait T<sub>BP</sub>. The Hardware End-of-Write detection method is described in the section below.

4.4.6 HARDWARE END-OF-WRITE DETECTION

The Hardware End-of-Write detection method eliminates the overhead of polling the Busy bit in the Software Status Register during an AAI Word program operation. The 8-bit command, 70H, configures the Serial Output (SO) pin to indicate Flash Busy status during AAI Word programming. (see Figure 4-6) The 8-bit command, 70H, must be executed prior to initiating an AAI Word-Program instruction. Once an internal programming operation begins, asserting CE# will immediately drive the status of the internal flash status

on the SO pin. A '0' indicates the device is busy and a '1' indicates the device is ready for the next instruction. De-asserting CE# will return the SO pin to tri-state. While in AAI and Hardware End-of-Write detection mode, the only valid instructions are AAI Word (ADH) and WRDI (04H).

To exit AAI Hardware End-of-Write detection, first execute WRDI instruction, 04H, to reset the Write-Enable-Latch bit (WEL=0) and AAI bit. Then execute the 8-bit DBSY command, 80H, to disable RY/BY# status during the AAI command. See Figures 4-7 and 4-8.

FIGURE 4-6: ENABLE SO AS HARDWARE RY/BY# DURING AAI PROGRAMMING

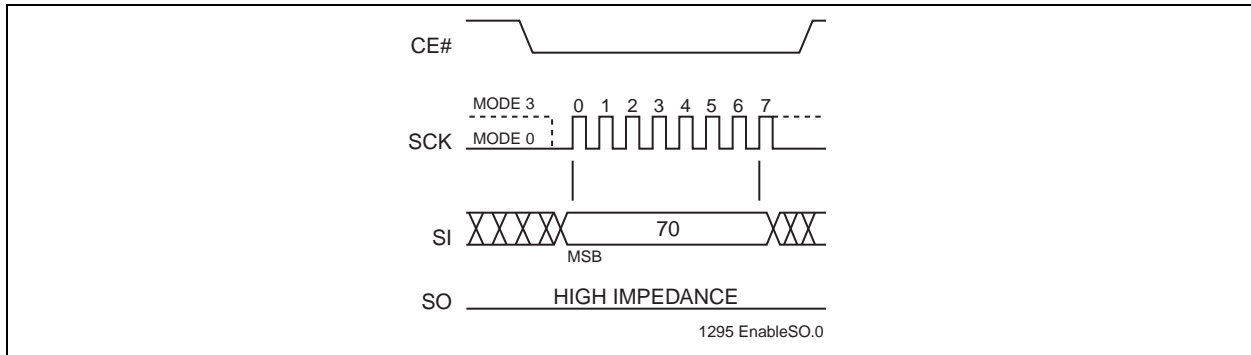
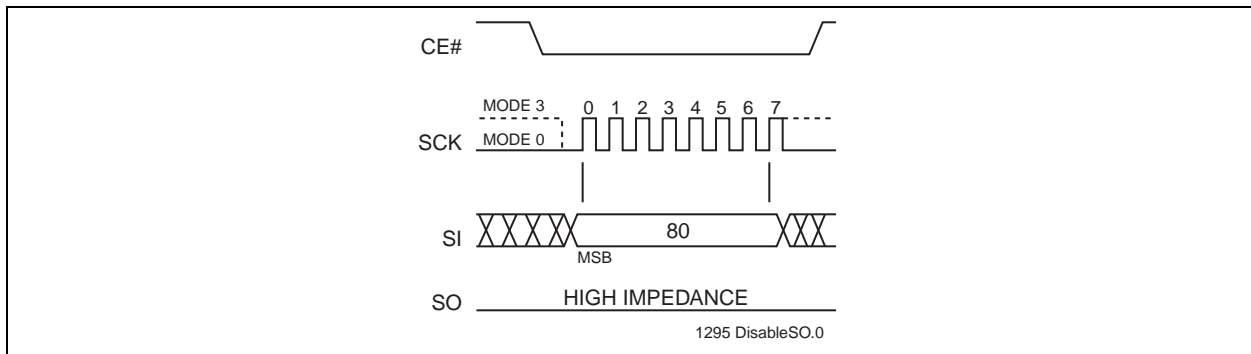
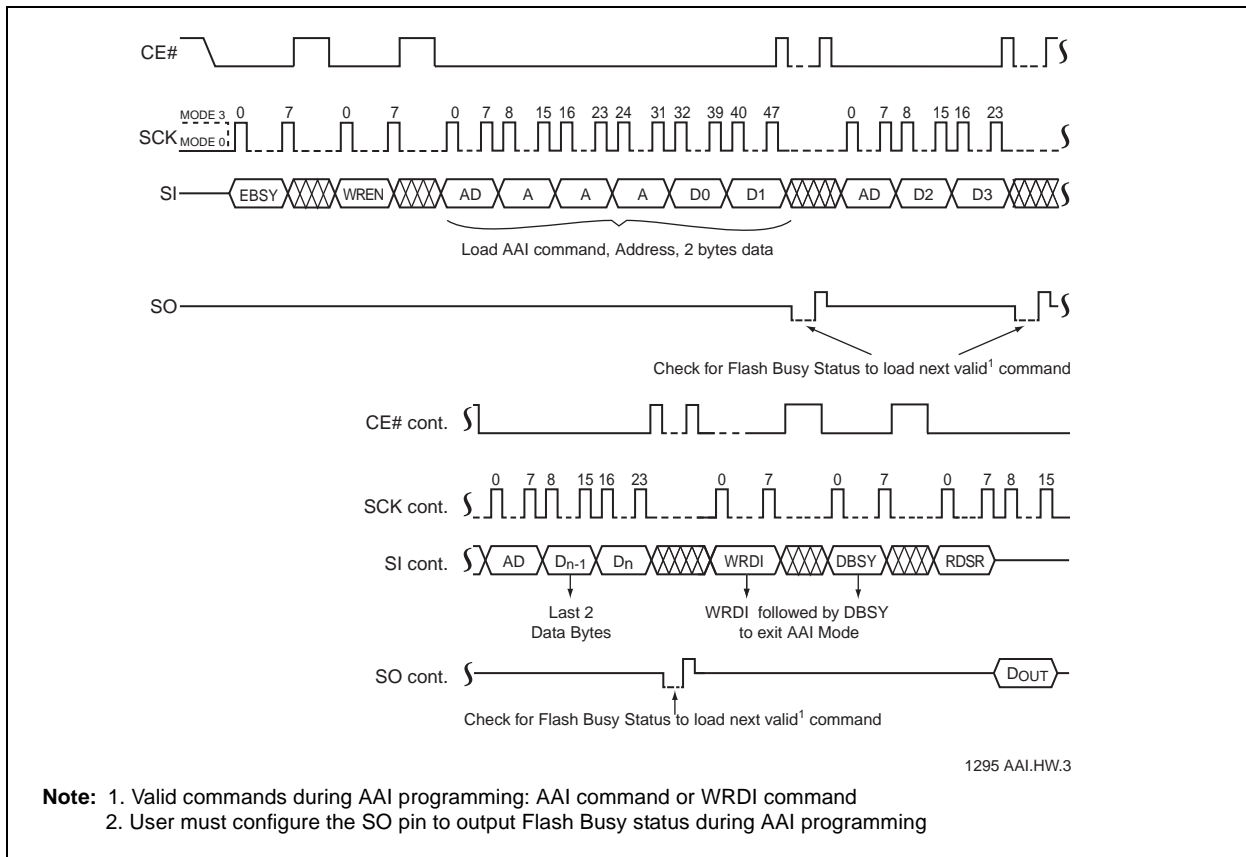


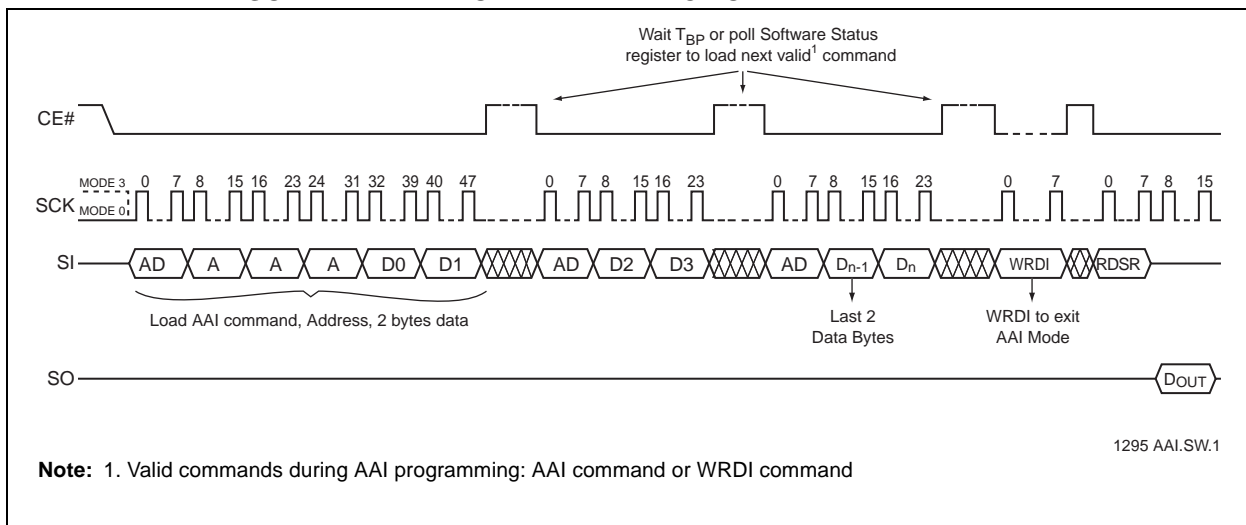
FIGURE 4-7: DISABLE SO AS HARDWARE RY/BY# DURING AAI PROGRAMMING



**FIGURE 4-8: AUTO ADDRESS INCREMENT (AAI) WORD-PROGRAM SEQUENCE WITH HARDWARE END-OF-WRITE DETECTION**



**FIGURE 4-9: AUTO ADDRESS INCREMENT (AAI) WORD-PROGRAM SEQUENCE WITH SOFTWARE END-OF-WRITE DETECTION**

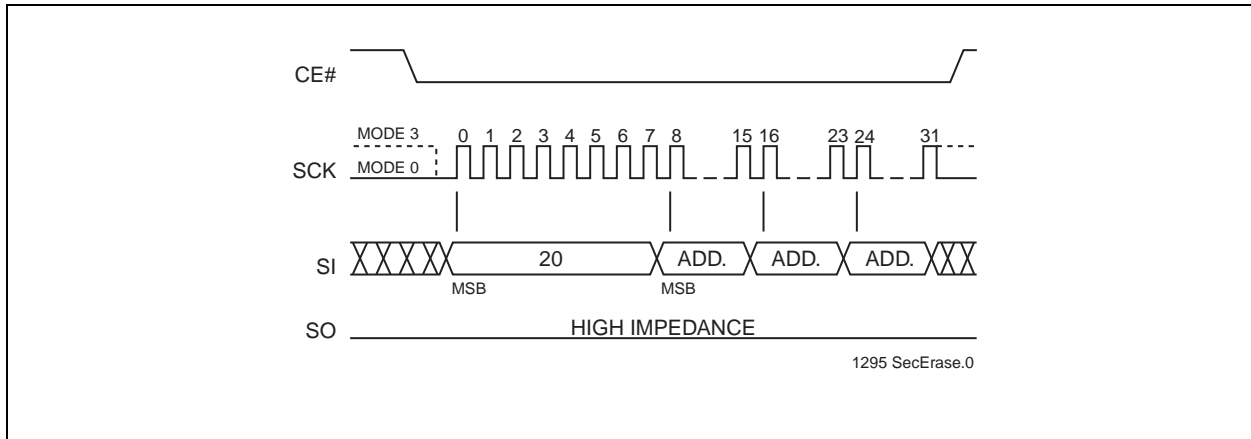


4.4.7 4-KBYTE SECTOR-ERASE

The Sector-Erase instruction clears all bits in the selected 4 KByte sector to FFH. A Sector-Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of any command sequence. The Sector-Erase instruction is initiated by executing an 8-bit command, 20H, followed by address

bits [A<sub>23</sub>-A<sub>0</sub>]. Address bits [A<sub>MS</sub>-A<sub>12</sub>] (A<sub>MS</sub> = Most Significant address) are used to determine the sector address (SA<sub>X</sub>), remaining address bits can be V<sub>IL</sub> or V<sub>IH</sub>. CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait T<sub>SE</sub> for the completion of the internal self-timed Sector-Erase cycle. See Figure 4-10 for the Sector-Erase sequence.

FIGURE 4-10: SECTOR-ERASE SEQUENCE

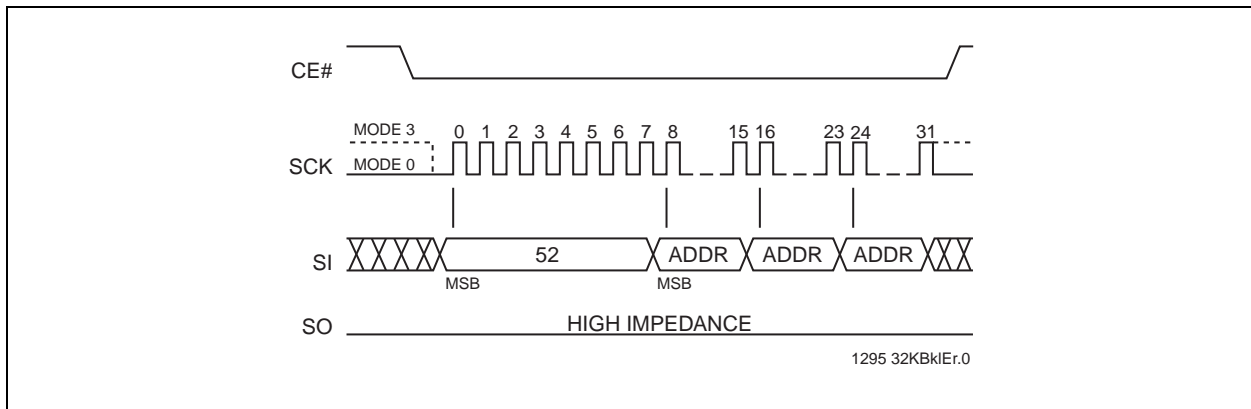


4.4.8 32-KBYTE AND 64-KBYTE BLOCK-ERASE

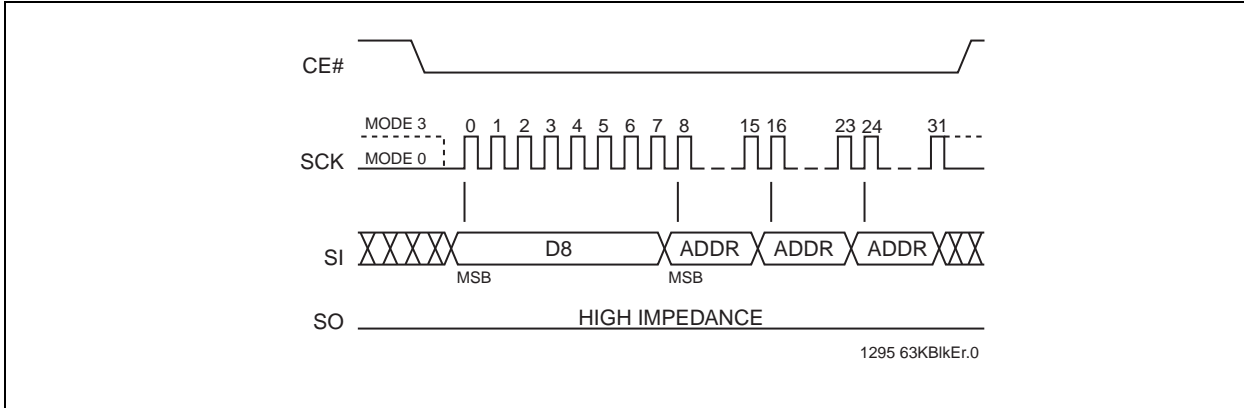
The 32-KByte Block-Erase instruction clears all bits in the selected 32 KByte block to FFH. A Block-Erase instruction applied to a protected memory area will be ignored. The 64-KByte Block-Erase instruction clears all bits in the selected 64 KByte block to FFH. A Block-Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of any command sequence. The 32-KByte Block-Erase instruction is initiated by executing an 8-bit command, 52H, followed by address bits [A<sub>23</sub>-A<sub>0</sub>]. Address bits [A<sub>MS</sub>-A<sub>15</sub>] (A<sub>MS</sub> = Most Sig-

nificant Address) are used to determine block address (BA<sub>X</sub>), remaining address bits can be V<sub>IL</sub> or V<sub>IH</sub>. CE# must be driven high before the instruction is executed. The 64-KByte Block-Erase instruction is initiated by executing an 8-bit command D8H, followed by address bits [A<sub>23</sub>-A<sub>0</sub>]. Address bits [A<sub>MS</sub>-A<sub>16</sub>] are used to determine block address (BA<sub>X</sub>), remaining address bits can be V<sub>IL</sub> or V<sub>IH</sub>. CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait T<sub>BE</sub> for the completion of the internal self-timed 32-KByte Block-Erase or 64-KByte Block-Erase cycles. See Figures 4-11 and 4-12 for the 32-KByte Block-Erase and 64-KByte Block-Erase sequences.

FIGURE 4-11: 32-KBYTE BLOCK-ERASE SEQUENCE



**FIGURE 4-12: 64-KBYTE BLOCK-ERASE SEQUENCE**

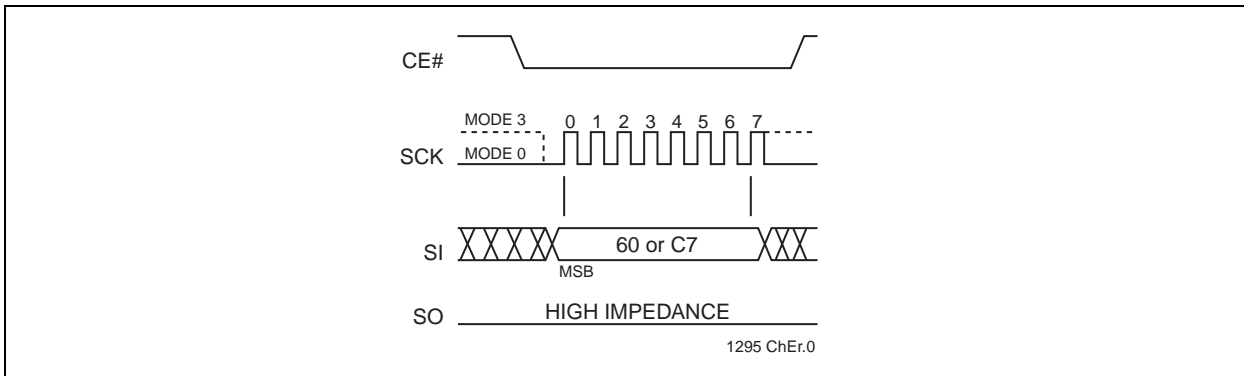


### 4.4.9 CHIP-ERASE

The Chip-Erase instruction clears all bits in the device to FFH. A Chip-Erase instruction will be ignored if any of the memory area is protected. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of the Chip-Erase instruction sequence. The Chip-Erase

instruction is initiated by executing an 8-bit command, 60H or C7H. CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait  $T_{CE}$  for the completion of the internal self-timed Chip-Erase cycle. See Figure 4-13 for the Chip-Erase sequence.

**FIGURE 4-13: CHIP-ERASE SEQUENCE**

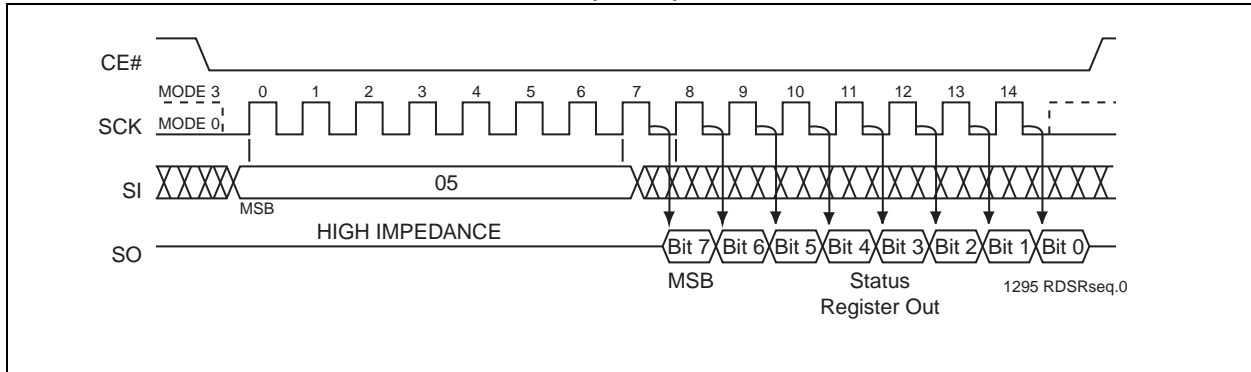


4.4.10 READ-STATUS-REGISTER (RDSR)

The Read-Status-Register (RDSR) instruction allows reading of the status register. The status register may be read at any time even during a Write (Program/Erase) operation. When a Write operation is in progress, the Busy bit may be checked before sending any new commands to assure that the new commands are

properly received by the device. CE# must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read-Status-Register is continuous with ongoing clock cycles until it is terminated by a low to high transition of the CE#. See Figure 4-14 for the RDSR instruction sequence.

FIGURE 4-14: READ-STATUS-REGISTER (RDSR) SEQUENCE

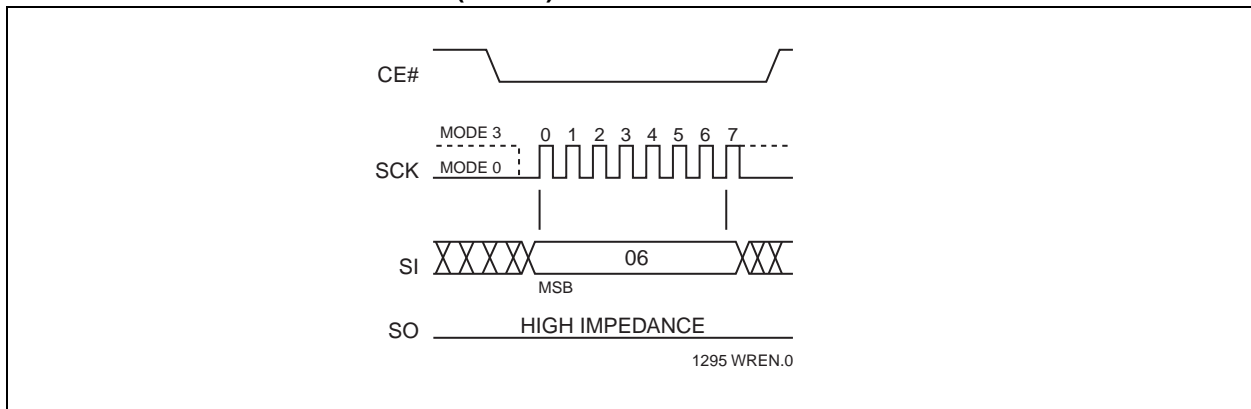


4.4.11 WRITE-ENABLE (WREN)

The Write-Enable (WREN) instruction sets the Write-Enable-Latch bit in the Status Register to 1 allowing Write operations to occur. The WREN instruction must be executed prior to any Write (Program/Erase) operation. The WREN instruction may also be used to allow

execution of the Write-Status-Register (WRSR) instruction; however, the Write-Enable-Latch bit in the Status Register will be cleared upon the rising edge CE# of the WRSR instruction. CE# must be driven high before the WREN instruction is executed.

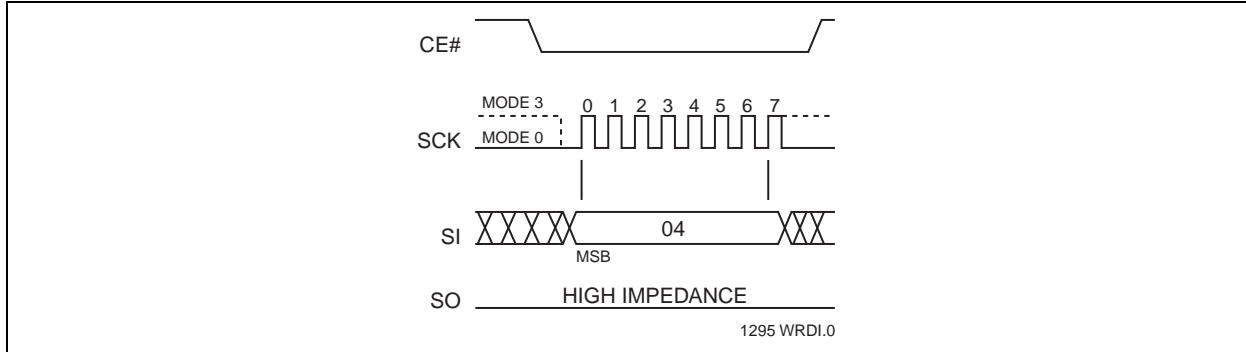
FIGURE 4-15: WRITE ENABLE (WREN) SEQUENCE



## 4.4.12 WRITE-DISABLE (WRDI)

The Write-Disable (WRDI) instruction resets the Write-Enable-Latch bit and AAI bit to 0 disabling any new Write operations from occurring. The WRDI instruction will not terminate any programming operation in prog-

ress. Any program operation in progress may continue up to  $T_{BP}$  after executing the WRDI instruction. CE# must be driven high before the WRDI instruction is executed.



**FIGURE 4-16: WRITE DISABLE (WRDI) SEQUENCE**

## 4.4.13 ENABLE-WRITE-STATUS-REGISTER (EWSR)

The Enable-Write-Status-Register (EWSR) instruction arms the Write-Status-Register (WRSR) instruction and opens the status register for alteration. The Write-Status-Register instruction must be executed immediately after the execution of the Enable-Write-Status-Register instruction. This two-step instruction sequence of the EWSR instruction followed by the WRSR instruction works like SDP (software data protection) command structure which prevents any accidental alteration of the status register values. CE# must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.

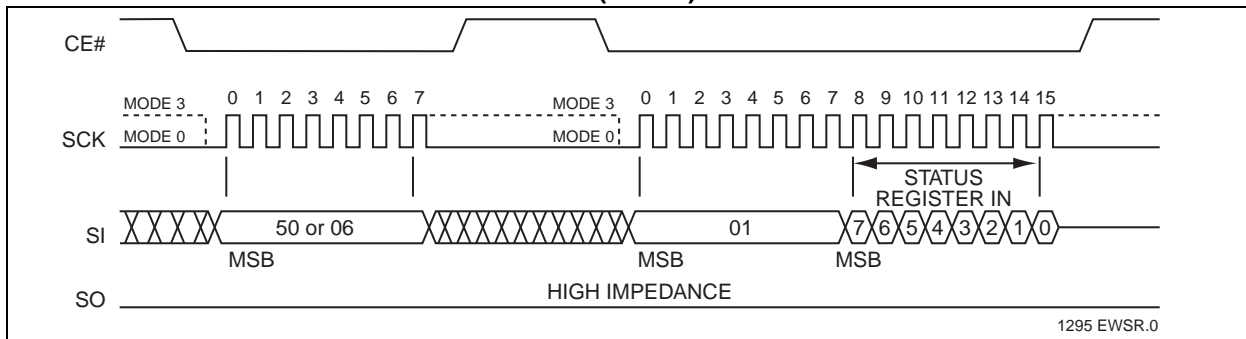
command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 4-17 for EWSR or WREN and WRSR instruction sequences.

Executing the Write-Status-Register instruction will be ignored when WP# is low and BPL bit is set to "1". When the WP# is low, the BPL bit can only be set from "0" to "1" to lock-down the status register, but cannot be reset from "1" to "0". When WP# is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, and BP1 and BP2 bits in the status register can all be changed. As long as BPL bit is set to 0 or WP# pin is driven high ( $V_{IH}$ ) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the bits in the status register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to "1" to lock down the status register as well as altering the BP0, BP1, and BP2 bits at the same time. See Table 4-1 for a summary description of WP# and BPL functions.

## 4.4.14 WRITE-STATUS-REGISTER (WRSR)

The Write-Status-Register instruction writes new values to the BP3, BP2, BP1, BP0, and BPL bits of the status register. CE# must be driven low before the

**FIGURE 4-17: ENABLE-WRITE-STATUS-REGISTER (EWSR) OR WRITE-ENABLE (WREN) AND WRITE-STATUS-REGISTER (WRSR) SEQUENCE**





4.4.15 JEDEC READ-ID

The JEDEC Read-ID instruction identifies the device as SST25VF040B and the manufacturer as Microchip. The device information can be read from executing the 8-bit command, 9FH. Following the JEDEC Read-ID instruction, the 8-bit manufacturer's ID, BFH, is output from the device. After that, a 16-bit device ID is shifted

out on the SO pin. Byte 1, BFH, identifies the manufacturer as Microchip. Byte 2, 25H, identifies the memory type as SPI Serial Flash. Byte 3, 8DH, identifies the device as SST25VF040B. The instruction sequence is shown in Figure 4-18. The JEDEC Read ID instruction is terminated by a low to high transition on CE# at any time during data output.

FIGURE 4-18: JEDEC READ-ID SEQUENCE

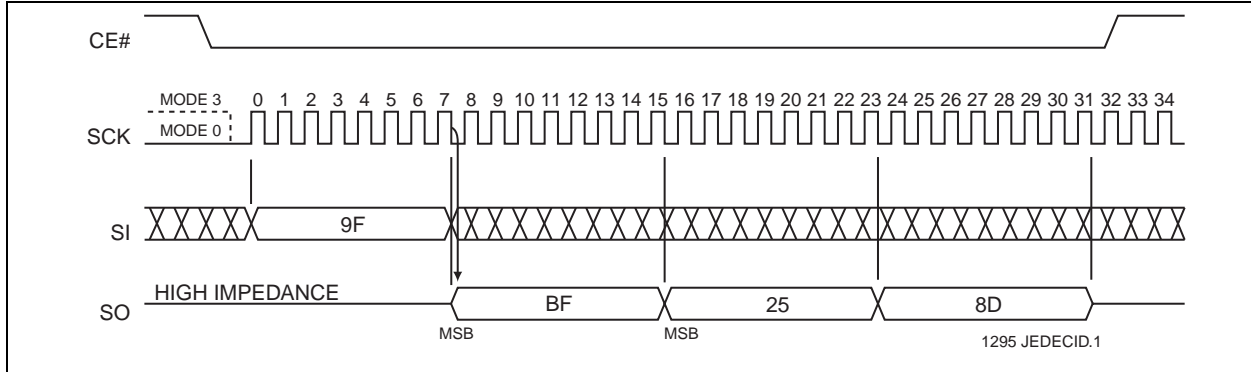


TABLE 4-5: JEDEC READ-ID DATA

Manufacturer's ID	Device ID	
	Memory Type	Memory Capacity
Byte1	Byte 2	Byte 3
BFH	25H	8DH

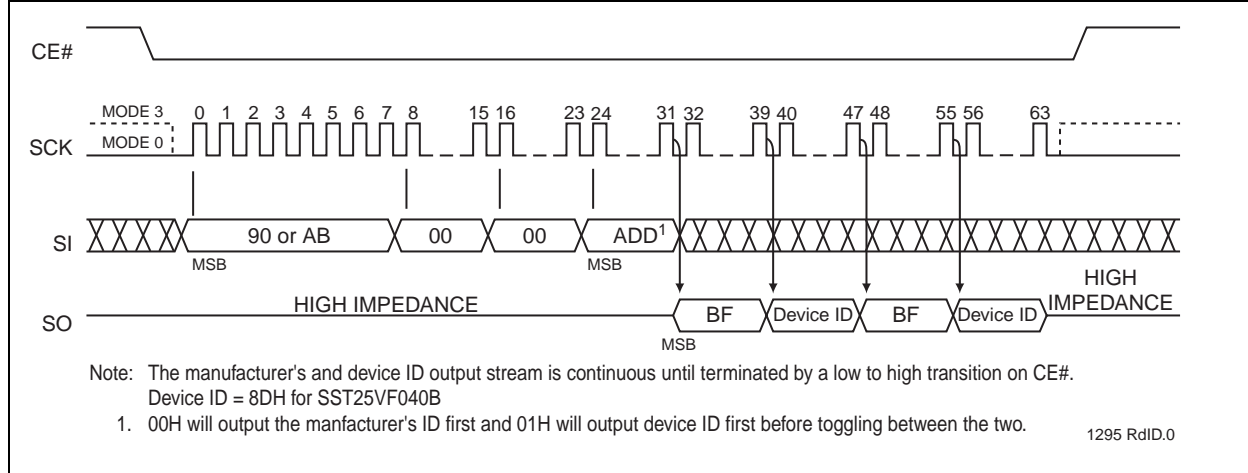
## 4.4.16 READ-ID (RDID)

The Read-ID instruction (RDID) identifies the devices as SST25VF040B and manufacturer as Microchip. This command is backward compatible to all SST25xFxxxA devices and should be used as default device identification when multiple versions of SPI Serial Flash devices are used in a design. The device information can be read from executing an 8-bit command, 90H or ABH, followed by address bits [A<sub>23</sub>-A<sub>0</sub>]. Following the

Read-ID instruction, the manufacturer's ID is located in address 00000H and the device ID is located in address 00001H. Once the device is in Read-ID mode, the manufacturer's and device ID output data toggles between address 00000H and 00001H until terminated by a low to high transition on CE#.

Refer to Tables 4-5 and 4-6 for device identification data.

**FIGURE 4-19: READ-ID SEQUENCE**



**TABLE 4-6: PRODUCT IDENTIFICATION**

	Address	Data
Manufacturer's ID	00000H	BFH
Device ID		
SST25VF040B	00001H	8DH

## 5.0 ELECTRICAL SPECIFICATIONS

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to $V_{DD}+0.5V$
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-2.0V to $V_{DD}+2.0V$
Package Power Dissipation Capability ( $T_A = 25^\circ C$ )	1.0W
Surface Mount Solder Reflow Temperature	260°C for 10 seconds
Output Short Circuit Current <sup>1</sup>	50 mA

1. Output shorted for no more than one second. No more than one output shorted at a time.

**TABLE 5-1: OPERATING RANGE**

Range	Ambient Temp	$V_{DD}$
Commercial	0°C to +70°C	2.7-3.6V
Industrial	-40°C to +85°C	2.7-3.6V

**TABLE 5-2: AC CONDITIONS OF TEST<sup>1</sup>**

Input Rise/Fall Time	Output Load
5ns	$C_L = 30\text{ pF}$

1. See Figures 5-5 and 5-6

**TABLE 5-3: DC OPERATING CHARACTERISTICS**

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
$I_{DDR}$	Read Current		10	mA	$CE\#=0.1 V_{DD}/0.9 V_{DD}$ @25 MHz, SO=open
$I_{DDR2}$	Read Current		15	mA	$CE\#=0.1 V_{DD}/0.9 V_{DD}$ @50 MHz, SO=open
$I_{DDW}$	Program and Erase Current		30	mA	$CE\#=V_{DD}$
$I_{SB}$	Standby Current		20	$\mu A$	$CE\#=V_{DD}$ , $V_{IN}=V_{DD}$ or $V_{SS}$
$I_{LI}$	Input Leakage Current		1	$\mu A$	$V_{IN}=\text{GND to } V_{DD}$ , $V_{DD}=V_{DD}\text{ Max}$
$I_{LO}$	Output Leakage Current		1	$\mu A$	$V_{OUT}=\text{GND to } V_{DD}$ , $V_{DD}=V_{DD}\text{ Max}$
$V_{IL}$	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}\text{ Min}$
$V_{IH}$	Input High Voltage	$0.7 V_{DD}$		V	$V_{DD}=V_{DD}\text{ Max}$
$V_{OL}$	Output Low Voltage		0.2	V	$I_{OL}=100\ \mu A$ , $V_{DD}=V_{DD}\text{ Min}$
$V_{OL2}$	Output Low Voltage		0.4	V	$I_{OL}=1.6\text{ mA}$ , $V_{DD}=V_{DD}\text{ Min}$
$V_{OH}$	Output High Voltage	$V_{DD}-0.2$		V	$I_{OH}=-100\ \mu A$ , $V_{DD}=V_{DD}\text{ Min}$

**TABLE 5-4: CAPACITANCE ( $T_A = 25^\circ C$ ,  $F=1\text{ MHz}$ , OTHER PINS OPEN)**

Parameter	Description	Test Condition	Maximum
$C_{OUT}^1$	Output Pin Capacitance	$V_{OUT} = 0V$	12 pF
$C_{IN}^1$	Input Capacitance	$V_{IN} = 0V$	6 pF

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 5-5: RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Minimum Specification	Units	Test Method
$N_{END}^1$	Endurance	10,000	Cycles	JEDEC Standard A117
$T_{DR}^1$	Data Retention	100	Years	JEDEC Standard A103
$I_{LTH}^1$	Latch Up	$100 + I_{DD}$	mA	JEDEC Standard 78

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 5-6: AC OPERATING CHARACTERISTICS**

Symbol	Parameter	25 MHz		50 MHz		Units
		Min	Max	Min	Max	
$F_{CLK}^1$	Serial Clock Frequency		25		50	MHz
$T_{SCKH}$	Serial Clock High Time	18		9		ns
$T_{SCKL}$	Serial Clock Low Time	18		9		ns
$T_{SCKR}^2$	Serial Clock Rise Time (Slew Rate)	0.1		0.1		V/ns
$T_{SCKF}$	Serial Clock Fall Time (Slew Rate)	0.1		0.1		V/ns
$T_{CES}^3$	CE# Active Setup Time	10		5		ns
$T_{CEH}^3$	CE# Active Hold Time	10		5		ns
$T_{CHS}^3$	CE# Not Active Setup Time	10		5		ns
$T_{CHH}^3$	CE# Not Active Hold Time	10		5		ns
$T_{CPH}$	CE# High Time	100		50		ns
$T_{CHZ}$	CE# High to High-Z Output		15		8	ns
$T_{CLZ}$	SCK Low to Low-Z Output	0		0		ns
$T_{DS}$	Data In Setup Time	5		2		ns
$T_{DH}$	Data In Hold Time	5		5		ns
$T_{HLS}$	HOLD# Low Setup Time	10		5		ns
$T_{HHS}$	HOLD# High Setup Time	10		5		ns
$T_{HLH}$	HOLD# Low Hold Time	10		5		ns
$T_{HHH}$	HOLD# High Hold Time	10		5		ns
$T_{HZ}$	HOLD# Low to High-Z Output		20		8	ns
$T_{LZ}$	HOLD# High to Low-Z Output		15		8	ns
$T_{OH}$	Output Hold from SCK Change	0		0		ns
$T_V$	Output Valid from SCK		15		8	ns
$T_{SE}$	Sector-Erase		25		25	ms
$T_{BE}$	Block-Erase		25		25	ms
$T_{SCE}$	Chip-Erase		50		50	ms
$T_{BP}$	Byte-Program		10		10	μs

1. Maximum clock frequency for Read Instruction, 03H, is 25 MHz
2. Maximum Rise and Fall time may be limited by  $T_{SCKH}$  and  $T_{SCKL}$  requirements
3. Relative to SCK.

FIGURE 5-1: SERIAL INPUT TIMING DIAGRAM

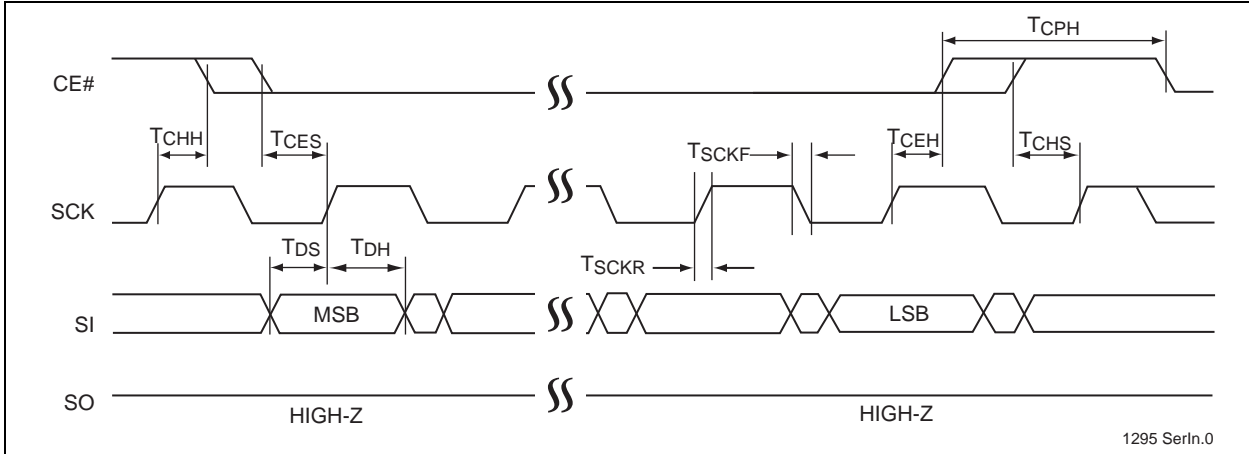


FIGURE 5-2: SERIAL OUTPUT TIMING DIAGRAM

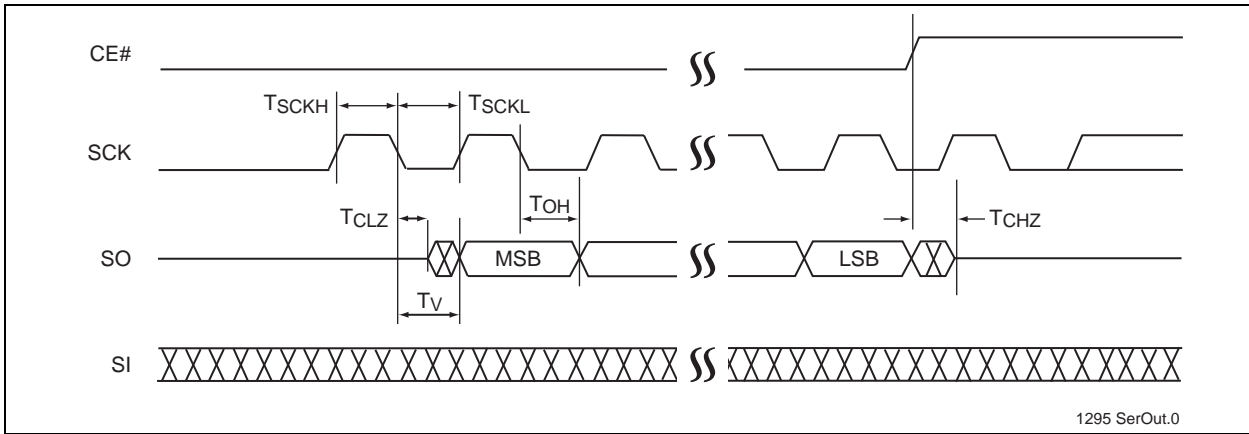
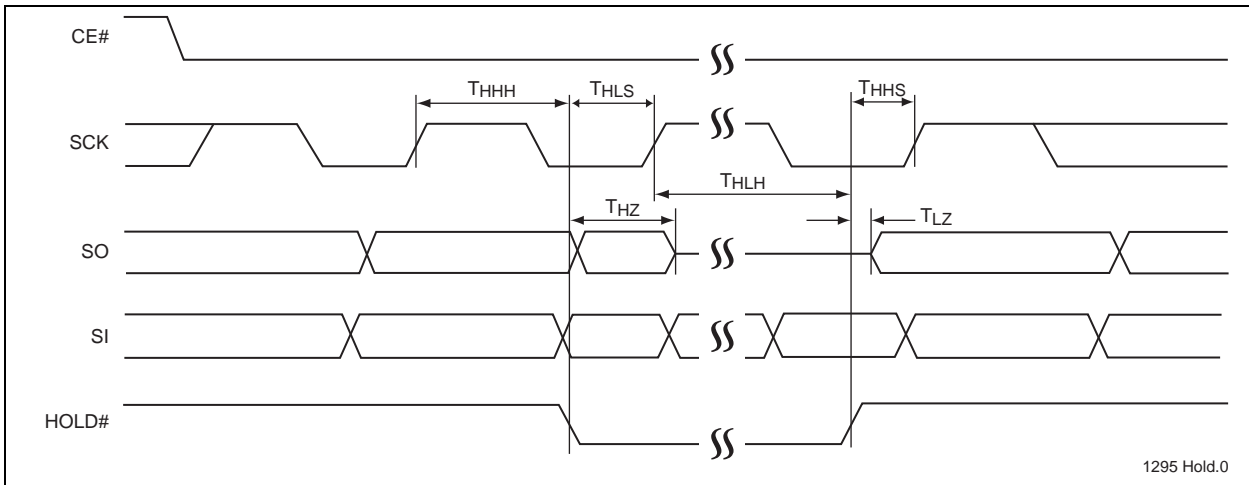


FIGURE 5-3: HOLD TIMING DIAGRAM



## 5.1 Power-Up Specifications

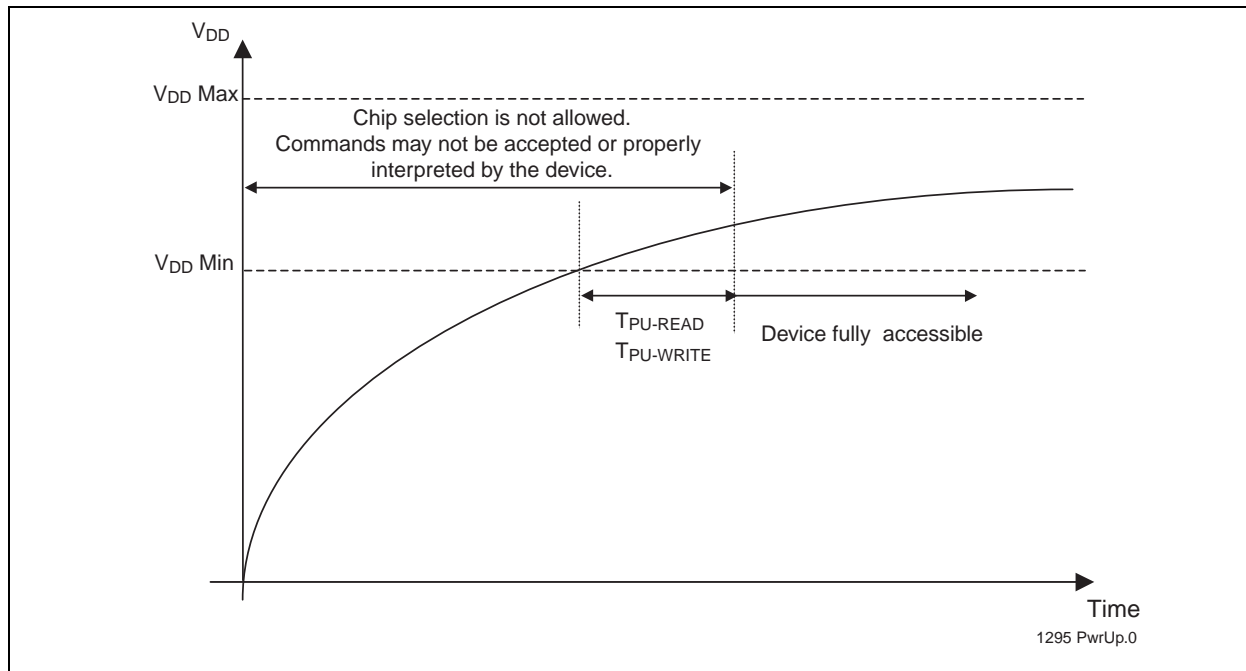
All functionalities and DC specifications are specified for a  $V_{DD}$  ramp rate of greater than 1V per 100 ms (0v - 3.0V in less than 300 ms). See [Table 5-7](#) and [Figure 5-4](#) for more information.

**TABLE 5-7: RECOMMENDED SYSTEM POWER-UP TIMINGS**

Symbol	Parameter	Minimum	Units
$T_{PU-READ}^1$	$V_{DD}$ Min to Read Operation	100	$\mu$ s
$T_{PU-WRITE}^1$	$V_{DD}$ Min to Write Operation	100	$\mu$ s

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**FIGURE 5-4: POWER-UP TIMING DIAGRAM**



**FIGURE 5-5: AC INPUT/OUTPUT REFERENCE WAVEFORMS**

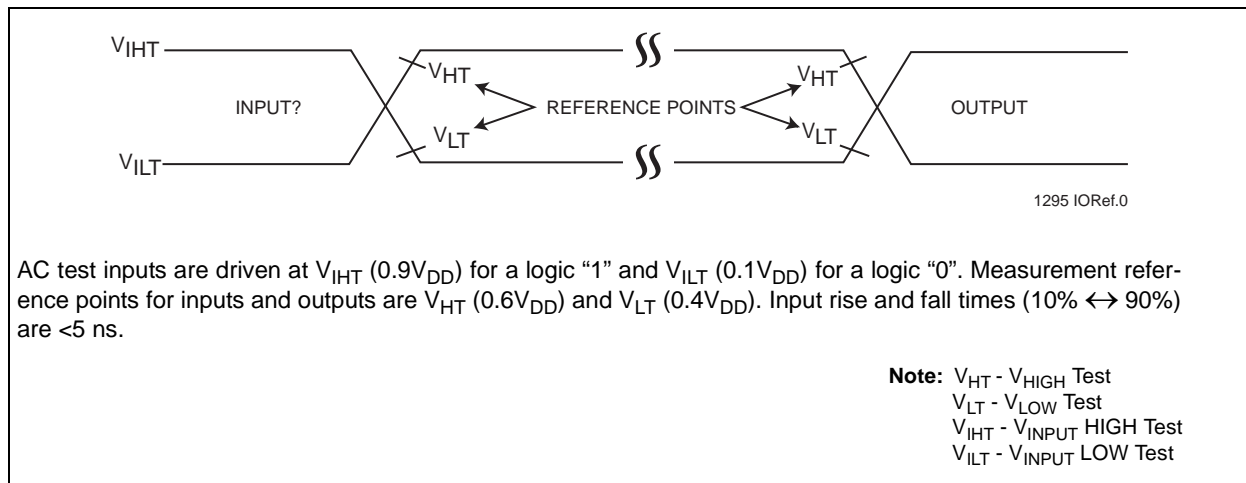
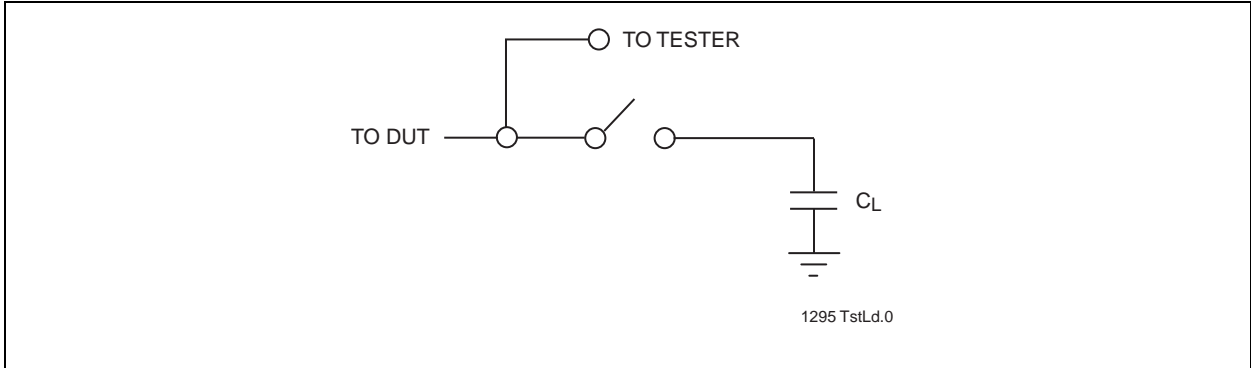


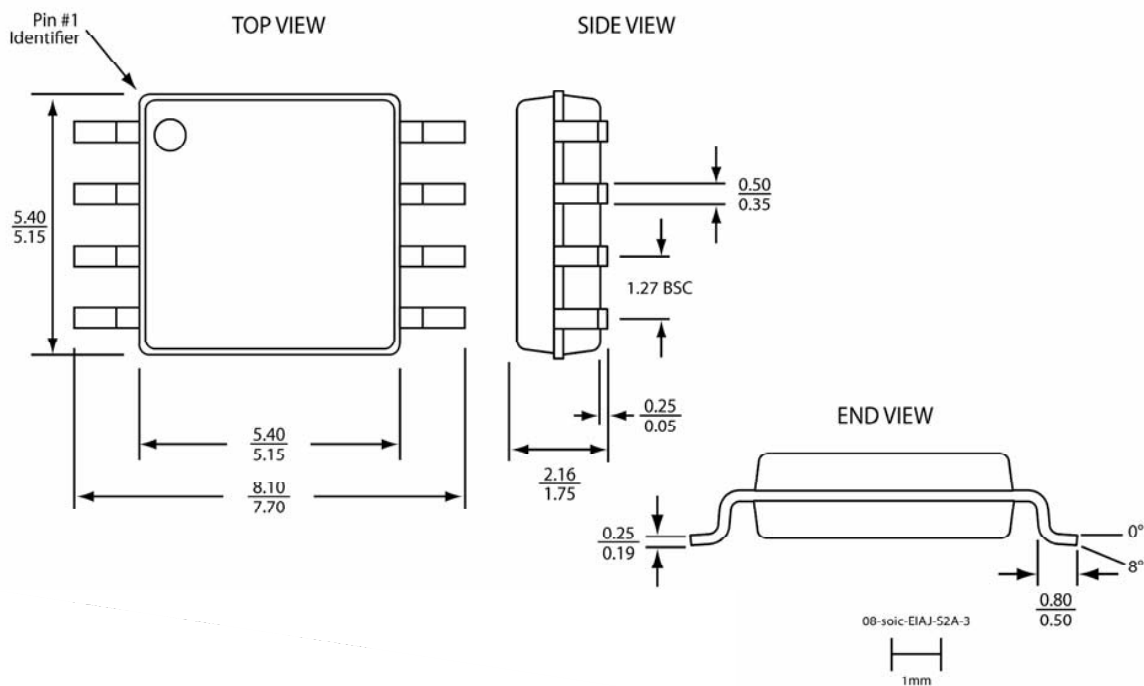
FIGURE 5-6: A TEST LOAD EXAMPLE



## 6.0 PACKAGING DIAGRAMS

### 8-Lead Small Outline Integrated Circuit (S2AE/F) - .208 Inch Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



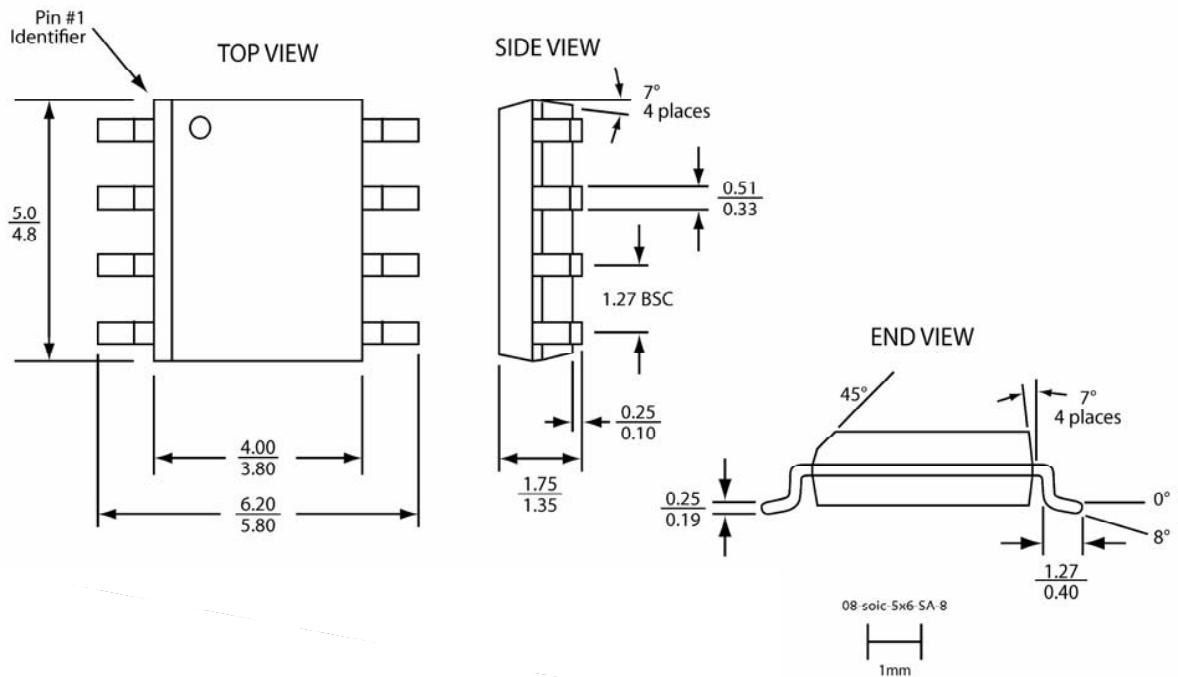
**Note:**

1. All linear dimensions are in millimeters (max/min).
2. Coplanarity: 0.1 mm
3. Maximum allowable mold flash is 0.15 mm at the package ends and 0.25 mm between leads.



## 8-Lead Small Outline Integrated Circuit (SAE/F) - 5x6 mm Body [SOIC]

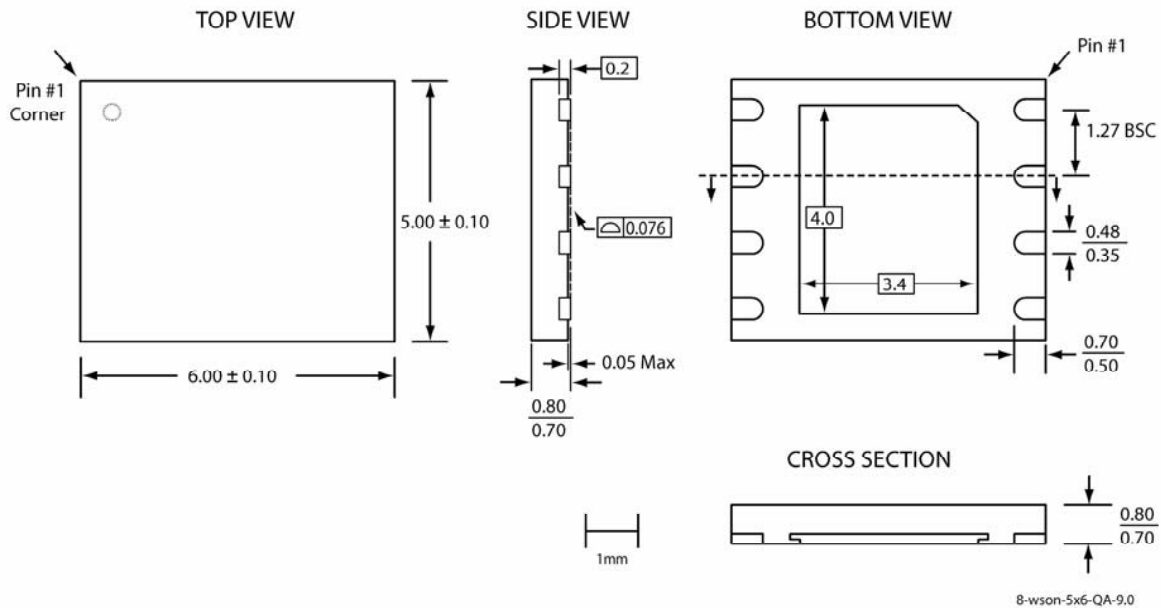
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

**Note:**

1. Complies with JEDEC publication 95 MS-012 AA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends and 0.25 mm between leads.

## 8-Lead Very, Very Thin Small Outline No-Leads (QAE/F) - 5x6 mm Body [WSON]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



**Note:**

1. All linear dimensions are in millimeters (max/min).
2. Untoleranced dimensions (shown with box surround) are nominal target dimensions.
3. The external paddle is electrically connected to the die back-side and possibly to certain VSS leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.

TABLE 6-1: REVISION HISTORY

Revision	Description	Date
00	<ul style="list-style-type: none"> <li>Initial release of data sheet</li> </ul>	Sep 2005
01	<ul style="list-style-type: none"> <li>Migrated document to a Data Sheet</li> <li>Updated Surface Mount Solder Reflow Temperature information</li> </ul>	Jan 2006
02	<ul style="list-style-type: none"> <li>Added 8-Lead SOIC (150 mils) package drawing.</li> <li>Updated Features and Product Description to include new package information.</li> <li>Updated Pin-Assignment, <a href="#">Figure 2-1</a></li> <li>Revised <a href="#">Figure 4-8</a> and <a href="#">Figure 4-9</a></li> </ul>	Jul 2007
03	<ul style="list-style-type: none"> <li>Updated document to reflect upgraded clock frequency to 80 MHz globally</li> <li>Updated Features</li> <li>Changed maximum frequency to 80 MHz in <a href="#">Table 4-4 on page 8</a></li> <li>Added IDDR3 to <a href="#">Table 5-3 on page 19</a></li> <li>Added 80 MHz column to <a href="#">Table 5-6 on page 20</a></li> <li>Updated Product Ordering Information and Valid Combinations on page 29</li> </ul>	Mar 2009
04	<ul style="list-style-type: none"> <li>Updated Product Ordering Information and Valid Combinations on page 29</li> <li>Added “<a href="#">Power-Up Specifications</a>” on page 22</li> <li>Modified High-Speed-Read values in <a href="#">Table 4-4 on page 8</a> and “<a href="#">High-Speed-Read (50 MHz)</a>” on page 9</li> </ul>	Jun 2009
05	<ul style="list-style-type: none"> <li>Added 50/33 MHz information throughout.</li> <li>Separated AC and DC Characteristics for SST25VF040B-50-4C-xxxF &amp; SST25VF040B-80-4I-xxxE</li> </ul>	Oct 2009
06	<ul style="list-style-type: none"> <li>Updated “Auto Address Increment (AAI) Word-Program”, “End-of-Write Detection”, and “<a href="#">Hardware End-of-Write Detection</a>” on page 11.</li> <li>Revised <a href="#">Figures 4-8</a> and <a href="#">4-9</a> on page 12.</li> <li>Updated document to new format.</li> </ul>	Feb 2011
A	<ul style="list-style-type: none"> <li>Removed “Recommended System Power-up Timings” from page 29.</li> <li>Released document under letter revision system.</li> <li>Updated Spec number from S71295 to DS25051</li> </ul>	Sep 2011
B	<ul style="list-style-type: none"> <li>EOL of all 80 MHz parts. Replacement parts are the 50 MHz counterparts found in this document.</li> <li>Removed all 80 MHz information. See DS20005264.</li> <li>Updated document to new format.</li> <li>Replaced all package drawings with drawings in the new format.</li> </ul>	Feb 2014
C	<ul style="list-style-type: none"> <li>Corrected an address bit on page 13</li> </ul>	Jun 2015
D	<ul style="list-style-type: none"> <li>Added Units column and corrected typo in <a href="#">Table 5-6</a>.</li> </ul>	July 2017

## THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at [www.microchip.com](http://www.microchip.com). This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

## CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at [www.microchip.com](http://www.microchip.com). Under "Support", click on "Customer Change Notification" and follow the registration instructions.

## CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

**Technical support is available through the web site at: <http://microchip.com/support>**

## 7.0 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. -		XX	-	XX	-	XX	-	X
Device	Operating Frequency	Minimum Endurance	Temp Range	Package	Tape/Reel Indicator			
Device:	SST25VF040B	= 4 Mbit, 2.7-3.6V, SPI Flash Memory						
Operating Frequency:	50	= 50 MHz						
Minimum Endurance:	4	= 10,000 cycles						
Temperature:	I	= -40°C to +85°C						
	C	= 0°C to +70°C						
Package:	QAF/QAE <sup>1</sup>	= WSON (6mm x 5mm Body), 8-lead						
	S2AF/S2AE <sup>1</sup>	= SOIC (200 mil Body), 8-lead						
	SAF/SAE <sup>1</sup>	= SOIC (150 mm Body), 8-lead						
Tape and Reel Flag:	T	= Tape and Reel						
1. Suffix E = Matte Tin finish Suffix F = Nickel plating with Gold top (outer) layer finish								

**Valid Combinations:**

- SST25VF040B-50-4C-SAF
- SST25VF040B-50-4C-SAF-T
- SST25VF040B-50-4I-SAF
- SST25VF040B-50-4I-SAF-T
- SST25VF040B-50-4I-SAE
- SST25VF040B-50-4I-SAE-T
- SST25VF040B-50-4C-S2AF
- SST25VF040B-50-4C-S2AF-T
- SST25VF040B-50-4I-S2AF
- SST25VF040B-50-4I-S2AF-T
- SST25VF040B-50-4I-S2AE
- SST25VF040B-50-4I-S2AE-T
- SST25VF040B-50-4C-QAF
- SST25VF040B-50-4C-QAF-T
- SST25VF040B-50-4I-QAF
- SST25VF040B-50-4I-QAF-T
- SST25VF040B-50-4I-QAE
- SST25VF040B-50-4I-QAE-T

NOTES:

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

**QUALITY MANAGEMENT SYSTEM  
CERTIFIED BY DNV  
= ISO/TS 16949 =**

**Trademarks**

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KEELoQ, KEELoQ logo, Klear, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2005-2017, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-0976-2



# MICROCHIP

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Austin, TX**  
Tel: 512-257-3370

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Novi, MI  
Tel: 248-848-4000

**Houston, TX**  
Tel: 281-894-5983

**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453  
Tel: 317-536-2380

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608  
Tel: 951-273-7800

**Raleigh, NC**  
Tel: 919-844-7510

**New York, NY**  
Tel: 631-435-6000

**San Jose, CA**  
Tel: 408-735-9110  
Tel: 408-436-4270

**Canada - Toronto**  
Tel: 905-695-1980  
Fax: 905-695-2078

### ASIA/PACIFIC

**Asia Pacific Office**  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon

**Hong Kong**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

**China - Beijing**  
Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

**China - Dongguan**  
Tel: 86-769-8702-9880

**China - Guangzhou**  
Tel: 86-20-8755-8029

**China - Hangzhou**  
Tel: 86-571-8792-8115  
Fax: 86-571-8792-8116

**China - Hong Kong SAR**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

**China - Qingdao**  
Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

**China - Shanghai**  
Tel: 86-21-3326-8000  
Fax: 86-21-3326-8021

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8864-2200  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

### ASIA/PACIFIC

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

**India - Bangalore**  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-3019-1500

**Japan - Osaka**  
Tel: 81-6-6152-7160  
Fax: 81-6-6152-9310

**Japan - Tokyo**  
Tel: 81-3-6880-3770  
Fax: 81-3-6880-3771

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-5778-366  
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7830

**Taiwan - Taipei**  
Tel: 886-2-2508-8600  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**Finland - Espoo**  
Tel: 358-9-4520-820

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**France - Saint Cloud**  
Tel: 33-1-30-60-70-00

**Germany - Garching**  
Tel: 49-8931-9700

**Germany - Haan**  
Tel: 49-2129-3766400

**Germany - Heilbronn**  
Tel: 49-7131-67-3636

**Germany - Karlsruhe**  
Tel: 49-721-625370

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Germany - Rosenheim**  
Tel: 49-8031-354-560

**Israel - Ra'anana**  
Tel: 972-9-744-7705

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Italy - Padova**  
Tel: 39-049-7625286

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Norway - Trondheim**  
Tel: 47-7289-7561

**Poland - Warsaw**  
Tel: 48-22-3325737

**Romania - Bucharest**  
Tel: 40-21-407-87-50

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**Sweden - Gothenberg**  
Tel: 46-31-704-60-40

**Sweden - Stockholm**  
Tel: 46-8-5090-4654

**UK - Wokingham**  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820