BROADCOM®

Data Sheet

ACPL-M50L, ACPL-054L, ACPL-W50L, ACPL-K54L

Low Power, 1 MBd Digital Optocoupler

Description

The Broadcom® ACPL-M50L (single-channel in SO-5 footprint), ACPL-054L (dual-channel in SO-8 footprint), ACPL-W50L (single-channel in stretched SO-6 footprint), and ACPL-K54L (dual-channel in stretched SO-8 footprint) are low power, low-input current, 1-MBd digital optocouplers.

These digital optocouplers use an insulating layer between the light-emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The ACPL-M50L/054L/W50L/K54L has an increased common mode transient immunity of 15 kV/µs minimum at V_{CM} = 1500V over a temperature range of –40°C to +105°C. The current transfer ratio (CTR) is 140% typical for ACPL-M50L or 130% typical for ACPL-054L/W50L/K54L at I_F = 3 mA. This digital optocoupler can be used in any TTL/CMOS, TTL/LSTTL, or wide bandwidth analog applications.

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage and/or degradation that might be induced by electrostatic discharge (ESD). The components featured in this data sheet are not to be used in military or aerospace applications or environments

Features

- Wide supply voltage V_{CC}: 2.7V to 24V
- Low drive current: 3 mA
- Open-collector output
- TTL compatible
- Compact SO-5, SO-8, stretched SO-6, and stretched SO-8 package
- 15 kV/µs high common-mode rejection at V_{CM} = 1500V
- Guaranteed performance from temperature range: –40°C to +105°C
- Low propagation delay: 1 µs max at 5V
- Worldwide safety approval:
  – UL1577 recognized, 3750 V_{rms}/1 min for ACPL-M50L/054L, 5000 V_{rms}/1 min for ACPL-W50L/K54L
  – CSA Approval
  – IEC/EN/DIN EN 60747-5-5 Approval for Reinforced Insulation

Applications

- Communications interface
- Digital signal isolation
- Micro-controller interface
- Feedback elements in switching power supplies
- Digital isolation for A/D, D/A conversion digital field

Figure 1: Functional Diagram

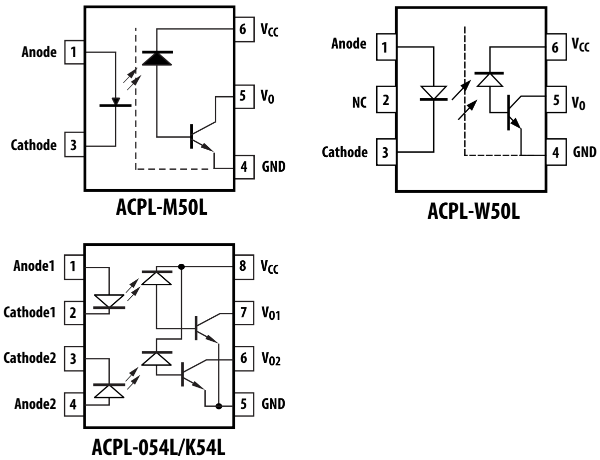


Table 1: Truth Table

LED	VO
ON	LOW
OFF	HIGH

NOTE: The connection of a 0.1-μF bypass capacitor between pins 4 and 6 for ACPL-M50L/W50L and between pins 5 and 8 for ACPL-054L/K54L is recommended.

Ordering Information

ACPL-M50L and ACPL-054L are UL Recognized with 3750 V_{rms} for 1 minute per UL1577. ACPL-W50L and ACPL-K54L are UL Recognized with 5000 V_{rms} for 1 minute per UL1577.

Table 2: Ordering Information

Part Number	Option RoHS Compliant	Package	Surface Mount	Tape and Reel	IEC/EN 60747-5-5	Quantity
ACPL-M50L	-000E	SO-5	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel
ACPL-054L	-000E	SO-8	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel
ACPL-W50L	-000E	Stretched SO-6	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1000 per reel
	-560E		X	X	X	1000 per reel
ACPL-K54L	-000E	Stretched SO-8	X			80 per tube
	-060E		X		X	80 per tube
	-500E		X	X		1000 per reel
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

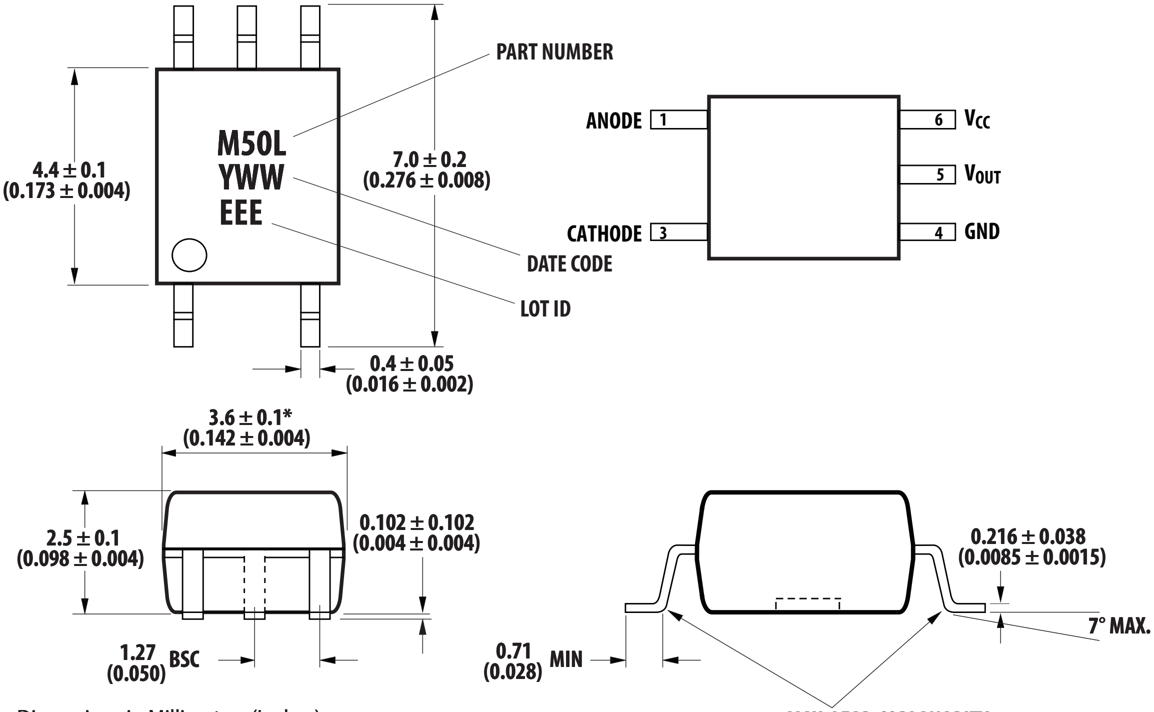
Example 1:

ACPL-M50L-500E to order product of Mini-flat Surface Mount 5-pin package in Tape and Reel packaging with RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

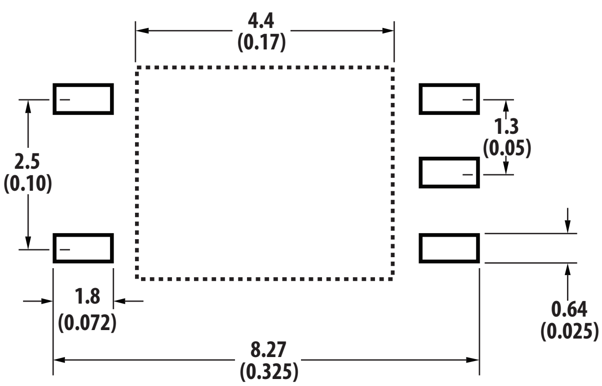
Package Outline Drawings

Figure 2: ACPL-M50L SO-5 Package (JEDEC M0-155)



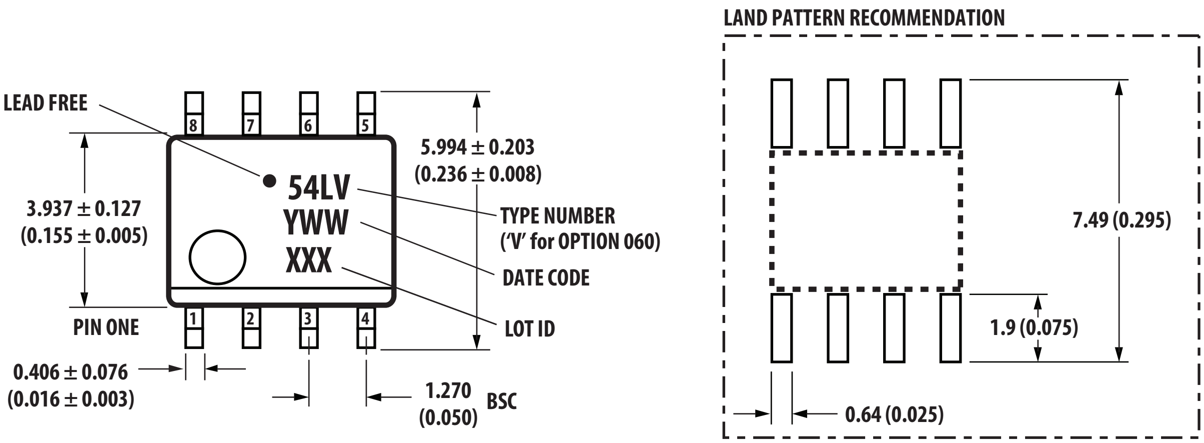
Dimensions in Millimeters (Inches)
* Maximum mold flash on each side is 0.15 mm (0.006)
Note: Floating lead protrusion is 0.15 mm (6 mils) max.

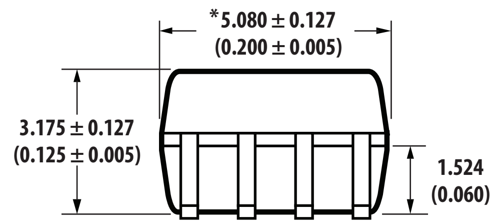
Figure 3: Land Pattern Recommendations

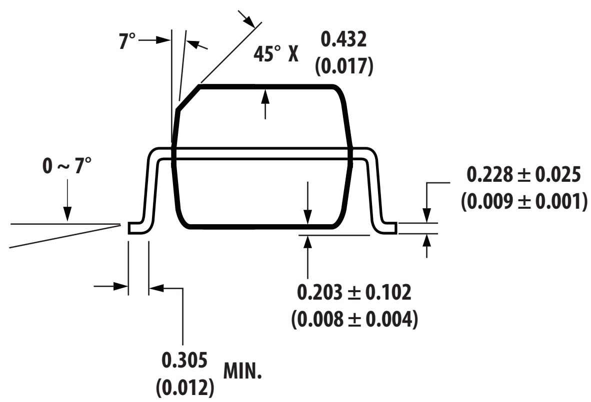


Dimension in Millimeters (Inches)

Figure 4: ACPL-054L (Small Outline SO-8 Package)







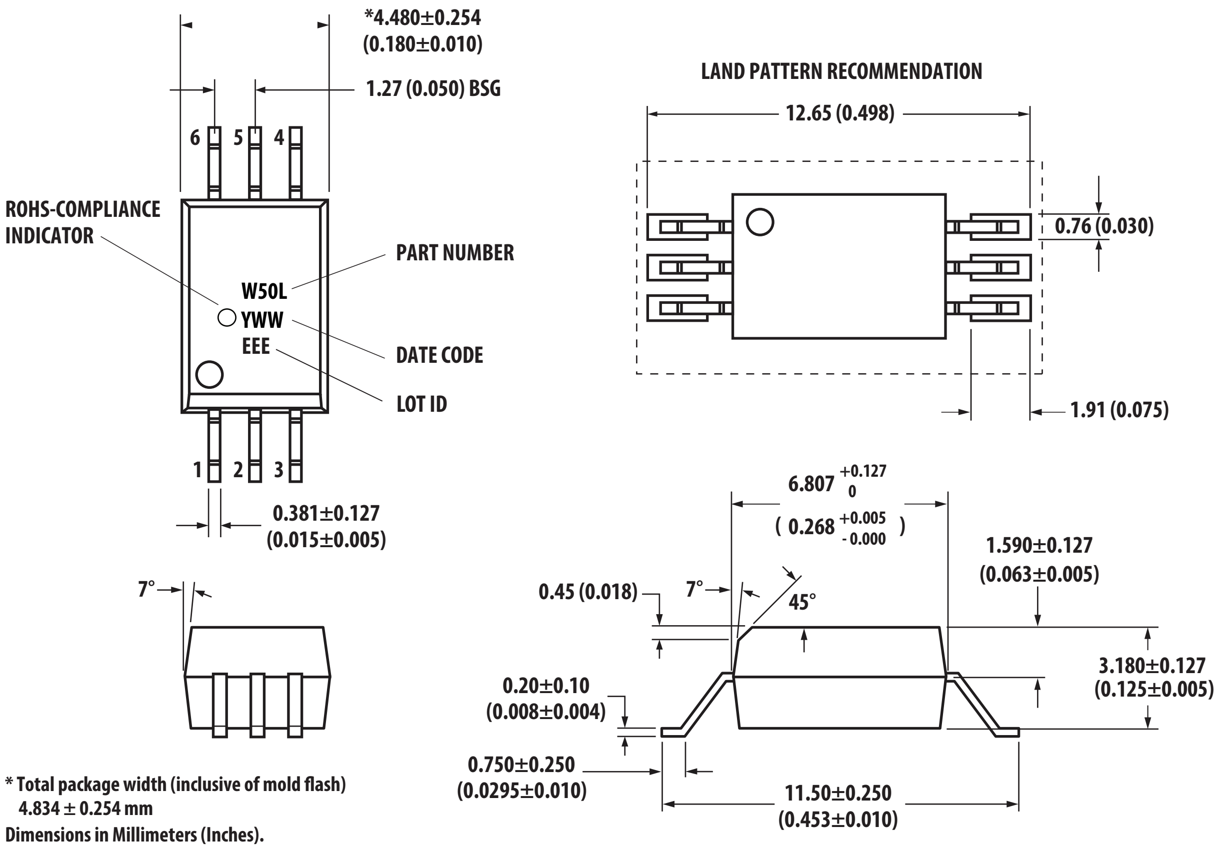
* Total package length (inclusive of mold flash) 5.207 ± 0.254 (0.205 ± 0.010)

Dimensions in Millimeters (Inches).
Lead coplanarity = 0.10 mm (0.004 inches) max.

Option number 500 not marked.

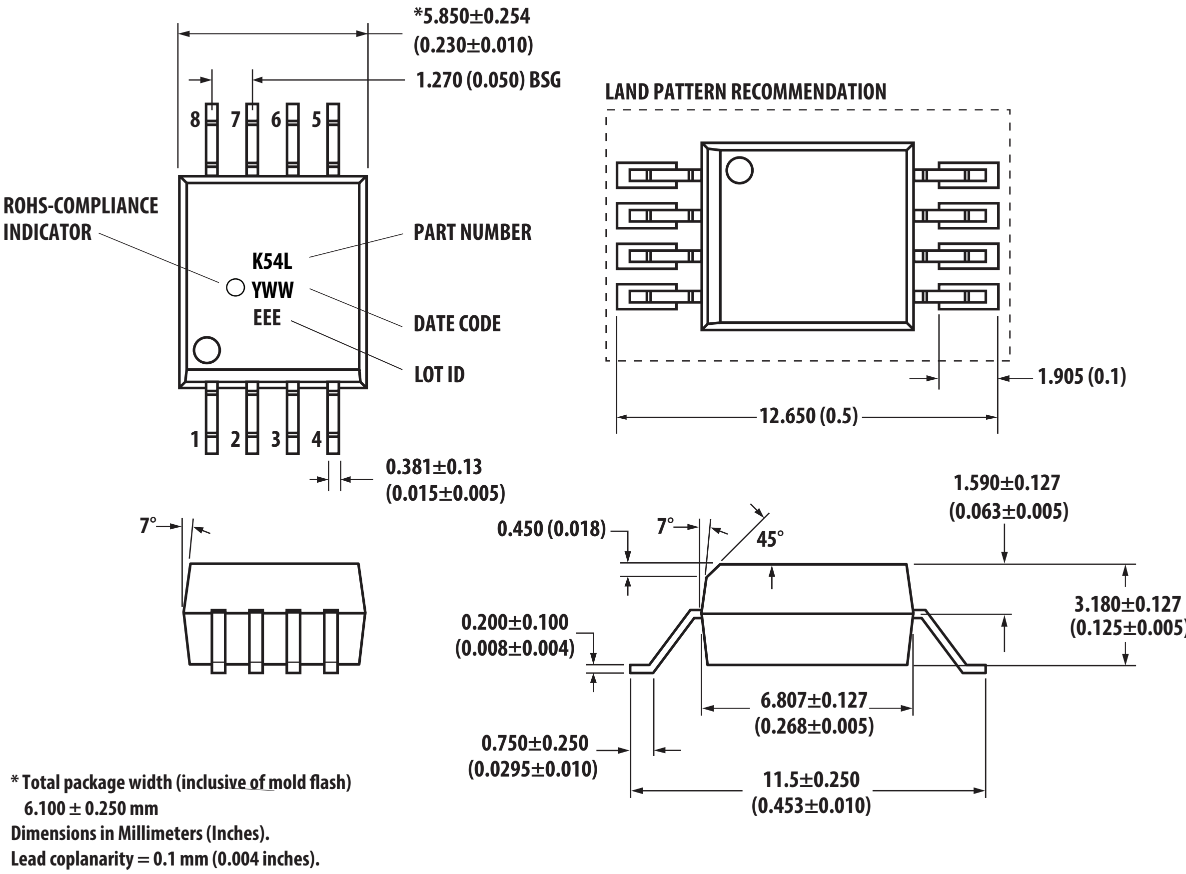
Note: Floating lead protrusion is 0.15 mm (6 mils) max.

Figure 5: ACPL-W50L Stretched SO-6 Package



* Total package width (inclusive of mold flash)
4.834 ± 0.254 mm
Dimensions in Millimeters (Inches).
Lead coplanarity = 0.1 mm (0.004 inches).

Figure 6: ACPL-K54L Stretched SO-8 Package



Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACPL-M50L/054L/W50L/K54L is approved by the following organizations.

UL	Approval under UL 1577, component recognition program up to V_{ISO} = 3750 V_{rms} for ACPL-M50L/054L and V_{ISO} = 5000 V_{rms} for ACPL-W50L/K54L.
CSA	Approval under CSA Component Acceptance Notice #5.
IEC/EN 60747-5-5	(Option 060E only).

Table 3: Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-M50L	ACPL-054L	ACPL-W50L ACPL-K54L	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	5	4.9	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	5	4.8	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	175	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa	—	Material Group (DIN VDE 0110, 1/89, Table 1)

Table 4: IEC/EN60747-5-5 Insulation Characteristics[a] (Option 060E)

Description	Symbol	Characteristic		Units
		ACPL-M50L/ 054L	ACPL-W50L/ K54L	
Installation classification per DIN VDE 0110/39, Table 1				—
For Rated Mains Voltage ≤ 150 V_{rms}		I – IV	I – IV	
For Rated Mains Voltage ≤ 300 V_{rms}		I – III	I – IV	
For Rated Mains Voltage ≤ 600 V_{rms}		I – II	I – III	
For Rated Mains Voltage ≤ 1000 V_{rms}			I – III	
Climatic Classification		55/105/21	55/105/21	—
Pollution Degree (DIN VDE 0110/39)		2	2	—
Maximum Working Insulation Voltage	V_{IORM}	560	1140	V_{peak}
Input to Output Test Voltage, Method b[a] $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1s, Partial discharge < 5 pC	V_{PR}	1050	2137	V_{peak}
Input to Output Test Voltage, Method a[a] $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, t_m = 10s, Partial discharge < 5 pC	V_{PR}	896	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60s)	V_{IOTM}	6000	8000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.				
Case Temperature	T_S	150	175	°C
Input Current[b]	$I_{S,\ INPUT}$	150	230	mA
Output Power[b]	$P_{S,\ OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	Ω

a. Refer to the optocoupler section of the *Isolation and Control Components Designer's Catalog*, under Product Safety Regulations section, (IEC/EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

b. Refer to the following figure for dependence of P_S and I_S on ambient temperature.

NOTE: These optocouplers are suitable for *safe electrical isolation* only within the safety limit data. Maintenance of the safety limit data shall be ensured by means of protective circuits.

Table 5: Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units
Storage Temperature		T_S	–55	125	°C
Operating Temperature		T_A	–40	105	°C
Lead Soldering Cycle	Temperature		—	260	°C
	Time		—	10	s
Average Forward Input Current[a]		$I_{F(avg)}$	—	20	mA
Peak Forward Input Current[b] (50% duty cycle, 1-ms pulse width)		$I_{F(peak)}$	—	40	mA
Peak Transient Input Current (≤1 µs pulse width, 300 ps)		$I_{F(trans)}$	—	1	A
Reversed Input Voltage		V_R	—	5	V
Input Power Dissipation[c]		P_{IN}	—	36	mW
Output Power Dissipation[d]		P_O	—	45	mW
Average Output Current		$I_{O(AVG)}$	—	8	mA
Peak Output Current		$I_{O(PEAK)}$	—	16	mA
Supply Voltage		V_{CC}	–0.5	30	V
Output Voltage		V_O	–0.5	24	V
Solder Reflow Temperature Profile		See Package Outline Drawings.			

a. Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C.

b. Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C.

c. Derate linearly above 85°C free-air temperature at a rate of 0.9 mW/°C.

d. Derate linearly above 85°C free-air temperature at a rate of 1.2 mW/°C.

Table 6: Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	2.7	24	V
Input Current, High Level	I_{FH}	3	10	mA
Operating Temperature	T_A	–40	105	°C
Forward Input Voltage (OFF)	$V_{F\ (OFF)}$	—	0.8	V

Electrical Specifications (DC)

Over recommended temperature (T_A = –40°C to +105°C) and supply voltage (2.7V ≤ V_{CC} ≤ 24V). All typical specifications are at T_A = 25°C.

Table 7: Electrical Specifications (DC)

Parameter	Sym.	Part Number	Min.	Typ.	Max.	Units	Conditions			Figure
Current Transfer Ratio	CTR[a]	ACPL-M50L	100	140	200	%	T_A = 25°C	V_O = 0.4V	V_{CC} = 3.3V or 5V, I_F = 3 mA	8, 9
			80	—	—	%		V_O = 0.5V		
		ACPL-054L ACPL-W50L ACPL-K54L	93	130	200	%	T_A = 25°C	V_O = 0.4V	V_{CC}= 3.3V or 5V, I_F = 3 mA	8, 9
			53	—	—	%		V_O = 0.5V		
Logic Low Output Voltage	V_{OL}		—	0.2	0.4	V	T_A = 25°C	I_O = 3 mA	V_{CC} = 3.3V or 5V, I_F = 3 mA	
			—	0.2	0.5	V		I_O = 1.6 mA		
Logic High Output Current	I_{OH}		—	0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5V	I_F =0 mA	10, 11
			—	0.01	1			V_O = V_{CC} = 24V		
			—	—	80			V_O = V_{CC} = 24V		
Logic Low Supply Currentper Channel	I_{CCL}		—	36	100	µA		I_F = 3 mA, V_O = open, V_{CC} = 24V		
Logic High Supply Current per Channel	I_{CCH}		—	0.02	2	µA		I_F = 0 mA, V_O = open, V_{CC} = 24V		
Input Forward Voltage	V_F		—	1.5	1.8	V	T_A= 25°C	I_F = 3 mA		7
			—	1.5	1.95	V		I_F = 3 mA		
Input Reversed Breakdown Voltage	BV_R		5	—	—	V		I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		—	–1.6	—	mV/°C		I_F= 3 mA		
Input Capacitance	C_{IN}		—	77	—	pF		F = 1 MHz, V_F = 0		

a. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.

Switching Specifications (ACPL-M50L)

Over recommended operating (T_A = –40°C to 105°C), I_F = 3 mA, (2.7V ≤ V_{CC} ≤ 24V), unless otherwise specified.

Table 8: Switching Specifications (ACPL-M50L)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions		Fig.
Propagation Delay Time to Logic Low at Output	T_{PHL}	—	0.2	0.5	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 3.3V, R_L= 1.2 kΩ, C_L = 15 pF, V_{THHL} = 1.5V	26
		—	0.2	1	µs			12, 26
		—	0.22	0.5	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 5.0V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5V	26
		—	0.22	1	µs			14, 26
		—	0.33	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 24V, R_L = 10 kΩ, C_L = 15 pF, V_{THHL} = 1.5V	26
		—	0.33	1.3	µs			16, 26
Propagation Delay Time to Logic High at Output	T_{PLH}	—	0.38	0.8	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 3.3V, R_L = 1.2 kΩ, C_L = 15 pF, V_{THLH} = 2.0V	26
		—	0.38	1.2	µs			12, 26
		—	0.31	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F= 3 mA, V_{CC} = 5.0V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THLH} = 2.0V	26
		—	0.31	1	µs			14, 26
		—	0.3	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 24V, R_L = 10 kΩ, C_L = 15 pF, V_{THLH} = 2.0V	26
		—	0.3	1	µs			16, 26
Pulse Width Distortion[a]	PWD	—	0.18	0.8	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 3.3V, R_L = 1.2 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	26
		—	0.18	1.2	µs			26
		—	0.1	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 5.0V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	26
		—	0.1	1	µs			26
		—	0.1	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 24V, R_L = 10 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH}= 2.0V	26
		—	0.1	1	µs			26
Propagation Delay Difference Between Any Two Parts[b]	t_{psk}	—	0.18	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 3.3V, R_L = 1.2 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	
		—	0.1	0.6	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 5.0V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	
		—	0.1	0.6	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 24V, R_L = 10 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	
Common Mode Transient Immunity at Logic High Output[c]	$\|CM_H\|$	15	25	—	kV/µs	T_A = 25°C	V_{CM} = 1500V, I_F = 0 mA,, R_L = 1.2 kΩ or 1.9 kΩ, V_{CC} = 3.3V or 5V	27
Common Mode Transient Immunity at Logic Low Output[d]	$\|CM_L\|$	15	20	—	kV/µs	T_A= 25°C	V_{CM} = 1500V, I_F = 3 mA, R_L = 1.2 kΩ, V_{CC} = 5V	27
		10	15	—	kV/µs		V_{CM} = 1500V, I_F = 3 mA, R_L = 1.2 kΩ, V_{CC} = 3.3V	27

a. Pulse Width Distortion (PWD) is defined as $|t_{PHL} – t_{PLH}|$ for any given device.

b. The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)

c. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (that is, V_O > 2.0V).

d. Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, VCM to assure that the output will remain in a Logic Low state (that is, V_O < 0.8V).

Switching Specifications (ACPL-054L/W50L/K54L)

Over recommended temperature (T_A = –40°C to +105°C), supply voltage (2.7V ≤ V_{CC} ≤ 24V) unless otherwise specified.

Table 9: Switching Specifications (ACPL-054L/W50L/K54L)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions		Fig
Propagation Delay Time to Logic Low at Output	T_{PHL}	—	0.2	0.5	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 3.3V, R_L = 1.8 kΩ, C_L = 15 pF, V_{THHL} = 1.5V	26
		—	0.2	1	µs			13, 26
		—	0.22	0.5	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 5.0V, R_L = 2.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5V	26
		—	0.22	1	µs			15, 26
		—	0.33	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 24V, R_L = 14.8 kΩ, C_L = 15 pF, V_{THHL}= 1.5V	26
		—	0.33	1.3	µs			17, 26
Propagation Delay Time to Logic High at Output	T_{PLH}	—	0.38	0.8	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 3.3V, R_L = 1.8 kΩ, C_L =1 5 pF, V_{THLH} = 2.0V	26
		—	0.38	1.4	µs			13, 26
		—	0.31	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 5.0V, R_L = 2.9 kΩ, C_L = 15 pF, V_{THLH} = 2.0V	26
		—	0.31	1	µs			15, 26
		—	0.3	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 24V, R_L = 14.8 kΩ, C_L = 15 pF, V_{THLH} = 2.0V	26
		—	0.3	1	µs			17, 26
Pulse Width Distortion[a]	PWD	—	0.18	0.8	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 3.3V, R_L = 1.8 kΩ, C_L = 15 pF, V_{THHL}= 1.5V, V_{THLH} = 2.0V	26
		—	0.18	1.4	µs			26
		—	0.1	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F= 3 mA, V_{CC} =5.0V, R_L = 2.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	26
		—	0.1	1	µs			26
		—	0.1	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 24V, R_L = 14.8 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	26
		—	0.1	1	µs			26
Propagation Delay Difference Between Any Two Parts[b]	t_{psk}	—	0.18	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F= 3 mA, V_{CC} = 3.3V, R_L = 1.8 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	
		—	0.1	0.6	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 5.0V, R_L = 2.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	
		—	0.1	0.6	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty cycle = 50%, I_F = 3 mA, V_{CC} = 24V, R_L = 14.8 kΩ, C_L = 15 pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	
Common Mode Transient Immunity at Logic High Output[c]	$\|CM_H\|$	15	25	—	kV/µs	T_A = 25°C	V_{CM} = 1500V, I_F = 0 mA,, R_L = 1.8 kΩ or 2.9 kΩ, V_{CC} = 3.3V or 5V	27
Common Mode Transient Immunity at Logic Low Output[d]	$\|CM_L\|$	15	20	—	kV/µs	T_A= 25°C	V_{CM} = 1500V, I_F = 3 mA, R_L = 2.9 kΩ, V_{CC} = 5V	27
		15	20	—	kV/µs		V_{CM} = 1500V, I_F = 3 mA, R_L = 1.8 kΩ, V_{CC} = 3.3V	27

a. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.

b. The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)

c. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (this is, V_O > 2.0V).

d. Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, VCM to assure that the output will remain in a Logic Low state (that is, V_O < 0.8V).

Package Characteristics

All typical at T_A = 25°C.

Table 10: Package Characteristics

Parameter	Symbol	Part Number	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage[a,b]	V_{ISO}	ACPL-M50L/054L	3750	—	—	V_{rms}	RH ≤ 50%, t = 1 min., T_A = 25°C
		ACPL-W50L/K54L	5000	—	—		
Input-Output Resistance[a]	R_{I-O}		—	1014	—	Ω	V_{I-O} = 500 Vdc
Input-Output Capacitance[a]	C_{I-O}		—	0.6	—	pF	f = 1 MHz, T_A = 25°C
Input-Input Insulation Leakage Current[c]	I_{I-I}		—	0.005	—	µA	RH ≤ 45%, t = 5s, V_{I-I} = 500 Vdc
Input-Input Resistance[c]	R_{I-I}		—	1011	—	Ω	
Input-Input Capacitance[c]	C_{I-I}		—	0.25	—	pF	f = 1 MHz

a. Device considered a two terminal device: pins 1 and 3 shorted together and pins 4, 5, and 6 shorted together for ACPL-M50L, pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together for ACPL-054L/K54L, pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together for ACPL-W50L.

b. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{rms} for 1 second for ACPL-M50L/054L and ≥ 6000 V_{rms} for 1 second for ACPL-W50L/K54L (leakage detection current limit, I_{I-O} ≤ 5 mA).

c. Measured between pins 1 and 2 shorted together and pins 3 and 4 shorted together for ACPL-054L/K54L.

Figure 7: Input Current vs. Forward Voltage

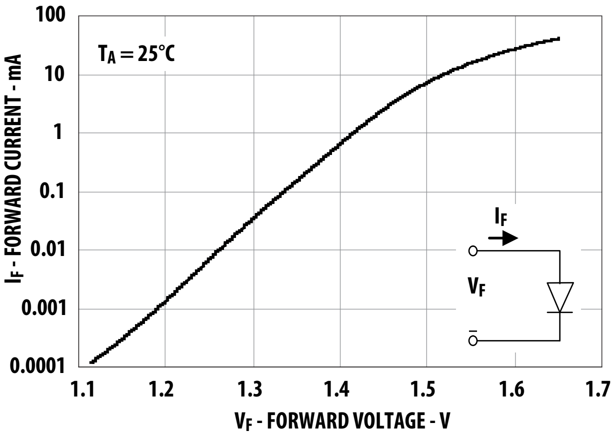


Figure 8: Typical Current Transfer Ratio vs. Temperature

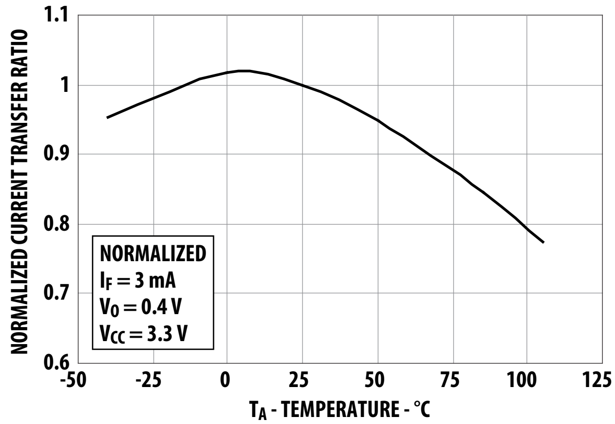


Figure 9: Typical Current Transfer Ratio vs. Temperature

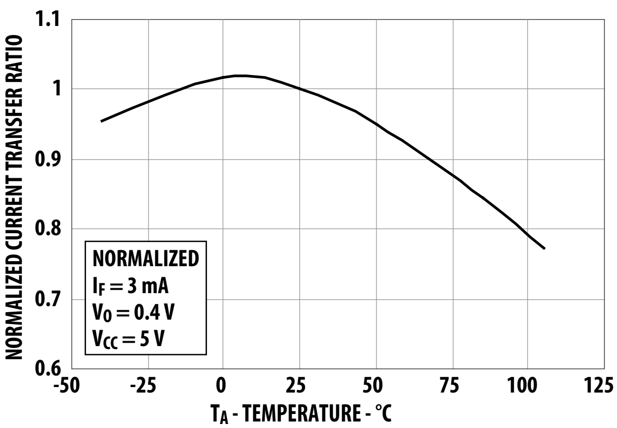


Figure 10: Typical Logic High Output Current vs. Temperature

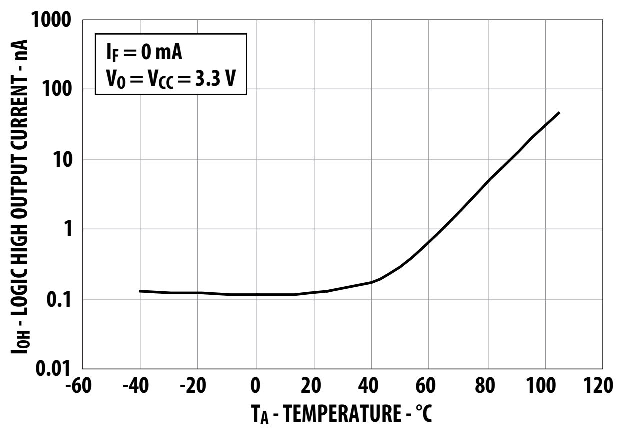


Figure 11: Typical Logic High Output Current vs. Temperature

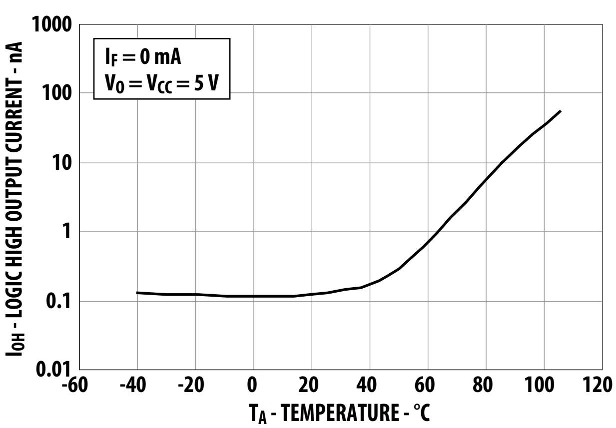


Figure 12: Typical Propagation Delay vs. Temperature (ACPL-M50L)

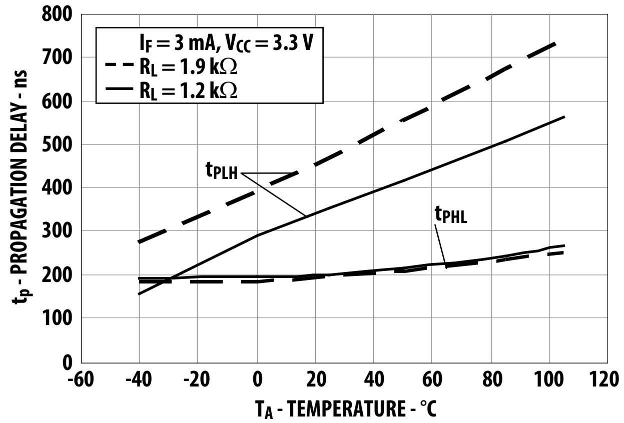


Figure 13: Typical Propagation Delay vs. Temperature (ACPL-054L/W50L/K54L)

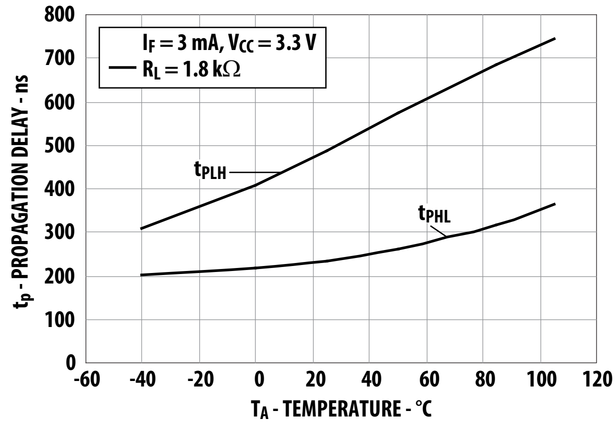


Figure 14: Typical Propagation Delay vs. Temperature (ACPL-M50L)

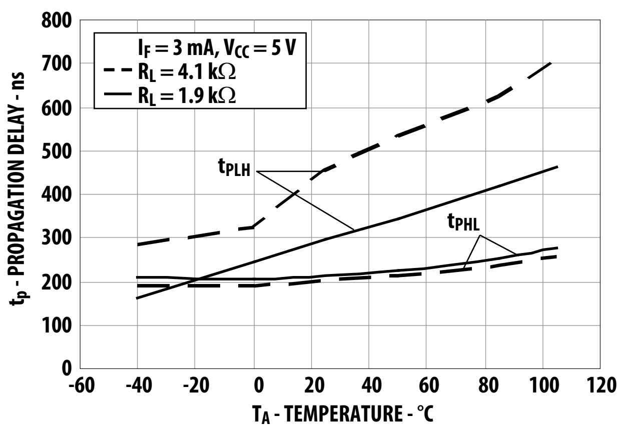


Figure 15: Typical Propagation Delay vs. Temperature (ACPL-054L/W50L/K54L)

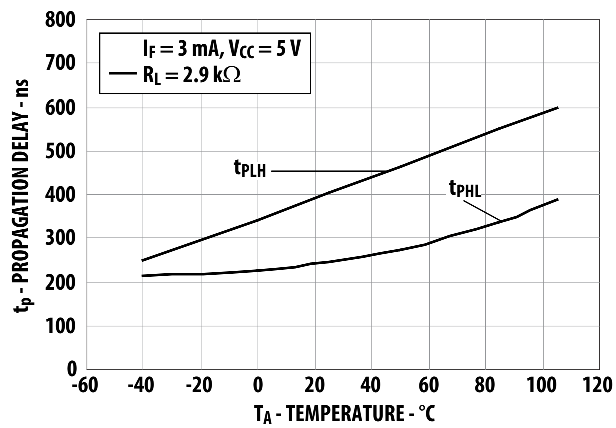


Figure 16: Typical Propagation Delay vs. Temperature (ACPL-M50L)

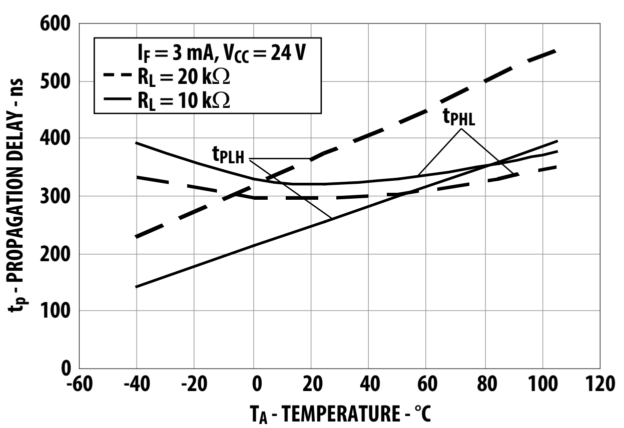


Figure 17: Typical Propagation Delay vs. Temperature (ACPL-054L/W50L/K54L)

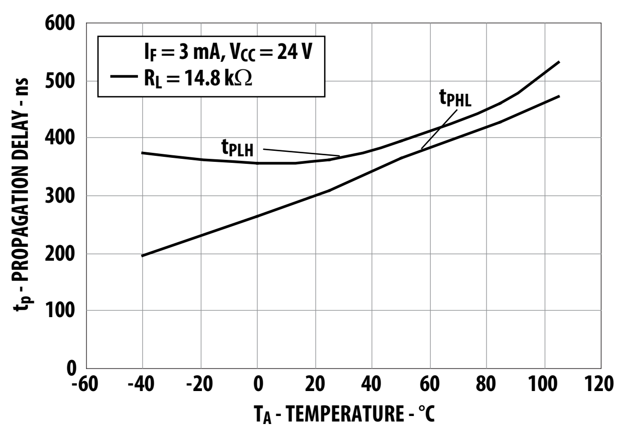


Figure 18: Typical Propagation Delay vs. Load Resistance

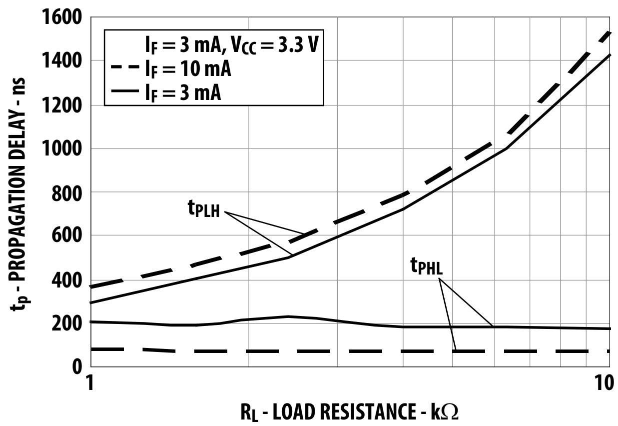


Figure 19: Typical Propagation Delay vs. Load Resistance

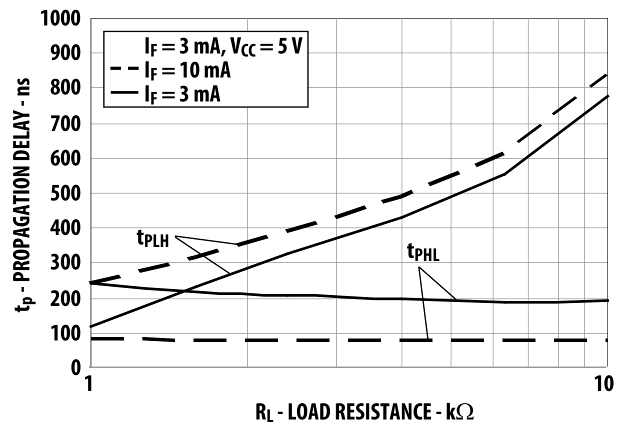


Figure 20: Typical Propagation Delay vs. Load Capacitance (ACPL-M50L)

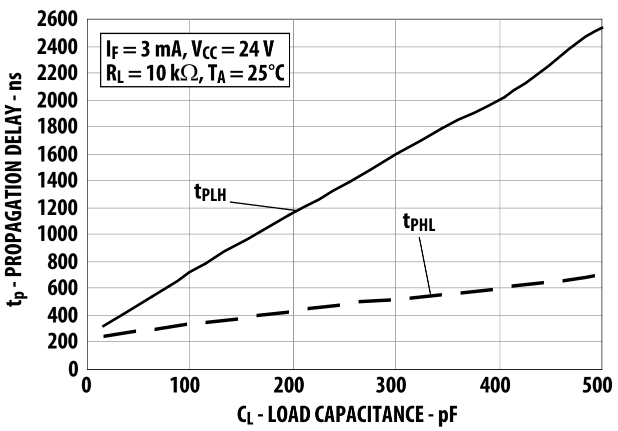


Figure 21: Typical Propagation Delay vs. Load Capacitance (ACPL-054L/W50L/K54L)

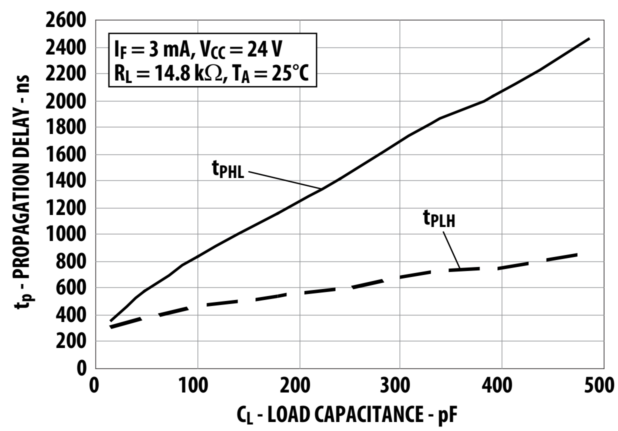


Figure 22: Typical Propagation Delay vs. Supply Voltage (ACPL-M50L)

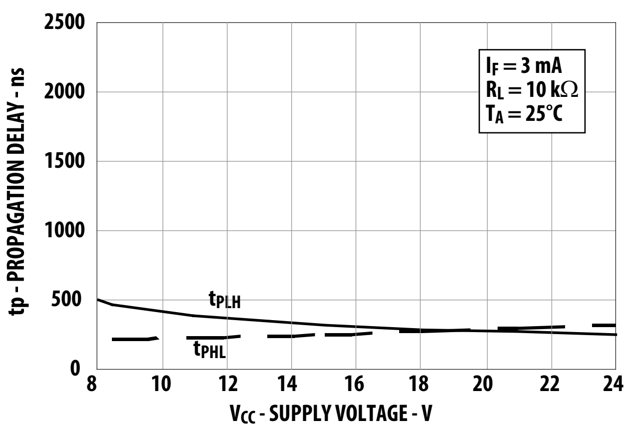


Figure 23: Typical Propagation Delay vs. Supply Voltage (ACPL-054L/W50L/K54L)

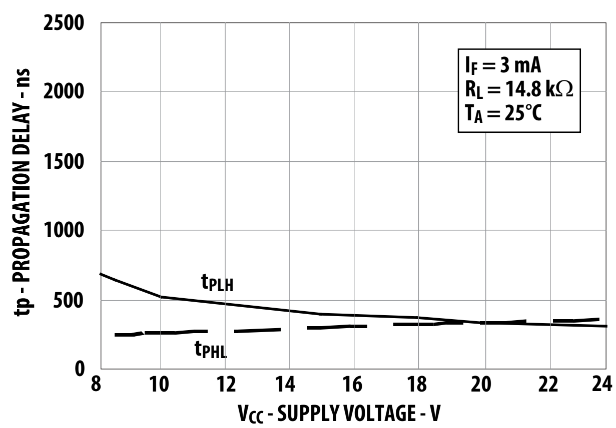


Figure 24: Typical Propagation Delay vs. Supply Current (ACPL-M50L)

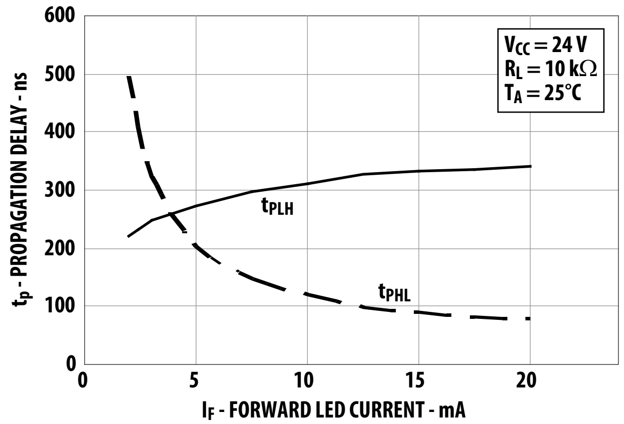


Figure 25: Typical Propagation Delay vs. Supply Current (ACPL-054L/W50L/K54L)

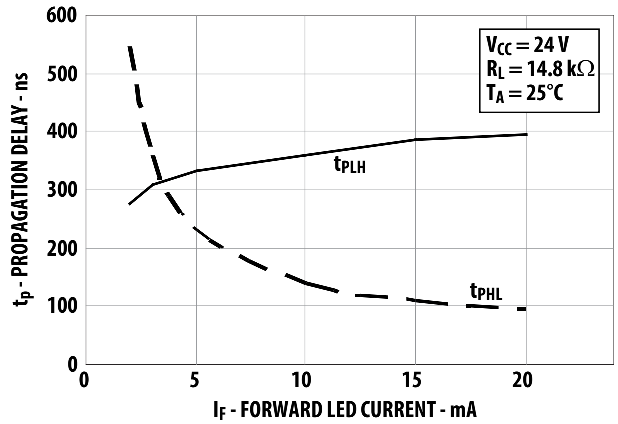


Figure 26: Switching Test Circuits

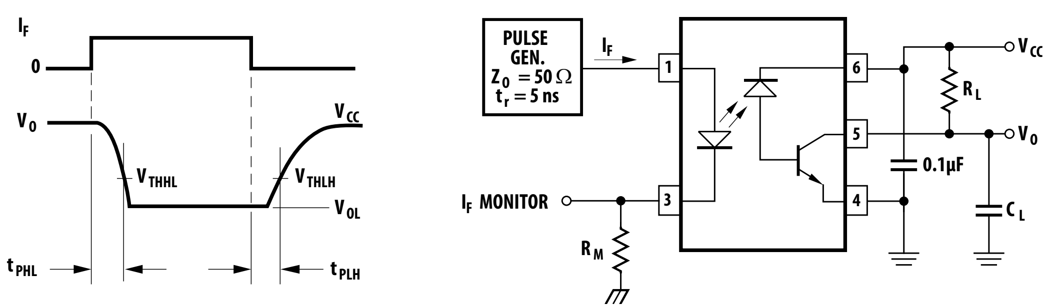


Figure 27: Test Circuit for Transient Immunity and Typical Waveforms

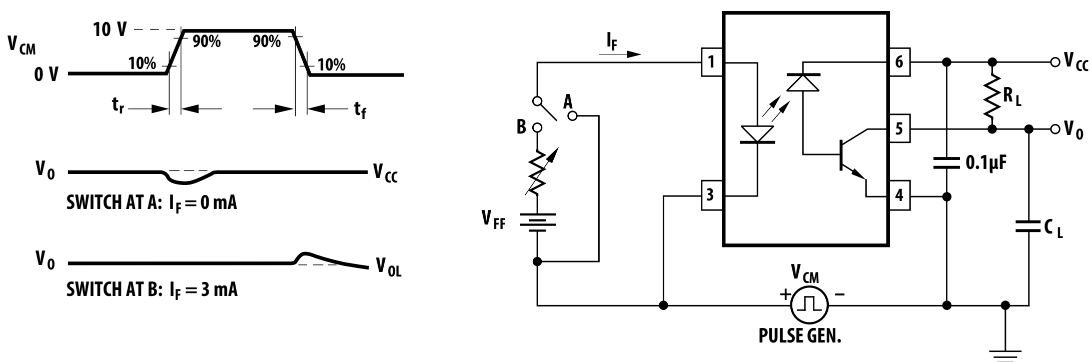


Figure 28: Current Transfer Ratio vs. Input Current

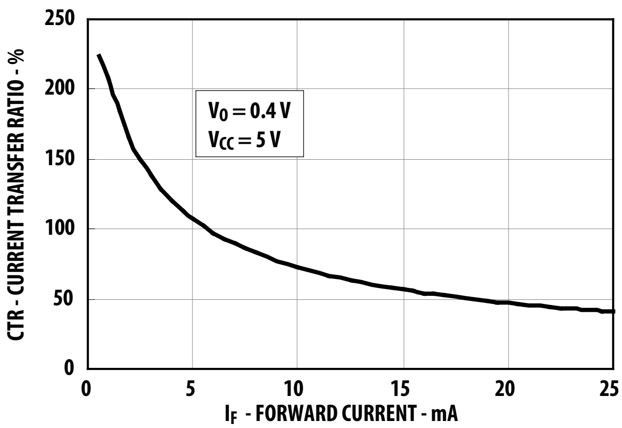


Figure 29: DC Pulse Transfer Characteristic