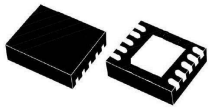
ST1S50

4 A monolithic synchronous step-down switching converter with high efficiency at light load

Datasheet - production data



VFDFPN10

Features

- 4 A output current
- 4.0 V to 18 V input voltage
- Output voltage adjustable from 0.8 V to 0.88 x V_{IN}
- 500 kHz switching frequency
- High efficiency at light load
- Programmable soft-start and enable
- Integrated 95 mΩ and 69 mΩ power MOSFETs
- All ceramic capacitor
- Power Good
- Cycle-by-cycle current limiting
- Short-circuit protection
- VFDFPN10 3 x 3 x 1 mm - 10 L

Applications

- Point of load for: STB, TVs, gateway
- Solid state disk drive, Blu-ray, DVD
- µP/ASIC/DSP/FPGA core and I/O supplies

Description

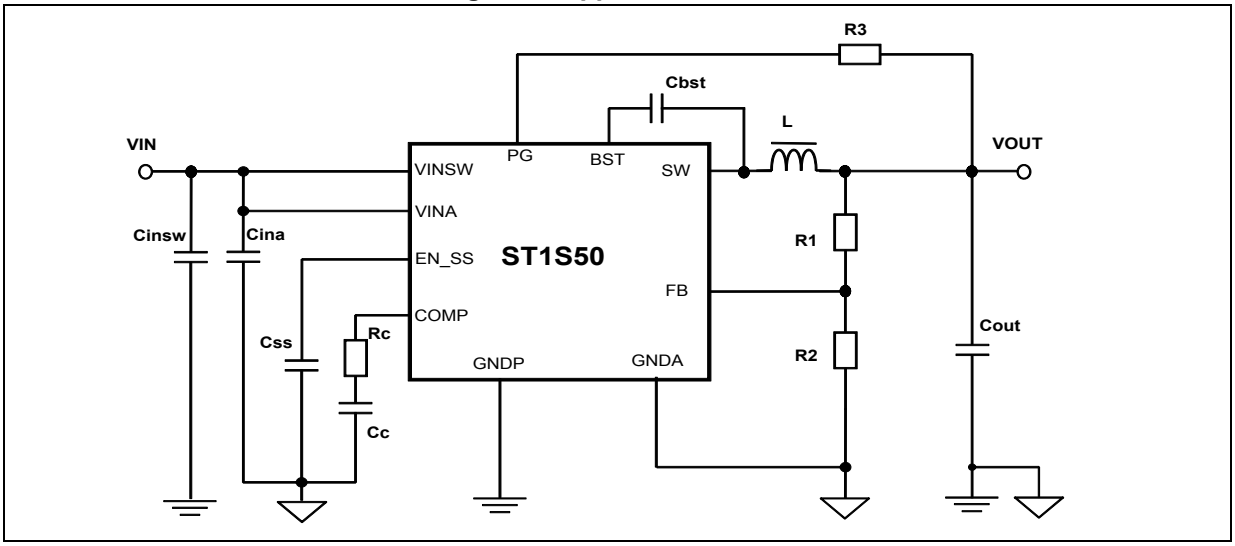
The ST1S50 device is a 500 kHz fixed frequency PWM synchronous step-down regulator. The ST1S50 operates from 4.0 V to 18 V input, while it regulates an output voltage as low as 0.8 V and up to 0.88 x V_{IN}.

The ST1S50 device integrates a 95 mΩ high-side switch and a 69 mΩ synchronous rectifier allowing very high efficiency with very low output voltages.

The peak current mode control with a special PFM mode enables high efficiency at a light load.

The ST1S50 device is available in a VFDFPN10 3 x 3 x 1 mm - 10 leads package.

Figure 1. Application circuit



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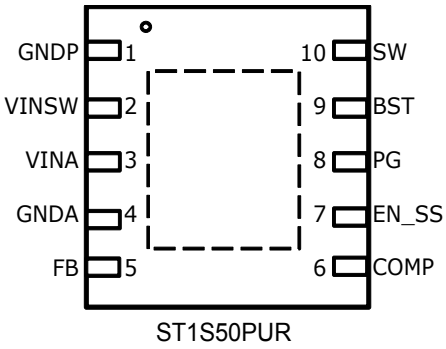
Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

No.	Type	Description
1	GNDP	Power ground. This pin has to be connected to the exposed pad of the device as shown in *Figure 11: PCB layout on page 22*.
2	VINSW	Power input voltage
3	VINA	Input voltage
4	GNDA	Ground. This pin has to be connected to the exposed pad of the device as shown in *Figure 11: PCB layout*.
5	FB	Feedback input. Connecting the output voltage directly to this pin the output voltage is regulated at 0.8 V. To have higher regulated voltages an external resistor divider is required from the V_{OUT} to the FB pin.
6	COMP	Error amplifier output; the RC network connected to this pin stabilizes the loop.
7	EN_SS	Enable and soft-start pin: the capacitor connected to this pin programmes the soft-start time.
8	PG	Power Good pin
9	BST	Bootstrap pin: the capacitor connected between SW and BST allows the proper high-side switch turn on.
10	SW	Output switching pin.

2 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{INSW}	Power input voltage	-0.3 to 20	V
V_{INA}	Input voltage	V_{INSW} +/- 0.3	
V_{COMP}, V_{EN_SS}, V_{FB}	Analog pin	-0.3 to 3	
V_{SW}	Output switching voltage	-1 to V_{IN}	
V_{PG}	Power Good	-0.3 to V_{INA} + 0.3 V	
VBST	Bootstrap pin (T_J from -25 °C to 150 °C)	-0.3 to 22	
	Bootstrap pin (T_J from -40 °C to -25 °C)	-0.3 to 21	
I_{FB}	FB current	-1 to +1	mA
P_{TOT}	Power dissipation at T_A < 60 °C	1.5	W
T_{OP}	Operating junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-55 to 150	°C

3 Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
R_{thJA}	Maximum thermal resistance junction ambient(1)	VFDFPN10	60	°C/W

1. Package mounted on the demonstration board.

4 Electrical characteristics

T_J = 25 °C, V_{CC} = 12 V, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
V_{IN}	Operating input voltage range	(1)	4		18	V
		(2)	4		17	
V_{INON}	Turn on V_{IN} threshold				3.5	
V_{INOFF}	Turn off V_{IN} threshold		3.0			
R_{DSON}-HS	High-side switch on resistance	I_{SW} = 750 mA		95		mΩ
R_{DSON}-LS	Low-side switch on resistance	I_{SW} = 750 mA		69		mΩ
I_{LIM}	Maximum limiting current	(3)		5.6		A
Oscillator						
F_{SW}	Switching frequency		400	500	600	kHz
D_{MAX}	Maximum duty cycle	(3)	88			%
Dynamic characteristics						
V_{FB}	Feedback voltage		0.784	0.8	0.816	V
		(4)	0.776	0.8	0.824	
Error amplifier						
Gm	Trans-conductance	(3)		250		µS
R_O	Output resistance	(3)		240		MΩ
DC characteristics						
I_Q	Quiescent current	Duty cycle = 0, no load V_{FB} = 1.2 V		500	600	µA
I_{QST-BY}	Total standby quiescent current	OFF			10	µA
I_{FB}	FB bias current			100		nA
Enable						
V_{EN}	EN threshold voltage	Device ON level	0.340			V
		Device OFF level			0.130	
Power Good						
PG	PG threshold			91		% V_{FB}
	PG threshold hysteresis			90		mV
	PG output voltage low	Isink = 6 mA open drain			400	mV

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
Soft-start						
I_{SS}	Soft-start current	V_{SS} = 0.2 V	150	350	550	nA
		V_{SS} = 1 V	4.4	5.4	6.4	µA
		V_{SS} = 2 V		0.5		mA
Protections(3)						
T_{SHDN}	Thermal shutdown			150		°C
	Hysteresis			15		
V_{FF2}	FB threshold voltage enabling the short-circuit protection			0.3		V
V_{FF1}	FB threshold voltage enabling the $f_{sw}/2$			0.734		
V_{OVP}	Overvoltage threshold on FB			880		mV
	Hysteresis			80		

1. Specification referred to T_J from -25 to +125 °C.
2. Specification referred to T_J from -40 to -25 °C.
3. Guaranteed by design.
4. Specification referred to T_J from -40 to +125 °C. Specification in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.

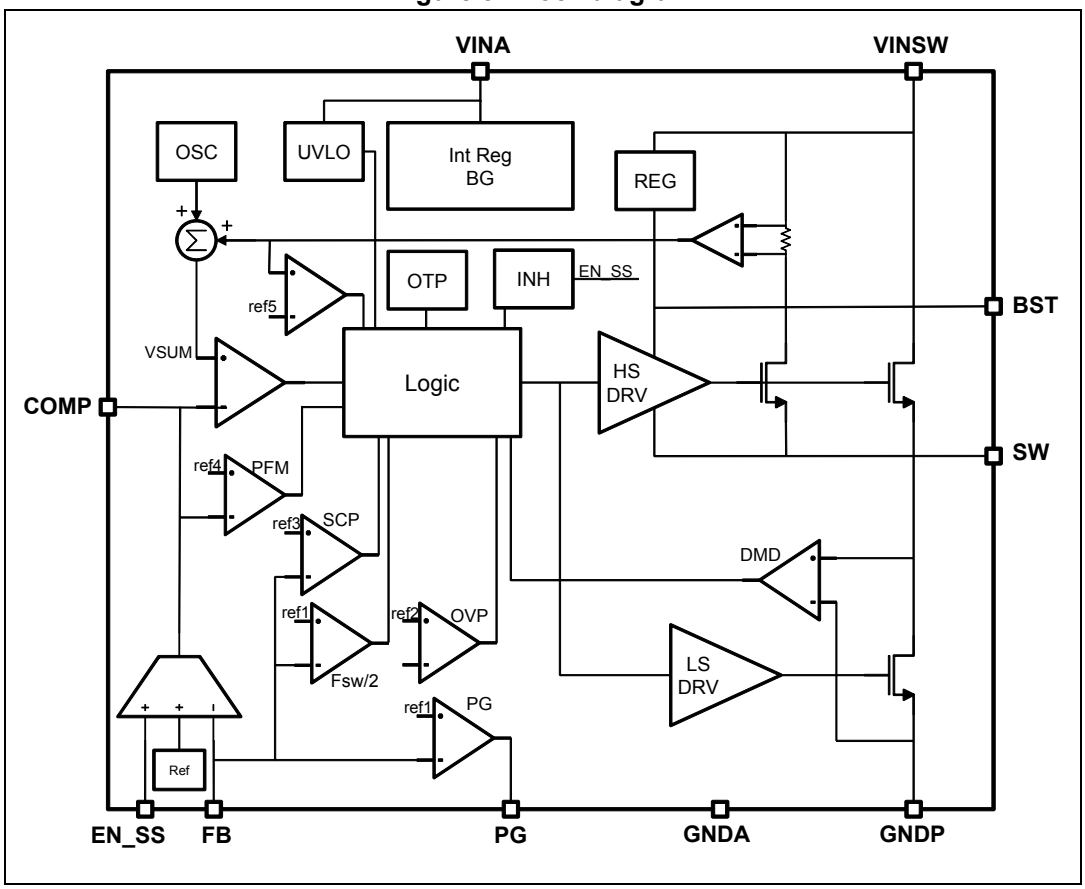
5 Functional description

The ST1S50 device is based on a “peak current mode”, constant frequency control. The output voltage V_{OUT} is sensed by the feedback pin (FB) compared to an internal reference (0.8 V) providing an error signal that, compared to the output of the current sense amplifier, controls the ON and OFF time of the power switches.

The main internal blocks are shown in the block diagram in *Figure 3*. They are:

- A fully integrated oscillator that provides the internal clock and the ramp for the slope compensation avoiding subharmonic instability.
- The adjustable soft-start circuitry to limit an inrush current during the start-up phase source a current on an external RC network.
- The trans-conductance error amplifier.
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switches.
- The drivers for embedded high-side and low-side N-channel power MOSFET switches.
- The high-side current sensing block.
- The low-side current sense to implement diode emulation.
- A voltage monitor circuitry (UVLO) that checks the input and internal voltages.
- A thermal shutdown block, to prevent a thermal runaway.

Figure 3. Block diagram



5.1 Programmable soft-start and enable

The soft-start is essential to assure a correct and safe startup of the step-down converter. It avoids an inrush current surge and makes the output voltage increases monothonically.

The soft-start is performed by ramping the non-inverting input (V_{REF}) of the error amplifier from 0 V to 0.8 V. The ramp of the reference voltage can be programmed selecting the soft-start capacitor that is connected between the EN_SS pin and ground.

The device sources 5 µA (typical) in the RC network, ramping the EN_SS pin logarithmically from 0.34 V to 1.7 V. The reference of the error amplifier ramps, starting when the EN_SS pin voltage is equal to 0.7 V (typ.), up from 0 V to 0.8 V accordingly.

Once the soft-start time ends, the EN_SS pin is internally tied to 3.3 V to avoid injecting noise.

5.2 Error amplifier and control loop stability

The error amplifier compares the FB pin voltage with the internal 0.8 V reference and it provides the error signal to be compared with the output of the current sense circuitry, that is the high-side power MOSFET current. Comparing the output of the error amplifier and the peak inductor current implements the peak current mode control loop.

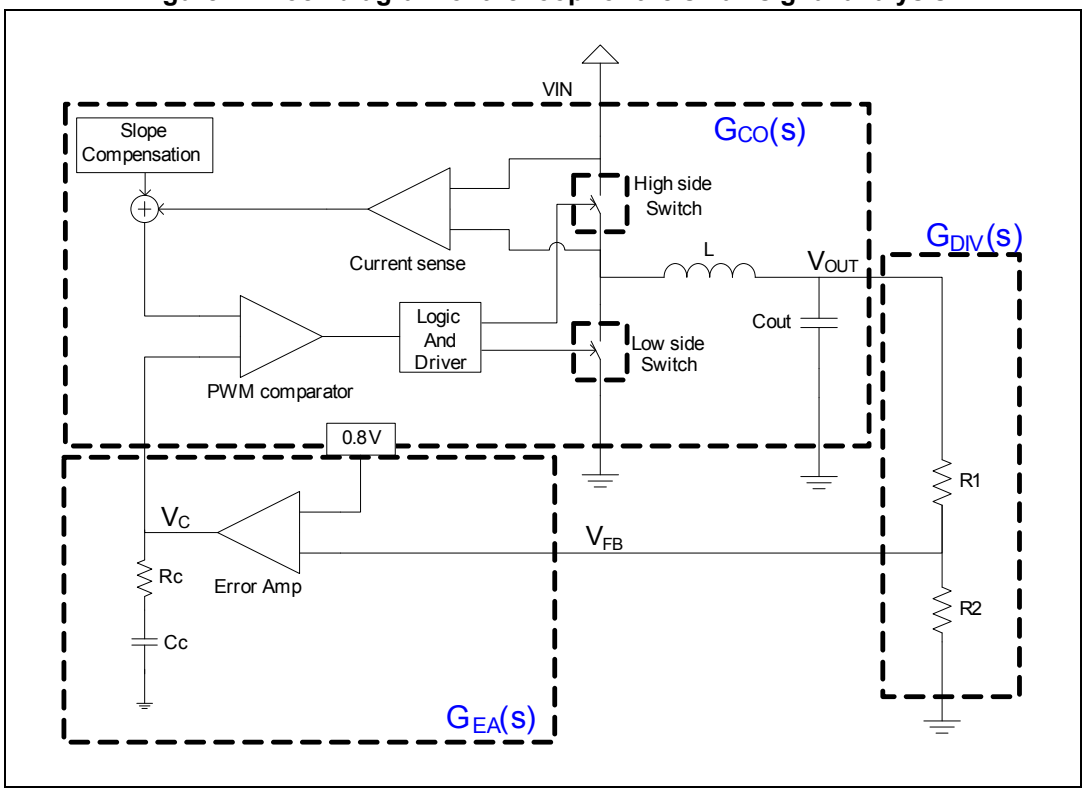
The error amplifier is a trans-conductance amplifier (OTA). The uncompensated characteristics are listed in *Table 5*.

Table 5. Error amplifier characteristics

Description	Value
DC gain	95 dB
Gm	250 µA/V
R_O	240 MΩ

In *Figure 4* is shown the simple small signal model for the peak current mode control loop.

Figure 4. Block diagram of the loop for the small signal analysis



Three main terms can be identified to obtain the loop transfer function:

1. From control (output of E/A) to output, $G_{CO}(s)$.
2. From output (V_{OUT}) to FB pin, $G_{DIV}(s)$.
3. From FB pin to control (output of E/A), $G_{EA}(s)$.

The transfer function from control to output $G_{CO}(s)$ results:

Equation 1

$$G_{CO}(s) = \frac{R_{LOAD}}{R_i} \cdot \frac{1}{1 + \frac{R_{out} \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \cdot F_H(s)$$

where R_{LOAD} represents load resistance, R_i the equivalent sensing resistor of the current sense circuitry, ω_p the single pole introduced by the LC filter and ω_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

Equation 2

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}}$$

Equation 3

$$\omega_p = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}}$$

where:

Equation 4

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = V_{pp} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \cdot R_i \end{cases}$$

S_n represents the ON time slope of the sensed inductor current, S_e the slope of the external ramp (V_{PP} peak-to-peak amplitude) that implements the slope compensation to avoid subharmonic oscillations at a duty cycle over 50%.

The sampling effect contribution $F_H(s)$ is:

Equation 5

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}}$$

where:

Equation 6

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]}$$

and

Equation 7

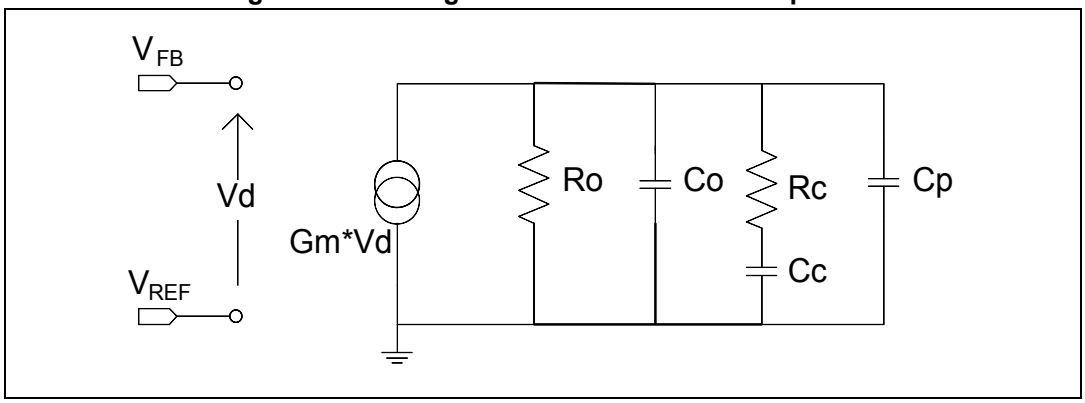
$$\omega_n = \pi \cdot f_{SW}$$

The resistor to adjust the output voltage gives the term from the output voltage to the FB pin. $G_{DIV}(s)$ is:

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2}$$

The transfer function from the FB to the COMP (output of E/A) introduces the singularities (poles and zeroes) to stabilize the loop. In *Figure 5* is shown the small signal model of the error amplifier with the internal compensation network.

Figure 5. Small signal model for the error amplifier



R_C and C_C are the compensation network, R_O represents output resistance of the error amplifier, Co represents the internal low frequency pole of the error amplifier.

R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability and can be neglected.

So $G_{EA}(s)$ results:

Equation 8

$$G_{EA}(s) = \frac{G_{EA0} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_c \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1}$$

Where $G_{EA} = G_m \cdot R_o$

The poles of this transfer function are (if $C_c >> C_0 + C_P$):

Equation 9

$$f_{P\,LF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

Equation 10

$$f_{P\,HF} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 11

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

So closing the loop, the loop gain $G_{LOOP}(s)$ is:

Equation 12

$$G_{LOOP}(s) = G_{CO}(s) \cdot G_{DIV}(s) \cdot G_{EA}(s)$$

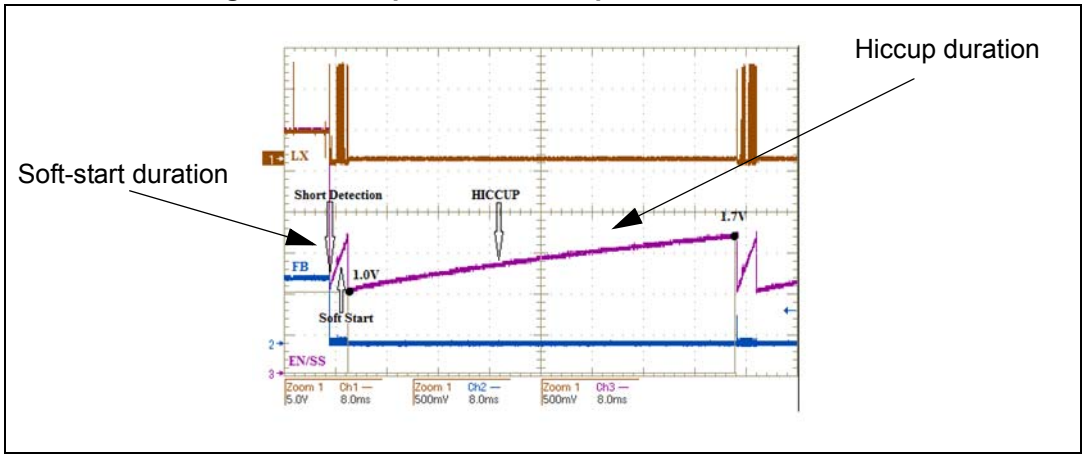
To stabilize the loop and then to have the proper phase margin (> 45°) with the requested bandwidth, R_C and C_C can be selected as described in *Section 6.4 on page 18*.

5.3 Overcurrent protection

The ST1S50 device implements the pulse-by-pulse overcurrent protection. The peak current is sensed through the high-side power MOSFET and when it exceeds the overcurrent threshold the high-side is immediately turned off and the low-side conducts the inductor current for the rest of the clock period.

During overload condition, since the duty cycle is not set by the control loop but it is limited by the overcurrent threshold, the output voltage drops out of regulation. If the FB falls below 0.734 V the switching frequency is divided by two to keep the inductor current limited around the I_{LIM} value.
The overload condition is allowed for 256 continuous clock cycles. In case the overload condition persists for longer than 257 clock cycles, the HICCUP protection is triggered: the device realizes a soft-start cycle and then, if the overcurrent protection is still triggered, stops switching activities and remains disabled for the HICCUP times. Then it restarts with a soft-start cycle.

Figure 6. Hiccup behavior with persistent short-circuit



The HICCUP time depends on the selected value of the soft-start capacitor, considering R_{SS} = 4.7 MΩ fixed value (see *Section 6.5 on page 19*).

Equation 13

$$T_{HICCUP}[s] = C_{SS}[F] \times 2853934$$

If the feedback falls below 0.3 V before the 256 clock cycle, as a symptom of a short-circuit, the HICCUP protection is triggered and the converter reacts as described above in this section.

The HICCUP is disabled during the startup to allow the V_{OUT} to start up properly in case of a big output capacitor requiring a high extra current to be charged.

5.4 Power Good function

The PG pin output is an open drain MOSFET. The PG is pulled low when the FB pin voltage is lower than 91% of the nominal internal reference (0.8 V). The PG pin is V_{IN} compatible.

5.5 Hysteretic thermal shutdown

The thermal shutdown block generates a signal that turns off the power stage if the junction temperature goes above 150 ^{o}C. Once the junction temperature goes back to about 130 ^{o}C, the device restarts in normal operation.

6 Application information

6.1 Input capacitor selection

The capacitor connected to the input has to be capable to support the maximum input operating voltage and the maximum RMS input current required by the device. The input capacitor is subject to a pulsed current, the RMS value of which is dissipated over its ESR, affecting the overall system efficiency.

So the input capacitor must have an RMS current rating higher than the maximum RMS input current and an ESR value compliant with the expected efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 14

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where I_o is the maximum DC output current, D is the duty cycle, η is the efficiency. Considering $\eta = 1$, this function has a maximum at D = 0.5 and it is equal to $I_o/2$.

The peak-to-peak voltage across the input capacitor can be calculated as:

Equation 15

$$V_{PP} = \frac{I_O}{C_{IN} \cdot F_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right] + ESR \cdot I_O$$

where ESR is equivalent series resistance of the capacitor.

Given the physical dimension, ceramic capacitors can meet well the requirements of the input filter sustaining a higher input RMS current than electrolytic / tantalum types. In this case the equation of C_{IN} as a function of the target peak-to-peak voltage ripple (V_{PP}) can be written as follows:

Equation 16

$$C_{IN} = \frac{I_O}{V_{PP} \cdot F_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

neglecting the small ESR of ceramic capacitors.

Considering η = 1, this function has its maximum in D = 0.5, thus, given the maximum peak-to-peak input voltage (V_{PP_MAX}), the minimum input capacitor (C_{IN_MIN}) value is:

Equation 17

$$C_{IN\_MIN} = \frac{I_O}{2 \cdot V_{PP\_MAX} \cdot F_{SW}}$$

Typically C_{IN} is dimensioned to keep the maximum peak-to-peak voltage ripple in the order of 1% of V_{INMAX}.

In *Table 6* some multi-layer ceramic capacitors suitable for this device are reported.

Table 6. Input MLCC capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)
Murata	GRM31	10	25
	GRM55	10	25
TDK	C3225	10	25

A ceramic bypass capacitor, as close as possible to the VINA pin, so that additional parasitic ESR and ESL are minimized, is suggested in order to prevent instability on the output voltage due to noise. The value of the bypass capacitor can go from 330 nF to 1 µF.

6.2 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor. So the minimum inductance value to have the expected current ripple has to be selected. The rule to fix the current ripple value is to have a ripple at 20% - 40% of the output current.

In the continuous current mode (CCM), the inductance value can be calculated by *Equation 18*:

Equation 18

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF}$$

Where T_{ON} is the conduction time of the high-side switch and T_{OFF} is the conduction time of the low-side switch (in CCM, $F_{SW} = 1 / (T_{ON} + T_{OFF})$). The maximum current ripple, given the V_{OUT}, is obtained at maximum T_{OFF}, that is at a minimum duty cycle (see *Section 6.1* to calculate minimum duty). So fixing ΔI_L= 20% to 30% of the maximum output current, the minimum inductance value can be calculated:

Equation 19

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{MAX}} \cdot \frac{1 - D_{MIN}}{F_{SWMIN}}$$

where F_{SWMIN} is the minimum switching frequency, according to *Table 4 on page 6*.

The peak current through the inductor is given by:

Equation 20

$$I_{L,PK} = I_O + \frac{\Delta I_L}{2}$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher is the inductor value, the higher is the average output current that can be delivered, without reaching the current limit.

In *Table 7* some inductor part numbers are listed.

Table 7. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	XPL7030	2.2 to 4.7	6.8 to 10.5
	XAL40xx, 50xx, 60xx	1.5 to 6.8	> 5
Würth	WE-HC/HCA	3.3 to 4.7	7 to 11
	WE-TPC typ XLH	3.6 to 6.2	4.5 to 6.4
	WE-PD type L	10	5.6
TDK	RLF7030T	2.2 to 4.7	4 to 6

6.3 Output capacitor selection

The current in the output capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge or discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be calculated starting from the current ripple obtained by the inductor selection.

Equation 21

$$\Delta V_{OUT} = ESR \cdot \Delta I_{MAX} + \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}}$$

For a ceramic (MLCC) capacitor the capacitive component of the ripple dominates the resistive one. Whilst for an electrolytic capacitor the opposite is true.

Since the compensation network is internal, the output capacitor should be selected in order to have a proper phase margin and then a stable control loop.

The equations of *Section 5.2 on page 9* will help to check loop stability given the application conditions, the value of the inductor and of the output capacitor.

In *Table 8* some capacitor series are listed.

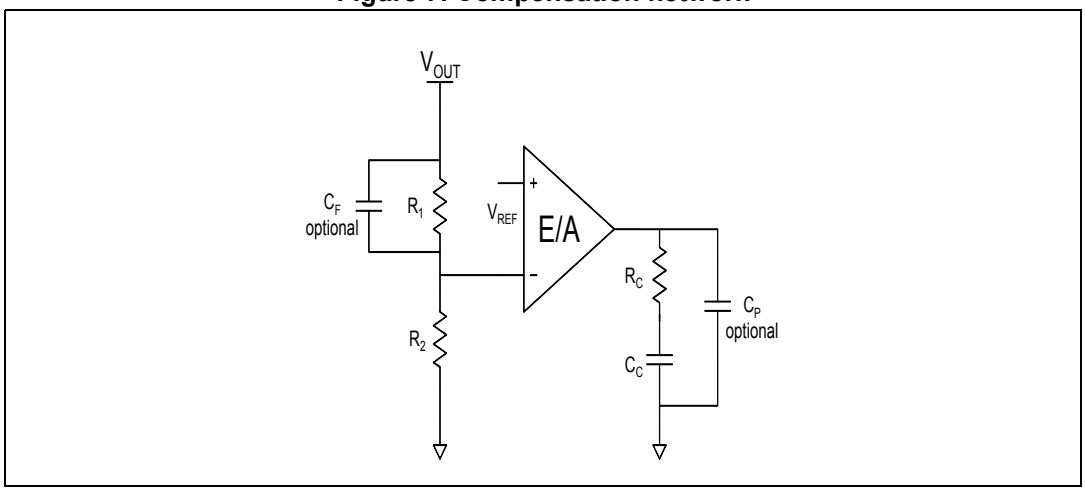
Table 8. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
Murata	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
Panasonic	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

6.4 Compensation network selection

The compensation network must be chosen to have a phase margin higher than 45° given the application condition (V_{IN}, V_{OUT}, L, C_{OUT}) and the requested bandwidth. The larger is the bandwidth, the faster is the loop response to the load transient. Maximum allowed bandwidth is one fourth/fifth of the switching frequency (that is 100 - 120 kHz).

Figure 7. Compensation network



Starting from the target bandwidth (f_{BW}) the compensation network values can be calculated to have a stable loop response basing *Equation 22* and *Equation 23*.

Given the target bandwidth f_{BW}, the resistor R_C results:

Equation 22

$$R_C = \frac{2\pi \cdot f_{BW} \cdot V_{OUT} \cdot C_{OUT} \cdot R_i}{G_m \cdot V_{REF}}$$

where C_{OUT} is the output capacitor (actual value properly derated according to the applied DC voltage), R_i is the equivalent sensing resistor of the current sense circuitry (0.3 V/A), *Gm* is the error amplifier trans-conductance (250 µS) and V_{REF} is the internal reference, 0.8 V.

The capacitor C_C has to be designed to place the zero of the compensation network (f_Z) at the frequency of the power stage pole ($f_P \cong 1 / (2\pi R_{LOAD} C_{OUT})$).

Equation 23

$$C_C = \frac{R_{LOAD} \cdot C_{OUT}}{R_C}$$

The capacitor C_P is optional and it can be used to cancel the zero from the ESR of the output capacitor.

The capacitor C_F can be used to have phase boost adding a further zero close to the crossover frequency. C_F inserts also a pole at very high frequency, usually negligible. The phase boost effect decreases as the V_{OUT} decreases.

6.5 Soft-start capacitor selection

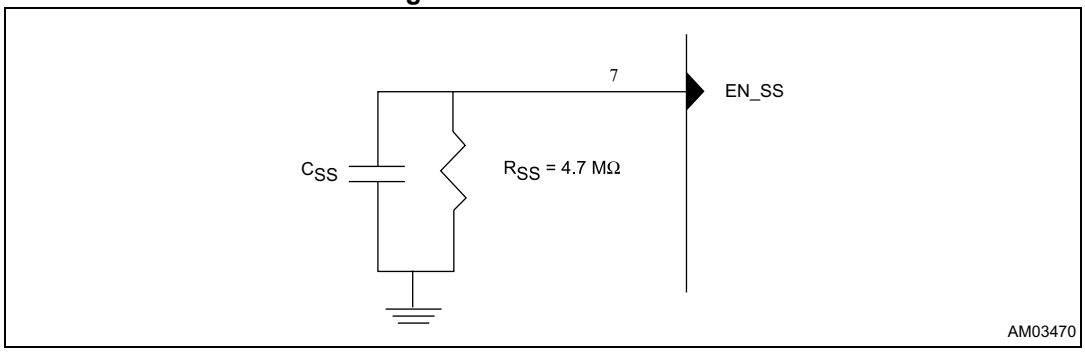
6.5.1 Reset time

The soft-start capacitor allows managing the correct rising of the output voltage to prevent a high inrush current. Moreover it introduces a reset time in case the device is disabled and re-enabled through UVLO.

The re-enable through UVLO, after disable though UVLO, must happen after a certain reset time to assure the proper startup. This reset time is a function of the soft-start capacitor.

A 4.7 MΩ resistor value in parallel to the soft-start capacitor is strongly recommended in order to predict the reset time.

Figure 8. Soft-start circuit

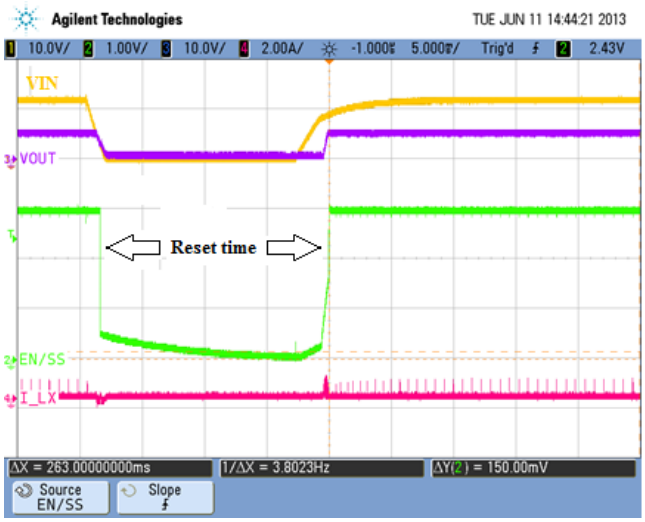


The reset time is so calculated:

Equation 24

$$t_{RESET} = C_{SS} \cdot 4.7M\Omega \cdot 1.97$$

Figure 9. Reset time



6.5.2 C_{SS} value

When the EN_SS pin is tied to ground the device is disabled. When the EN_SS is released a current is a source in the soft-start capacitor connected to the pin. No minimum soft-start time is assured in case of no capacitor connected.

The FB voltage starts to rise when the EN/SS voltage is equal to 0.7 V (typ.), start threshold, and reaches the V_{REF}voltage when the EN/SS voltage is equal to 1.5 V (typ.), stop threshold.

Considering the 4.7 MΩ resistor value (see *Section 6.5.1*), the soft-start capacitor can be determined by:

Equation 25

$$C_{SS}[F] = \frac{T_{SS}[s]}{154873}$$

Where T_{SS} is the target soft-start time.

A delay can be observed from EN_SS release and the real V_{OUT} rising since the EN_SS voltage needs to ramp from zero to the enable threshold (340 mV) with a pull-up current of 350 nA. The delay results:

Equation 26

$$t_{DELAY} = \frac{0.340V \cdot C_{SS}}{350nA}$$

6.6 Thermal dissipation

The thermal design is important to prevent the thermal shutdown of the device if junction temperature goes above 150 °C. The three different sources of losses within the device are:

a) conduction losses due to ON resistance of the high-side switch (R_{HS}) and low-side switch (R_{LS}); these are equal to:

Equation 27

$$P_{COND} = R_{HS} \cdot I_{OUT}^{2} \cdot D + R_{LS} \cdot I_{OUT}^{2} \cdot (1 - D)$$

Where *D* is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between the V_{OUT} and V_{IN}, but actually it is slightly higher to compensate the losses of the regulator.

b) switching losses due to the high-side power MOSFET turn ON and OFF; these can be calculated as:

Equation 28

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot Fsw = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

Where T_{RISE} and T_{FALL} are the overlap times of the voltage across the high-side power switch (V_{DS}) and the current flowing into it during turn ON and turn OFF phases, as shown in *Figure 10*. T_{SW} is the equivalent switching time. For this device the typical value for the equivalent switching time is 20 ns.

c) Quiescent current losses, calculated as:

Equation 29

$$P_Q = V_{IN} \cdot I_Q$$

where I_Q is the quiescent current (I_Q = 500 µA maximum).

The junction temperature T_J can be calculated as:

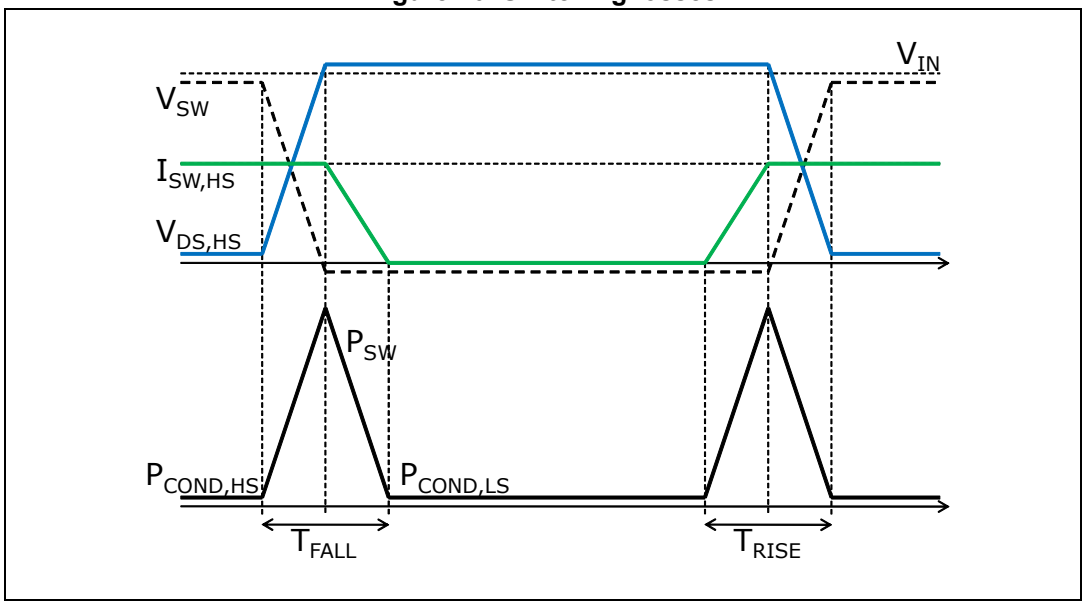
Equation 30

$$T_J = T_A + Rth_{JA} \cdot P_{TOT}$$

Where T_A is the ambient temperature and P_{TOT} is the sum of the power losses just seen.

R_{thJA} is equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The R_{thJA} measured on the demonstration board described in *Section 6.7* is about 60 °C/W for the VFDFPN10 package.

Figure 10. Switching losses



6.7 Layout consideration

The PC board layout of the switching DC/DC regulator is very important to minimize the noise injected in high impedance nodes, to reduce interferences generated by the high switching current loops and to optimize the reliability of the device.

In order to avoid EMC problems, the high switching current loops have to be as short as possible. In the buck converter two are the high switching current loops: during the ON-time, the pulsed current flows through the input capacitor, the high-side power switch, the inductor and the output capacitor; during the OFF-time, through the low-side power switch, the inductor and the output capacitor.

An input capacitor connected to VINSW has to be placed as close as possible to the device, to avoid spikes on VINSW due to the stray inductance and the pulsed input current.

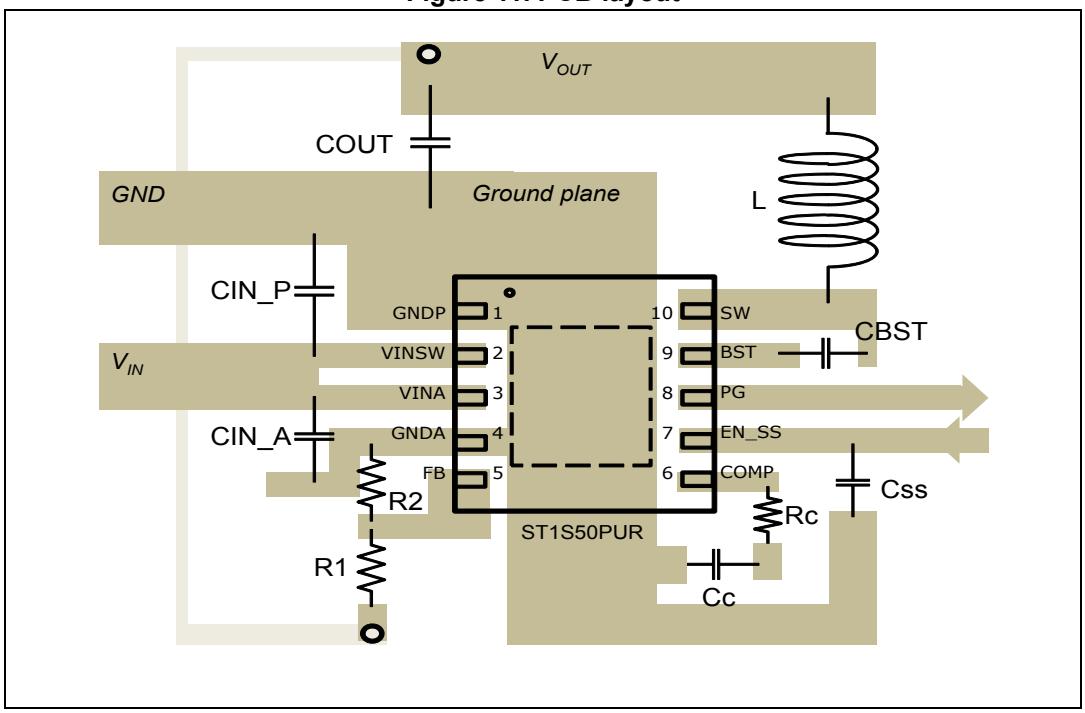
In order to prevent dynamic unbalance between VINSW and VINA, the trace connecting the VINA pin to the input must be derived from VINSW.

The feedback pin (FB) connected to an external resistor divider is a high impedance node. The interferences can be minimized by routing the feedback node with a very short trace and as far away as possible from high current paths

A single point connection from signal ground to power ground is suggested.

Thanks to the exposed pad of the device, the ground plane helps to reduce thermal resistance junction to ambient; so a large ground plane, soldered to the exposed pad, enhances the thermal performance of the converter allowing high power conversion.

Figure 11. PCB layout



6.8 Demonstration board

Figure 12. Demonstration board schematic

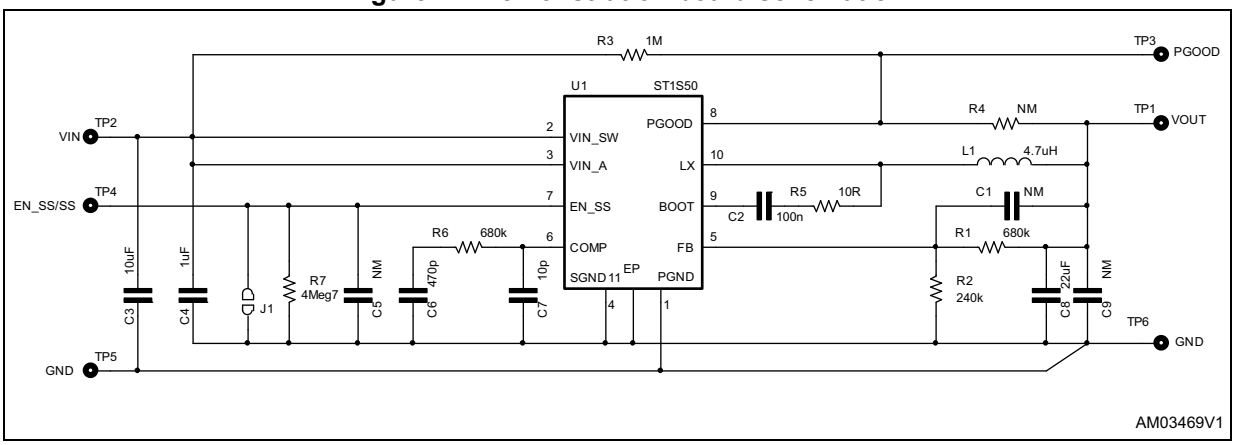


Table 9. Component list

Reference	Part number	Description	Manufacturer
U1	ST1S50PUR		STMicroelectronics®
L1	XAL6060-472MEC	4.7 µH, Isat = 10.5 A, Irms = 8 A	Coilcraft
C1		Optional	
C2		100 nF, 25 V	
C3	GRM31CR61E106KA12L	10 µF, 25 V, X5R, 1206	Murata
C4	GRM21BR71E225KA73L	2.2 µF, 25 V, X7R, 0805	Murata
C5		22 nF, 50 V, 0603	
C6		470 pF, 50 V, 0603	
C7		10 pF, 50 V, 0603	
C8	GRM32ER61E226KE15L	22 µF, 25 V, X5R, 1210	Murata
R1		16 kΩ, 1%, 0.1 W, 0603	
R2		5.1 kΩ, 1%, 0.1 W, 0603	
R3		N.M.	
R4		1 MΩ, 1%, 0.1 W, 0603	
R5		10 Ω, 1%, 0.1 W, 0603	
R6		68 kΩ, 1%, 0.1 W, 0603	
R7		4.7 MΩ, 1%, 0.1 W, 0603	

7 Typical characteristics

Figure 13. Efficiency vs. I_{OUT} - V_{IN} = 12 V

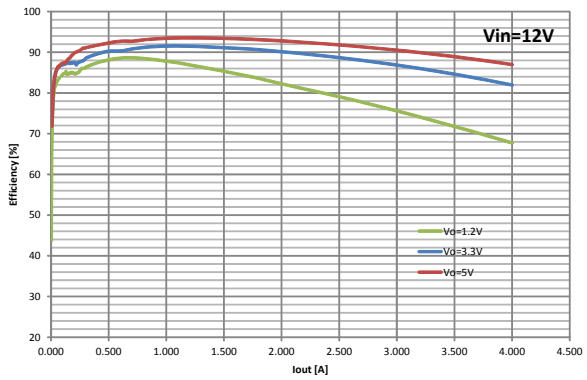


Figure 14. Efficiency vs. I_{OUT} - V_{IN} = 5 V

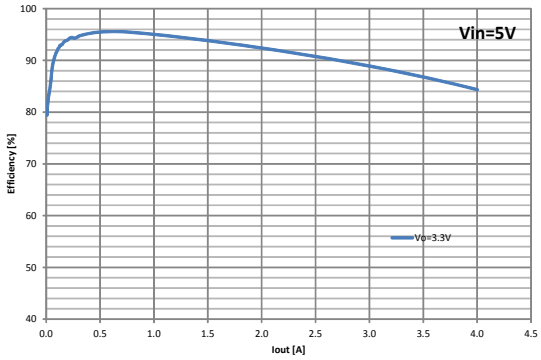


Figure 15. Start-up releasing EN_SS pin

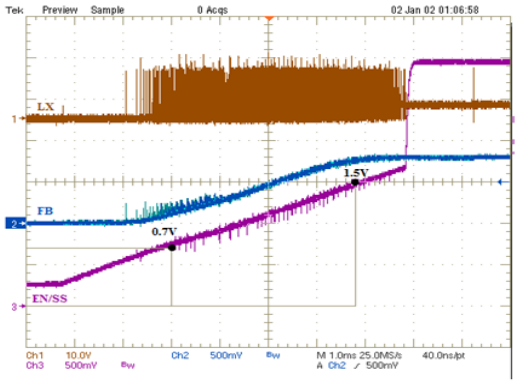


Figure 16. Long overload condition

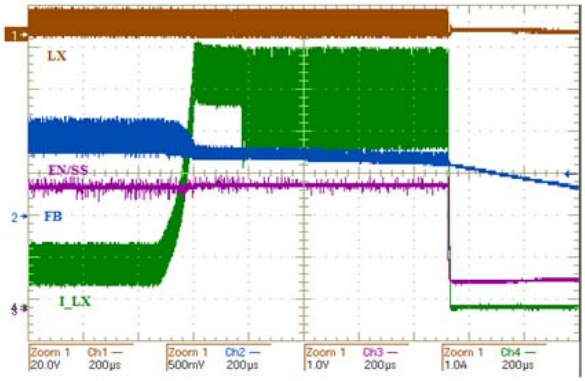
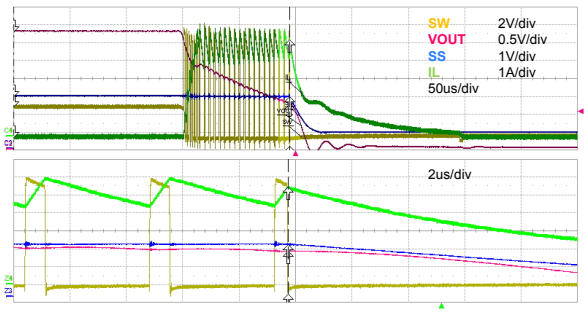


Figure 17. Quick overload



V_{IN}=12V, V_{OUT}=3.3V, quick overcurrent V_{FB} falls below 0.3V

Figure 18. Start-up with shorted V_{OUT}

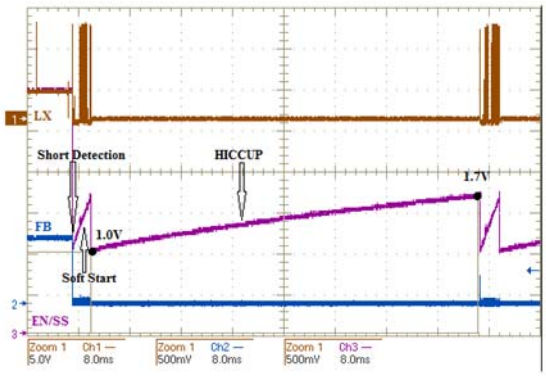
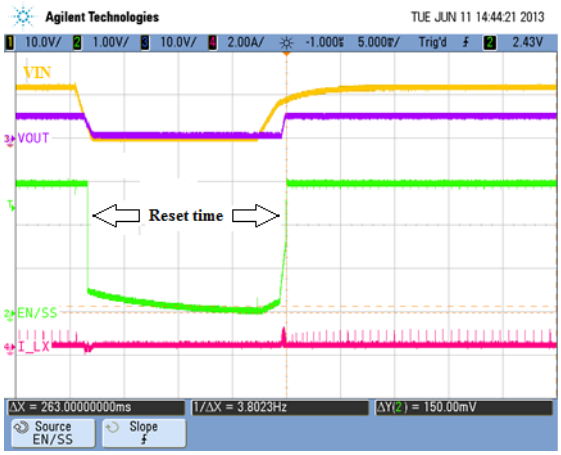


Figure 19. Reset time



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

VFDFPN10 package information

Figure 20. VFDFPN10 (3 x 3 x 1 mm) package outline (bottom view)

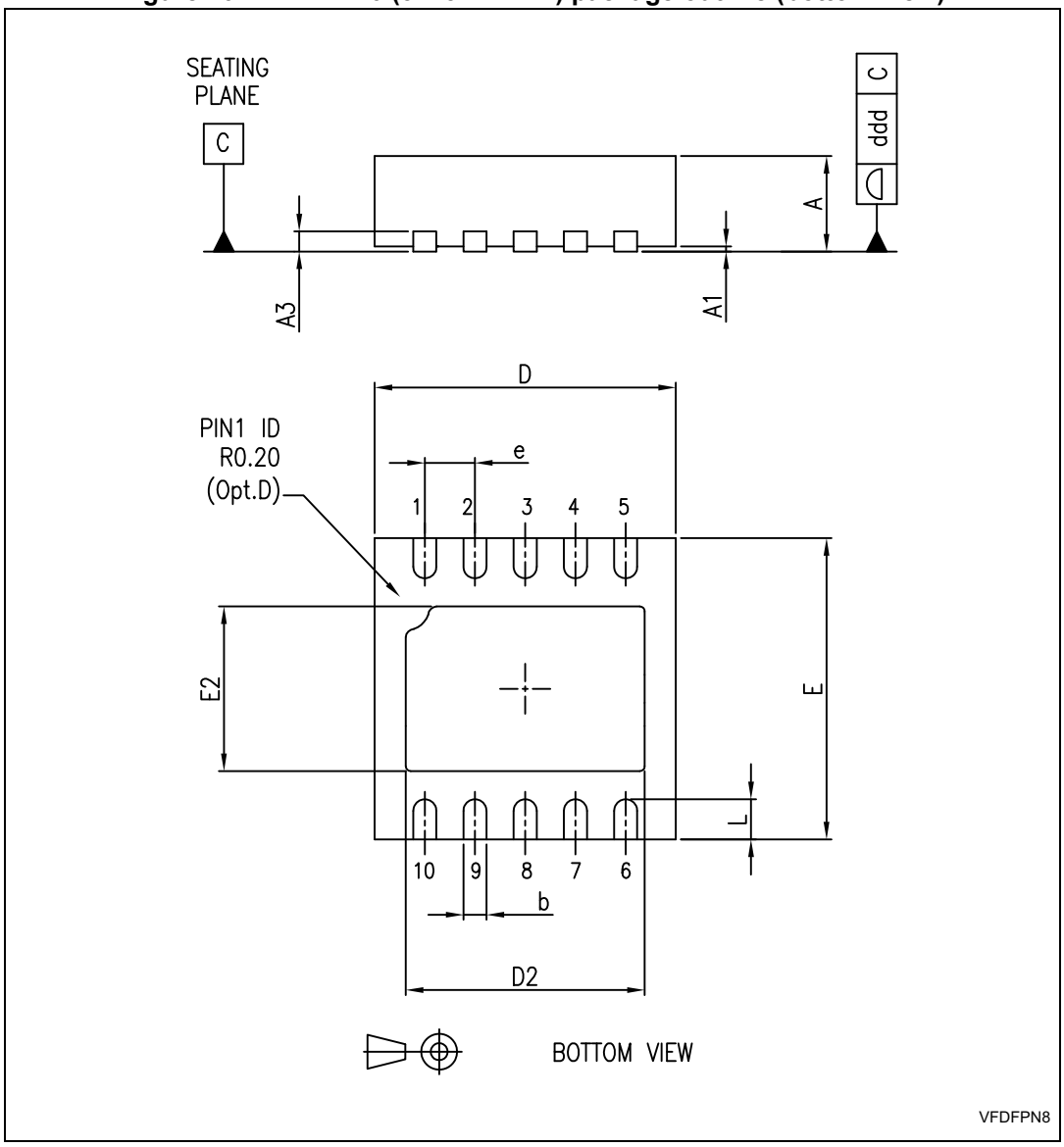


Table 10. VFDFPN10 (3 x 3 x 1 mm) package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D		3.00	
D2	2.234	2.384	2.484
E		3.00	
E2	1.496	1.646	1.746
e		0.50	
L	0.30	0.40	0.50
ddd		0.05	

9 Order code

Table 11. Ordering information

Order code	Package	Packing
ST1S50PUR	VFDFPN10 3 x 3 x 1 mm - 10L	Tape and reel

10 Revision history

Table 12. Document revision history

Date	Revision	Changes
18-Dec-2013	1	Initial release.
24-Feb-2014	2	Replaced label “preliminary data” by “production data” on page 1.
01-Jul-2014	3	Updated *Table 1: Pin description on page 4* (updated “Description” of pins: 1 GNDP and 4 GNDA). Updated *Figure 12* (replaced by new figure). Updated *Table 11* (added “Packing” column).
23-Mar-2015	4	Replaced package name VFDFPN8 by VFDFPN10 in the whole document. Minor modifications throughout document.