19-2272; Rev 0; 1/02

Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

General Description

The single MAX4091, dual MAX4092, and quad MAX4094 operational amplifiers combine excellent DC accuracy with Rail-to-Rail® operation at the input and output. Since the common-mode voltage extends from V_{CC} to V_{EE}, the devices can operate from either a single supply (2.7V to 6V) or split supplies (±1.35V to ±3V). Each op amp requires less than 130µA of supply current. Even with this low current, the op amps are capable of driving a 1kΩ load, and the input-referred voltage noise is only 12nV/√Hz. In addition, these op amps can drive loads in excess of 2000pF.

The precision performance of the MAX4091/MAX4092/MAX4094 combined with their wide input and output dynamic range, low-voltage, single-supply operation, and very low supply current, make them an ideal choice for battery-operated equipment, industrial, and data acquisition and control applications. In addition, the MAX4091 is available in space-saving 5-pin SOT23, 8-pin µMAX, and 8-pin SO packages. The MAX4092 is available in 8-pin µMAX and SO packages, and the MAX4094 is available in 14-pin TSSOP and 14-pin SO packages.

Applications

- Portable Equipment
- Battery-Powered Instruments
- Data Acquisition and Control
- Low-Voltage Signal Conditioning

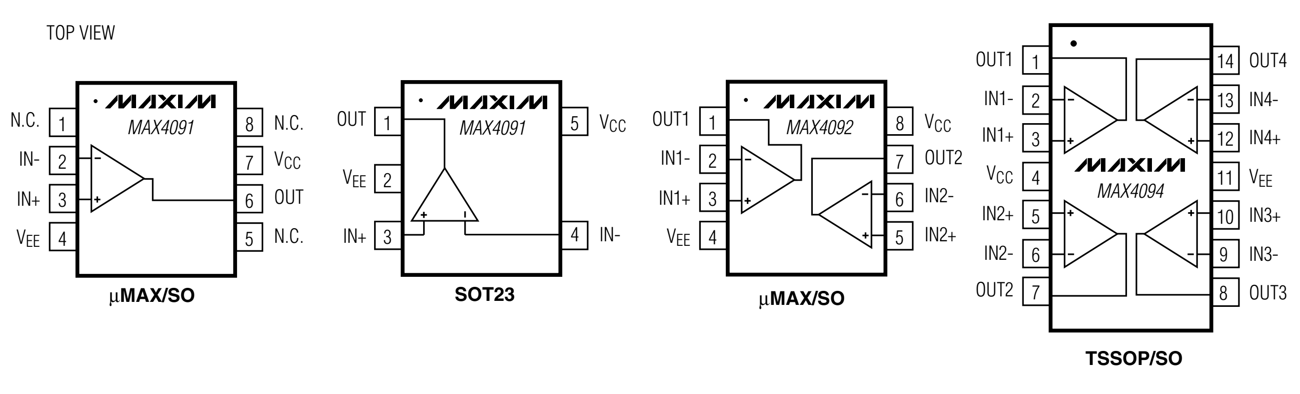
Features

- ♦ **Low-Voltage, Single-Supply Operation (2.7V to 6V)**
- ♦ **Beyond-the-Rails™ Inputs**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **30µV Offset Voltage**
- ♦ **Rail-to-Rail Output Swing with 1kΩ Load**
- ♦ **Unity-Gain Stable with 2000pF Load**
- ♦ **165µA (max) Quiescent Current Per Op Amp**
- ♦ **500kHz Gain-Bandwidth Product**
- ♦ **High Voltage Gain (115dB)**
- ♦ **High Common-Mode Rejection Ratio (90dB) and Power-Supply Rejection Ratio (100dB)**
- ♦ **Temperature Range (-40°C to +125°C)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4091AUK-T	-40°C to +125°C	5 SOT23-5
MAX4091ASA	-40°C to +125°C	8 SO
MAX4091AUA	-40°C to +125°C	8 µMAX
MAX4092ASA	-40°C to +125°C	8 SO
MAX4092AUA	-40°C to +125°C	8 µMAX
MAX4094AUD	-40°C to +125°C	14 TSSOP
MAX4094ASD	-40°C to +125°C	14 SO

Pin Configurations/Functional Diagrams



Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.
Beyond-the-Rails is a trademark of Maxim Integrated Products, Inc.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})..7V
Common-Mode Input Voltage..........(V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Differential Input Voltage ....±(V_{CC} - V_{EE})
Input Current (IN+, IN-) ....±10mA
Output Short-Circuit Duration
OUT shorted to GND or V_{CC}.................................Continuous
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C)...........571mW
8-Pin SO (derate 5.88mW/°C above +70°C)...............471mW
8-Pin μMAX (derate 4.1mW/°C above +70°C) 330mW
14-Pin SO (derate 8.33mW/°C above +70°C).............667mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C) 727mW
Operating Temperature Range ....-40°C to +125°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 6V, V_{EE} = GND, V_{CM} = 0, V_{OUT} = V_{CC}/2, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Voltage Range	V_{CC}	Inferred from PSRR test		2.7		6.0	V
Supply Current	I_{CC}	V_{CM} = V_{CC}/2	V_{CC} = 2.7V		115	165	μA
			V_{CC} = 5V		130	185	
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} to V_{CC}			0.03	1.4	mV
Input Bias Current	I_B	V_{CM} = V_{EE} to V_{CC}			20	180	nA
Input Offset Current	I_{OS}	V_{CM} = V_{EE} to V_{CC}			0.2	7	nA
Input Common-Mode Range	V_{CM}	Inferred from CMRR test		V_{EE} - 0.05		V_{CC} + 0.05	V
Common-Mode Rejection Ratio	CMRR	(V_{EE} - 0.05V) ≤ V_{CM} ≤ (V_{CC} + 0.05V)		71	90		dB
Power-Supply Rejection Ratio	PSRR	2.7V ≤ V_{CC} ≤ 6V		86	100		dB
Large-Signal Voltage Gain (Note 1)	A_{VOL}	V_{CC} = 2.7V, R_L = 100kΩ 0.25V ≤ V_{OUT} ≤ 2.45V	Sourcing	83	105		dB
			Sinking	81	105		
		V_{CC} = 2.7V, R_L = 1kΩ 0.5V ≤ V_{OUT} ≤ 2.2V	Sourcing	91	105		
			Sinking	78	90		
		V_{CC} = 5.0V, R_L = 100kΩ 0.25V ≤ V_{OUT} ≤ 4.75V	Sourcing	87	115		
			Sinking	83	115		
		V_{CC} = 5.0V, R_L = 1kΩ 0.5V ≤ V_{OUT} ≤ 4.5V	Sourcing	97	110		
			Sinking	84	100		
Output Voltage Swing High (Note 1)	V_{OH}	$\|V_{CC} - V_{OUT}\|$	R_L = 100kΩ		15	69	mV
			R_L = 1kΩ		130	210	
Output Voltage Swing Low (Note 1)	V_{OL}	$\|V_{OUT} - V_{EE}\|$	R_L = 100kΩ		15	70	mV
			R_L = 1kΩ		80	220	
AC CHARACTERISTICS							
Gain-Bandwidth Product	GBWP	R_L = 100kΩ, C_L = 100pF			500		kHz
Phase Margin	ϕ_M	R_L = 100kΩ, C_L = 100pF			60		degrees
Gain Margin		R_L = 100kΩ, C_L = 100pF			10		dB
Slew Rate	SR	R_L = 100kΩ, C_L = 15pF			0.20		V/μs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.7V to 6V, V_{EE} = GND, V_{CM} = 0, V_{OUT} = V_{CC}/2, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Noise Voltage Density	e_N	f = 10kHz		12		nV/√Hz
Input-Noise Current Density		f = 10kHz		1.5		pA/√Hz
Noise Voltage (0.1Hz to 10Hz)				16		μV_{RMS}
Total Harmonic Distortion Plus Noise	THD + N	f = 1kHz, R_L = 10kΩ, C_L = 15pF, A_V = 1, V_{OUT} = $2V_{P-P}$		0.003		%
Capacitive-Load Stability	C_{LOAD}	A_V = 1		2000		pF
Settling Time	t_S	To 0.1%, 2V step		12		µs
Power-On Time	t_{ON}	V_{CC} = 0 to 3V step, V_{IN} = V_{CC}/2, A_V = 1		2		µs
Op-Amp Isolation		f = 1kHz (MAX4092/MAX4094)		125		dB

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 6V, V_{EE} = GND, V_{CM} = 0, V_{OUT} = V_{CC}/2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values specified at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Voltage Range	V_{CC}	Inferred from PSRR test		2.7		6.0	V
Supply Current	I_{CC}	V_{CM} = V_{CC}/2	V_{CC} = 2.7V			200	µA
			V_{CC} = 5V			225	
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} to V_{CC}				±3.5	mV
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$				±2		µV/°C
Input Bias Current	I_B	V_{CM} = V_{EE} to V_{CC}				±200	nA
Input Offset Current	I_{OS}	V_{CM} = V_{EE} to V_{CC}				±20	nA
Input Common-Mode Range	V_{CM}	Inferred from CMRR test		V_{EE} - 0.05		V_{CC} + 0.05	V
Common-Mode Rejection Ratio	CMRR	(V_{EE} - 0.05V) ≤ V_{CM} ≤ (V_{CC} + 0.05V)		62			dB
Power-Supply Rejection Ratio	PSRR	2.7V ≤ V_{CC} ≤ 6V		80			dB
Large-Signal Voltage Gain (Note 1)	A_{VOL}	V_{CC} = 2.7V, R_L = 100kΩ 0.25V ≤ V_{OUT} ≤ 2.45V	Sourcing	82			dB
			Sinking	80			
		V_{CC} = 2.7V, R_L = 1kΩ 0.5V ≤ V_{OUT} ≤ 2.2V	Sourcing	90			
			Sinking	76			
		V_{CC} = 5V, R_L = 100kΩ 0.25V ≤ V_{OUT} ≤ 4.75V	Sourcing	86			
			Sinking	82			
		V_{CC} = 5V, R_L = 1kΩ 0.5V ≤ V_{OUT} ≤ 4.5V	Sourcing	94			
			Sinking	80			
Output Voltage Swing High (Note 1)	V_{OH}	$\lvert V_{CC} - V_{OUT} \rvert$	R_L = 100kΩ			75	mV
			R_L = 1kΩ			250	
Output Voltage Swing Low (Note 1)	V_{OL}	$\lvert V_{OUT} - V_{EE} \rvert$	R_L = 100kΩ			75	mV
			R_L = 1kΩ			250	

Note 1: R_L is connected to V_{EE} for A_{VOL} sourcing and V_{OH} tests. R_L is connected to V_{CC} for A_{VOL} sinking and V_{OL} tests.

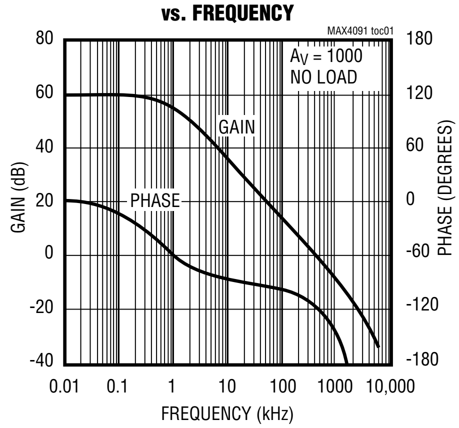
Note 2: All specifications are 100% tested at T_A = +25°C. Specification limits over temperature (T_A = T_{MIN} to T_{MAX}) are guaranteed by design, not production tested.

Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

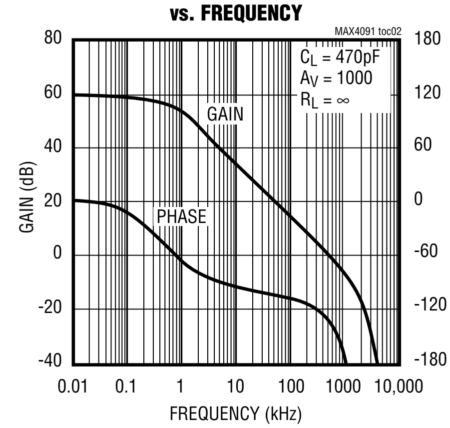
Typical Operating Characteristics

(V_{CC} = 5V, V_{EE} = 0, T_A = +25°C, unless otherwise noted.)

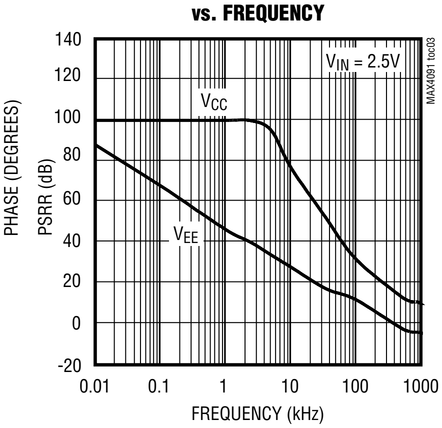
GAIN AND PHASE vs. FREQUENCY



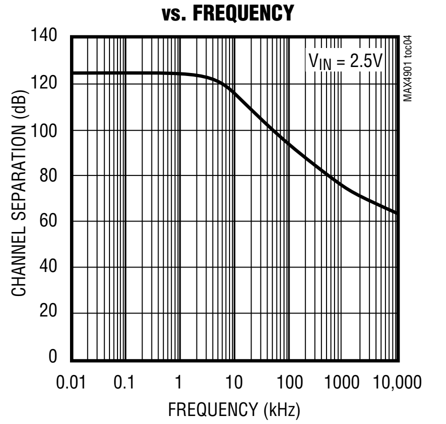
GAIN AND PHASE vs. FREQUENCY



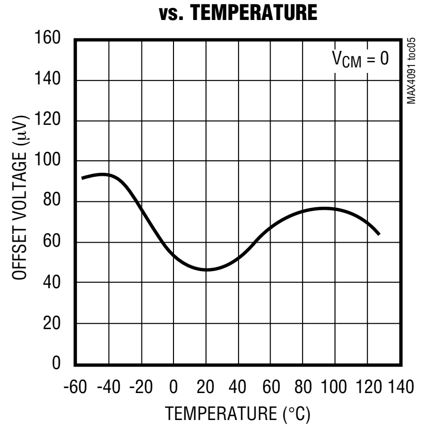
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



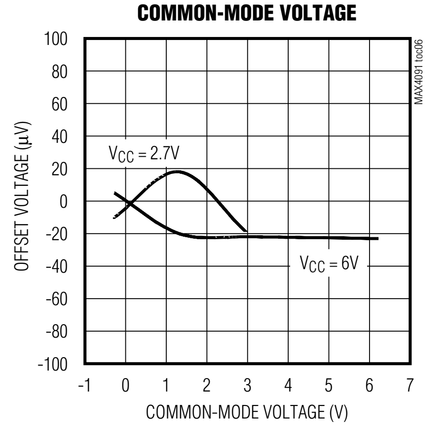
CHANNEL ISOLATION vs. FREQUENCY



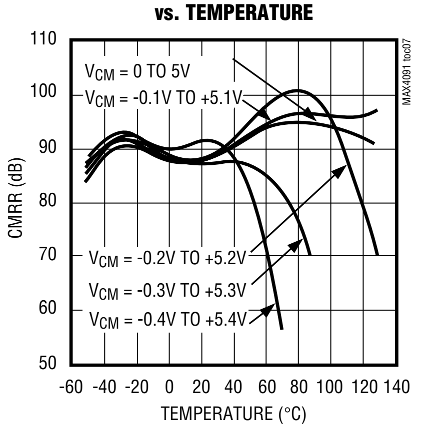
OFFSET VOLTAGE vs. TEMPERATURE



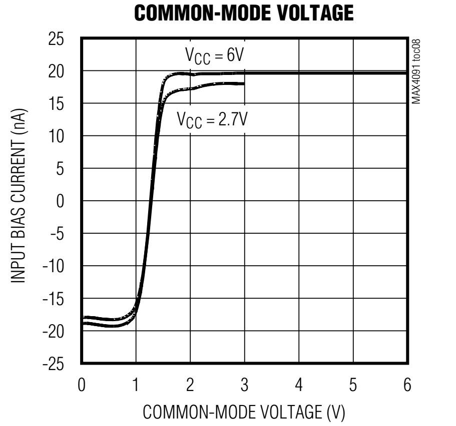
OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



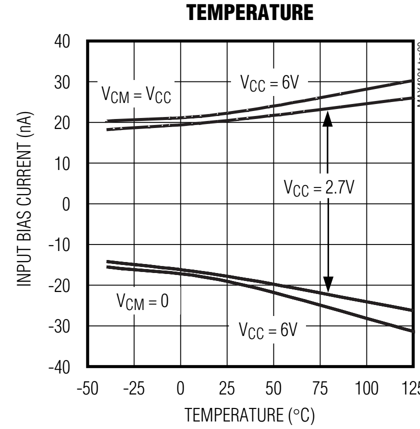
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



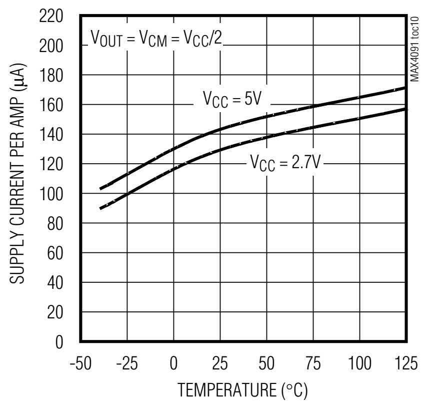
INPUT BIAS CURRENT vs. TEMPERATURE



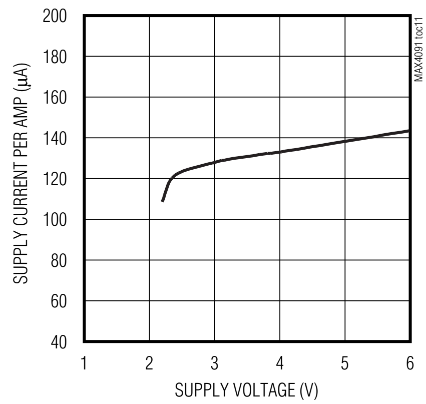
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = 0, T_A = +25°C, unless otherwise noted.)

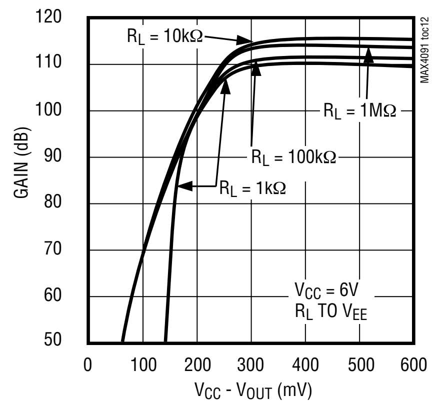
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



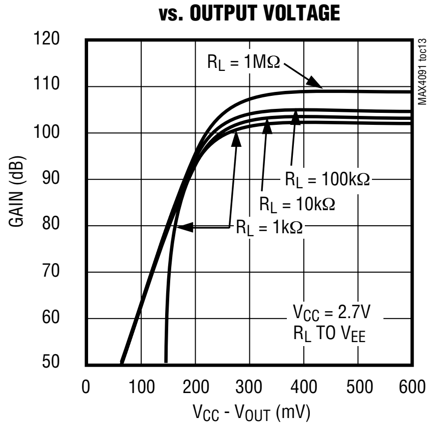
SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE



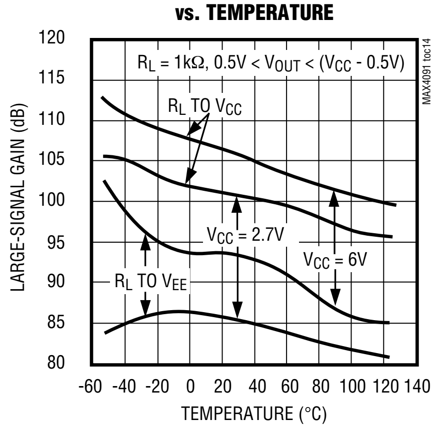
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



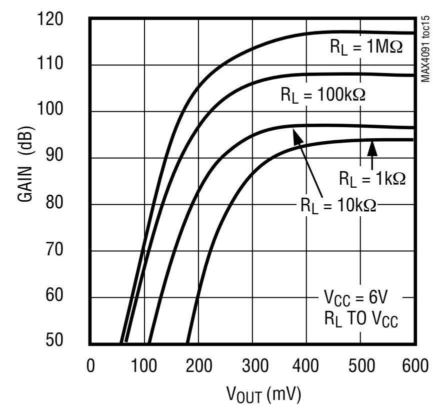
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



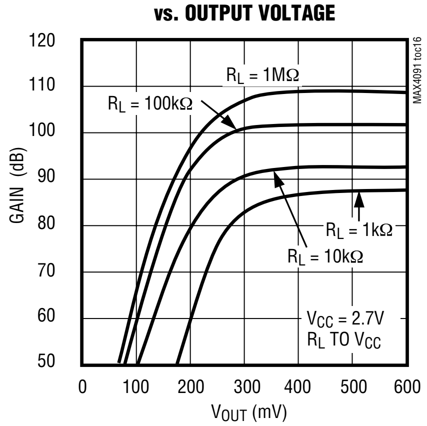
LARGE-SIGNAL GAIN vs. TEMPERATURE



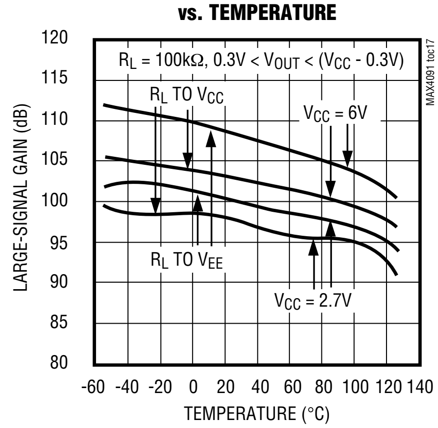
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



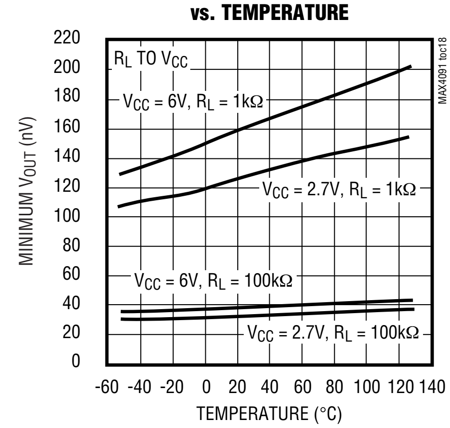
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



LARGE-SIGNAL GAIN vs. TEMPERATURE



MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE

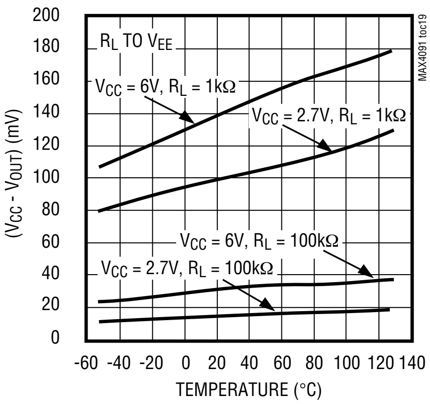


Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

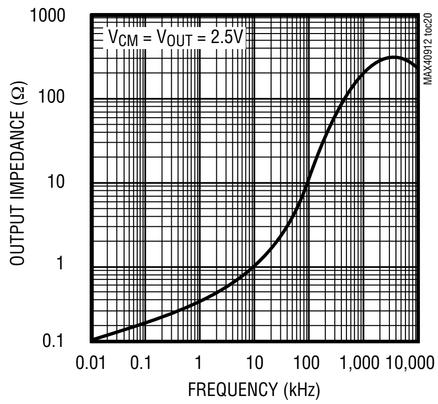
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = 0, T_A = +25°C, unless otherwise noted.)

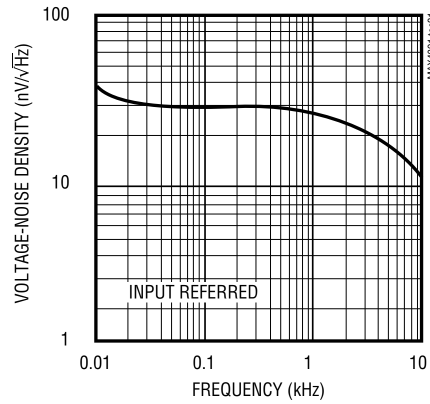
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



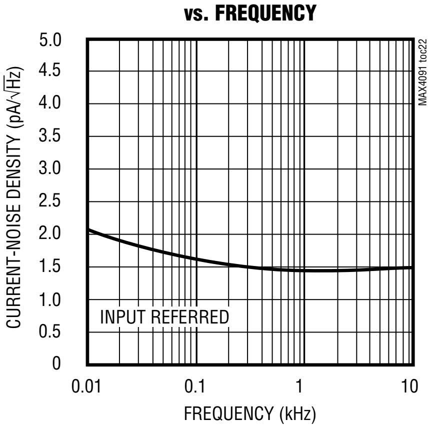
OUTPUT IMPEDANCE vs. FREQUENCY



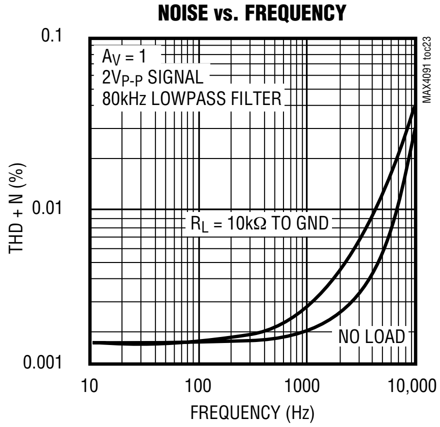
VOLTAGE-NOISE DENSITY vs. FREQUENCY



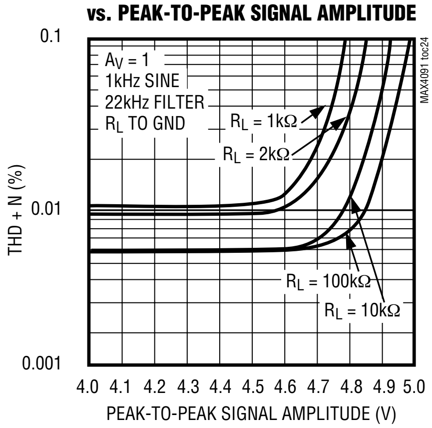
CURRENT-NOISE DENSITY vs. FREQUENCY



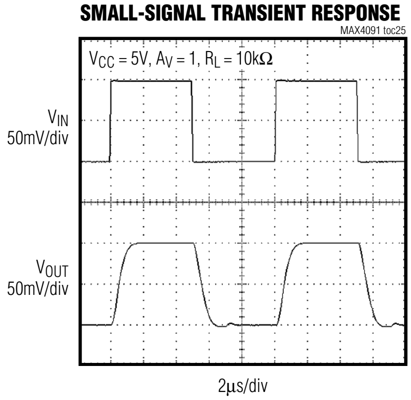
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



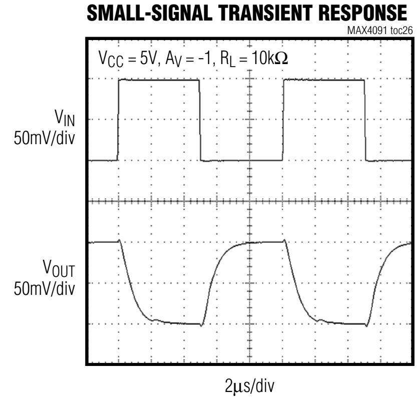
TOTAL HARMONIC DISTORTION PLUS NOISE vs. PEAK-TO-PEAK SIGNAL AMPLITUDE



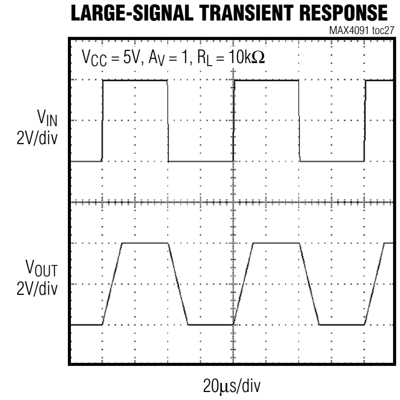
SMALL-SIGNAL TRANSIENT RESPONSE



SMALL-SIGNAL TRANSIENT RESPONSE



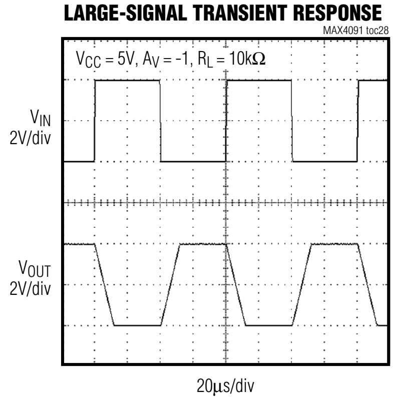
LARGE-SIGNAL TRANSIENT RESPONSE



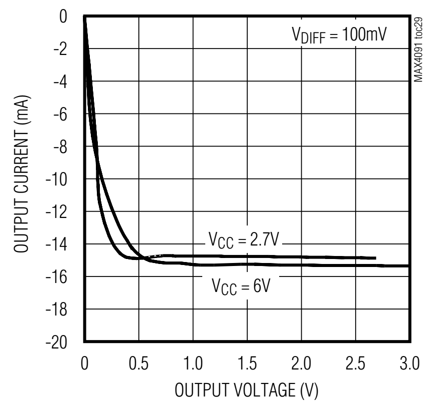
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = 0, T_A = +25°C, unless otherwise noted.)

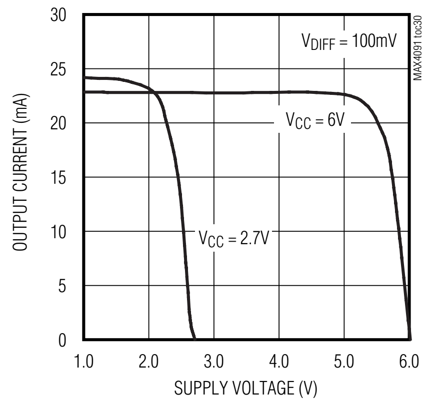
LARGE-SIGNAL TRANSIENT RESPONSE



SINK CURRENT vs. OUTPUT VOLTAGE



SOURCE CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN				NAME	FUNCTION
MAX4091 SOT23	MAX4091 SO/µMAX	MAX4092	MAX4094		
1	6	—	—	OUT	Amplifier Output
2	4	4	11	V_{EE}	Negative Supply
3	3	—	—	IN+	Noninverting Input
4	2	—	—	IN-	Inverting Input
5	7	8	4	V_{CC}	Positive Supply
—	1, 5, 8	—	—	N.C.	No Connection. Not internally connected.
—	—	1	1	OUT1	Amplifier 1 Output
—	—	2	2	IN1-	Amplifier 1 Inverting Input
—	—	3	3	IN1+	Amplifier 1 Noninverting Input
—	—	5	5	IN2+	Amplifier 2 Noninverting Input
—	—	6	6	IN2-	Amplifier 2 Inverting Input
—	—	7	7	OUT2	Amplifier 2 Output
—	—	—	8	OUT3	Amplifier 3 Output
—	—	—	9	IN3-	Amplifier 3 Inverting Input
—	—	—	10	IN3+	Amplifier 3 Noninverting Input
—	—	—	12	IN4+	Amplifier 4 Noninverting Input
—	—	—	13	IN4-	Amplifier 4 Inverting Input
—	—	—	14	OUT4	Amplifier 4 Output

Detailed Description

The single MAX4091, dual MAX4092 and quad MAX4094 op amps combine excellent DC accuracy with rail-to-rail operation at both input and output. With their precision performance, wide dynamic range at low supply voltages, and very low supply current, these op amps are ideal for battery-operated equipment, industrial, and data acquisition and control applications.

Applications Information

Rail-to-Rail Inputs and Outputs

The MAX4091/MAX4092/MAX4094's input common-mode range extends 50mV beyond the positive and negative supply rails, with excellent common-mode rejection. Beyond the specified common-mode range, the outputs are guaranteed not to undergo phase reversal or latchup. Therefore, the MAX4091/MAX4092/MAX4094 can be used in applications with common-mode signals, at or even beyond the supplies, without the problems associated with typical op amps.

The MAX4091/MAX4092/MAX4094's output voltage swings to within 15mV of the supplies with a 100kΩ load. This rail-to-rail swing at the input and the output substantially increases the dynamic range, especially in low-supply-voltage applications. Figure 1 shows the input and output waveforms for the MAX4092, configured as a unity-gain noninverting buffer operating from a single 3V supply. The input signal is $3.0V_{P-P}$, a 1kHz sinusoid centered at 1.5V. The output amplitude is approximately $2.98V_{P-P}$.

Input Offset Voltage

Rail-to-rail common-mode swing at the input is obtained by two complementary input stages in parallel, which feed a folded cascaded stage. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages close to the positive rail.

The offsets of the two pairs are trimmed. However, there is some residual mismatch between them. This mismatch results in a two-level input offset characteristic, with a transition region between the levels occurring at a common-mode voltage of approximately 1.3V above V_{EE}. Unlike other rail-to-rail op amps, the transition region has been widened to approximately 600mV in order to minimize the slight degradation in CMRR caused by this mismatch.

The input bias currents of the MAX4091/MAX4092/MAX4094 are typically less than 20nA. The bias current flows into the device when the NPN input stage is active, and it flows out when the PNP input stage is active. To reduce the offset error caused by input bias current flowing through external source resistances, match the effective resistance seen at each input. Connect resistor R3 between the noninverting input and ground when using the op amp in an inverting configuration (Figure 2a); connect resistor R3 between the noninverting input and the input signal when using the op amp in a noninverting configuration (Figure 2b). Select R3 to equal the parallel combination of R1 and R2. High source resistances will degrade noise performance, due to the the input current noise (which is multiplied by the source resistance).

Input Stage Protection Circuitry

The MAX4091/MAX4092/MAX4094 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of back-to-back diodes between IN+ and IN- with two 1.7kΩ resistors in series (Figure 3). The diodes limit the differential voltage applied to the amplifiers' internal circuitry to no more than V_F, where V_F is the diodes' forward-voltage drop (about 0.7V at +25°C).

Input bias current for the ICs (±20nA) is specified for small differential input voltages. For large differential input voltages (exceeding V_F), this protection circuitry increases the input current at IN+ and IN-:

$$\text{INPUT CURRENT} = \frac{[(V_{IN+}) - (V_{IN-})] - V_F}{2 \times 1.7k\Omega}$$

Output Loading and Stability

Even with their low quiescent current of less than 130µA per op amp, the MAX4091/MAX4092/MAX4094 are well suited for driving loads up to 1kΩ while maintaining DC accuracy. Stability while driving heavy capacitive loads is another key advantage over comparable CMOS rail-to-rail op amps.

In op amp circuits, driving large capacitive loads increases the likelihood of oscillation. This is especially true for circuits with high-loop gains, such as a unity-gain voltage follower. The output impedance and a capacitive load form an RC network that adds a pole to the loop response and induces phase lag. If the pole frequency is low enough—as when driving a large capacitive load—the circuit phase margin is degraded, leading to either an under-damped pulse response or oscillation.

The MAX4091/MAX4092/MAX4094 can drive capacitive loads in excess of 2000pF under certain conditions (Figure 4). When driving capacitive loads, the greatest potential for instability occurs when the op amp is sourcing approximately 200µA. Even in this case, stability is maintained with up to 400pF of output capacitance. If the output sources either more or less current, stability is increased. These devices perform well with a 1000pF pure capacitive load (Figure 5). Figures 6a, 6b, and 6c show the performance with a 500pF load in parallel with various load resistors.

To increase stability while driving large-capacitive loads, connect a pullup resistor to V_{CC} at the output to decrease the current the amplifier must source. If the amplifier is made to sink current rather than source, stability is further increased.

Frequency stability can be improved by adding an output isolation resistor (R_S) to the voltage-follower circuit (Figure 7). This resistor improves the phase margin of the circuit by isolating the load capacitor from the op amp's output. Figure 8a shows the MAX4092 driving 5000pF ($R_L \geq 100k\Omega$), while Figure 8b adds a 47Ω isolation resistor.

Because the MAX4091/MAX4092/MAX4094 have excellent stability, no isolation resistor is required, except in the most demanding applications. This is beneficial because an isolation resistor would degrade the low-frequency performance of the circuit.

Power-Up Settling Time

The MAX4091/MAX4092/MAX4094 have a typical supply current of 130µA per op amp. Although supply current is already low, it is sometimes desirable to reduce it further by powering down the op amp and associated ICs for periods of time. For example, when using a MAX4092 to buffer the inputs of a multi-channel analog-to-digital converter (ADC), much of the circuitry could be powered down between data samples to increase battery life. If samples are taken infrequently, the op amps, along with the ADC, may be powered down most of the time.

When power is reapplied to the MAX4091/MAX4092/MAX4094, it takes some time for the voltages on the supply pin and the output pin of the op amp to settle. Supply settling time depends on the supply voltage, the value of the bypass capacitor, the output impedance of the incoming supply, and any lead resistance or inductance between components. Op amp settling time depends primarily on the output voltage and is slew-rate limited. With the noninverting input to a voltage follower held at midsupply (Figure 9), when the supply steps from 0 to V_{CC}, the output settles in approximately 2µs for V_{CC} = 3V (Figure 10a) and 8µs for V_{CC} = 5V (Figure 10b).

Power Supplies and Layout

The MAX4091/MAX4092/MAX4094 operate from a single 2.7V to 6V power supply, or from dual supplies of ±1.35V to ±3V. For single-supply operation, bypass the power supply with a 0.1µF capacitor. If operating from dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize both trace lengths and resistor leads and place external components close to the op amp's pins.

Chip Information

MAX4091 TRANSISTOR COUNT: 168

MAX4092 TRANSISTOR COUNT: 336

MAX4094 TRANSISTOR COUNT: 670

PROCESS: Bipolar

Test Circuits/Timing Diagrams

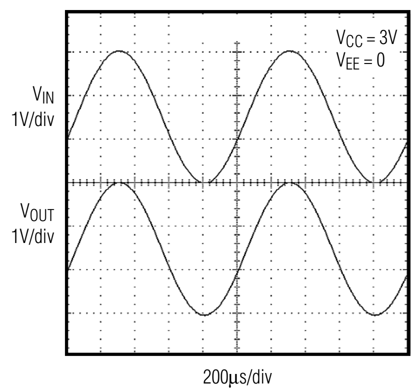


Figure 1. Rail-to-Rail Input and Output Operation

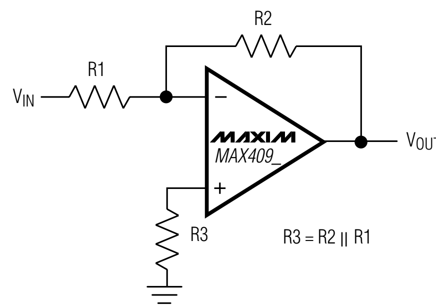


Figure 2a. Reducing Offset Error Due to Bias Current: Inverting Configuration

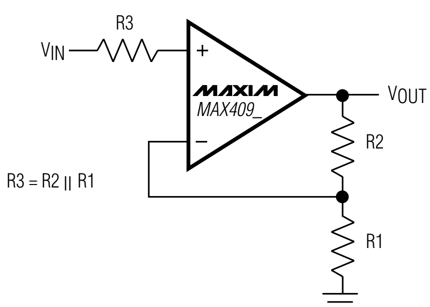


Figure 2b. Reducing Offset Error Due to Bias Current: Noninverting Configuration

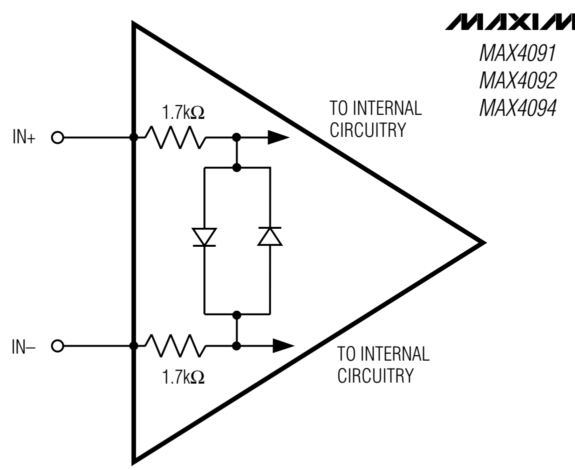


Figure 3. Input Stage Protection Circuitry

Test Circuits/Timing Diagrams (continued)

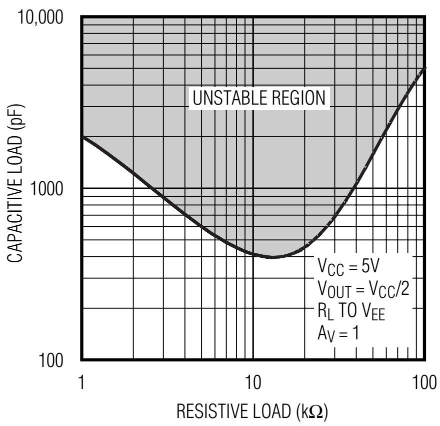


Figure 4. Capacitive-Load Stable Region Sourcing Current

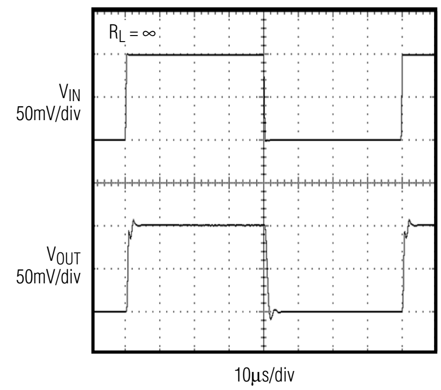


Figure 5. MAX4092 Voltage Follower with 1000pF Load

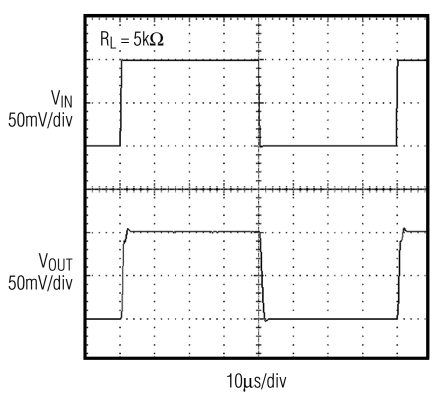


Figure 6a. MAX4092 Voltage Follower with 500pF Load (R_L = 5kΩ)

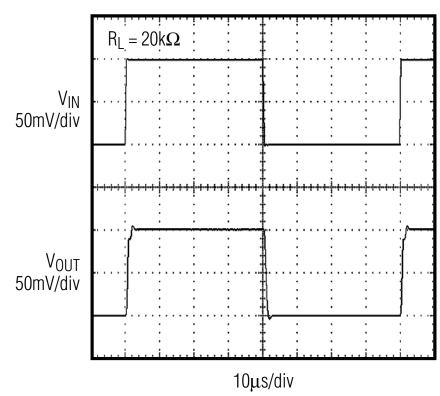


Figure 6b. MAX4092 Voltage Follower with 500pF Load (R_L = 20kΩ)

Single/Dual/Quad, Micropower, Single-Supply, Rail-to-Rail Op Amps

Test Circuits/Timing Diagrams (continued)

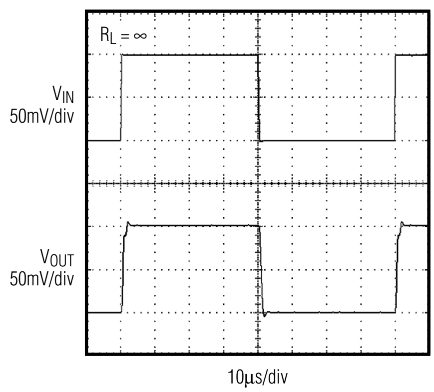


Figure 6c. MAX4092 Voltage Follower with 500pF Load ($R_L = \infty$)

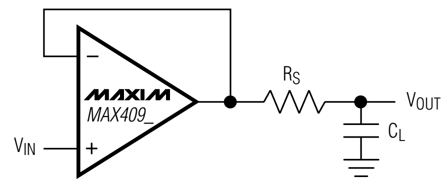


Figure 7. Capacitive-Load Driving Circuit

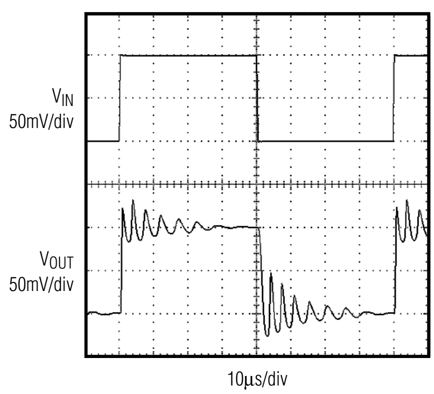


Figure 8a. Driving a 5000pF Capacitive Load

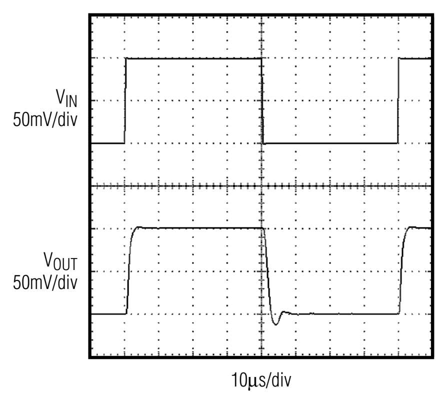


Figure 8b. Driving a 5000pF Capacitive Load with a 47Ω Isolation Resistor

Test Circuits/Timing Diagrams (continued)

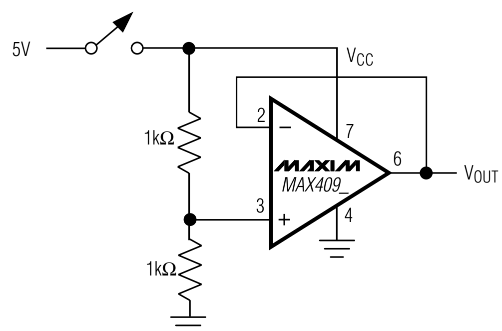


Figure 9. Power-Up Test Configuration

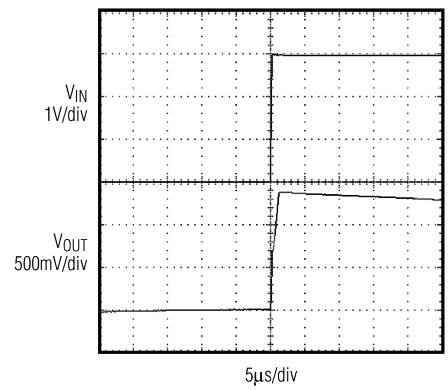


Figure 10a. Power-Up Settling Time (V_{CC} = +3V)

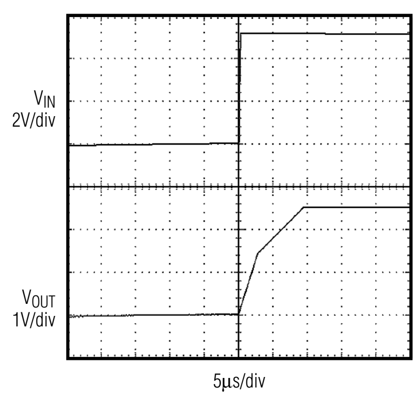
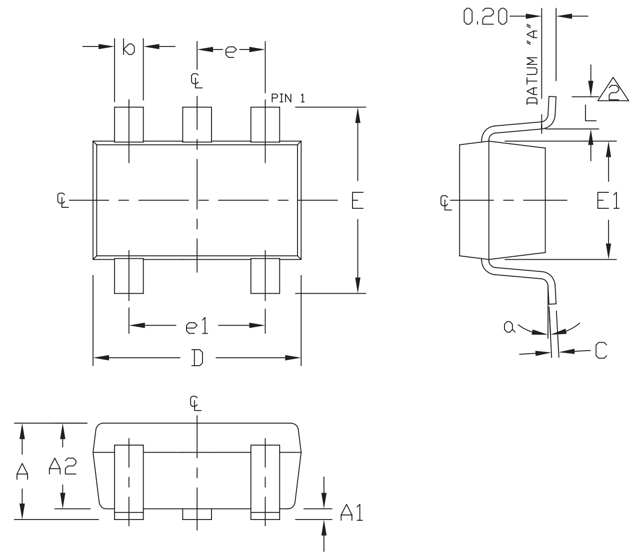


Figure 10b. Power-Up Settling Time (V_{CC} = +5V)

Package Information

SOT5L.EPS

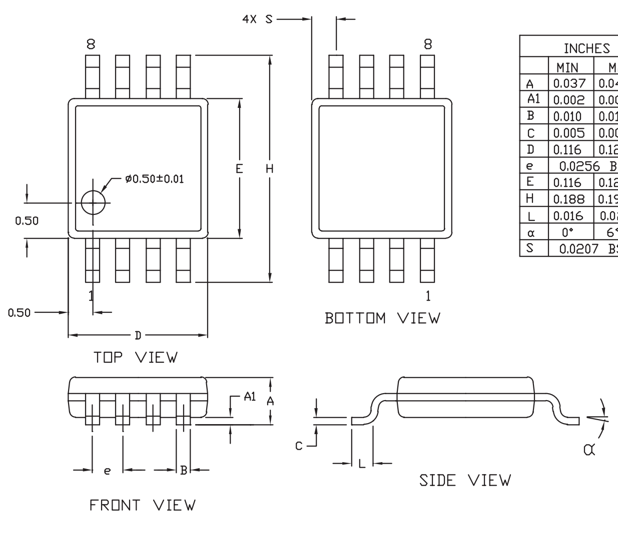


SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
e1	1.90 REF	
α	0°	10°

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. MEETS JEDEC MO178.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SOT-23, 5L
APPROVAL | DOCUMENT CONTROL NO. 21-0057 | REV C | 1/1

8LUMAXD.EPS

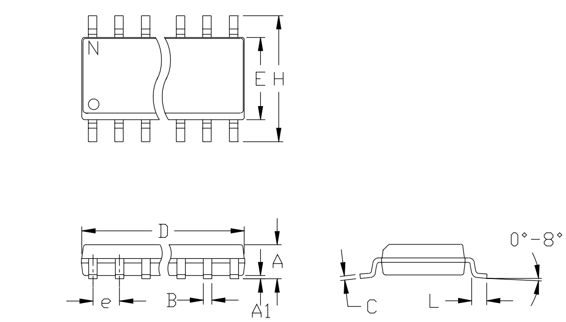


	INCHES		MILLIMETERS		JEDEC INCHES		JEDEC MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10	---	0.043	---	1.10
A1	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15
B	0.010	0.014	0.25	0.36	0.010	0.016	0.25	0.40
C	0.005	0.007	0.13	0.18	0.005	0.009	0.13	0.23
D	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.64 BSC	
E	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
H	0.188	0.198	4.78	5.03	0.193 BSC		4.9 BSC	
L	0.016	0.026	0.41	0.66	0.016	0.027	0.40	0.70
α	0°	6°	0°	6°	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC					

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 8L uMAX
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV I | 1/1

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

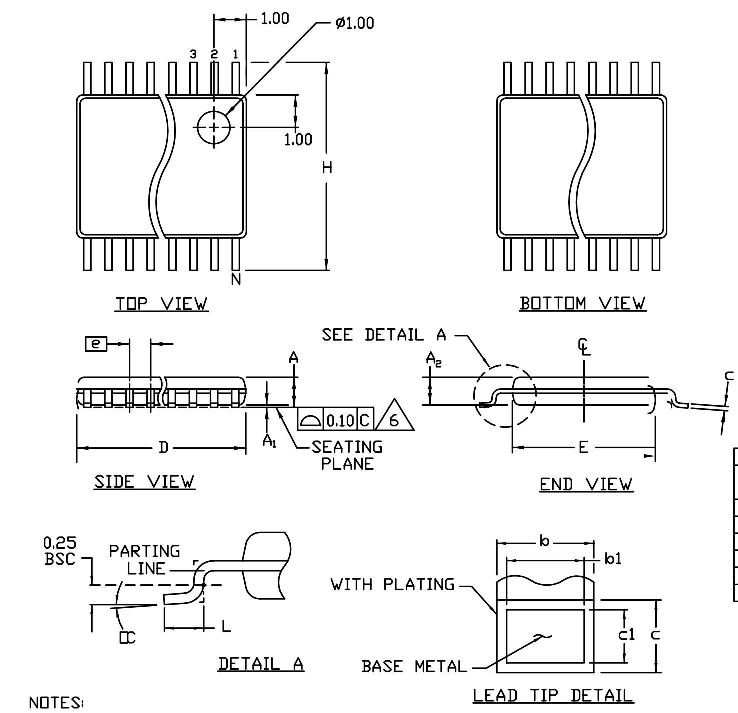
	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | DOCUMENT CONTROL NUMBER: 21-0041 REV: A

Package Information (continued)

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	E	1/1