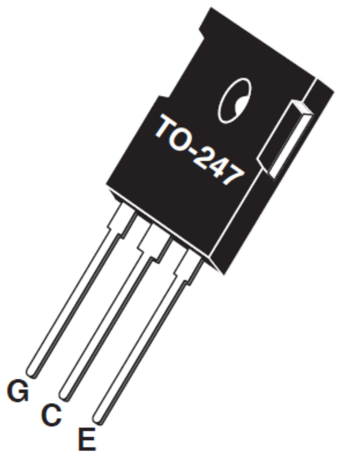
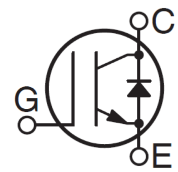
1200 V, 13 A Power MOS 7™ PT IGBT with DQ Diode

APT13GP120BDQ1G

Product Overview

1200 V, 13 A at 70 kHz Power MOS 7 punch-through (PT) IGBT with co-packaged anti-parallel DQ diode, TO-247





G—Gate
C—Collector
E—Emitter

Features

- Low conduction loss and saturation voltage
- Low gate charge
- Ultrafast tail current shutoff
- Soft recovery
- High operating frequency
- Reverse-bias safe operating area (RBSOA) rated
- RoHS compliant

1. Device Specifications: IGBT

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{CES}	Collector-emitter voltage	1200	V
V_{GE}	Gate-emitter voltage	±20	
I_{C1}	Continuous collector current at T_C = 25 °C	41	A
I_{C2}	Continuous collector current at T_C = 100 °C	20	
I_{CM}	Pulsed collector current[1] at T_C = 150 °C	50	
RBSOA	Reverse-bias safe operating area at T_J = 150 °C and 960 V	50	A
P_D	Total power dissipation T_C = 25 °C	250	W

Note:

1. Repetitive rating: Pulse width and case temperature are limited by maximum junction temperature.

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$R_{\Theta JC}$	Junction-to-case thermal resistance (IGBT)		0.35	0.50	°C/W
$R_{\Theta JC}$	Junction-to-case thermal resistance (diode)		0.80	1.18	
T_J, T_{STG}	Operating and storage junction temperature range	–55		150	°C
T_L	Lead temperature for 10 seconds			300	
	Mounting torque, M3 screw			10	lbf·in
				1.1	N·m
Wt	Package weight		0.22		oz
			6.2		g

1.2 Electrical Performance

The following table shows the static characteristics of this device. T_J = 25 °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{GE} = 0 V, I_G = 500 μA	1200			V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 1 mA	3	4.5	6	
$V_{CE(ON)}$	Collector-emitter on voltage	V_{GE} = 15 V, I_C = 13 A		3.3	3.9	
		V_{GE} = 15 V, I_C = 13 A, T_J = 125 °C		3.0		
I_{CES}	Collector cut-off current[1]	V_{CE} = 1200 V, V_{GE} = 0 V		0.3	500	μA
		V_{CE} = 1200 V, V_{GE} = 0 V, T_J = 125 °C			3500	
I_{GES}	Gate-emitter leakage current	V_{GE} = ±20 V			±100	nA

Note:

1. I_{CES} includes both IGBT and FRED leakages.

The following table shows the dynamic characteristics of this device. T_J = 25 °C unless otherwise specified.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	V_{GE} = 0 V V_{CE} = 25 V ƒ = 1 MHz		1145		pF
C_{res}	Reverse transfer capacitance			15		
C_{oes}	Output capacitance			90		
V_{GEP}	Gate-to-emitter plateau voltage	Gate charge		7.5		V
Q_G	Total gate charge[1]	V_{GE} = 15 V V_{CE} = 600 V I_C = 13 A		55		nC
Q_{GE}	Gate-emitter charge			8		
Q_{GC}	Gate-collector ("Miller") charge			26		
RBSOA	Reverse bias safe operating area	T_J = 150 °C R_G = 5 Ω V_{GE} = 15 V V_{CE} = 960 V L = 100 µH	50			A
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V V_{GE} =15 V I_C = 13 A R_G = 5 Ω T_J = 25 °C		9		ns
t_r	Current rise time			12		
$t_{d(off)}$	Turn-off delay time			28		
t_f	Current fall time			34		
E_{on1}	Turn-on switching energy[2]			115		µJ
E_{on2}	Turn-on switching energy (diode)[3]			330		
E_{off}	Turn-off switching energy[4]			165		
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V V_{GE} = 15 V I_C = 13 A R_G = 5 Ω T_J = 125 °C		9		ns
t_r	Current rise time			12		
$t_{d(off)}$	Turn-off delay time			70		
t_f	Current fall time			200		
E_{on1}	Turn-on switching energy[2]			225		µJ
E_{on2}	Turn-on switching energy (diode)[3]			710		
E_{off}	Turn-off switching energy[4]			840		

Notes:

1. See MIL-STD-750 Method 3471.
2. E_{on1} is the clamped inductive turn-on-energy of the IGBT only, without the effect of a commutating diode reverse recovery current adding to the IGBT turn-on loss. (See Figure 1-25.)
3. E_{on2} is the clamped inductive turn-on energy that includes a commutating diode reverse recovery current in the IGBT turn-on switching loss. (See Figures 1-22, 1-23.)
4. E_{off} is the clamped inductive turn-off energy measured in accordance with JEDEC standard JESD24-1. (See Figures 1-22, 1-24.)

1.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 1-1. Output Characteristics

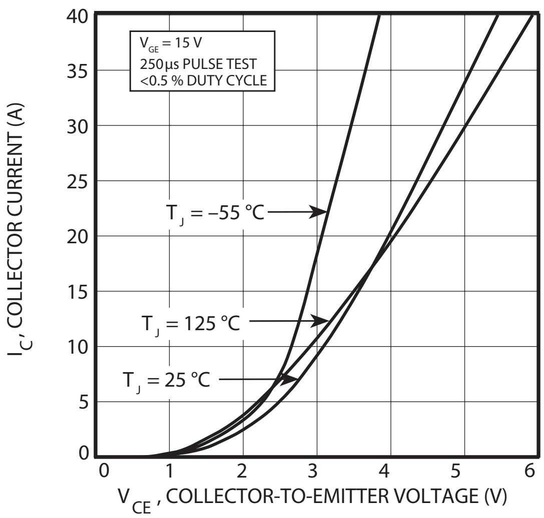


Figure 1-2. Output Characteristics

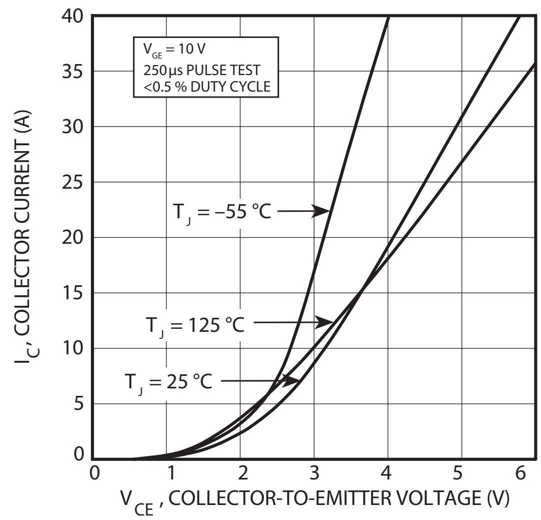


Figure 1-3. Transfer Characteristics

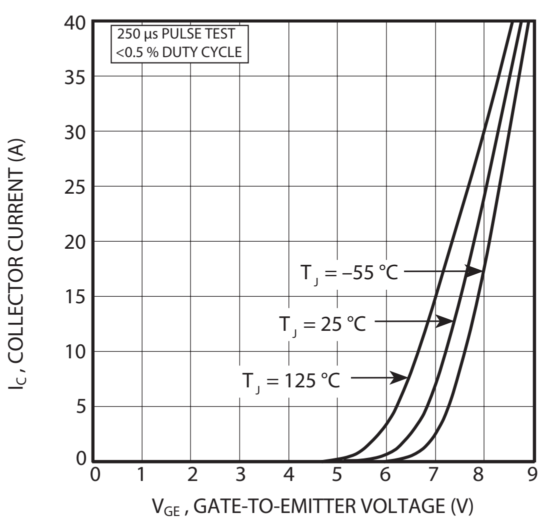


Figure 1-4. Gate Charge

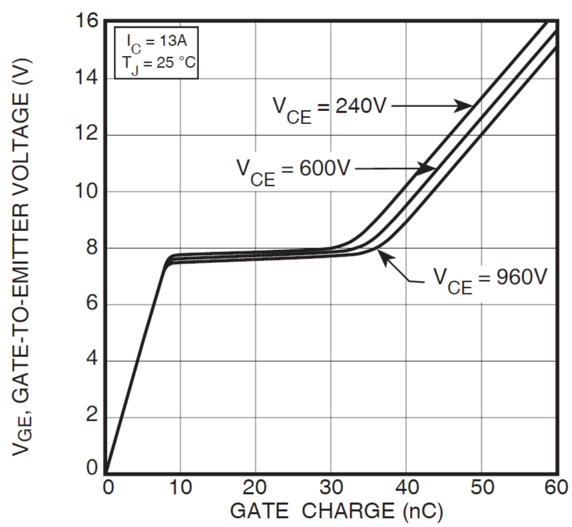


Figure 1-5. On-State Voltage vs. Gate-to- Emitter Voltage

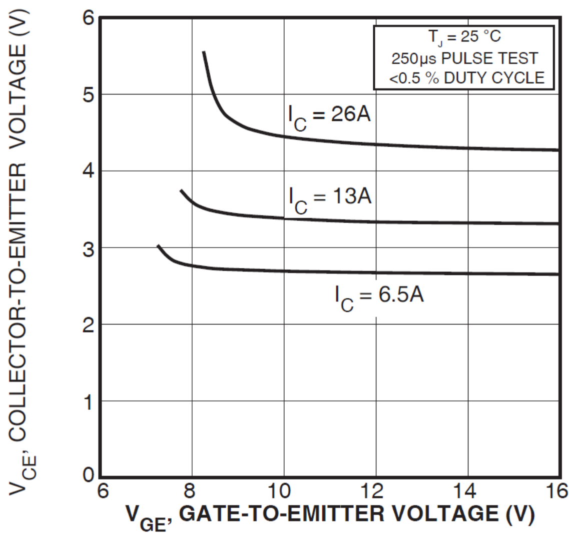


Figure 1-6. On-State Voltage vs. Junction Temperature

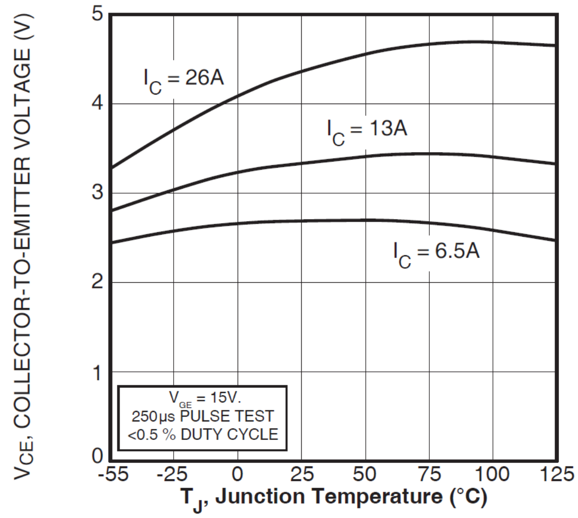


Figure 1-7. Breakdown Voltage vs. Junction Temperature

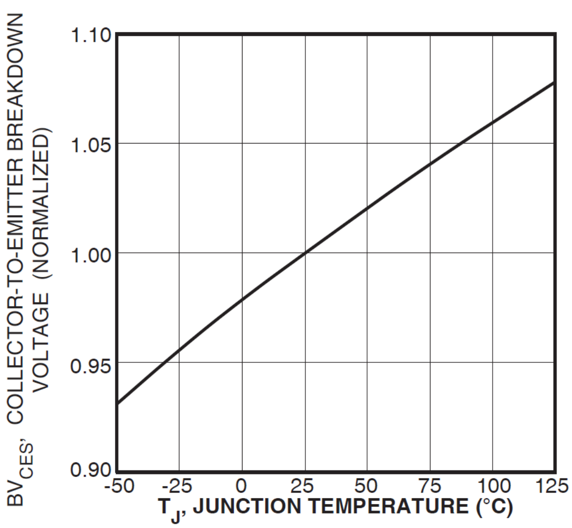


Figure 1-8. DC Collector Current vs. Case Temperature

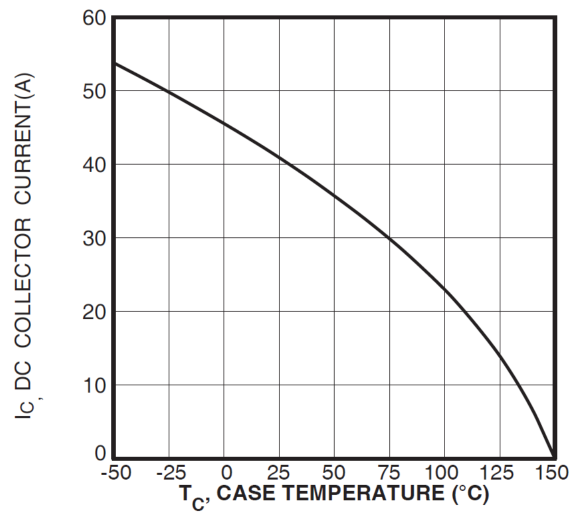


Figure 1-9. Turn-On Delay Time vs. Collector Current

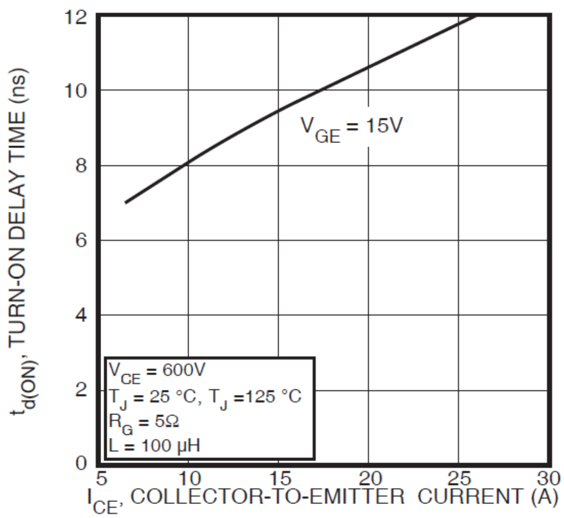


Figure 1-10. Turn-Off Delay Time vs. Collector Current

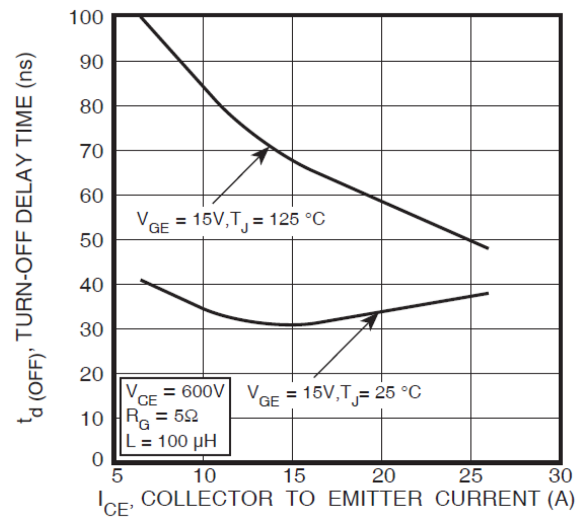


Figure 1-11. Current Rise Time vs. Collector Current

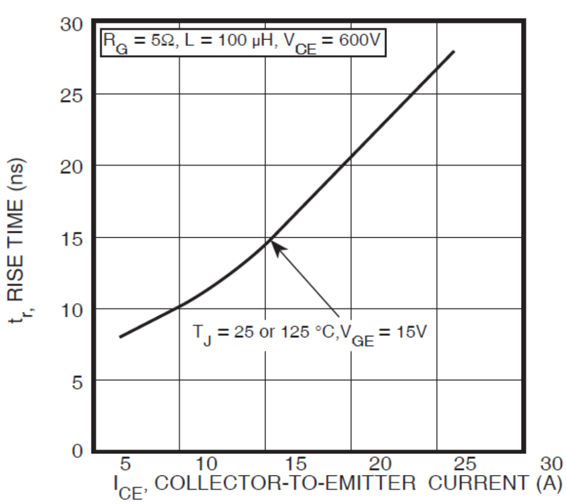


Figure 1-12. Current Rise Time vs. Collector Current

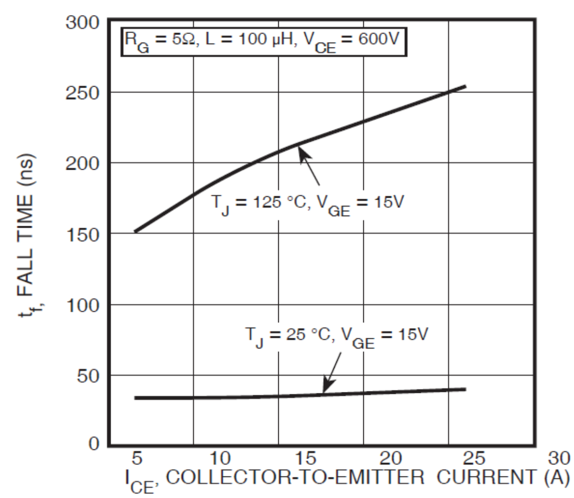


Figure 1-13. Turn-On Energy Loss vs. Collector Current

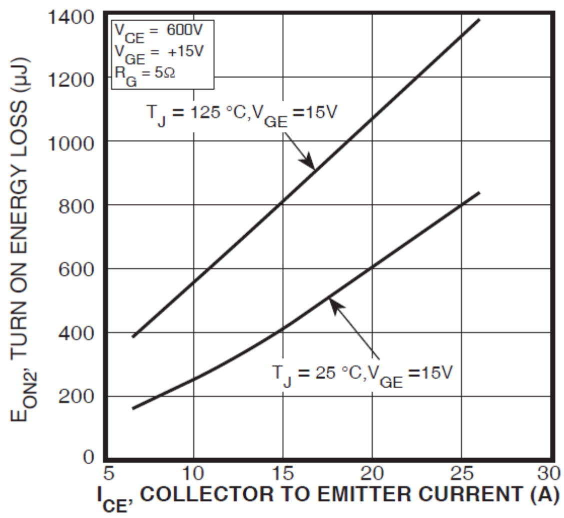


Figure 1-14. Turn-Off Energy Loss vs. Collector Current

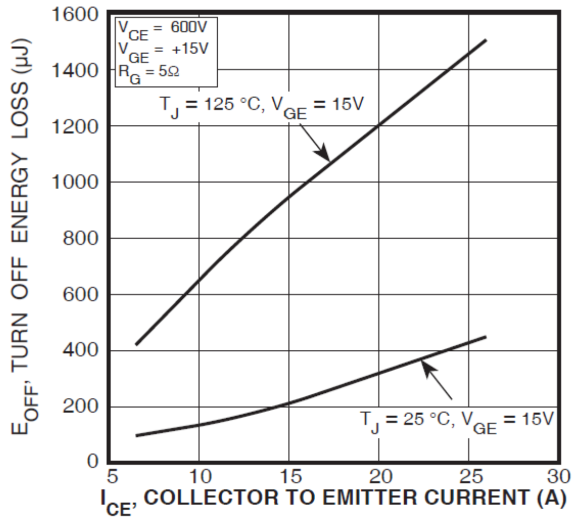


Figure 1-15. Switching Energy Losses vs. Gate Resistance

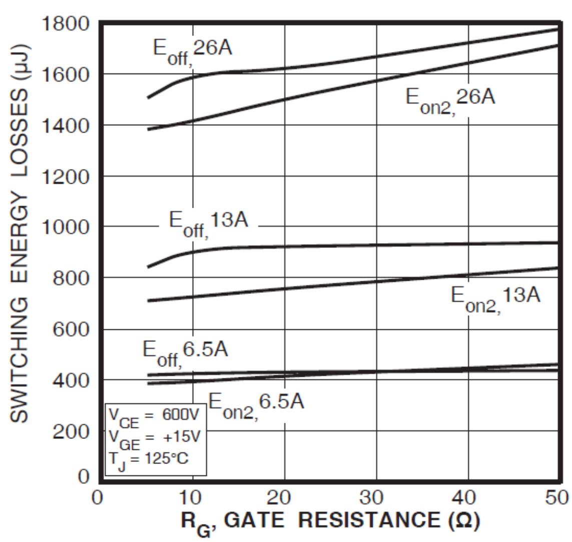


Figure 1-16. Switching Energy Losses vs. Junction Temperature

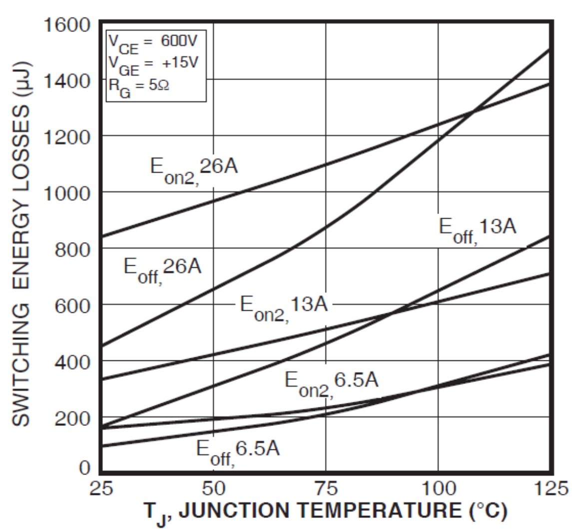


Figure 1-17. Capacitance vs. Collector-To-Emitter Voltage

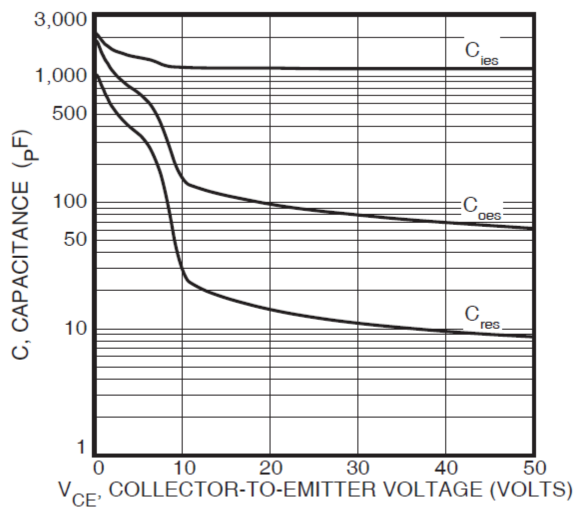


Figure 1-18. Reverse Bias Safe Operating Area

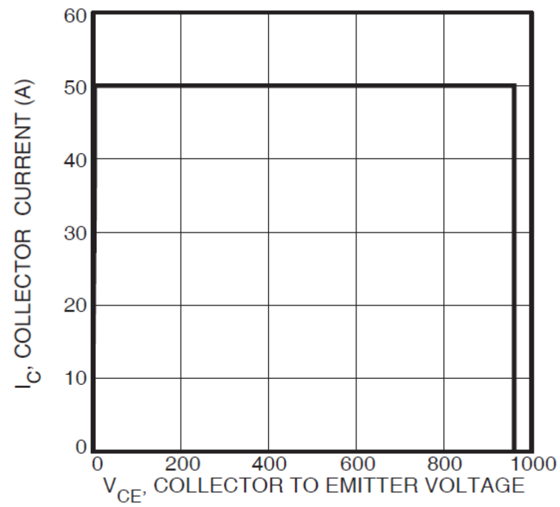


Figure 1-19. Maximum Transient Thermal Impedance

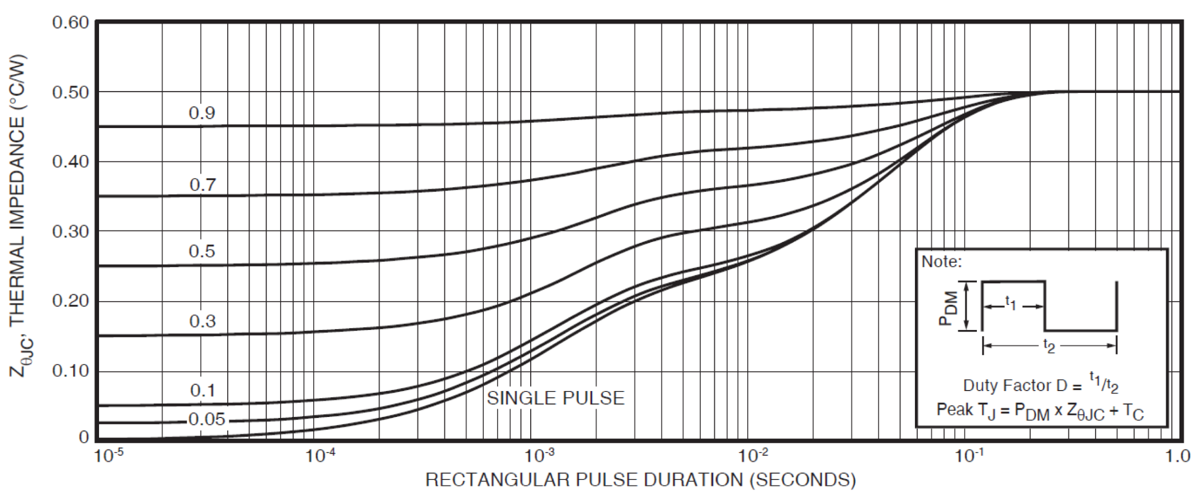


Figure 1-20. Transient Thermal Impedance Model

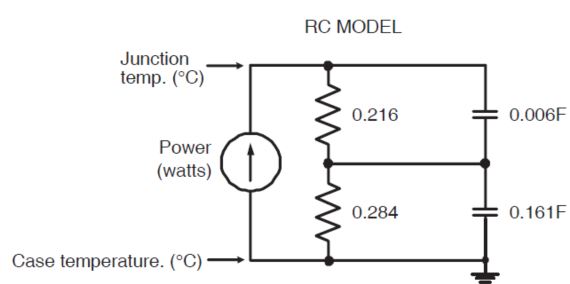
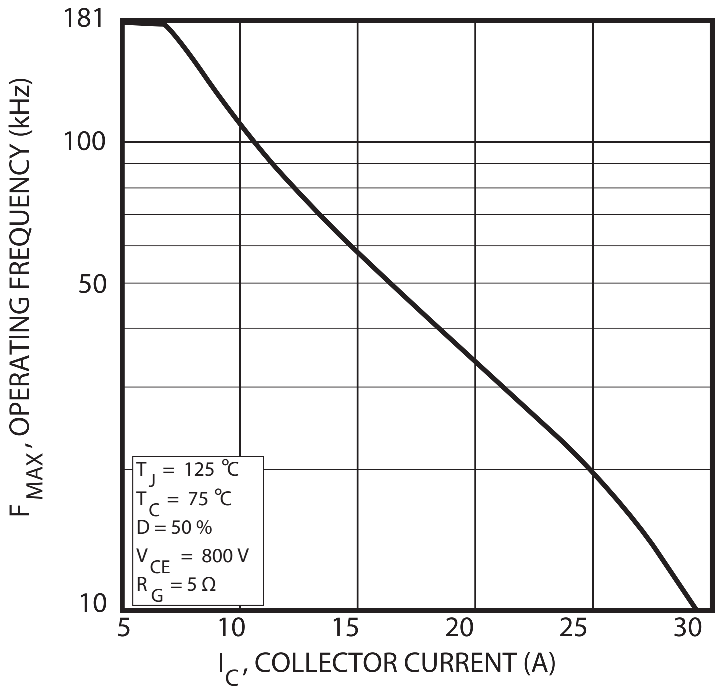


Figure 1-21. Operating Frequency vs. Collector Current



$$F_{max} = \min(f_{max}, f_{max2})$$

$$f_{max1} = \frac{0.05}{t_{d(on)} + t_r + t_{d(off)} + t_f}$$

$$f_{max2} = \frac{P_{diss} - P_{cond}}{E_{on2} + E_{off}}$$

$$P_{diss} = \frac{T_J - T_C}{R_{\Theta JC}}$$

Figure 1-22. Inductive Switching Test Circuit

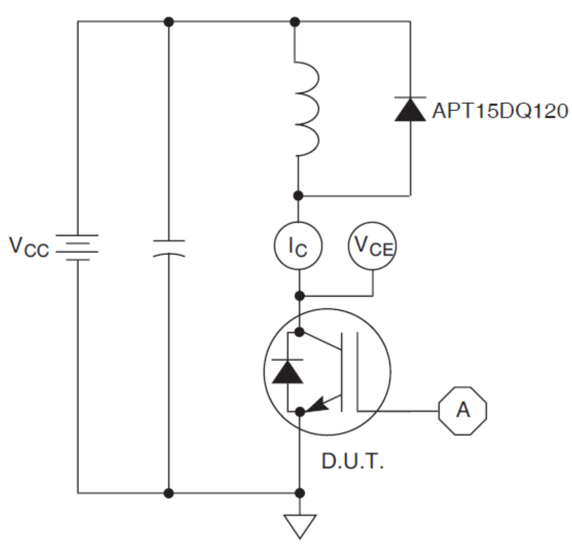


Figure 1-23. Turn-on Switching Waveforms and Definitions

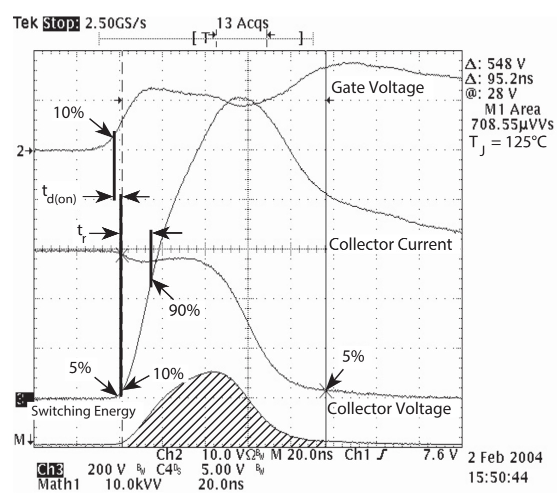


Figure 1-24. Turn-off Switching Waveforms and Definitions

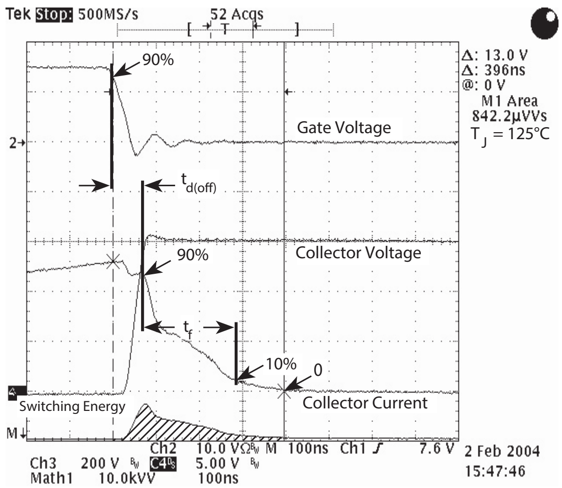
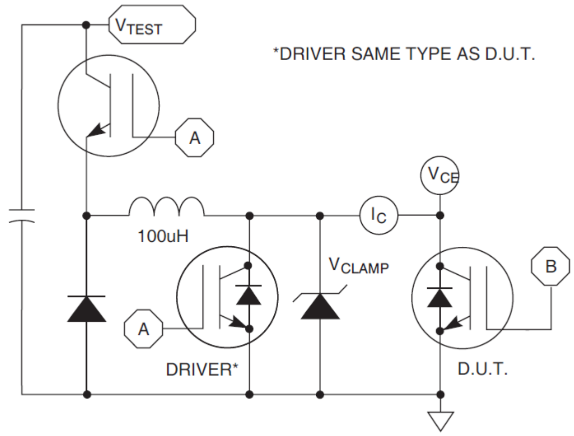


Figure 1-25. E_{on1} Test Circuit



2. Device Specifications: Ultrafast Soft Recovery Anti-Parallel Diode

This section shows the specifications of the Ultrafast Soft Recovery Anti-Parallel Diode.

2.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the anti-parallel diode.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_F(AV)	Maximum average forward current (T_C = 127 °C, Duty Cycle = 0.5)	15	A
I_F(RMS)	RMS forward current (square wave, 50% duty)	29	
I_{FSM}	Non-repetitive forward surge current (T_J = 45 °C, 8.3 ms)	110	

2.2 Electrical Performance

The following table shows the static characteristics of the anti-parallel diode. T_J = 25 °C unless otherwise specified.

Table 2-2. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
V_F	Forward voltage	I_F = 13 A		2.7		V
		I_F = 26 A		3.3		
		I_F = 13 A, T_J = 125 °C		2.3		

The following table shows the dynamic characteristics of the anti-parallel diode. T_J = 25 °C unless otherwise specified.

Table 2-3. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	I_F = 1 A di_F/dt = –100 A/μs V_R = 30 V		21		ns
t_{rr}	Reverse recovery time	I_F = 15 A di_F/dt = –200 A/μs V_R = 800 V		240		
Q_{rr}	Reverse recovery charge			260		nC
I_{RRM}	Maximum reverse recovery current			3		A
t_{rr}	Reverse recovery time	I_F = 15 A di_F/dt = –200 A/μs V_R = 800 V T_C = 125 °C		290		ns
Q_{rr}	Reverse recovery charge			960		nC
I_{RRM}	Maximum reverse recovery current			6		A
t_{rr}	Reverse recovery time	I_F = 15 A di_F/dt = –1000 A/μs V_R = 800 V T_C = 125 °C		130		ns
Q_{rr}	Reverse recovery charge			1340		nC
I_{RRM}	Maximum reverse recovery current			19		A

2.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 2-1. Maximum Transient Thermal Impedance

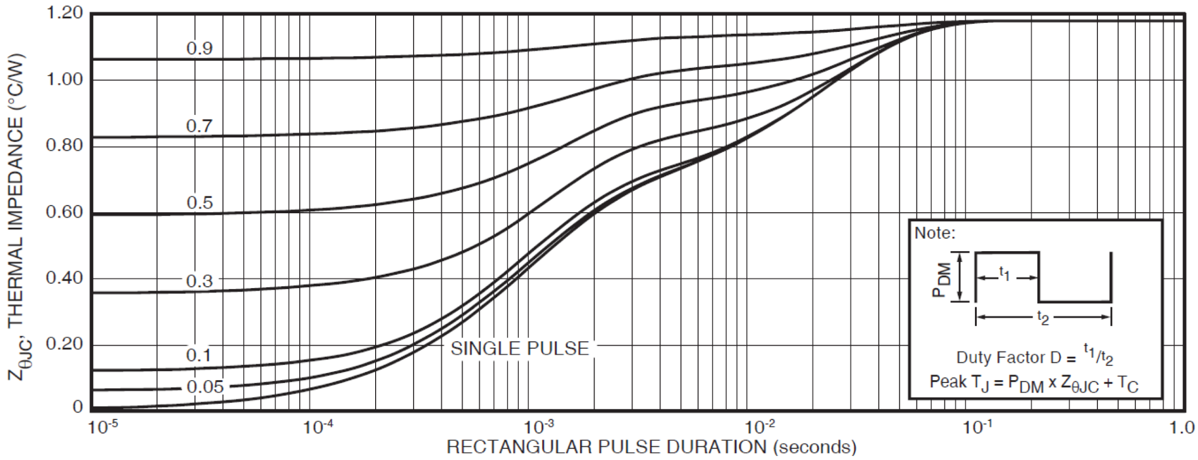


Figure 2-2. Transient Thermal Impedance Model

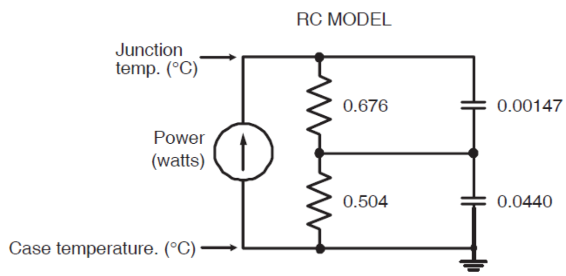


Figure 2-3. Forward Current vs. Forward Voltage

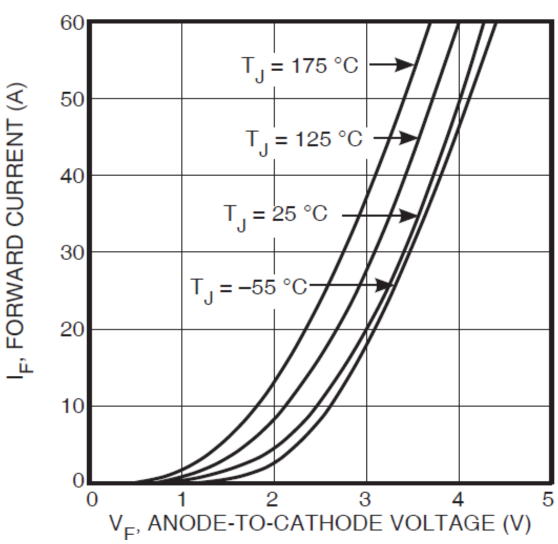


Figure 2-4. Reverse Recovery Time vs. Current Rate of Change

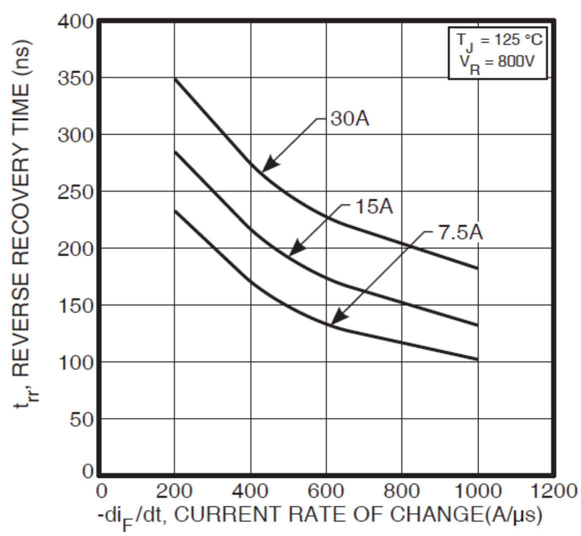


Figure 2-5. Reverse Recovery Charge vs. Current Rate of Change

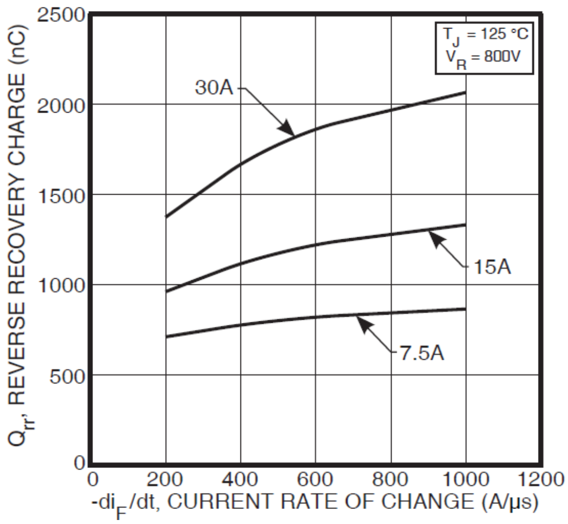


Figure 2-6. Reverse Recovery Charge vs. Current Rate of Change

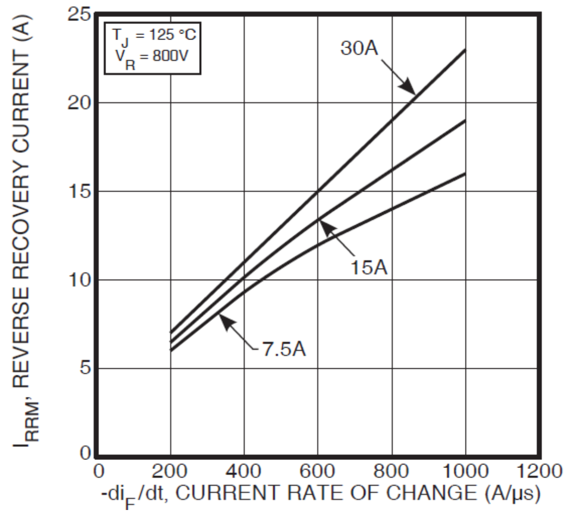


Figure 2-7. Dynamic Parameters vs. Junction Temperature

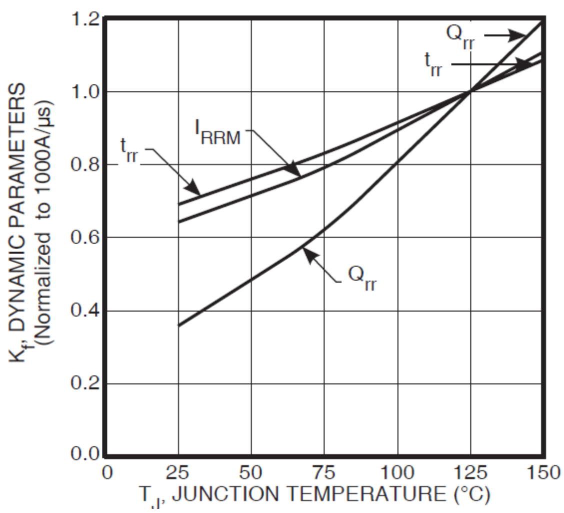


Figure 2-8. Maximum Avgerage Forward Current vs. Case Temperature

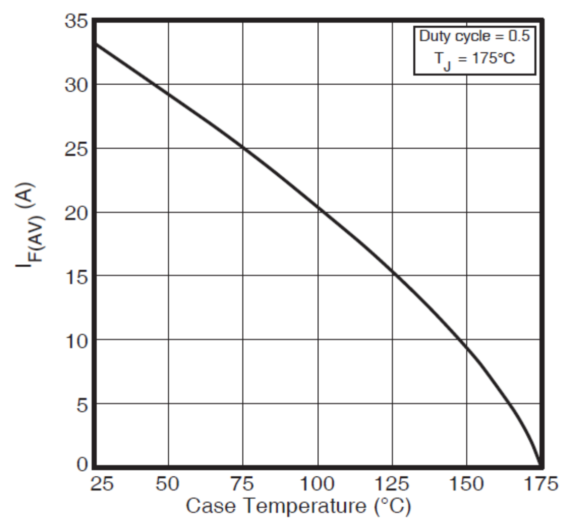
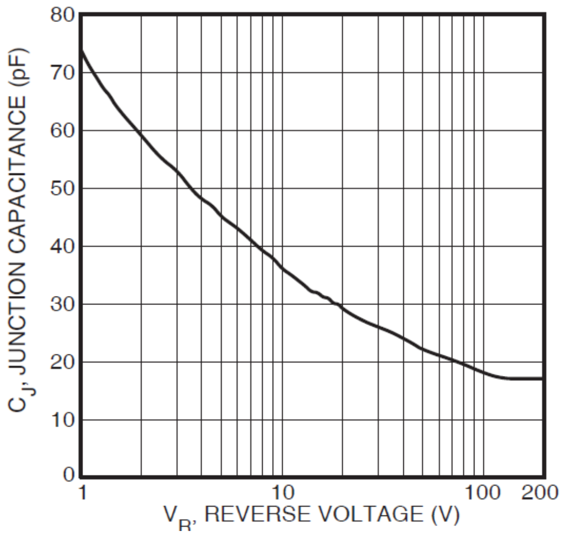


Figure 2-9. Junction Capacitance vs. Reverse Voltage



The following figure shows the diode test circuit of this device.

Figure 2-10. Diode Test Circuit

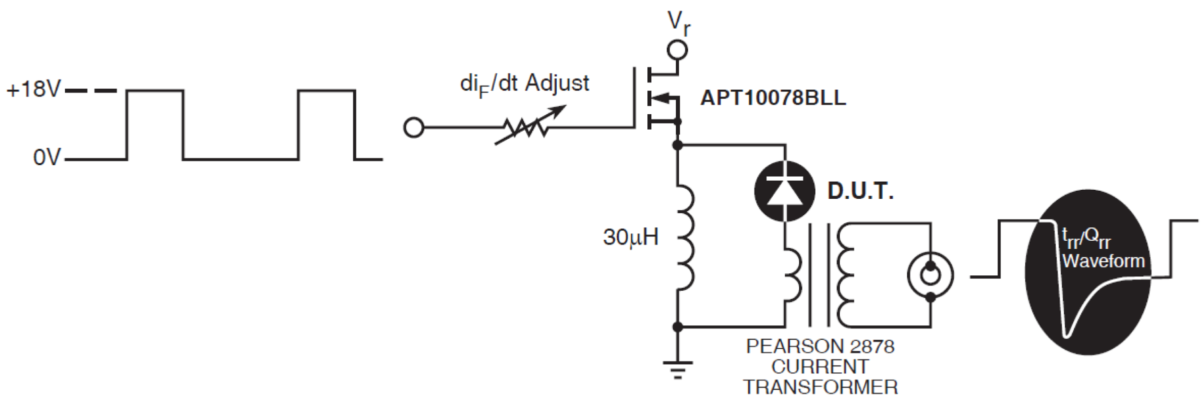
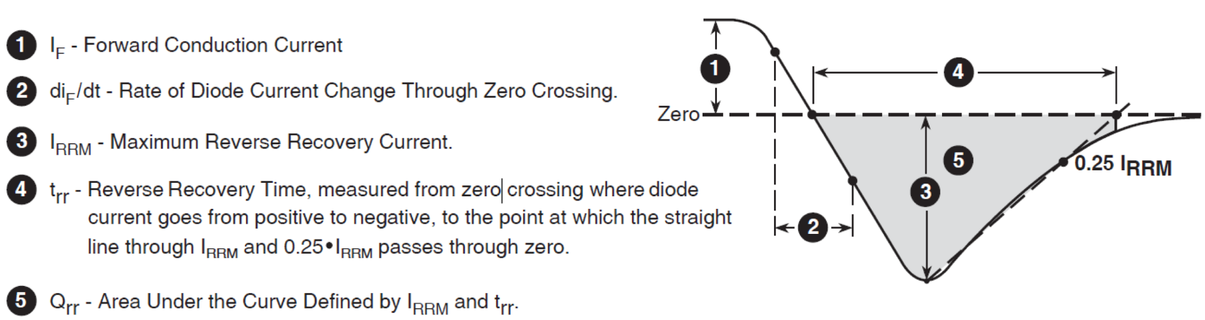


Figure 2-11. Diode Reverse Recovery Waveform and Definitions



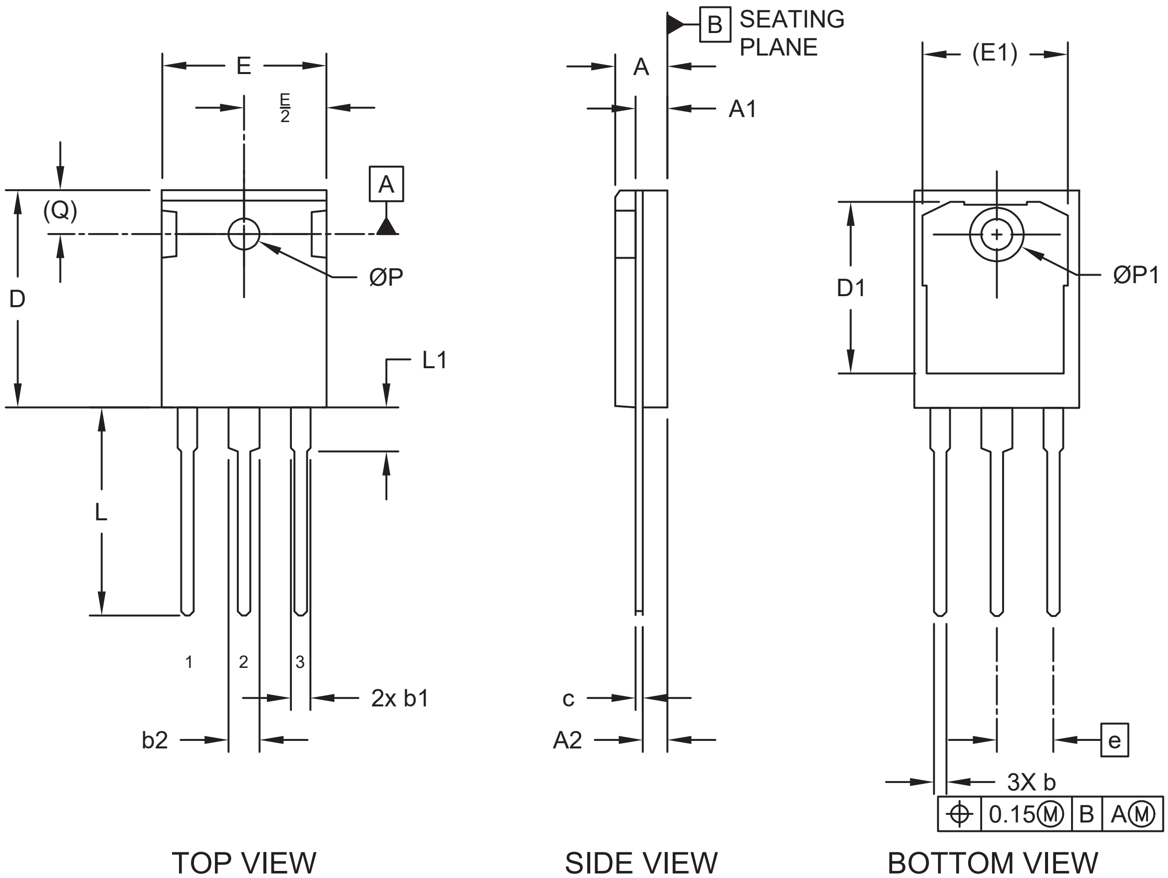
3. Package Specification

This section shows the package specification of this device.

3.1 Package Outline Drawing

The following figure illustrates the TO-247 package outline of this device.

Figure 3-1. Package Outline Drawing



The following table shows the TO-247 dimensions and should be used in conjunction with the package outline drawing.

Table 3-1. TO-247 Dimensions

Dimension Limits		Dimensions (inches)		
		Min.	Nom.	Max.
Number of leads	N	3		
Pitch	e	0.215 BSC		
Overall height	A	0.185	0.197	0.209
Tab height	A1	0.059	0.0785	0.098
Seating plane to lead	A2	0.087	0.0945	0.102
Lead width	b	0.040	0.0475	0.055
Lead shoulder width (×2)	b1	0.065	0.0745	0.084

...........continued

Dimension Limits		Dimensions (inches)		
		Min.	Nom.	Max.
Lead shoulder width	b2	0.113	0.118	0.123
Lead thickness	c	0.016	0.0235	0.031
Lead length	L	0.780	0.790	0.800
Lead shoulder length	L1	0.157	0.167	0.177
Molded body length	D	0.819	0.832	0.845
Thermal pad length	D1	0.650	0.6695	0.689
Total width	E	0.610	0.625	0.640
Thermal pad width	E1	0.531	0.551	0.571
Hole center to tab edge	Q		0.242 REF	
Hole diameter	ØP	0.138	0.144	0.150
Thermal pad hole diameter	ØP1	0.280	0.2875	0.295

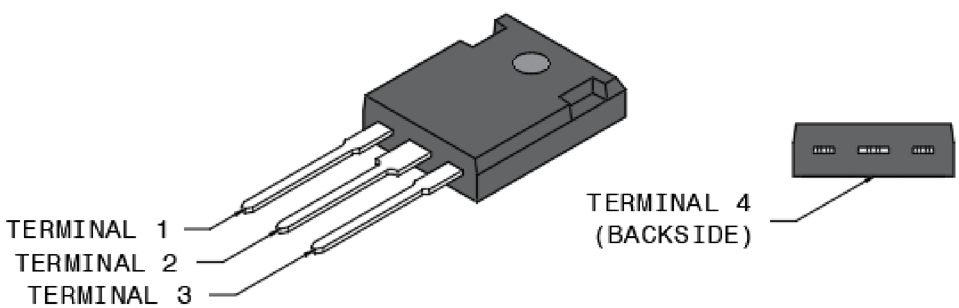
Notes: Dimensioning and tolerancing per ASME Y14.5M

- BSC: Basic dimension—Theoretically exact value shown without tolerances.
- REF: Reference dimension—Usually without tolerance, for information purposes only.

3.2 Terminal Pinout

The following figure illustrates the terminal pinout of this device.

Figure 3-2. Terminal Pinout



The following table shows the electrical signal terminal pinout of this device.

Table 3-2. Electrical Signal Terminal Pinout

Terminal	Definition
TERMINAL 1	Gate
TERMINAL 2	Collector, Diode Cathode
TERMINAL 3	Emitter, Diode Anode
TERMINAL 4	Collector, Diode Cathode

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	02/2024	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00005261A, which replaces the previous Microsemi literature number 050-7446.
Initial releases (Microsemi Revisions A and B)	05/2005 – 06/2005	Initial releases.

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