

PROTECTION PRODUCTS - RailClamp

Description

RailClamps are surge rated diode arrays designed to protect high speed data interfaces. The RClamp series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by **ESD** (electrostatic discharge), **CDE** (cable discharge events), **EFT** (electrical fast transients), and **lightning**.

The unique design of these devices incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.

The RClamp™0508M has a low typical capacitance of 3pF and may be used on lines operating up to 1GHz. This makes the device ideal for protection of high-speed data lines such as USB 2.0, Firewire, DVI, and gigabit Ethernet interfaces.

The low capacitance array configuration allows the user to protect eight high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (15kV air, 8kV contact discharge).

Features

- ◆ ESD protection for high-speed data lines to **IEC 61000-4-2 (ESD) 15kV (air), 8kV (contact) IEC 61000-4-4 (EFT) 40A (5/50ns) IEC 61000-4-5 (Lightning) 12A (8/20µs)**
- ◆ Array of surge rated diodes with internal TVS
- ◆ Small package saves board space
- ◆ Protects eight I/O lines operating up to **1GHz**
- ◆ Low capacitance: **3pF** typical
- ◆ Low clamping voltage
- ◆ Low operating voltage: 5.0V
- ◆ Solid-state silicon-avalanche technology

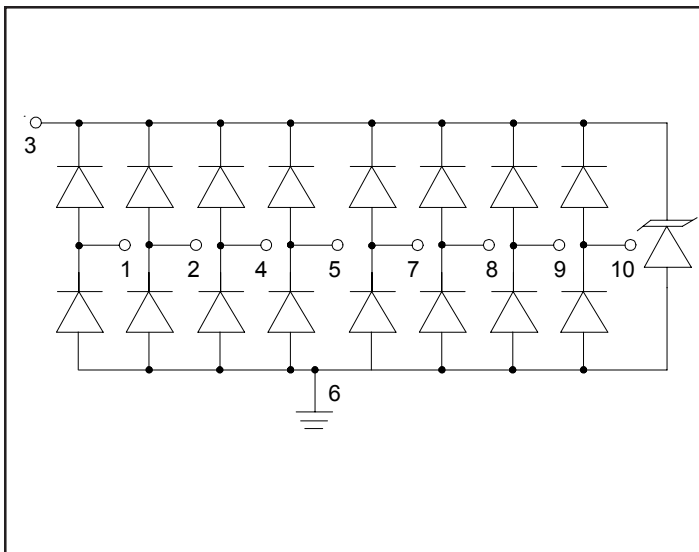
Mechanical Characteristics

- ◆ JEDEC MSOP-10L package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Marking code and date code
- ◆ Packaging : Tape and Reel per EIA 481
- ◆ Lead Finish: Matte Tin

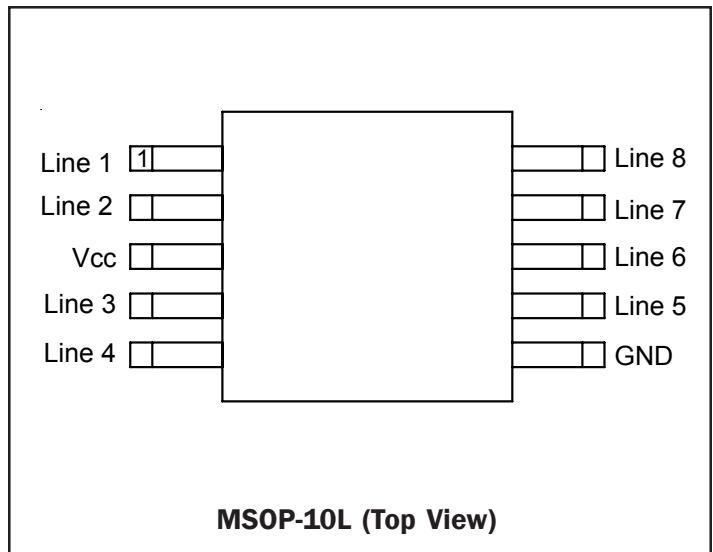
Applications

- ◆ USB 2.0 Power & Data Line Protection
- ◆ Video Graphics Cards
- ◆ Monitors and Flat Panel Displays
- ◆ Digital Video Interface (DVI)
- ◆ High Definition Multi-Media Interface (HDMI)
- ◆ 10/100/1000 Ethernet
- ◆ ATM Interfaces
- ◆ IEEE 1394 Firewire Ports

Circuit Diagram



PIN Configuration



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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	300	Watts
Peak Pulse Current (tp = 8/20μs)	I_{pp}	12	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 8	kV
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

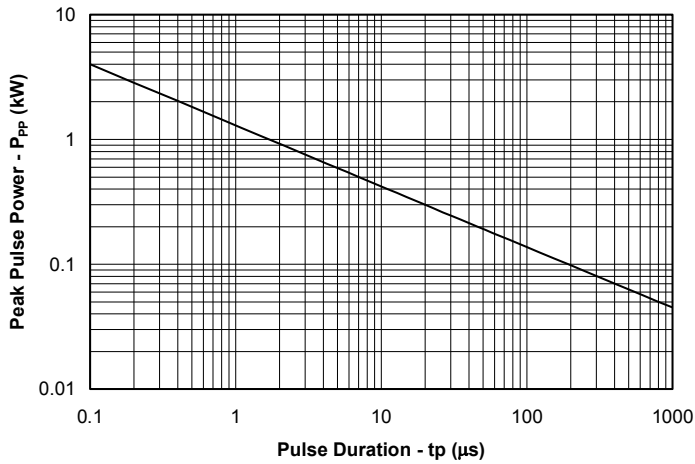
Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 3 to 6			5	V
Reverse Breakdown Voltage	V_{BR}	$I_L = 1mA$ Pin 3 to 6	6			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T=25°C$ Pin 3 to 6			5	μA
Forward Voltage	V_f	$I_f = 15mA$			1.2	V
Clamping Voltage	V_C	$I_{pp} = 1A, tp = 8/20μs$ Any I/O pin to Ground			12.5	V
Clamping Voltage	V_C	$I_{pp} = 5A, tp = 8/20μs$ Any I/O pin to Ground			17.5	V
Clamping Voltage	V_C	$I_{pp} = 12A, tp = 8/20μs$ Any I/O pin to Ground			25	V
Junction Capacitance	C_j	$V_R = 0V, f = 1MHz$ Any I/O pin to Ground		3	5	pF
		$V_R = 0V, f = 1MHz$ Between I/O pins		1.5		pF

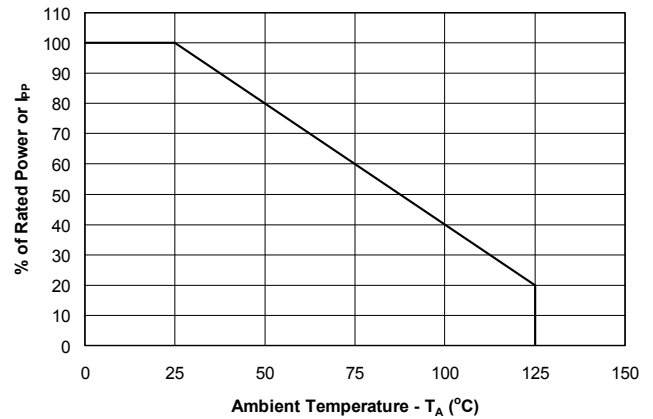
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Typical Characteristics

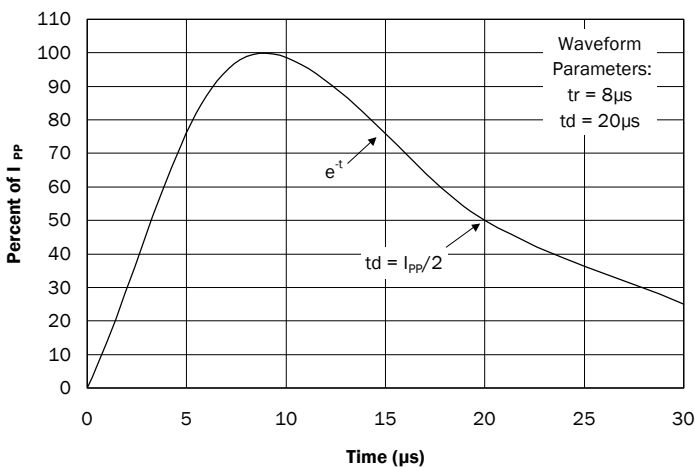
Non-Repetitive Peak Pulse Power vs. Pulse Time



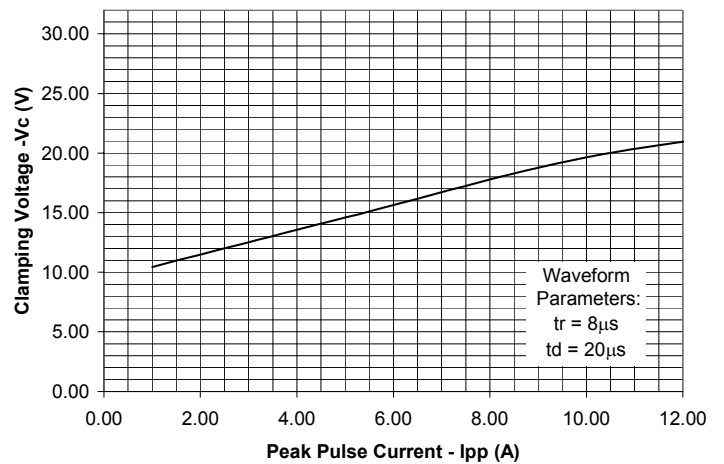
Power Derating Curve



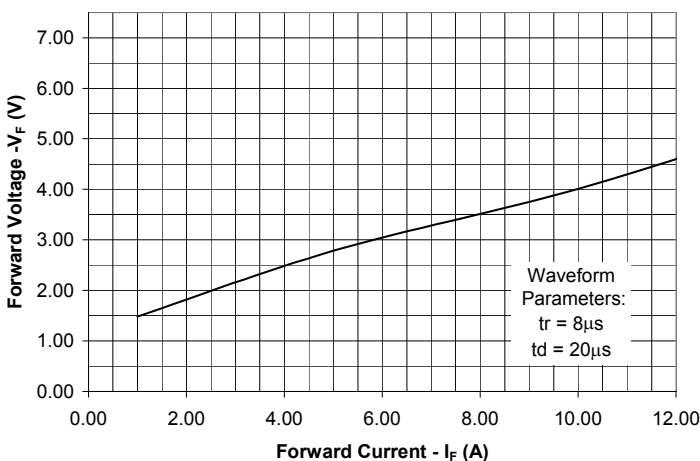
Pulse Waveform



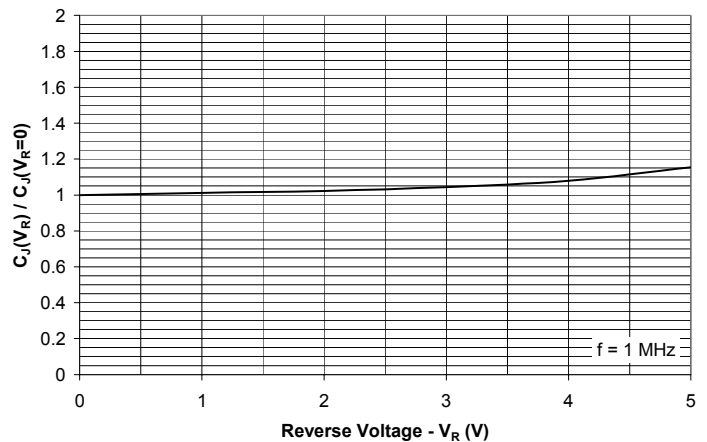
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



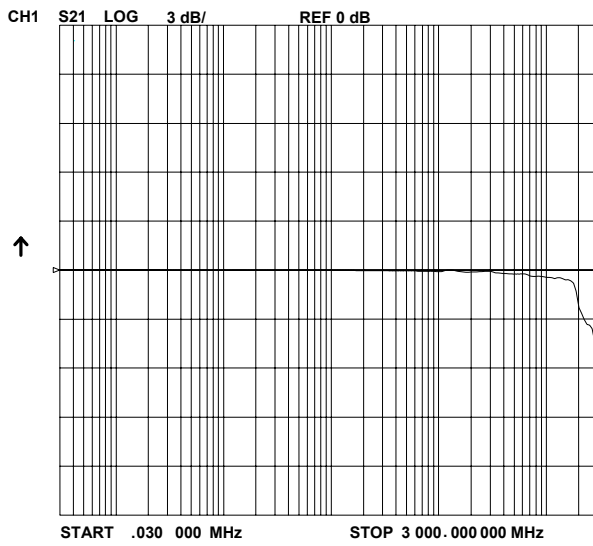
Normalized Capacitance vs. Reverse Voltage



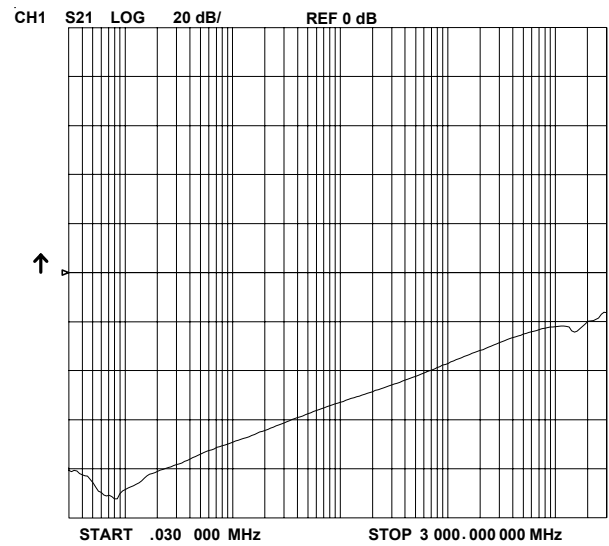
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Typical Characteristics (Con't)

Insertion Loss S21



Analog Cross Talk



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Applications Information

Device Connection Options for Protection of Eight High-Speed Data Lines

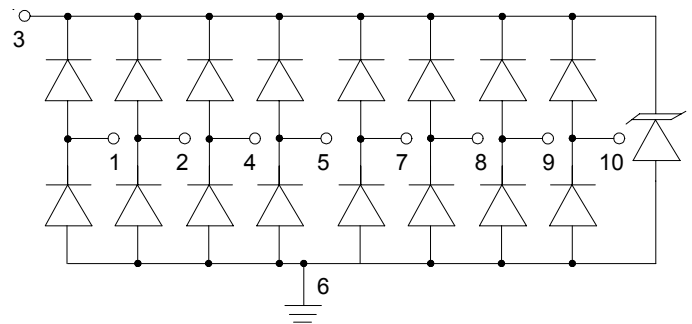
This device is designed to protect eight data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_f) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 2, 4, 5, 7, 8, 9, and 10. The negative reference is connected at pin 6. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pin 3. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 3 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. In applications where the supply rail does not exit the system, the internal TVS may be used as the reference. In this case, pin 3 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

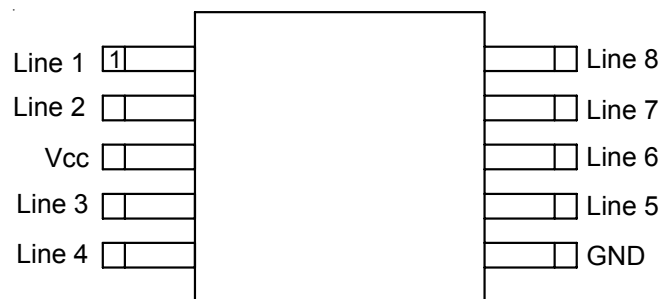
Universal Serial Bus ESD Protection

The RClamp0508M may be used to protect USB 2.0 ports on monitors, computers, peripherals or portable systems. Each device will protect up to four USB ports. When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.

Schematic



Pin Configuration



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Applications Information

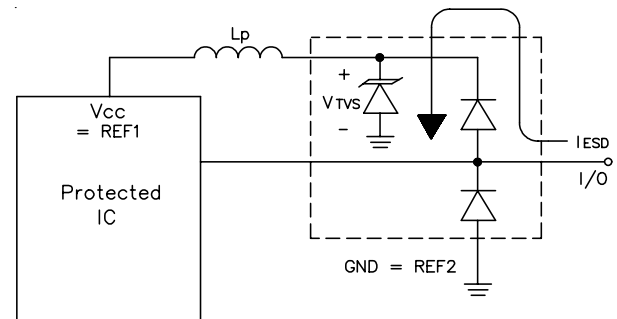
ESD Protection With RailClamps®

RailClamps are optimized for ESD protection using the rail-to-rail topology. They are designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The RailClamp's integrated TVS diode helps to mitigate the effects of parasitic inductance in the power supply connection. During an ESD event, the current will be directed through the integrated TVS diode to ground. The maximum voltage seen by the protected IC due to this path will be the clamping voltage of the device. The line loading capacitance is minimized by using low capacitance steering diodes. The steering diodes are scaled to handle high current ESD events without damage or degradation. The end result is a highly reliable, integrated solution that eliminates the guess work associated with using discrete components.

Matte Tin Lead Finish

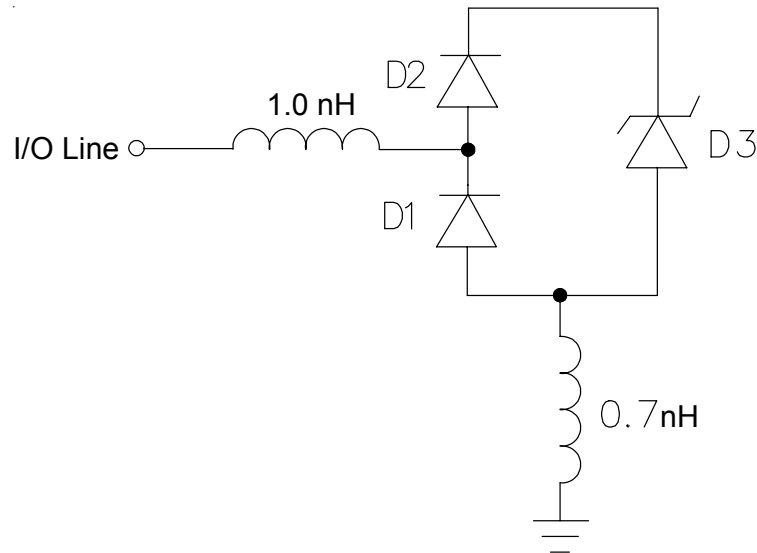
Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Rail-To-Rail Protection Using RailClamp TVS Arrays



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Applications Information - SPICE Model

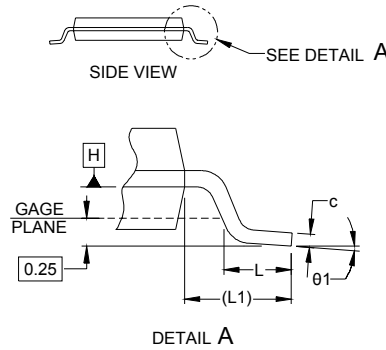
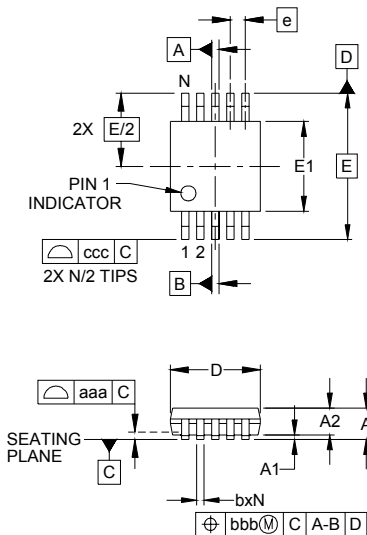


RClamp0508M Spice Model

RClamp0508M Spice Parameters				
Parameter	Unit	D1 (LCRD)	D2 (LCRD)	D3 (TVS)
IS	Amp	10E-14	10E-14	10E-14
BV	Volt	180	20	8.59
VJ	Volt	0.62	0.59	0.6
RS	Ohm	0.31	0.37	0.500
IBV	Amp	1E-3	1E-3	1E-3
CJO	Farad	3E-12	1E-12	360E-12
TT	sec	2.541E-9	2.541E-9	2.541E-9
M	--	0.01	0.01	0.334
N	--	1.1	1.1	1.1
EG	eV	1.11	1.11	1.11

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Outline Drawing - MSOP 10L

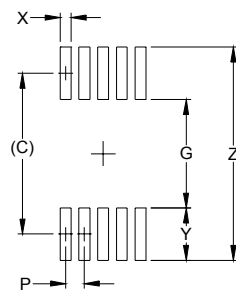


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	10			10		
theta 1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

Land Pattern - MSOP 10L



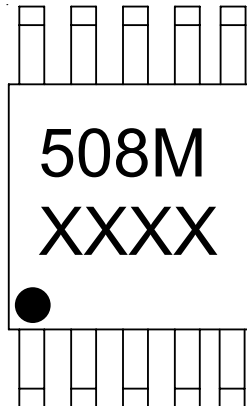
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

PROTECTION PRODUCTS

Marking Codes



- * XXXX = Date Code
- ** Dot indicates Pin 1

Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
RClamp0508M.TBT	Matte Sn	3,000	7 Inch

RailClamp and RClamp are marks of Semtech Corporation

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