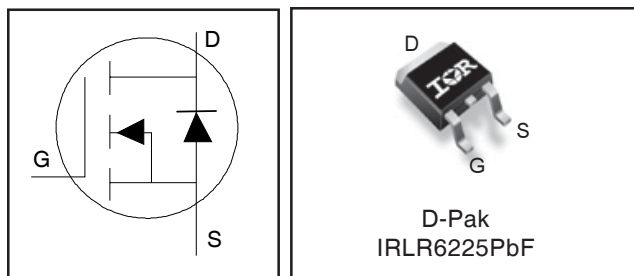


# IRLR6225PbF

HEXFET® Power MOSFET

$V_{DS}$	<b>20</b>	<b>V</b>
$R_{DS(on) \max}$ (@ $V_{GS} = 4.5V$ )	<b>4.0</b>	<b>mΩ</b>
$R_{DS(on) \max}$ (@ $V_{GS} = 2.5V$ )	<b>5.2</b>	<b>mΩ</b>
$Q_g$ (typical)	<b>48</b>	<b>nC</b>
$R_G$ (typical)	<b>2.2</b>	<b>Ω</b>
$I_D$	<b>42</b> <sup>⑥</sup>	<b>A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Applications

- Battery Protection Switch

## Features and Benefits

### Features

Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

results in  
⇒

### Benefits

Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLR6225PbF	D-PAK	Tube/Bulk	75	
IRLR6225TRPbF	D-PAK	Tape and Reel	2000	

## Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	20	V
$V_{GS}$	Gate-to-Source Voltage	±12	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	100 <sup>⑥</sup>	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	63 <sup>⑥</sup>	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	400	
$P_D @ T_C = 25^\circ C$	Power Dissipation <sup>⑤</sup>	63	W
$P_D @ T_C = 100^\circ C$	Power Dissipation <sup>⑤</sup>	25	
	Linear Derating Factor <sup>⑤</sup>	0.5	
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Notes <sup>①</sup> through <sup>⑥</sup> are on page 8

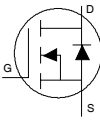
## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	6.6	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	3.2	4.0	mΩ	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 21A ③
		—	4.2	5.2		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 17A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	0.5	0.8	1.1	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50μA
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-4.0	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 12V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -12V
g <sub>fs</sub>	Forward Transconductance	205	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 21A
Q <sub>g</sub>	Total Gate Charge	—	48	72	nC	V <sub>DS</sub> = 10V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 17A See Fig.17 & 18
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	2.6	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	3.6	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	19	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	23	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	23	—		
Q <sub>oss</sub>	Output Charge	—	21	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
R <sub>G</sub>	Gate Resistance	—	2.2	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	9.7	—	ns	V <sub>DD</sub> = 10V, V <sub>GS</sub> = 4.5V I <sub>D</sub> = 17A R <sub>G</sub> = 1.8Ω See Fig.15
t <sub>r</sub>	Rise Time	—	37	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	63	—		
t <sub>f</sub>	Fall Time	—	52	—		
C <sub>iss</sub>	Input Capacitance	—	3770	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 10V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	915	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	650	—		

## Avalanche Characteristics

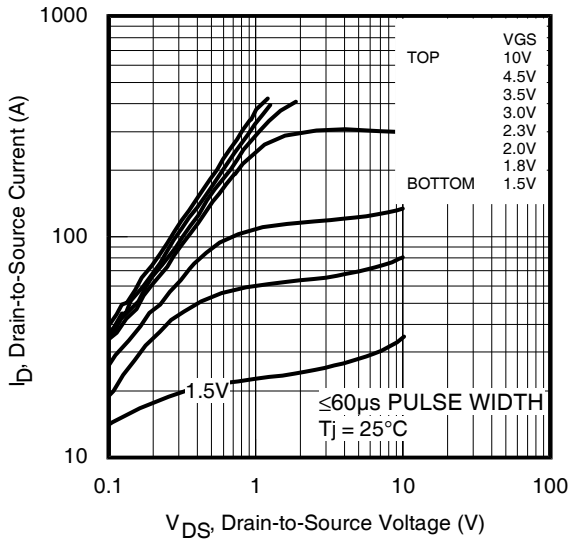
	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	170	mJ
I <sub>AR</sub>	Avalanche Current ①	—	17	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	—	6.3	mJ

## Diode Characteristics

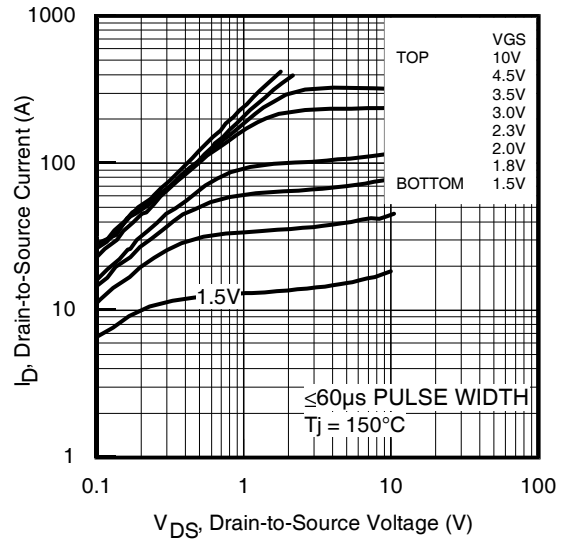
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode) ⑥	—	—	100⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	400		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 17A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	35	53	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 17A, V <sub>DD</sub> = 10V
Q <sub>rr</sub>	Reverse Recovery Charge	—	57	86	nC	di/dt = 200A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Time is dominated by parasitic Inductance				

## Thermal Resistance

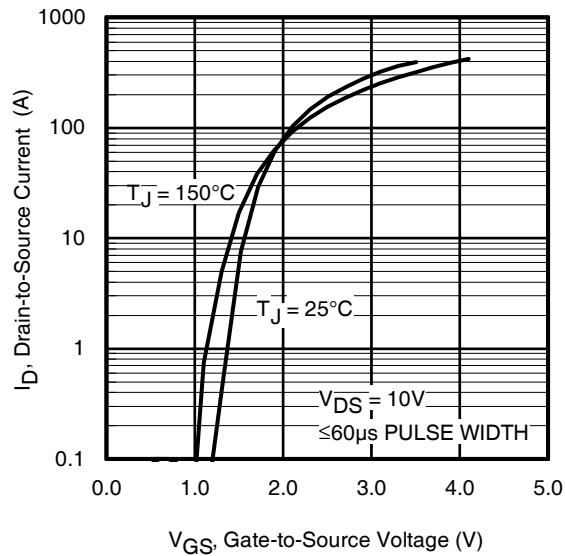
	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ④	—	2.0	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount) ⑤	—	50	
R <sub>θJA</sub>	Junction-to-Ambient ⑤	—	110	



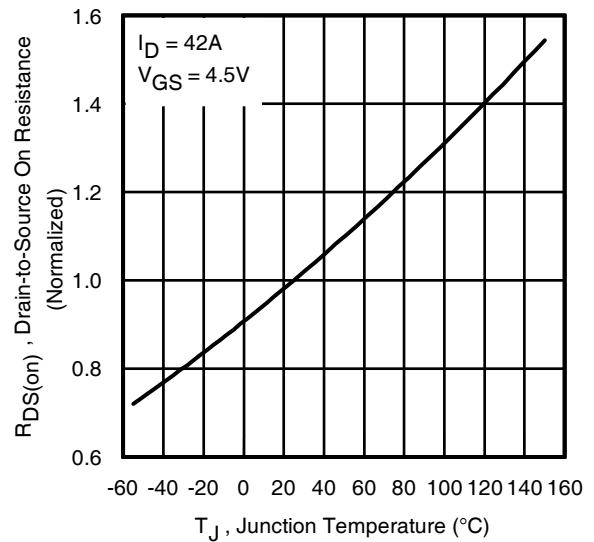
**Fig 1.** Typical Output Characteristics



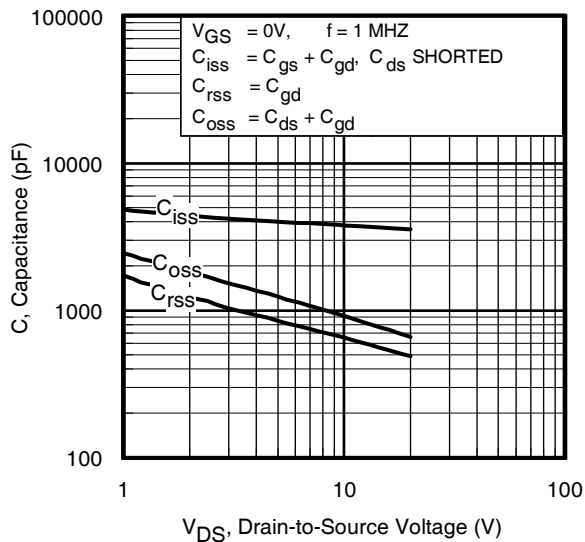
**Fig 2.** Typical Output Characteristics



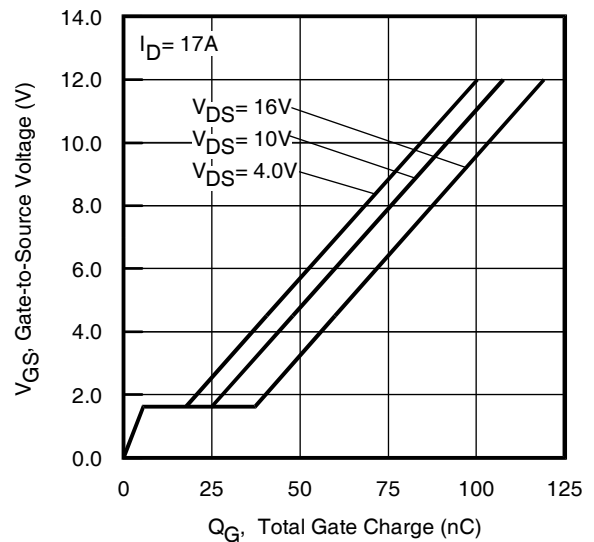
**Fig 3.** Typical Transfer Characteristics



**Fig 4.** Normalized On-Resistance vs. Temperature



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage  
[www.irf.com](http://www.irf.com)



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

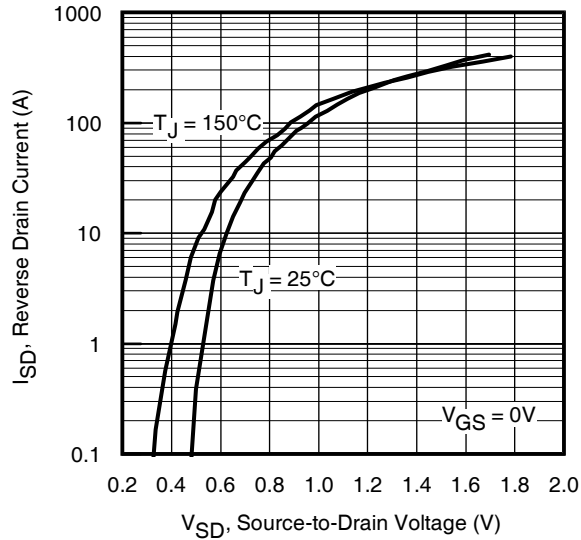


Fig 7. Typical Source-Drain Diode Forward Voltage

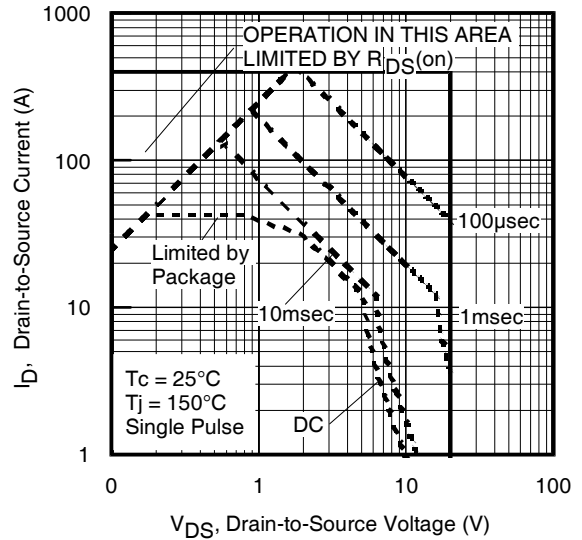


Fig 8. Maximum Safe Operating Area

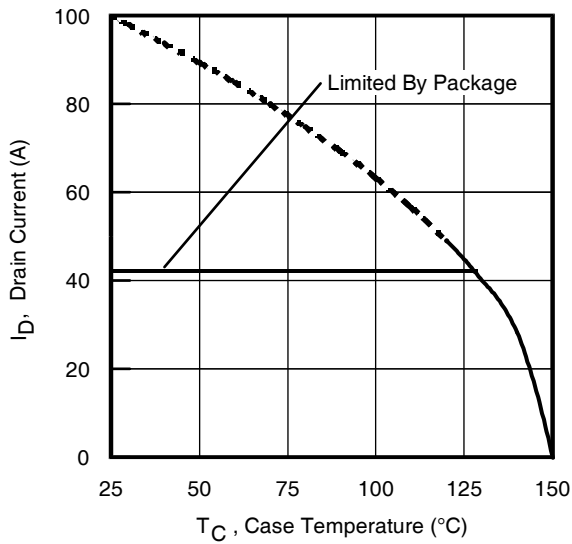


Fig 9. Maximum Drain Current vs. Case (Bottom) Temperature

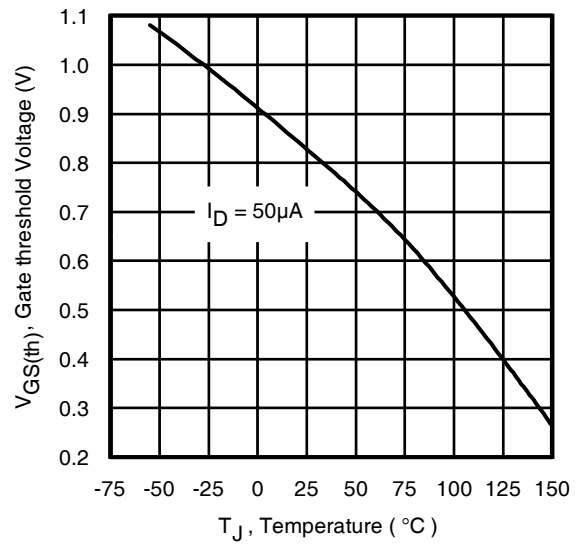


Fig 10. Threshold Voltage vs. Temperature

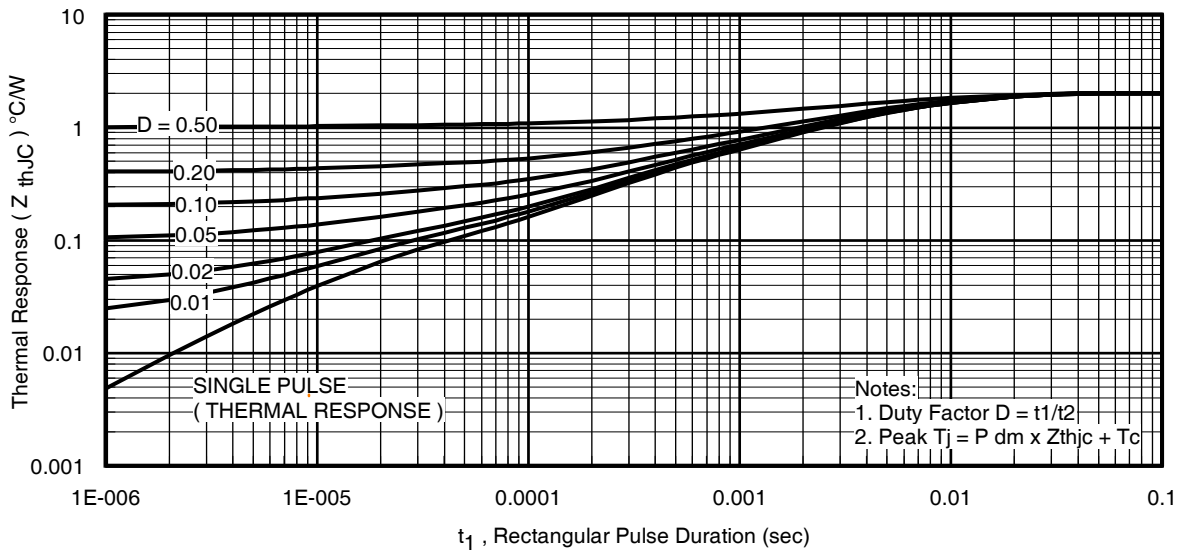
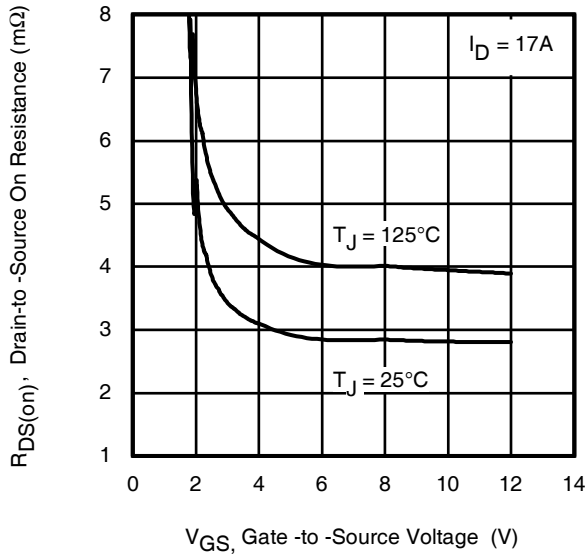
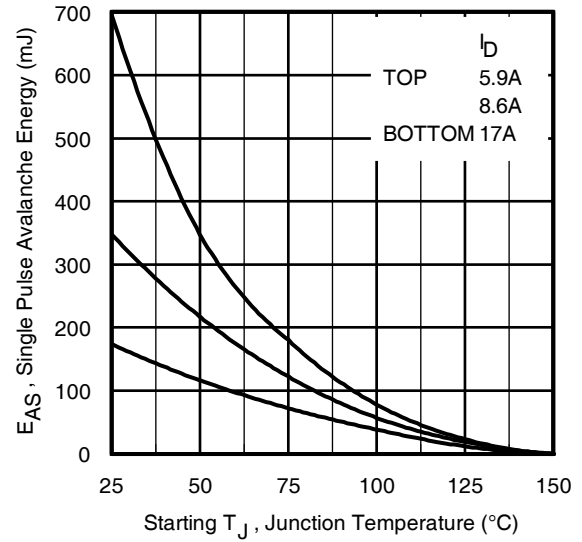


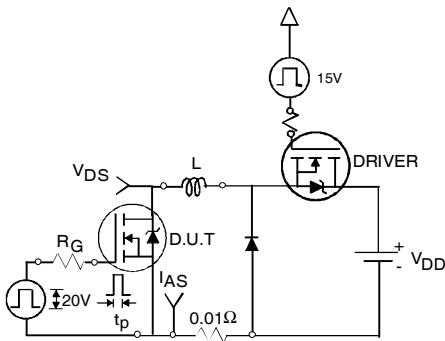
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)



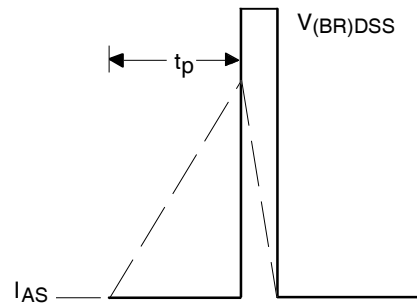
**Fig 12.** On-Resistance vs. Gate Voltage



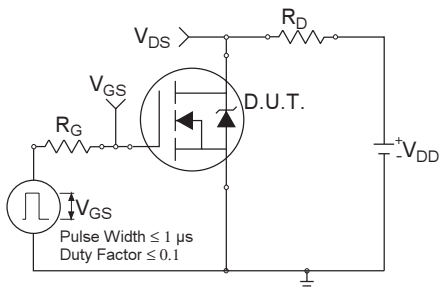
**Fig 13.** Maximum Avalanche Energy vs. Drain Current



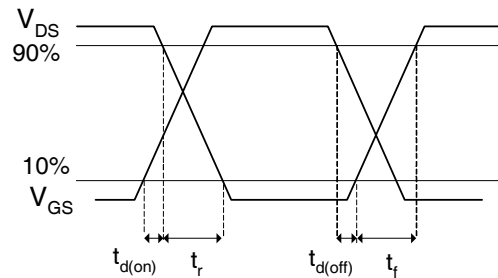
**Fig 14a.** Unclamped Inductive Test Circuit



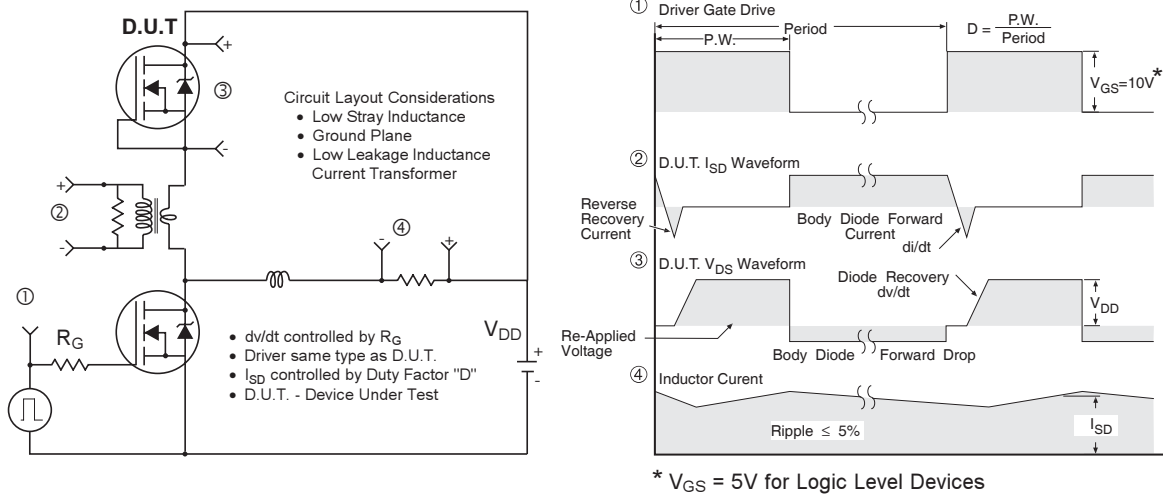
**Fig 14b.** Unclamped Inductive Waveforms



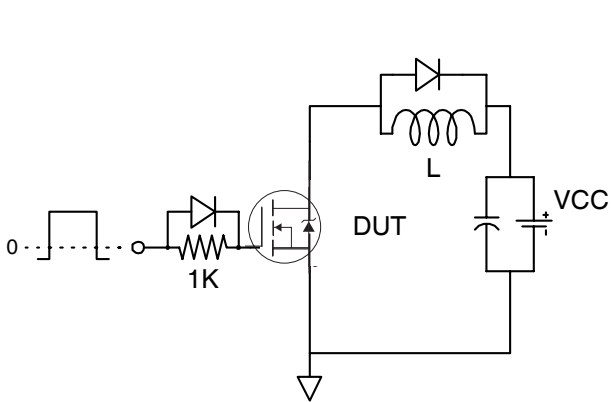
**Fig 15a.** Switching Time Test Circuit



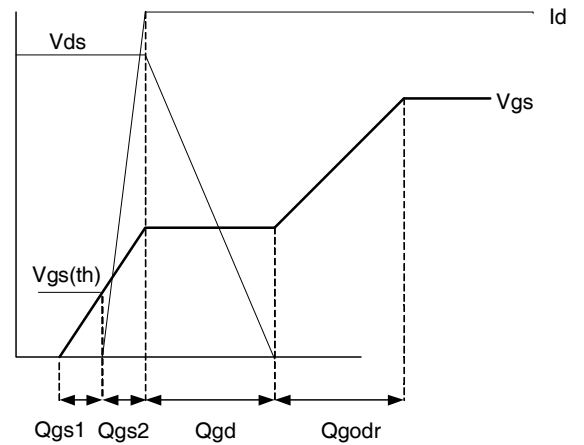
**Fig 15b.** Switching Time Waveforms



**Fig 16. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**



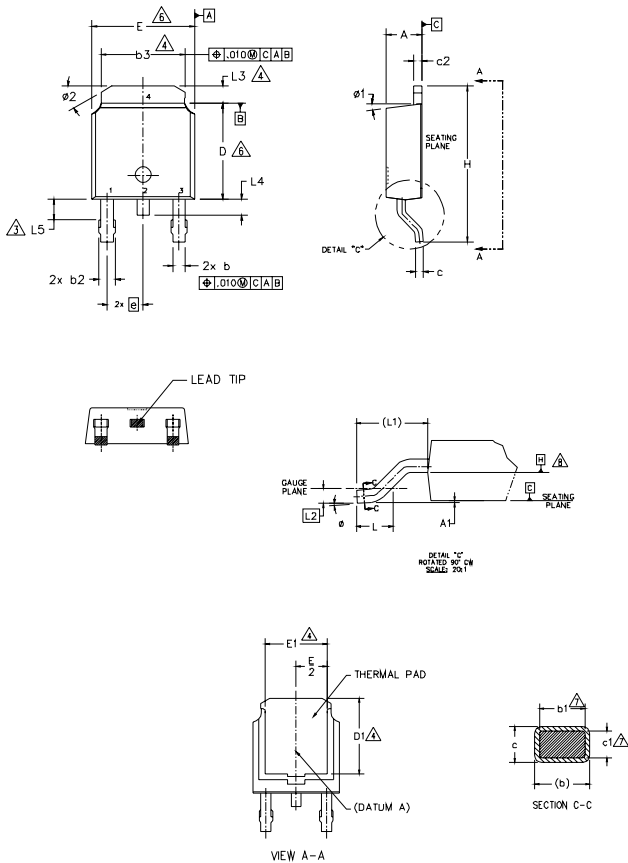
**Fig 17. Gate Charge Test Circuit**



**Fig 18. Gate Charge Waveform**

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
phi	0"	10"	0"	10"	
phi1	0"	15"	0"	15"	
phi2	25"	35"	25"	35"	

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBT & CoPAK**

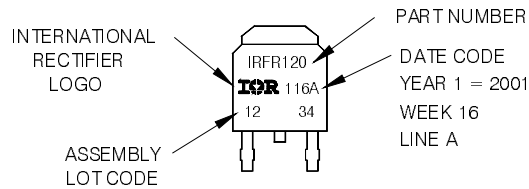
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

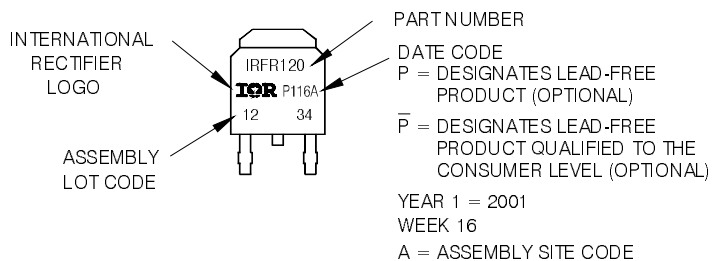
EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"

"P̄" in assembly line position indicates  
"Lead-Free" qualification to the consumer-level



OR

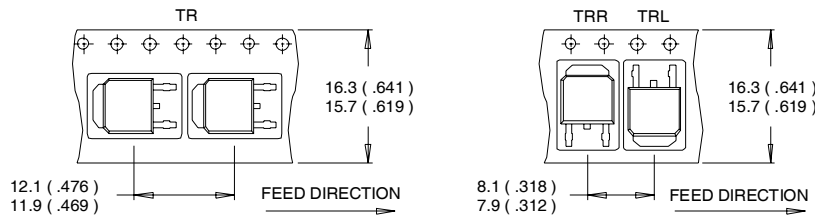


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

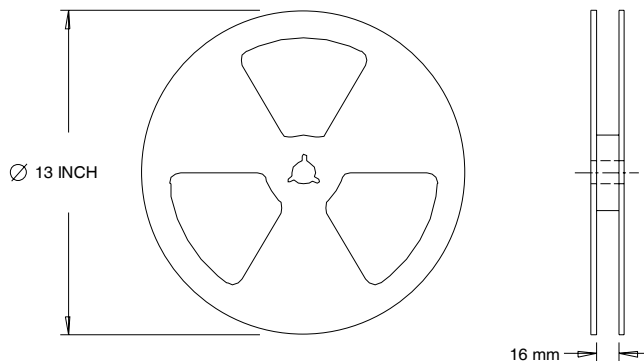
# IRLR6225PbF

## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. OUTLINE CONFORMS TO EIA-481.

### Qualification information<sup>†</sup>

Qualification level	Industrial <sup>††</sup> (per JEDEC JESD47F <sup>†††</sup> guidelines)	
Moisture Sensitivity Level	D-PAK	MSL1 (per JEDEC J-STD-020D <sup>†††</sup> )
RoHS compliant	Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site

<http://www.irf.com/product-info/reliability>

<sup>††</sup> Higher qualification ratings may be available should the user have such requirements.

Please contact your International Rectifier sales representative for further information:

<http://www.irf.com/whoto-call/salesrep/>

<sup>†††</sup> Applicable version of JEDEC standard at the time of product release.

#### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.2\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 17\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package is limited to 42A by production test capability.

Data and specifications subject to change without notice.