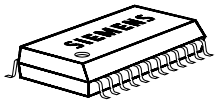
SIEMENS

PLL with I²C Bus for AM/FM Receivers SDA 4331X

1 Overview



P-DSO-24-1

1.1 Features

- 155 MHz FM and 40 MHz AM input frequency
- 30 mVeff AM and 50 mVeff FM sensitivity
- Additional open drain ports controlled by I²C Bus
- 2-pin quartz oscillator
- Fast phase detector with short anti-backlash pulses and polarity reversal
- Charge pump current programmable in four steps up to 4.5 mA
- Frequency resolution of 1, 5 and 10 kHz AM and 12.5, 25 and 50 kHz FM
- P-DSO-24 package

Type	Ordering Code	Package
SDA 4331X	Q67100-H5139	P-DSO-24-1

1.2 Application

The SDA 4331X provides separated input and output ports for AM and FM and is well suited for extremely fast loop settling times in the FM mode.

1.3 Pin Configuration

(top view)

P-DSO-24-1

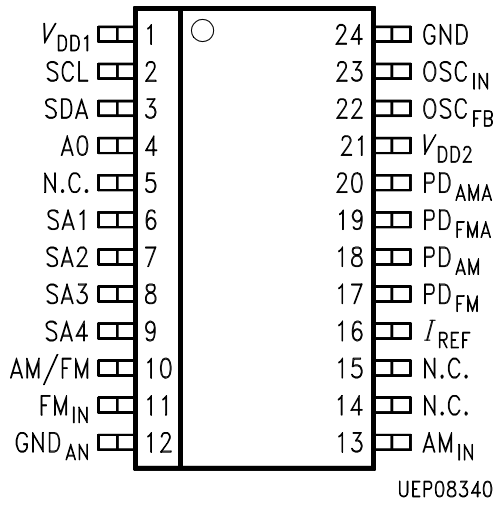


Figure 1

1.4 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
1	V_{DD1}		Supply voltage digital (5 V)
2	SCL	I	Clock I^2C Bus
3	SDA	I/O	Data I^2C Bus
4	A0	I	Address selection, sets the LSB of the IC-address
5	N.C.		
6 … 9	SA1 … SA4	O	10 V open drain output, controlled via I^2C Bus
10	AM/FM	O	10 V open drain output, indicating the operation mode (H = AM)
11	FM_{IN}	I	Input for the FM signal from VCO
12	GND_{AN}		Ground analog
13	AM_{IN}	I	Input for the AM signal from VCO
14	N.C.		
15	N.C.		
16	I_{REF}	I	Reference current, setting the base current level for the charge pumps
17	PD_{FM}	O	FM charge pump output
18	PD_{AM}	O	AM charge pump output
19	PD_{FMA}	O	Source follower output FM
20	PD_{AMA}	O	Source follower output AM
21	V_{DD2}		Supply voltage digital for charge pump and source followers (up to 10 V)
22	OSC_{FB}	I/O	Oscillator feedback, quartz terminal
23	OSC_{IN}	I	Oscillator input, quartz terminal, optionally input for external reference
24	GND		Ground digital

1.5 Functional Block Diagram

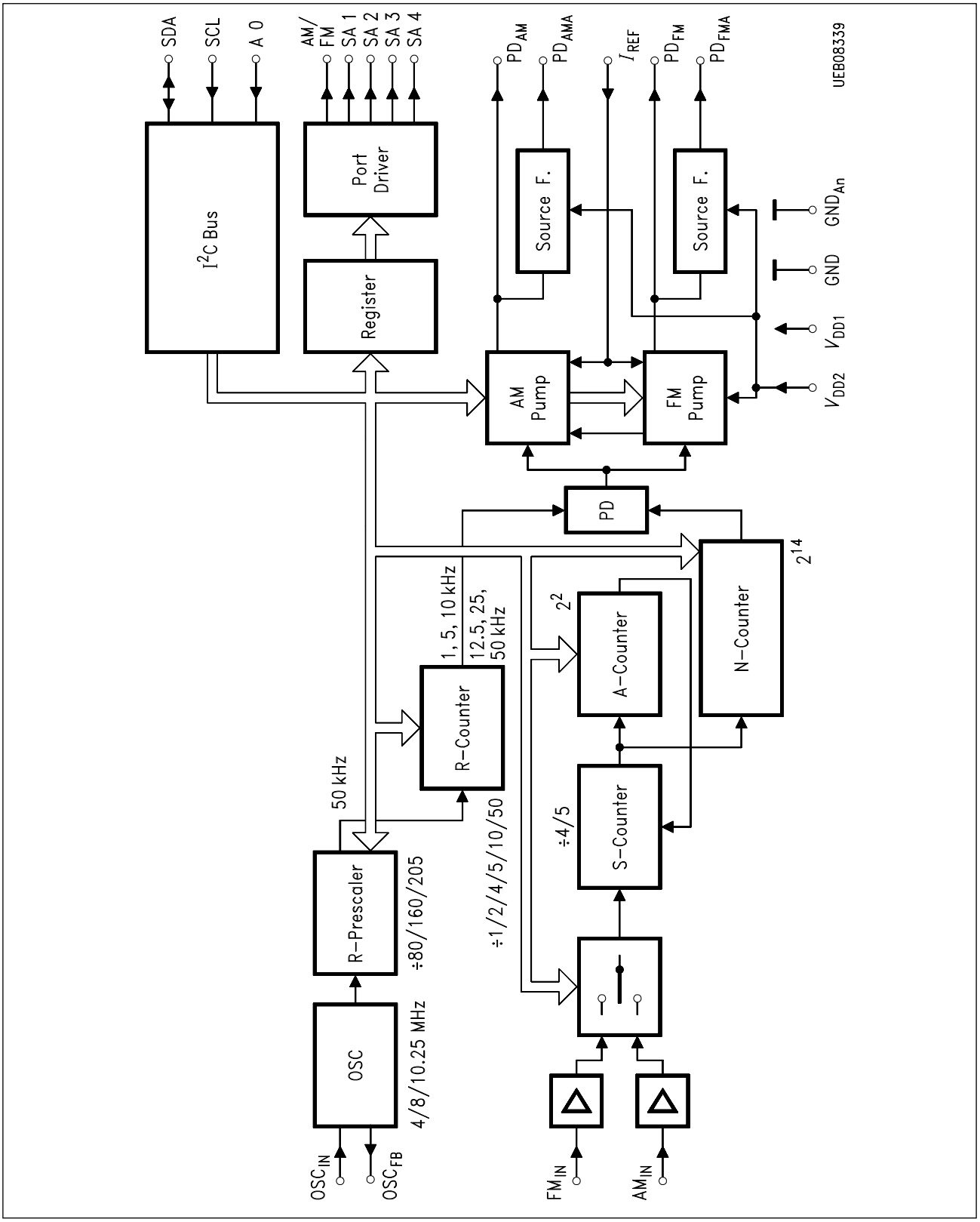


Figure 2
Block Diagram

2 Functional Description

The SDA 4331X is a radio PLL controlled via I²C Bus for frequency synthesis in the AM and FM range.

3 Circuit Description

The reference frequency for the PLL is derived from the quartz oscillator OSC[1)]. The R-prescaler can be adapted to quartz frequencies of 4, 8 or 10.25 MHz, respectively, yielding an internal 50 kHz reference. Programming the R-counter sets the phase detector reference frequency to 1, 5 or 10 kHz in the AM mode or to 12.5, 25 or 50 kHz in the FM mode. The VCO frequency is set by programming the A/N-counter which operates as dual-modulus counter for FM and AM using a divide by 4/5 swallow counter.

The phase detector drives two different charge pumps for AM and FM mode. Additional source followers are connected to the charge pump. There are four programmable current levels for each charge pump. The supply voltage for the charge pump and the source followers is supplied via the V_{DD2} pin and can reach 10 V maximum. AM/FM is an open drain output as well as the additional outputs SA1 … SA4 which are controlled by I²C Bus.

The I²C Bus interface provides slave receiver functions. There are two addresses selected by the A0 pin. The I²C-protocol (see **diagram 1**) contains one string for programming all counters and functions. The transfer may be stopped optionally after each word if the remaining functions are not to be altered. After power ON all control signals are undefined, so that the complete write sequence must be executed.

[1)] The power dissipation of the quartz is given by:
$P_V = 2 \times R_1 (\Pi \times f_Q \times (C_O + C_L) \times V_{DD})^2$
R_1 … Series resistance of the quartz
f_Q … Quartz frequency
C_O … Parallel capacitance of the quartz
C_L … Load capacitance, including input capacitance of the IC

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

T_A = – 25 °C to 85 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{DD1}	– 0.3	6	V	
Supply voltage	V_{DD2}	– 0.3	10.5	V	
Input voltage	V_{IN}	– 0.3	V_{DD1} + 0.3	V	
Power dissipation per output	P_Q		10	mW	
Power dissipation	P_{tot}		t.b.d.	mW	
Storage temperature	T_S	– 40	125	°C	
Output voltage SA1 … SA4, AM/FM	V_{QH}		10.5	V	
ESD voltage (HBM: 1.5 kΩ, 100 pF)	V_{ESD}	– 1	1	kV	

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

4.2 Operational Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD1}	4.5	5	5.5	V
Supply voltage	V_{DD2}	9		10.3	V
Supply current	I_{DD1}		4	10	mA
Supply current[1)]	I_{DD2}			0.5	mA
Ambient temperature	T_A	– 25		+ 85	°C
Output voltage SA1 … SA4, AM/FM	V_{QH}			V_{DD2}	V

[1)] Measurement conditions: No load on pins 17 … 20.

Note: In the operating range the functions given in the circuit description are fulfilled.

4.3 AC/DC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input AM_{IN}						
Input voltage (sine wave)	V_{IN}	30			mVeff	V_{DD1} = 4.5 V 0.5 MHz < f_{IN} < 40 MHz
Input capacitance	C			4	pF	
Input current	I_{IN}	– 50		50	µA	$0 \le V_{IN} \le V_{DD1}$
Input FM_{IN}						
Input voltage (sine wave)	V_{IN}	 50 120			 mVeff mVeff	V_{DD1} = 4.5 V 20 MHz < f_{IN} < 120 MHz 10 MHz < f_{IN} < 155 MHz
Input capacitance	C			4	pF	
Input current	I_{IN}	– 100		100	µA	$0 \le V_{IN} \le V_{DD1}$
Input OSC_{IN}						
Input voltage (sine wave)	V_{IN}	 100 150 200			 mVeff mVeff mVeff	V_{DD1} = 4.5 V f_{IN} = 4 MHz f_{IN} = 8 MHz f_{IN} = 10.25 MHz
Input capacitance	C			10	pF	
Input current	I_{IN}	– 30		30	µA	$0 \le V_{Q} \le V_{DD1}$
Input/Output SDA						
H-input voltage	V_{IH}	$0.7 \times V_{DD1}$		V_{DD1}	V	
L-input voltage	V_{IL}	0		$0.3 \times V_{DD1}$	V	
L-output voltage	V_{QL}			0.4	V	I_{QL} = 3 mA, V_{DD1} = 5 V, C_L = 400 pF
Input leakage current	$I_{Leakage}$	– 10		10	µA	$0 \le V_{IN} \le V_{DD1}$
Input capacitance	C			10	pF	

4.3 AC/DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Inputs SCL, A0						
H-input voltage	V_{IH}	$0.7 \times V_{DD1}$		V_{DD1}	V	
L-input voltage	V_{IL}	0		$0.3 \times V_{DD1}$	V	
Input leakage current	$I_{Leakage}$	– 10		10	µA	$0 \le V_{IN} \le V_{DD1}$
Input capacitance	C			10	pF	
Outputs SA1, SA2, SA3, SA4, AM/FM (open drain outputs)						
L-output voltage	V_{QL}			0.4	V	I_{QL} = 1 mA V_{DD1} = 5 V
	V_{QL}			0.1	V	I_{QL} = 0.1 mA
Input I_{REF}						
Input current	I_{IN}	t.b.d.	100	t.b.d.	µA	
Voltage at I_{REF}	V_{IREF}		1.2		V	I_{IN} = 100 µA
Output PD_{FM}						
PD current A	I_Q		± 4.5		mA	V_{PD} = 4 V
PD current B	I_Q		± 3		mA	
PD current C	I_Q		± 1.5		mA	
PD current D	I_Q		± 150		µA	
Output PD_{AM}						
PD current A	I_Q		± 450		µA	V_{PD} = 4 V
PD current B	I_Q		± 300		µA	
PD current C	I_Q		± 150		µA	
PD current D	I_Q		± 30		µA	

4.3 AC/DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output PD_{FMA}						
H-output voltage	V_{QH}	7.5	7.7		V	I_{QH} = 2 mA $V_{PD\,FM} = V_{DD2}$ = 9 V
H-output current	I_{QH}		2	5	mA	$V_{PD\,FM} = V_{DD2}$ = 9 V
L-output current	I_{QL}	10			µA	$V_{PD\,FM}$ = GND V_Q = 4 V
Output PD_{AMA}						
H-output voltage	I_{QH}		1	2.5	mA	$V_{PD\,AM}$ = 5 V
L-output current	I_{QL}	0.1			mA	$V_{PD\,AM}$ = GND V_Q = 5 V

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

Table 1
Programming of Mode and Frequency Resolution

AM/FM	R1	R0	Mode	Frequency Resolution [MHz]
0	0	1	FM	12.5
0	1	0	FM	25
0	1	1	FM	50
1	0	1	AM	1
1	1	0	AM	5
1	1	1	AM	10

Table 2
Programming R-prescaler

RP1	RP0	Divide Ratio	Quartz Frequency [MHz]
0	0	1:1	Test mode only
0	1	1:80	4
1	0	1:160	8
1	1	1:205	10.25

Table 3
Programming Phase Detector

PD1	PD0	Current Level
0	0	D
0	1	C
1	0	B
1	1	A

PPD	Polarity
0	Normal
1	Invers

Table 4
Programming Test Mode

T1	T2	SA1	SA2	SA3	SA4
0	0	Controlled by I^2C Bus			
1	0	PD_MUX	Clk_50 kHz	N_A_CLN	

T3	Operation
0	Normal
1	Test reset

Diagram 1: I²C Protocol

Slave-receive (Write)

START
1
1
0
0
1
0
0/1
0
ACK
MSB
N14
N13
N12
N11
N10
N9
N8
ACK
N7
N6
N5
N4
N3
N2
N1
LSB
ACK

A/N-counter

[STOP or START]
AM/FM
PD1
PD0
IF
SA4
SA3
SA2
SA1
ACK
[STOP or START]
G1
G0
F0
R1
R0
RP1
RP0
0
ACK
[STOP or START]
PPD
T0 (= 0)
T1 (= 0)
T2 (= 0)
T3 (= 0)
X
X
X
ACK
STOP or START

[STOP or START]:
Optional STOP or START condition, after power ON the complete sequence has to be programmed.

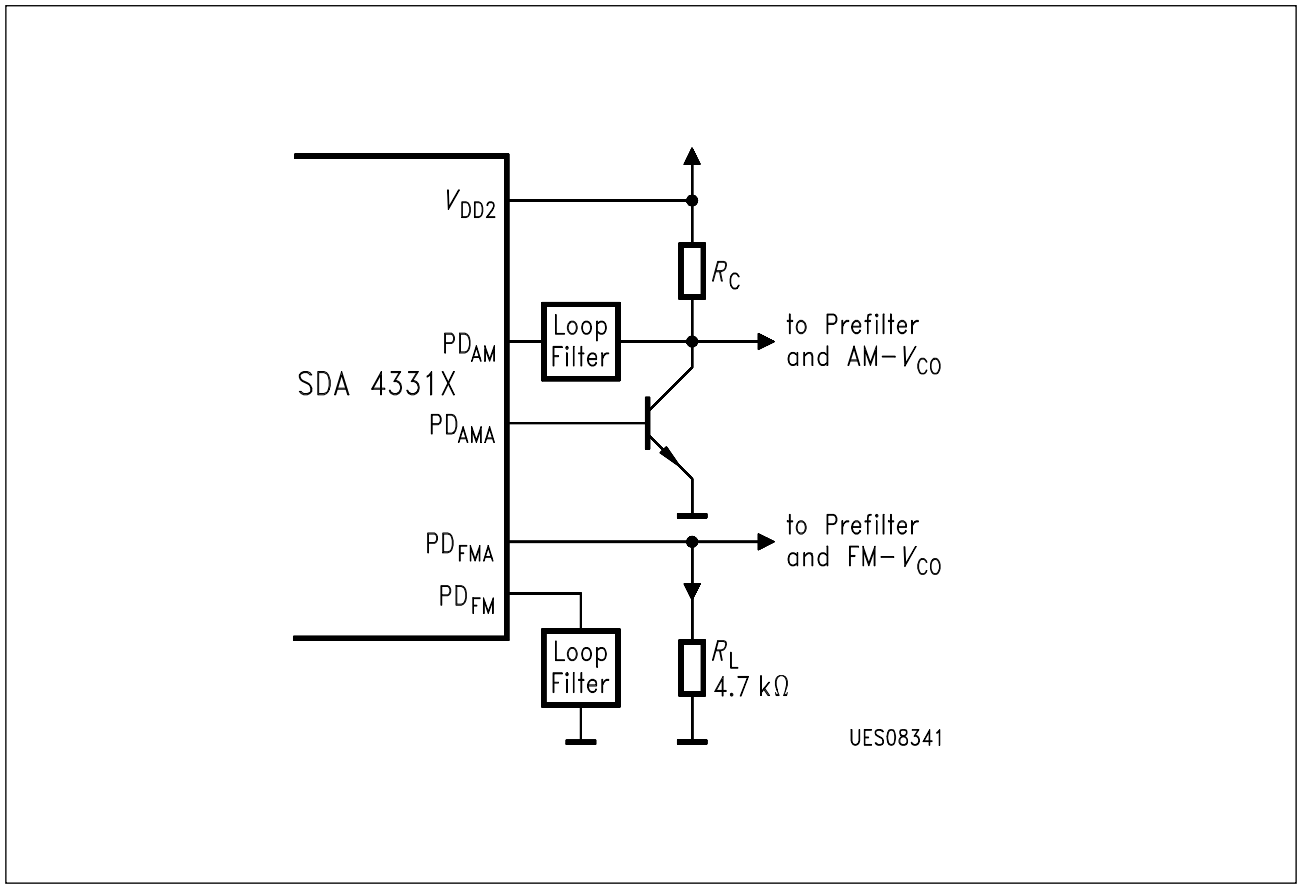
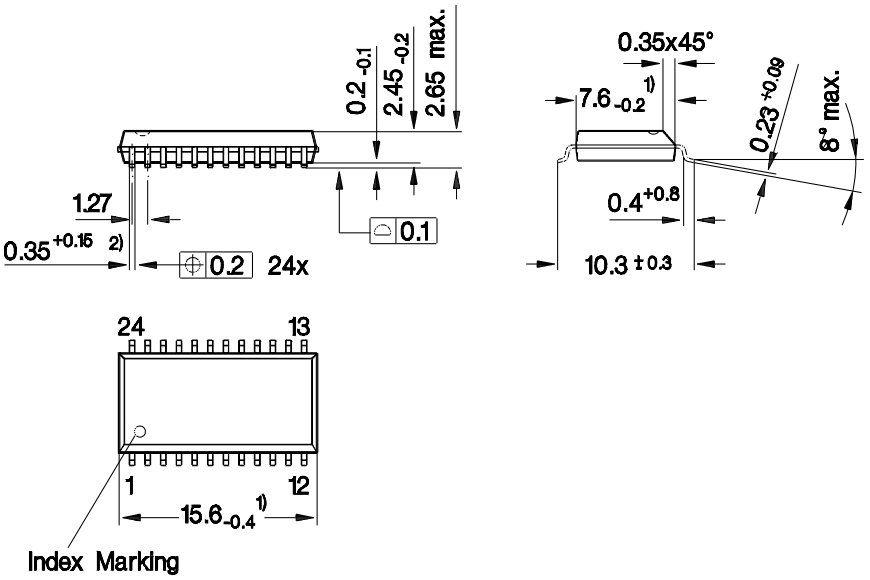


Figure 3
Application Circuit for AM and FM Charge Pump Output

5 Package Outlines

P-DSO-24-1
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

GPS05144

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm