



# FDN86265P

## P-Channel PowerTrench<sup>®</sup> MOSFET

-150 V, -0.8 A, 1.2 Ω

### Features

- Max  $r_{DS(on)}$  = 1.2 Ω at  $V_{GS} = -10\text{ V}$ ,  $I_D = -0.8\text{ A}$
- Max  $r_{DS(on)}$  = 1.4 Ω at  $V_{GS} = -6\text{ V}$ ,  $I_D = -0.7\text{ A}$
- Very low RDS-on mid voltage P-channel silicon technology optimised for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL tested
- RoHS Compliant

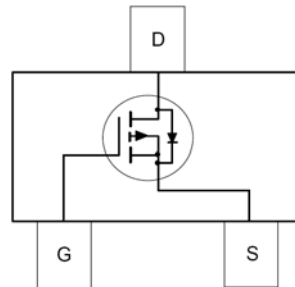
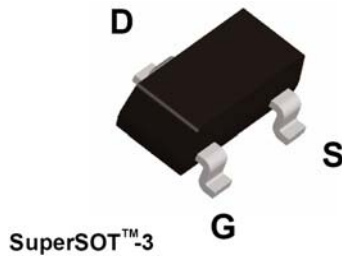


### General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been optimized for the on-state resistance and yet maintain superior switching performance.

### Applications

- Active Clamp Switch
- Load Switch



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	-150	V
$V_{GS}$	Gate to Source Voltage	±25	V
$I_D$	-Continuous (Note 1a)	-0.8	A
	-Pulsed	-5	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	6	mJ
$P_D$	Power Dissipation (Note 1a)	1.5	W
	Power Dissipation (Note 1b)	0.6	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	80	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
265	FDN86265P	SSOT-3	7"	8 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-129		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -120\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	-2	-3.3	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{ V}$ , $I_D = -0.8\text{ A}$		0.85	1.2	$\Omega$
		$V_{GS} = -6\text{ V}$ , $I_D = -0.7\text{ A}$		0.96	1.4	
		$V_{GS} = -10\text{ V}$ , $I_D = -0.8\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		1.54	2.2	
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{ V}$ , $I_D = -0.8\text{ A}$		1.5		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		158	210	pF
$C_{oss}$	Output Capacitance			17	25	pF
$C_{rss}$	Reverse Transfer Capacitance			1.6	5	pF
$R_g$	Gate Resistance		0.1	3.3	6.7	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -75\text{ V}$ , $I_D = -0.8\text{ A}$ , $V_{GS} = -10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		5.7	12	ns
$t_r$	Rise Time			2.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			7.9	16	ns
$t_f$	Fall Time			9.9	20	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } -10\text{ V}$	$V_{DD} = -75\text{ V}$ , $I_D = -0.8\text{ A}$	2.9	4.1	nC
$Q_{gs}$	Gate to Source Gate Charge			0.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			0.8		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -0.8\text{ A}$ (Note 2)		-0.86	-1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = -0.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		49	78	ns
$Q_{rr}$	Reverse Recovery Charge			70	112	nC

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $80\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper

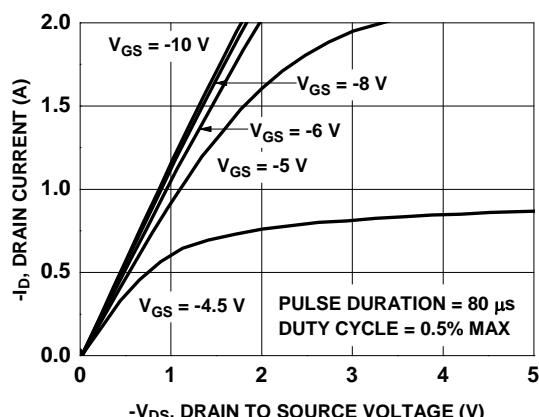


b)  $180\text{ }^\circ\text{C/W}$  when mounted on a minimum pad.

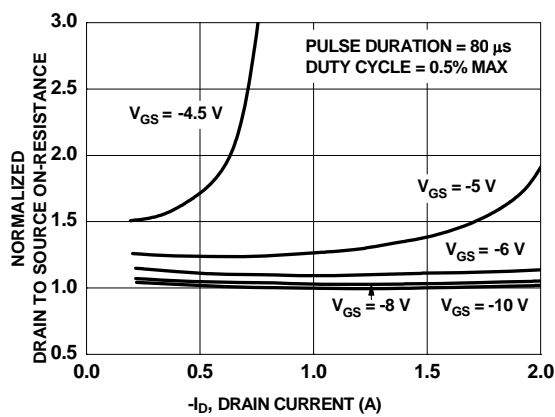
- Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

- Starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 3\text{ mH}$ ,  $I_{AS} = -2\text{ A}$ ,  $V_{DD} = -150\text{ V}$ ,  $V_{GS} = -10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = -9\text{ A}$ .

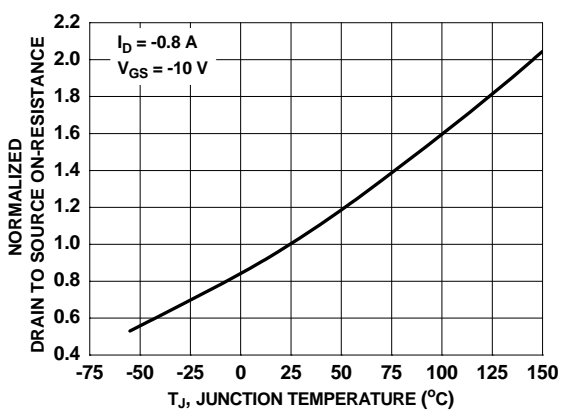
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



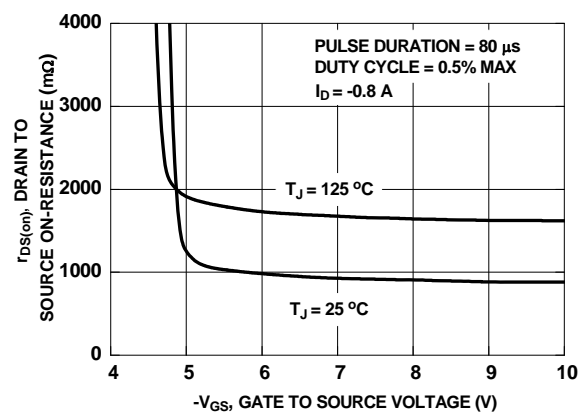
**Figure 1. On Region Characteristics**



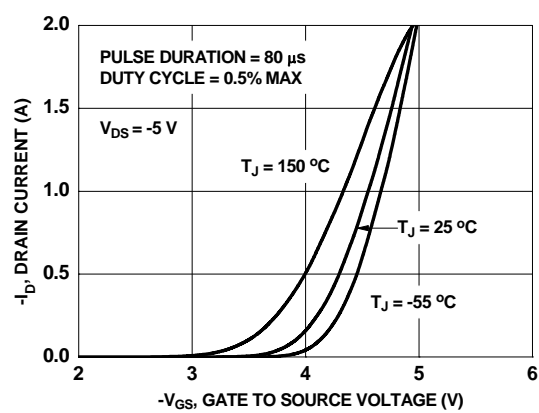
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



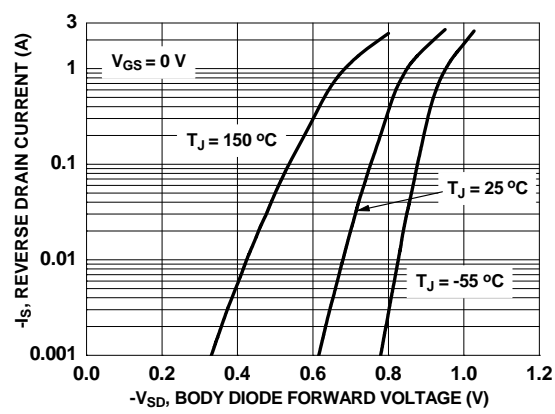
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

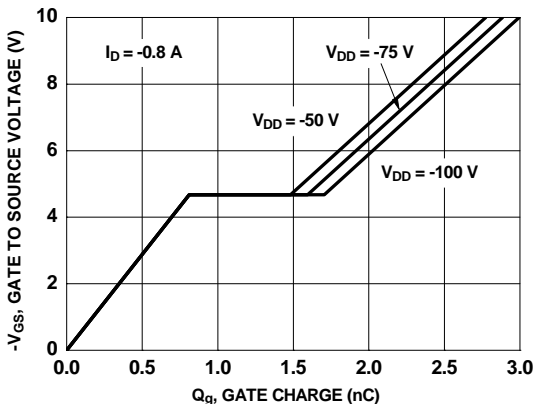


**Figure 5. Transfer Characteristics**

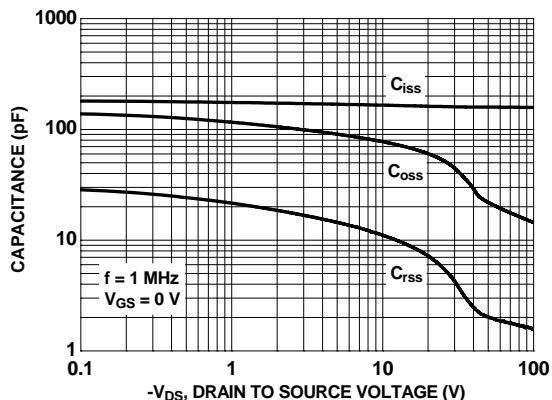


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

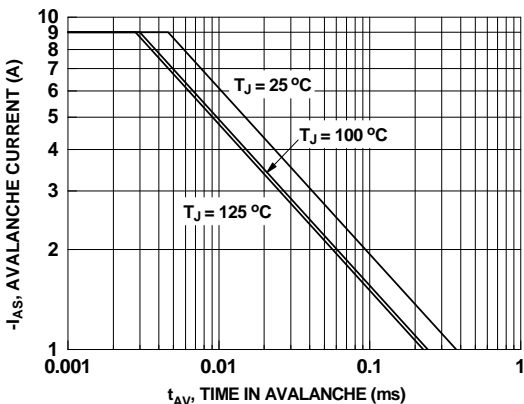
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



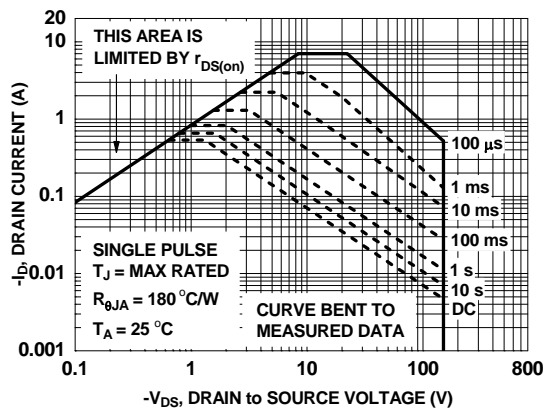
**Figure 7. Gate Charge Characteristics**



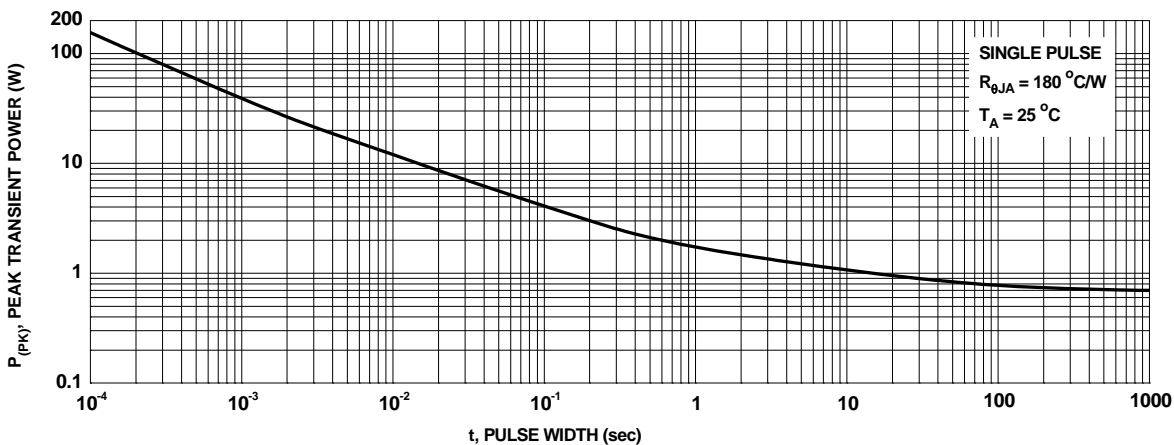
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Unclamped Inductive Switching Capability**

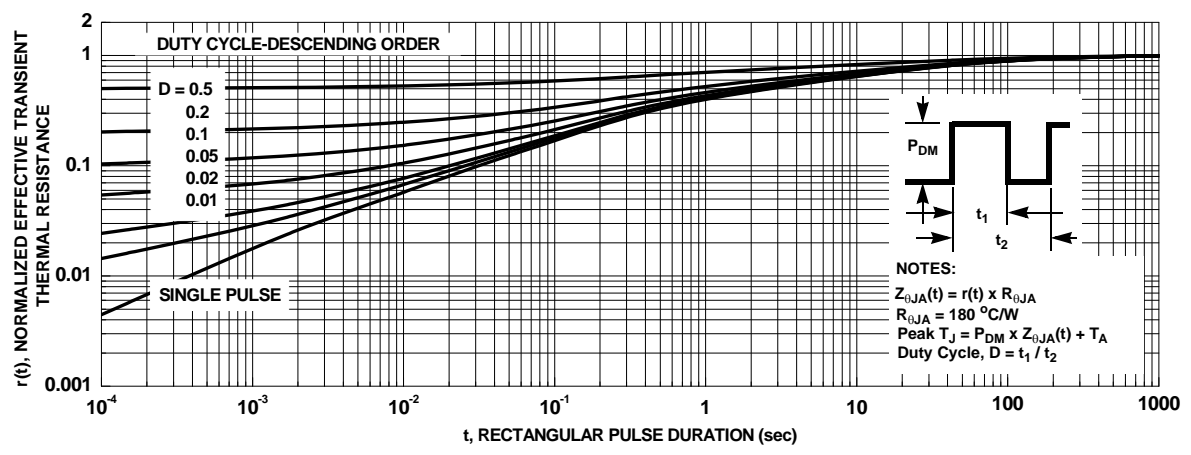


**Figure 10. Forward Bias Safe Operating Area**



**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted







**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**



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