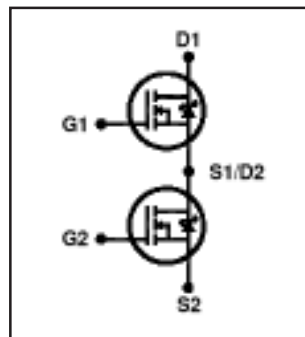


# IRFI4212H-117P

## Features

- Integrated half-bridge package
- Reduces the part count by half
- Facilitates better PCB layout
- Key parameters optimized for Class-D audio amplifier applications
- Low  $R_{DS(ON)}$  for improved efficiency
- Low  $Q_g$  and  $Q_{sw}$  for better THD and improved efficiency
- Low  $Q_{rr}$  for better THD and lower EMI
- Can delivery up to 150W per channel into 4Ω load in half-bridge configuration amplifier
- Lead-free package

Key Parameters ⑤		
$V_{DS}$	100	V
$R_{DS(ON)}$ typ. @ 10V	58	mΩ
$Q_g$ typ.	12	nC
$Q_{sw}$ typ.	6.9	nC
$R_{G(int)}$ typ.	3.4	Ω
$T_J$ max	150	°C



G1, G2	D1, D2	S1, S2
Gate	Drain	Source

## Description

This Digital Audio MosFET Half-Bridge is specifically designed for Class D audio amplifier applications. It consists of two power MosFET switches connected in half-bridge configuration. The latest process is used to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery, and internal Gate resistance are optimized to improve key Class D audio amplifier performance factors such as efficiency, THD and EMI. These combine to make this Half-Bridge a highly efficient, robust and reliable device for Class D audio amplifier applications.

## Absolute Maximum Ratings ⑤

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	±20	
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	11	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	6.8	
$I_{DM}$	Pulsed Drain Current ①	44	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation ④	18	W
$P_D$ @ $T_C = 100^\circ\text{C}$	Power Dissipation ④	7.0	
	Linear Derating Factor	0.14	W/°C
$E_{AS}$	Single Pulse Avalanche Energy②	41	mJ
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

## Thermal Resistance ⑤

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	7.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (free air)	—	65	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified) ⑤

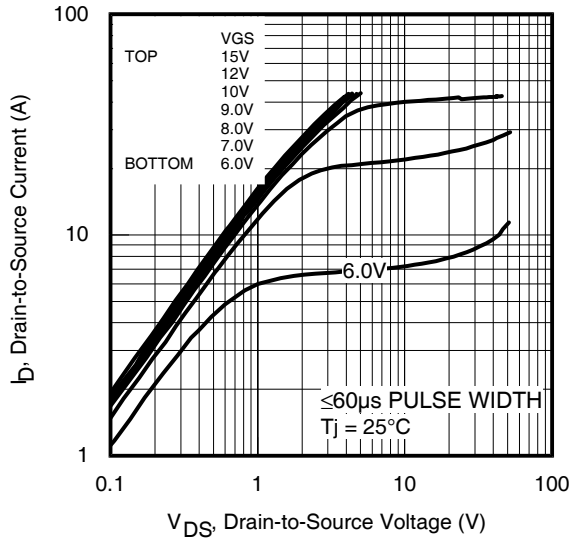
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.09	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	58	72.5	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6.6A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-11	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	11	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 6.6A
Q <sub>g</sub>	Total Gate Charge	—	12	18	nC	V <sub>DS</sub> = 80V V <sub>GS</sub> = 10V I <sub>D</sub> = 6.6A See Fig. 6 and 15
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	1.6	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	0.71	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	6.2	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	3.5	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	6.9	—		
R <sub>G(int)</sub>	Internal Gate Resistance	—	3.4	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	4.7	—	ns	V <sub>DD</sub> = 50V, V <sub>GS</sub> = 10V ③ I <sub>D</sub> = 6.6A R <sub>G</sub> = 2.5Ω
t <sub>r</sub>	Rise Time	—	8.3	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	9.5	—		
t <sub>f</sub>	Fall Time	—	4.3	—		
C <sub>iss</sub>	Input Capacitance	—	490	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 50V f = 1.0MHz, See Fig.5 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V
C <sub>oss</sub>	Output Capacitance	—	64	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	34	—		
C <sub>oss eff.</sub>	Effective Output Capacitance	—	110	—		
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		

## Diode Characteristics ⑤

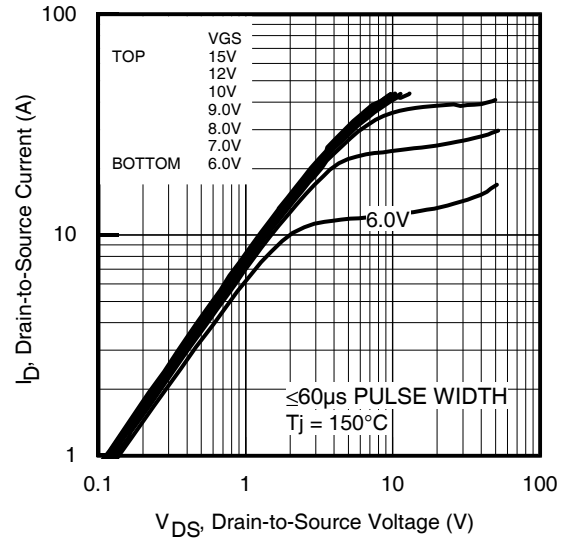
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub> @ T <sub>C</sub> = 25°C	Continuous Source Current (Body Diode)	—	—	11	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	44		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 6.6A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	36	54	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 6.6A
Q <sub>rr</sub>	Reverse Recovery Charge	—	56	84	nC	di/dt = 100A/μs ③

### Notes:

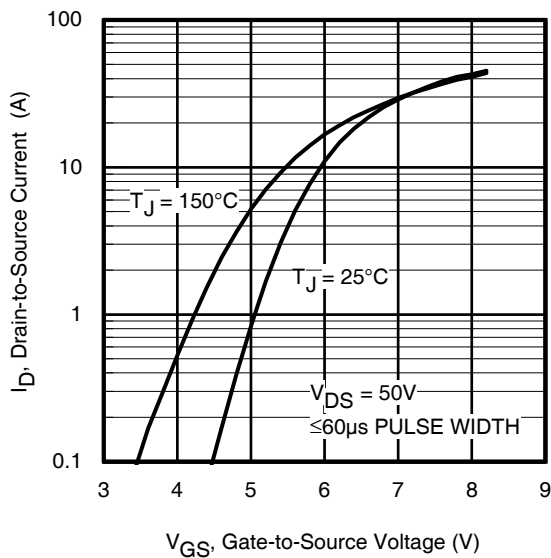
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting T<sub>J</sub> = 25°C, L = 1.9mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 6.6A.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ R<sub>θ</sub> is measured at T<sub>J</sub> of approximately 90°C.
- ⑤ Specifications refer to single MosFET.



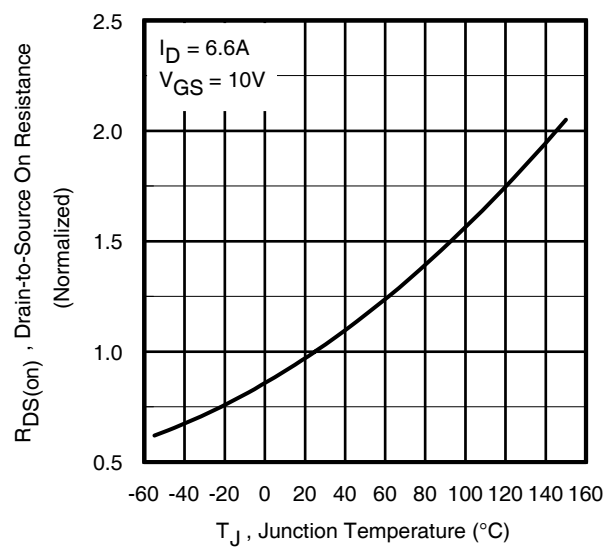
**Fig 1.** Typical Output Characteristics



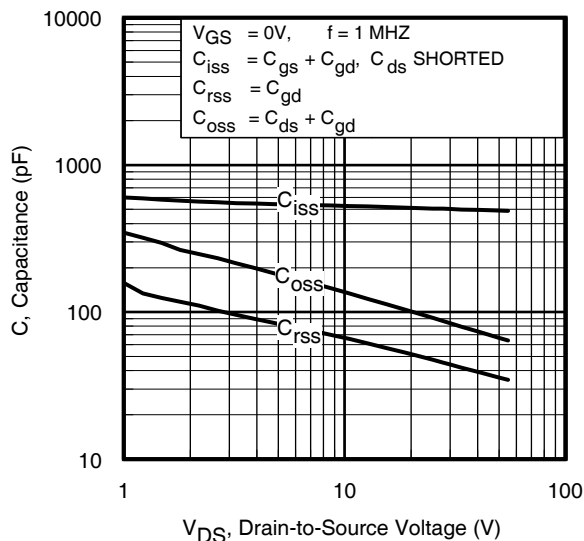
**Fig 2.** Typical Output Characteristics



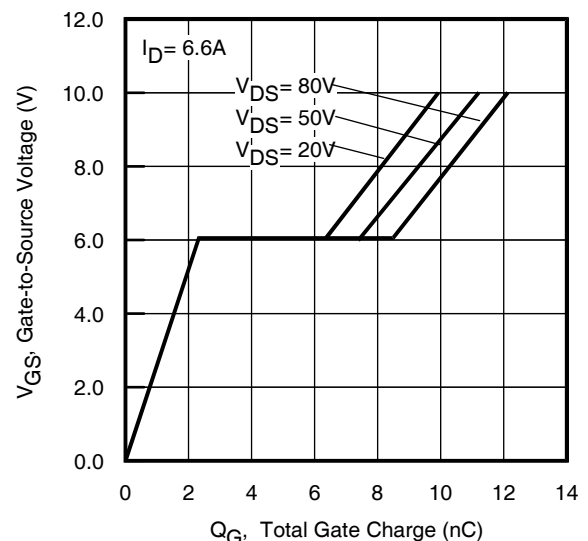
**Fig 3.** Typical Transfer Characteristics



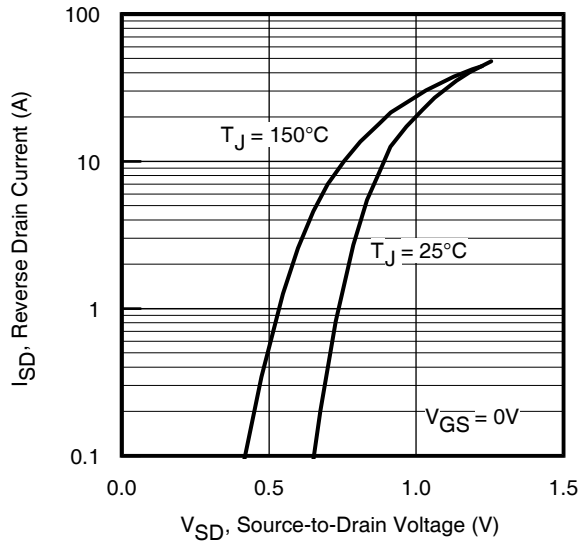
**Fig 4.** Normalized On-Resistance vs. Temperature



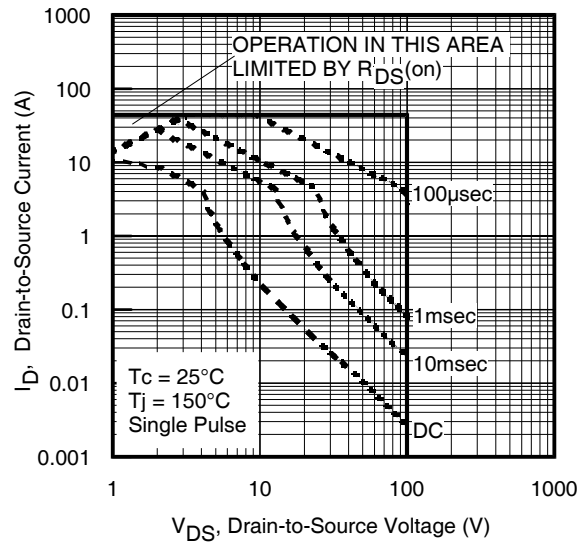
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage  
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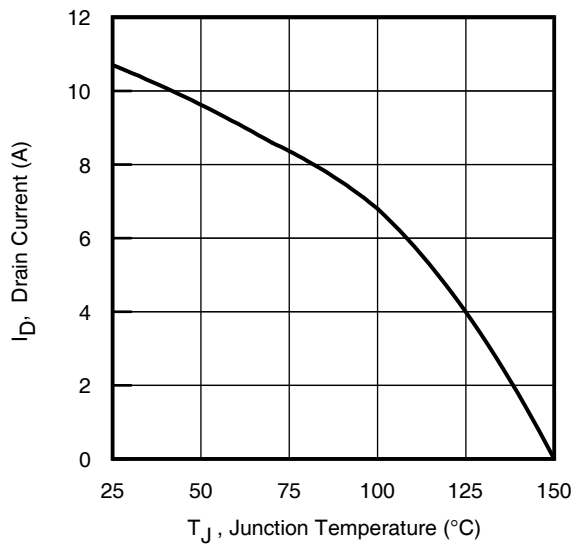
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



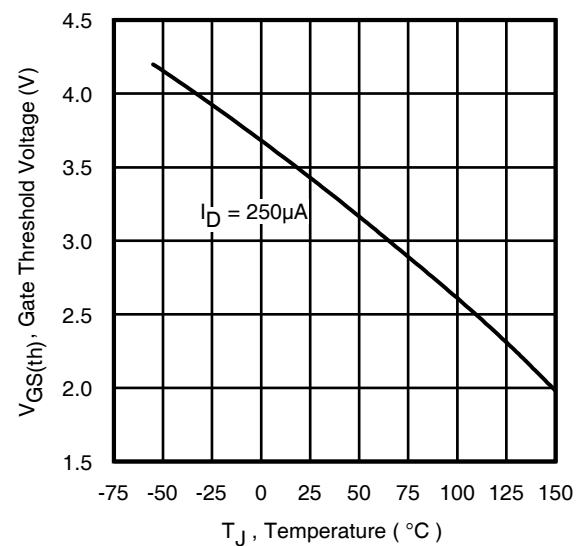
**Fig 7.** Typical Source-Drain Diode Forward Voltage



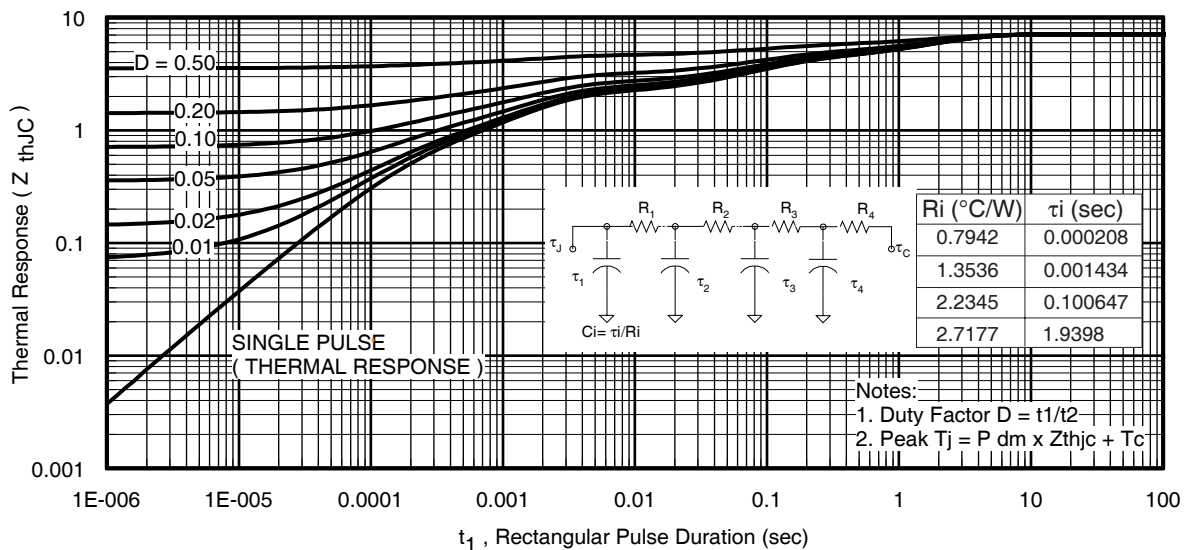
**Fig 8.** Maximum Safe Operating Area



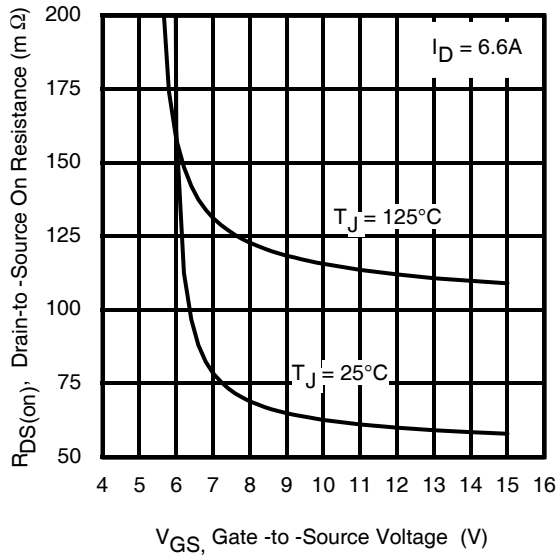
**Fig 9.** Maximum Drain Current vs. Junction Temperature



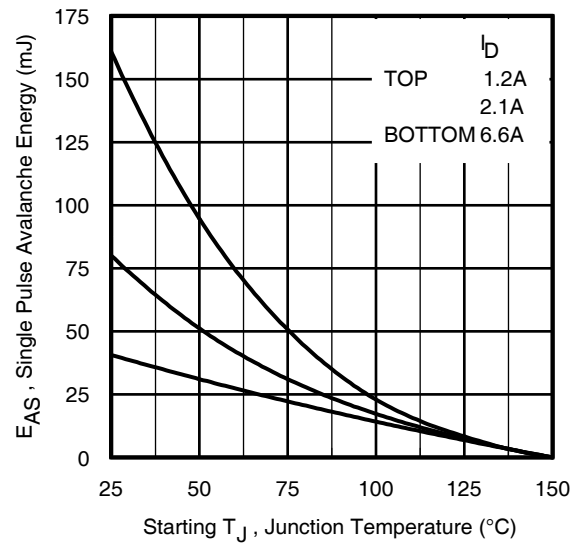
**Fig 10.** Threshold Voltage vs. Temperature



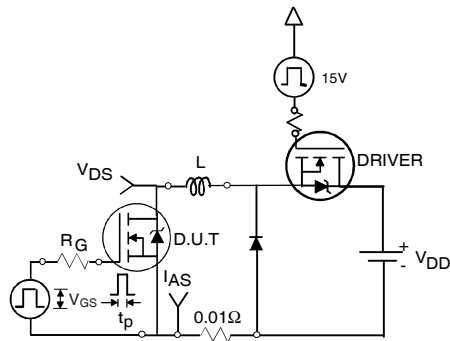
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



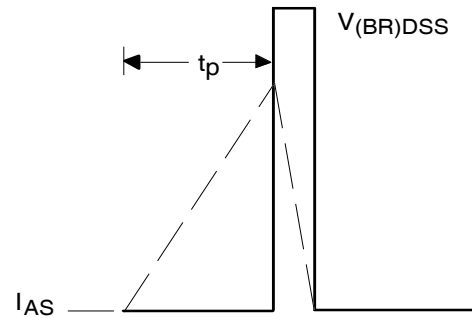
**Fig 12.** On-Resistance vs. Gate Voltage



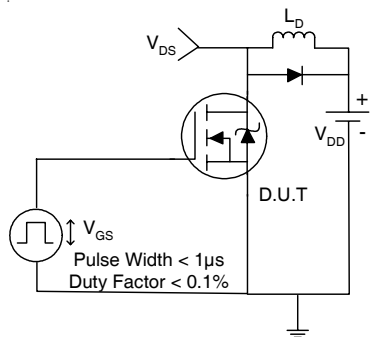
**Fig 13a.** Maximum Avalanche Energy vs. Drain Current



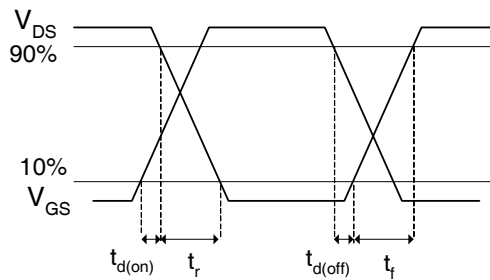
**Fig 13b.** Unclamped Inductive Test Circuit



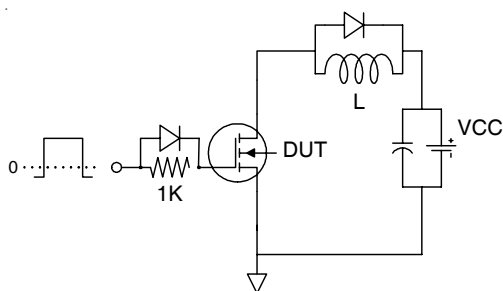
**Fig 13c.** Unclamped Inductive Waveforms



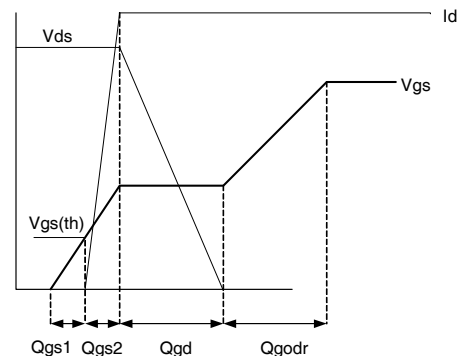
**Fig 14a.** Switching Time Test Circuit



**Fig 14b.** Switching Time Waveforms



**Fig 15a.** Gate Charge Test Circuit

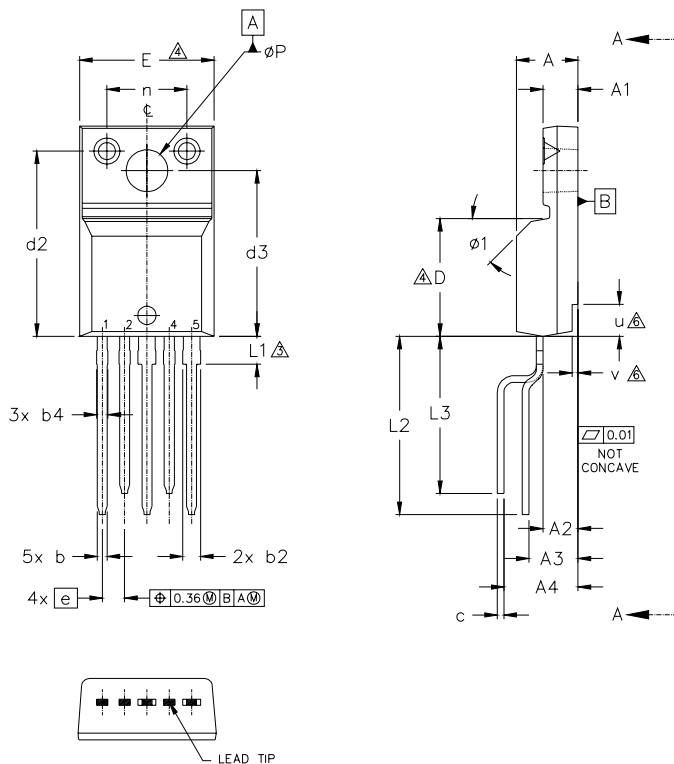


**Fig 15b** Gate Charge Waveform

# IRFI4212H-117P

## TO-220 Full-Pak 5-Pin Package Outline, Lead-Form Option 117

(Dimensions are shown in millimeters (inches))



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
  - 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  - LEAD DIMENSION AND FINISH UNCONTROLLED IN LT.
  - 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
  - 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
  - 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
  - 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.57	4.83	.180	.190		
A1	2.57	2.83	.101	.111		
A2	2.51	2.85	.099	.112		
A3	3.73	4.24	.147	.167		
A4	5.79	6.29	.228	.248		
b	0.61	0.95	0.24	.037		
b1	0.56	0.90	.022	0.35		5
b2	1.13	1.48	0.44	.058		
b3	1.08	1.43	0.42	.056		5
b4	0.76	1.06	.030	.042		
b5	0.71	1.01	.028	.040		5
c	0.33	0.63	.013	.025		
c1	0.28	0.58	.011	.023		5
D	8.65	9.80	.341	.386		4
d1	15.80	16.12	.622	.635		
d2	13.97	14.22	.550	.560		
d3	12.30	12.92	.484	.509		
E	9.63	10.63	.379	.419	4	

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
e	1.70	BSC	.067	BSC	3
L	13.20	13.73	.520	.541	
L1	1.91	2.31	.075	.091	
L2	12.7	13.46	.500	.530	
L3	10.92	11.68	.430	.460	6
n	6.05	6.15	.238	.242	
øP	3.05	3.45	.120	.136	6
u	2.40	2.50	.094	.098	
v	0.40	0.50	.016	.020	
ø1	-	.45*	-	.45*	

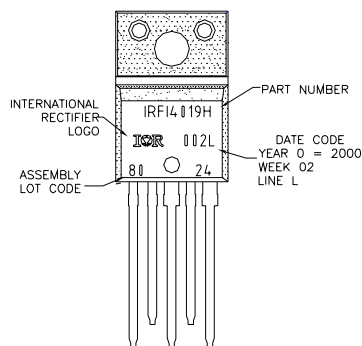
**LEAD ASSIGNMENTS**

- 1 - SOURCE 2
- 2 - GATE 2
- 3 - DRAIN 2 / SOURCE 1
- 4 - GATE 1
- 5 - DRAIN 1

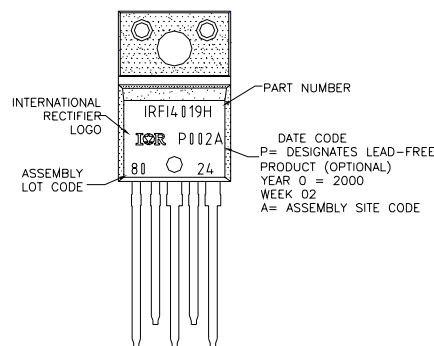
## TO-220 Full-Pak 5-Pin Part Marking Information

EXAMPLE: THIS IS AN IRFI4019H WITH  
LOT CODE 8024  
ASSEMBLED ON WW02,2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead Free"



OR



TO-220AB Full-Pak 5-Pin package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.  
This product has been designed for the Consumer market.  
Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>