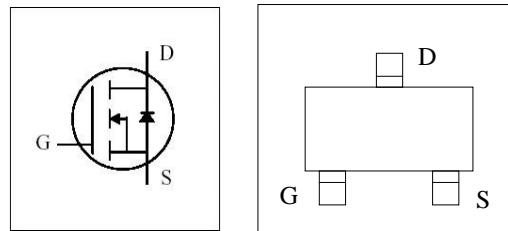
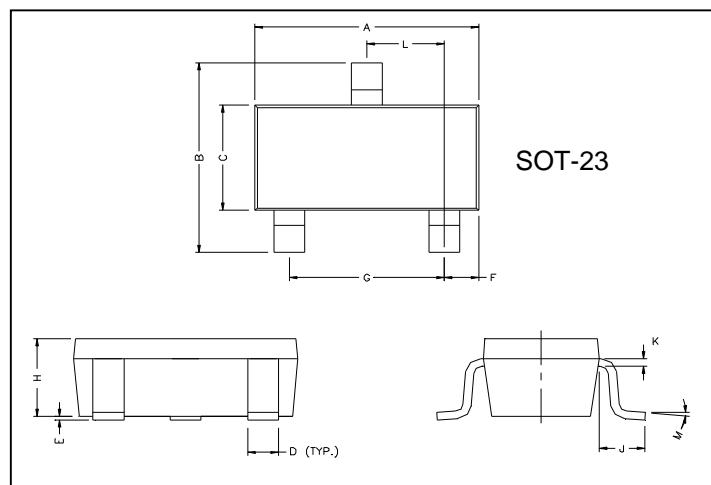


V_{DS} = 20V**R_{D(S)}(ON), V_{GS}@ 4.5V, I_{DS}@ 2.0A < 50mΩ****R_{D(S)}(ON), V_{GS}@ 2.5V, I_{DS}@ 1.0A < 80mΩ****Features**

Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

Package Dimensions

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.80	3.00	G	1.80	2.00
B	2.30	2.50	H	0.90	1.1
C	1.20	1.40	K	0.10	0.20
D	0.30	0.50	J	0.35	0.70
E	0	0.10	L	0.92	0.98
F	0.45	0.55	M	0°	10°

Maximum Ratings and Thermal Characteristics (TA = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±12	
Continuous Drain Current	I _D	2.3	A
Pulsed Drain Current ¹⁾	I _{DM}	6	
Maximum Power Dissipation ²⁾	P _D	0.6	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

Notes

1) Pulse width limited by maximum junction temperature.

2) Surface Mounted on FR4 Board, t ≤ 5 sec.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Miax.	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Drain-Source On-State Resistance ¹⁾	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 2A$			50	$m\Omega$
		$V_{GS} = 2.5V, I_D = 1A$			80	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.6		1.1	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 19.5V, V_{GS} = 0V$			1	μA
Gate Body Leakage	I_{GSS}	$V_{GS} = 12V, V_{DS} = 0V$			100	nA
Forward Transconductance ¹⁾	g_{fs}	$V_{DS} = 5V, I_D = 2.3A$		10	—	S
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = 10V, I_D = 2.3A$		5.4		nC
Gate-Source Charge	Q_{gs}			0.65		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10V, RL = 5.5\Omega$		12		ns
Turn-On Rise Time	t_r			36		
Turn-Off Delay Time	$t_{d(off)}$			34		
Turn-Off Fall Time	t_f	$R_G = 6\Omega$		10		
Input Capacitance	C_{iss}			340		pF
Output Capacitance	C_{oss}			115		
Reverse Transfer Capacitance	C_{rss}			33		
Diode Forward Voltage	V_{SD}	$I_S = 1.0A, V_{GS} = 0V$			1.2	V

¹⁾ Pulse test: pulse width <= 300us, duty cycle<= 2%

Typical Electrical and Thermal Characteristics

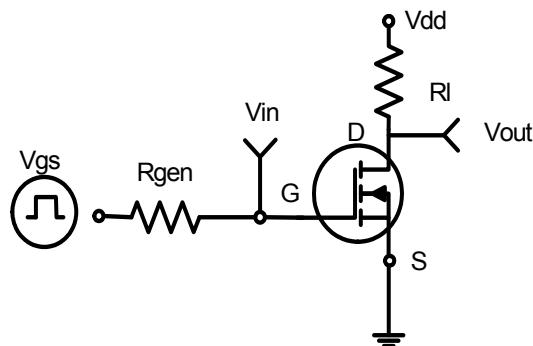


Figure 1:Switching Test Circuit

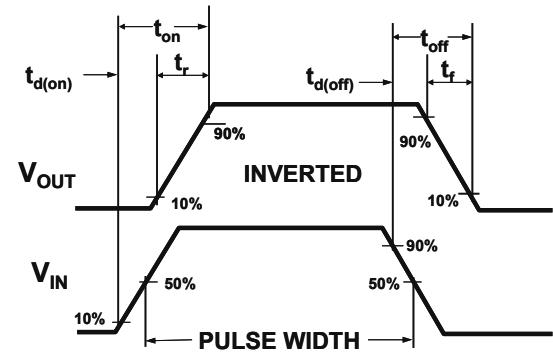


Figure 2:Switching Waveforms

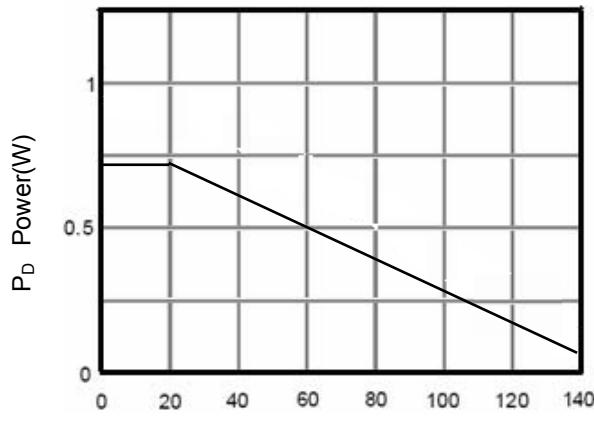


Figure 3 Power Dissipation

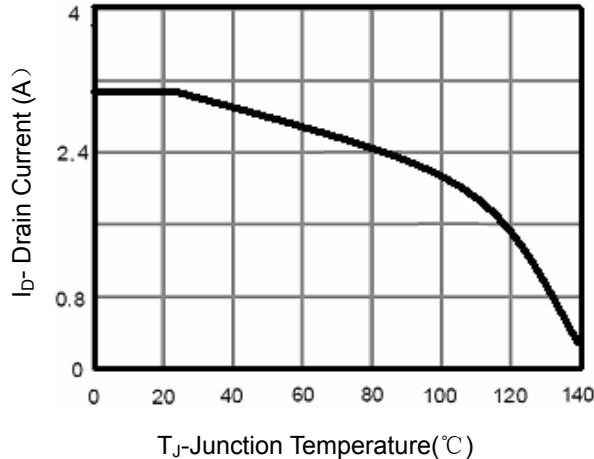


Figure 4 Drain Current

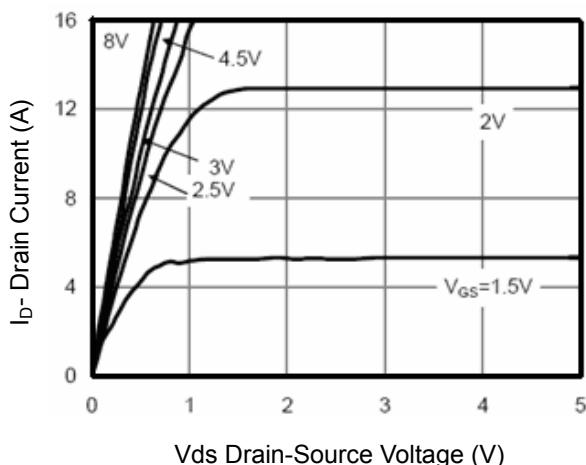


Figure 5 Output Characteristics

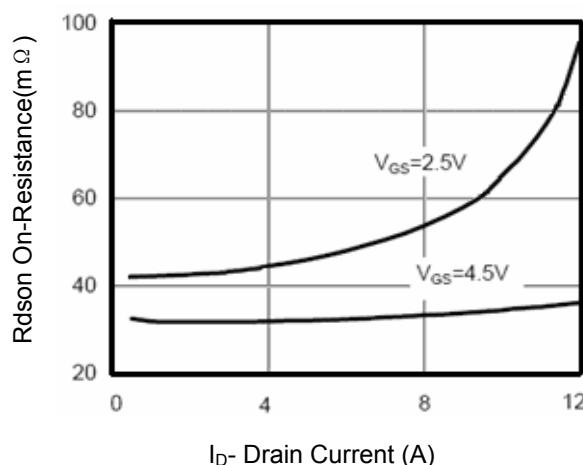


Figure 6 Drain-Source On-Resistance

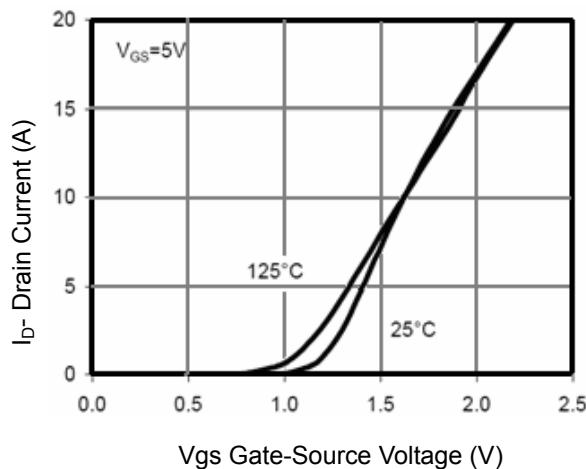


Figure 7 Transfer Characteristics

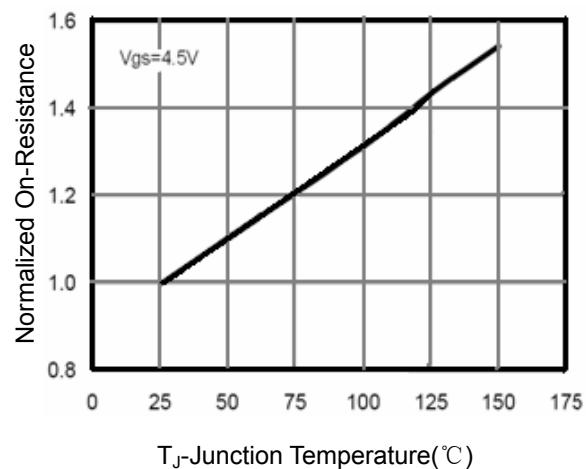


Figure 8 Drain-Source On-Resistance

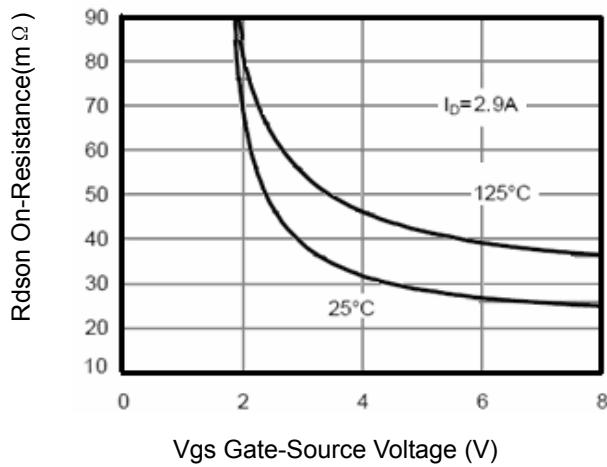


Figure 9 $R_{DS(on)}$ vs V_{GS}

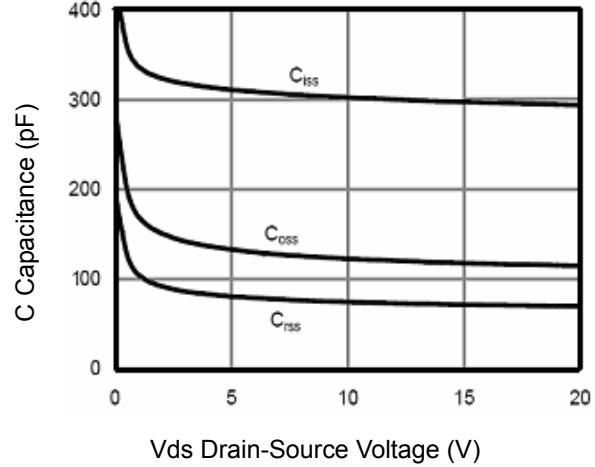


Figure 10 Capacitance vs V_{DS}

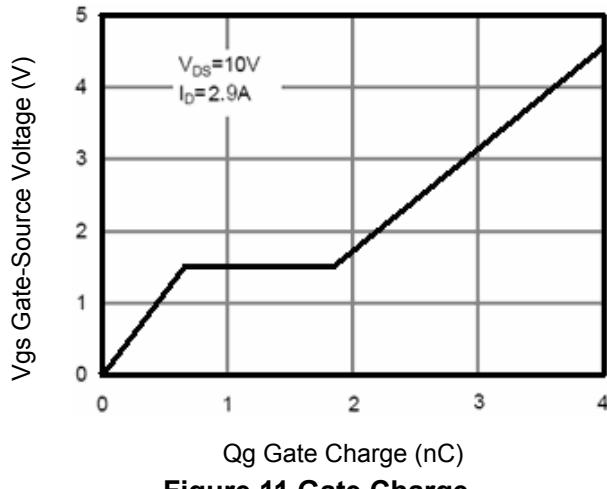


Figure 11 Gate Charge

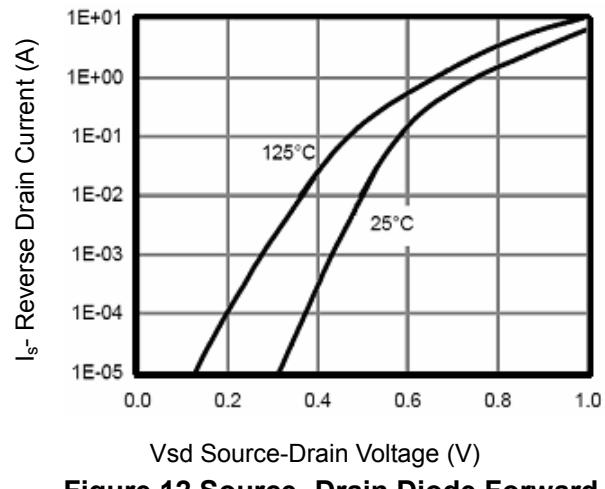


Figure 12 Source-Drain Diode Forward