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74LVXC3245

8-Bit Dual Supply Configurable Voltage Interface Transceiver with 3-STATE Outputs

Features

- Bidirectional interface between 3V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Implements proprietary EMI reduction circuitry
- Flexible V_{CCB} operating range
- Allows B Port and V_{CCB} to float simultaneously when \overline{OE} is HIGH
- Functionally compatible with the 74 series 245

General Description

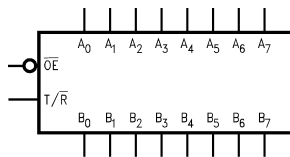
The LVXC3245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The V_{CCA} pin accepts a 3V supply level. The A Port is a dedicated 3V port. The V_{CCB} pin accepts a 3V-to-5V supply level. The B Port is configured to track the V_{CCB} supply level respectively. A 5V level on the V_{CC} pin will configure the I/O pins at a 5V level and a 3V V_{CC} will configure the I/O pins at a 3V level. The A Port should interface with a 3V host system and the B Port to the card slots. This device will allow the V_{CCB} voltage source pin and I/O pins on the B Port to float when \overline{OE} is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

Ordering Code:

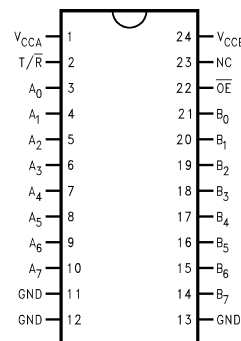
Order Number	Package Number	Package Description
74LVXC3245WM	M24B	224-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVXC3245QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
74LVXC3245MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol/s



Connection Diagram/s



Pin Descriptions

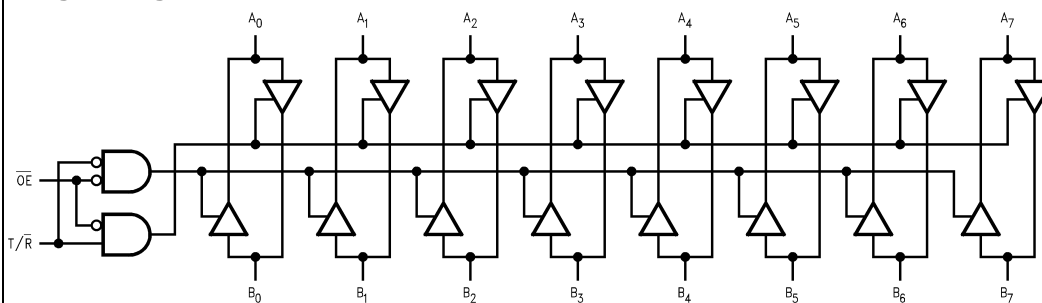
Pin Names	Description
\overline{OE}	Output Enable Input
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A Inputs or 3-STATE Outputs
B ₀ -B ₇	Side B Inputs or 3-STATE Outputs

Truth Table/s

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Logic Diagram/s



Absolute Maximum Ratings (Note 1)			Recommended Operating Conditions (Note 2)			
Supply Voltage (V_{CCA}, V_{CCB})		-0.5V to +7.0V	V_{CCA}		2.7V to 3.6V	
DC Input Voltage (V_I) @ $\overline{OE}, T/\overline{R}$		-0.5V to $V_{CCA} + 0.5V$	V_{CCB}		3.0V to 5.5V	
DC Input/Output Voltage ($V_{I/O}$)			Input Voltage (V_I) @ $\overline{OE}, T/\overline{R}$		0V to V_{CCA}	
@ A_n		-0.5V to $V_{CCA} + 0.5V$	Input Output Voltage ($V_{I/O}$)			
@ B_n		-0.5V to $V_{CCB} + 0.5V$	@ A_n		0V to V_{CCA}	
DC Input Diode Current (I_{IK})			@ B_n		0V to V_{CCB}	
@ $\overline{OE}, T/\overline{R}$		± 20 mA	Free Air Operating Temperature (T_A)		-40°C to +85°C	
DC Output Diode (I_{OK}) Current		± 50 mA	Minimum Input Edge Rate ($\Delta t/\Delta V$)		8 ns/V	
DC Output Source or Sink Current (I_O)		± 50 mA	V_{IN} from 30% to 70% of V_{CC}			
DC V_{CC} or Ground Current			V_{CC} @ 3.0V, 4.5V, 5.5V			
per Output Pin (I_{CC} or I_{GND})		± 50 mA				
and Max Current		± 200 mA				
Storage Temperature Range (T_{STG})		-65°C to +150°C				
DC Latch-Up Source or Sink Current		± 300 mA				

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The A Port unused pins (inputs or I/Os) must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
				Typ	Guaranteed Limits	Typ	Guaranteed Limits		
V_{IHA}	Minimum HIGH Level Input Voltage	A_n	2.7	3.0		2.0	2.0	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
		\overline{OE}	3.0	3.6		2.0	2.0		
		T/\overline{R}	3.6	5.5		2.0	2.0		
V_{IHB}		B_n	2.7	3.0		2.0	2.0	V	
			3.0	3.6		2.0	2.0		
			3.6	5.5		3.85	3.85		
V_{ILA}	Maximum LOW Level Input Voltage	A_n	2.7	3.0		0.8	0.8	V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
		\overline{OE}	3.0	3.6		0.8	0.8		
		T/\overline{R}	3.6	5.5		0.8	0.8		
V_{ILB}		B_n	2.7	3.0		0.8	0.8	V	
			3.0	3.6		0.8	0.8		
			3.6	5.5		1.65	1.65		
V_{OHA}	Minimum HIGH Level Output Voltage		3.0	3.0	2.99	2.9	2.9	V	$I_{OUT} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
			3.0	3.0	2.85	2.56	2.46		
			3.0	3.0	2.65	2.35	2.25		
			2.7	3.0	2.5	2.3	2.2		
			2.7	4.5	2.3	2.1	2.0		
V_{OHB}			3.0	3.0	2.99	2.9	2.9	V	$I_{OUT} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
			3.0	3.0	2.85	2.56	2.46		
			3.0	3.0	2.65	2.35	2.25		
			3.0	4.5	4.25	3.86	3.76		
V_{OLA}	Maximum LOW Level Output Voltage		3.0	3.0	0.002	0.1	0.1	V	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
			3.0	3.0	0.21	0.36	0.44		
			2.7	3.0	0.11	0.36	0.44		
			2.7	4.5	0.22	0.42	0.5		
V_{OLB}			3.0	3.0	0.002	0.1	0.1	V	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
			3.0	3.0	0.21	0.36	0.44		
			3.0	4.5	0.18	0.36	0.44		
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}, T/\overline{R}$		3.6	3.6		± 0.1	± 1.0	μA	$V_I = V_{CCA}, \text{GND}$
			3.6	5.5		± 0.1	± 1.0		

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CCA} (V)	V _{CCB} (V)	T _A = 25°C		T _A = -40°C to +85°C		Units	Conditions
				Typ	Guaranteed Limits				
I _{OZA}	Maximum 3-STATE Output Leakage @ A _n	3.6	3.6		±0.5	±5.0	μA	V _I = V _{IL} , V _{IH} , OE = V _{CCA} V _O = V _{CCA} , GND	
		3.6	5.5		±0.5	±5.0			
I _{OZB}	Maximum 3-STATE Output Leakage @ B _n	3.6	3.6		±0.5	±5.0	μA	V _I = V _{IL} , V _{IH} , OE = V _{CCA} V _O = V _{CCB} , GND	
		3.6	5.5		±0.5	±5.0			
ΔI _{CC}	Maximum I _{CC} /Input	B _n	3.6	5.5	1.0	1.35	mA	V _I = V _{CCB} - 2.1V V _I = V _{CC} - 0.6V	
		All Inputs	3.6	3.6		0.35			0.5
I _{CCA1}	Quiescent V _{CCA} Supply Current as B Port Floats	3.6	Open		5	50	μA	A _n = V _{CCA} or GND B _n = Open, OE = V _{CCA} , T/R = V _{CCA} , V _{CCB} = Open	
I _{CCA2}	Quiescent V _{CCA} Supply Current	3.6	3.6		5	50	μA	A _n = V _{CCA} or GND, B _n = V _{CCB} or GND, OE = GND, T/R = GND	
		3.6	5.5		5	50			
I _{CCB}	Quiescent V _{CCB} Supply Current	3.6	3.6		5	50	μA	A _n = V _{CCA} or GND, B _n = V _{CCB} or GND, OE = GND, T/R = V _{CCA}	
		3.6	5.5		8	80			
V _{OLPA}	Quiet Output Maximum Dynamic	3.3	3.3		0.8		V	(Note 3)(Note 4)	
V _{OLPB}	V _{OL}	3.3	3.3		0.8		V	(Note 3)(Note 4)	
		3.3	5.0		1.5				
V _{OLVA}	Quiet Output Minimum Dynamic	3.3	3.3		-0.8		V	(Note 3)(Note 4)	
		3.3	5.0		-0.8				
V _{OLVB}	V _{OL}	3.3	3.3		-0.8		V	(Note 3)(Note 4)	
		3.3	5.0		-1.2				
V _{IHDA}	Minimum HIGH Level Dynamic	3.3	3.3		2.0		V	(Note 3)(Note 5)	
		3.3	5.0		2.0				
V _{IHDB}	Input Voltage	3.3	3.3		2.0		V	(Note 3)(Note 5)	
		3.3	5.0		3.5				
V _{ILDA}	Maximum LOW Level Dynamic	3.3	3.3		0.8		V	(Note 3)(Note 5)	
		3.3	5.0		0.8				
V _{ILDB}	Input Voltage	3.3	3.3		0.8		V	(Note 3)(Note 5)	
		3.3	5.0		1.5				

Note 3: Worst case package.

Note 4: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 5: Max number of Data Inputs (n) switching. (n-1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IH}), 0V to threshold (V_{IL}), f = 1 MHz.

AC Electrical Characteristics												
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 2.7\text{V}-3.6\text{V}$ $V_{CCB} = 4.5\text{V}-5.5\text{V}$			$T_A = -40^\circ\text{C to }+85^\circ\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 2.7\text{V}-3.6\text{V}$ $V_{CCB} = 4.5\text{V}-5.5\text{V}$		$T_A = +25^\circ\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 2.7\text{V}-3.6\text{V}$ $V_{CCB} = 3.0\text{V}-3.6\text{V}$			$T_A = -40^\circ\text{C to }+85^\circ\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 2.7\text{V}-3.6\text{V}$ $V_{CCB} = 3.0\text{V}-3.6\text{V}$		Units
		Min	Typ (Note 6)	Max	Min	Max	Min	Typ (Note 7)	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	4.8	8.0	1.0	8.5	1.0	5.5	8.5	1.0	9.0	ns
t_{PLH}	A to B	1.0	3.9	6.5	1.0	7.0	1.0	5.2	8.0	1.0	8.5	
t_{PHL}	Propagation Delay	1.0	3.8	6.5	1.0	7.0	1.0	4.4	7.0	1.0	7.5	ns
t_{PLH}	B to A	1.0	4.3	7.5	1.0	8.0	1.0	5.1	7.5	1.0	8.0	
t_{PZL}	Output Enable Time	1.0	4.7	8.0	1.0	8.5	1.0	6.0	9.0	1.0	9.5	ns
t_{PZH}	$\overline{\text{OE}}$ to B	1.0	4.8	8.5	1.0	9.0	1.0	6.1	9.5	1.0	10.0	
t_{PZL}	Output Enable Time	1.0	5.9	9.5	1.0	10.0	1.0	6.4	10.0	1.0	10.5	ns
t_{PZH}	$\overline{\text{OE}}$ to A	1.0	5.4	9.0	1.0	9.5	1.0	5.8	9.0	1.0	9.5	
t_{PHZ}	Output Disable Time	1.0	4.0	8.0	1.0	8.5	1.0	6.3	9.5	1.0	10.0	ns
t_{PLZ}	$\overline{\text{OE}}$ to B	1.0	3.8	7.5	1.0	8.0	1.0	4.5	8.0	1.0	8.5	
t_{PHZ}	Output Disable Time	1.0	4.6	9.5	1.0	10.0	1.0	5.2	9.5	1.0	10.0	ns
t_{PLZ}	$\overline{\text{OE}}$ to A	1.0	3.1	6.5	1.0	7.0	1.0	3.4	6.5	1.0	7.0	
t_{OSHL}	Output to Output											ns
t_{OSLH}	Skew (Note 8) Data to Output		1.0	1.5		1.5		1.0	1.5		1.5	

Note 6: Typical values at $V_{CCA} = 3.3\text{V}$, $V_{CCB} = 5.0\text{V}$ @ 25°C .

Note 7: Typical values at $V_{CCA} = 3.3\text{V}$, $V_{CCB} = 3.3\text{V}$ @ 25°C .

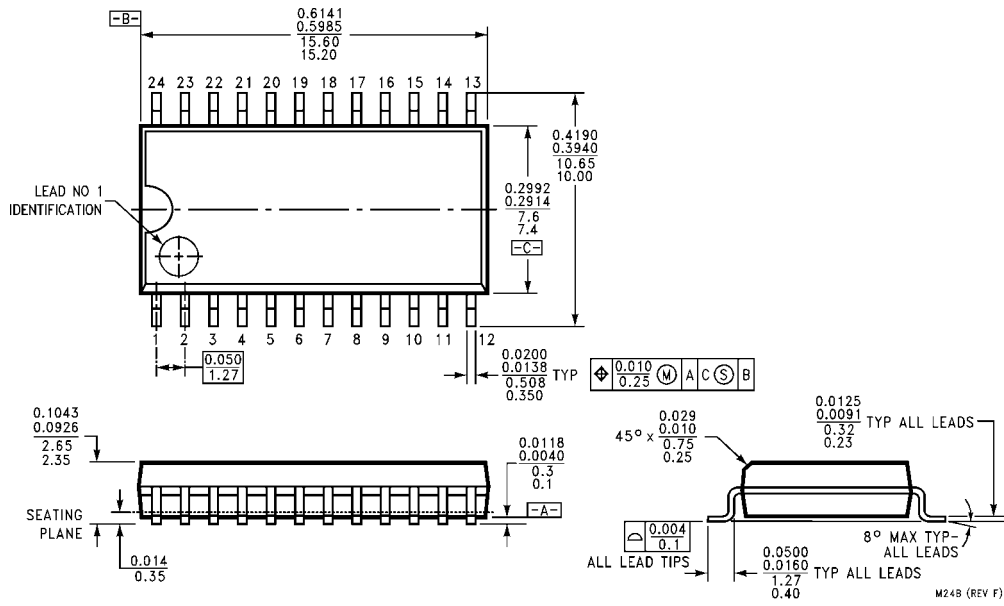
Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

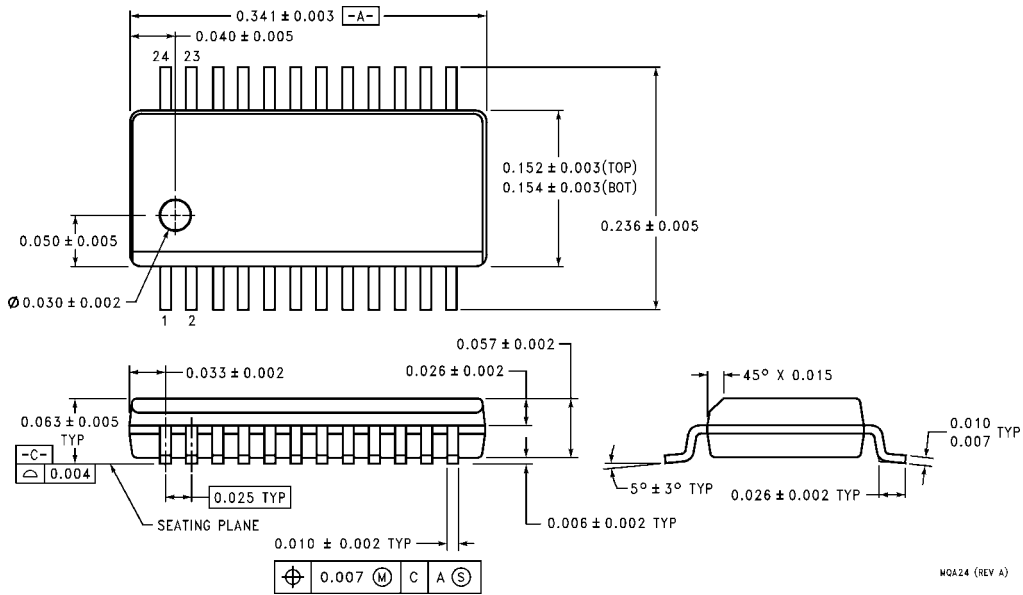
Symbol	Parameter	Typ	Units	Conditions	
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$	
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{CCA} = 3.3\text{V}$ $V_{CCB} = 5.0\text{V}$	
C_{PD}	Power Dissipation Capacitance (Note 9)	A→B	50	pF	$V_{CCB} = 5.0\text{V}$
		B→A	40	pF	$V_{CCA} = 3.3\text{V}$

Note 9: C_{PD} is measured at 10 MHz.

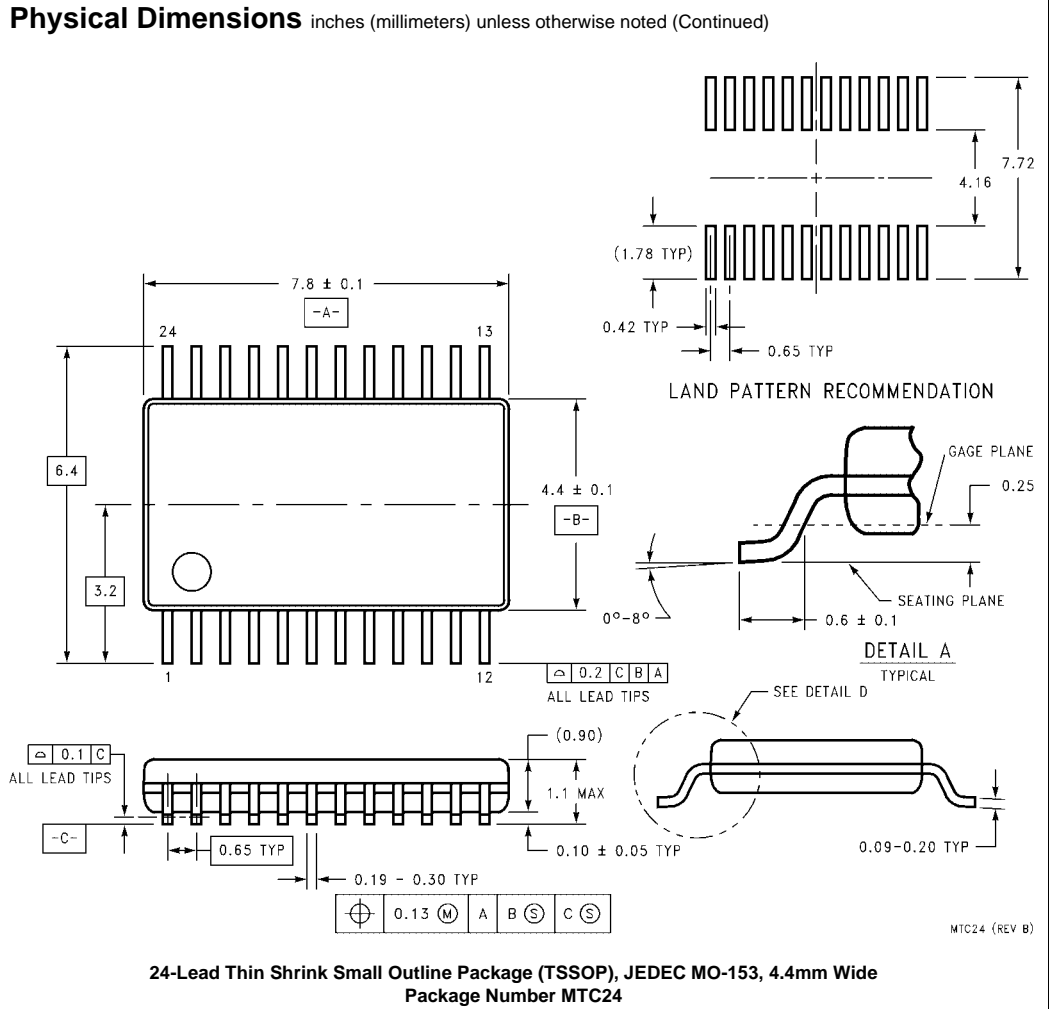
Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M24B**



**24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA24**



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Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 138

74LVXC3245 — 8-Bit Dual Supply Configurable Voltage Interface Transceiver with 3-STATE Outputs

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