

SN74LVC1G07 Single Buffer/Driver With Open-Drain Output

1 Features

- Available in the Ultra Small 0.64-mm² Package (DPW) With 0.5-mm Pitch
- Supports 5-V V_{CC} Operation
- Input and Open-Drain Output Accept Voltages up to 5.5 V
- Can Translate Up or Down
- Max t_{pd} of 4.2 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receiver
- Blu-ray Player and Home Theater
- DVD Recorder and Player
- Desktop or Notebook PC
- Digital Radio or Internet Radio Player
- Digital Video Camera (DVC)
- Embedded PC
- GPS: Personal Navigation Device
- Mobile Internet Device
- Network Projector Front End
- Portable Media Player
- Pro Audio Mixer
- Smoke Detector
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablet: Enterprise
- Audio Dock: Portable
- DLP Front Projection System
- DVR and DVS
- Digital Picture Frame (DPF)
- Digital Still Camera

3 Description

This single buffer/driver is designed for 1.65-V to 5.5-V V_{CC} operation.

The output of the SN74LVC1G07 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

The SN74LVC1G07 is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 mm × 0.8 mm.

Device Information

DEVICE NAME	PACKAGE ⁽¹⁾	BODY SIZE
SN74LVC1G07DBV	SOT-23 (5)	2.9mm × 1.6mm
SN74LVC1G07DCK	SC70 (5)	2.0mm × 1.25mm
SN74LVC1G07DPW	X2SON (5)	0.8mm × 0.8mm
SN74LVC1G07DRY	SON (6)	1.45mm × 1.0mm
SN74LVC1G07DSF	SON (6)	1.0mm × 1.0mm
SN74LVC1G07DRL	SOT (5)	1.6mm × 1.2mm
SN74LVC1G07YZP	DSBGA (6)	1.38mm × 0.88mm
SN74LVC1G07YZV	DSBGA (4)	0.88mm × 0.88mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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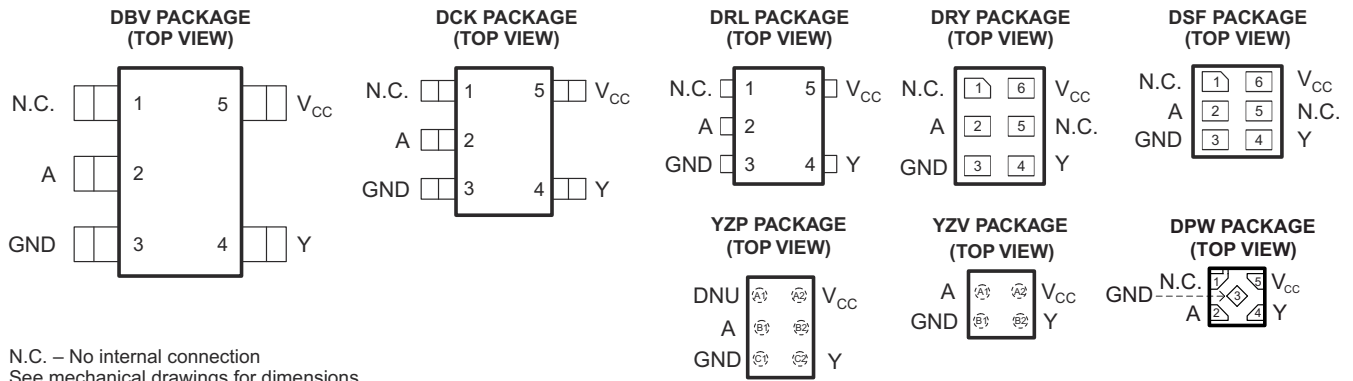
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision AD (May 2016) to Revision AE (September 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
Changes from Revision AC (April 2014) to Revision AD (April 2016)	Page
• Changed 4 pin to 5 pin on DPW package in <i>Device Information</i> table.....	1
• Added DRL, YZP, and YZV package information and body size dimensions to <i>Device Information</i> table	1
• Moved "T _{stg} Storage temperature range" from <i>ESD Ratings</i> table to <i>Absolute Maximum Ratings</i> table.....	4
• Added "T _j Junction temperature range" to <i>Absolute Maximum ratings</i> table.....	4
• Split "T _A Operating free-air temperature" into package specific temperature ranges in <i>Recommended Operating Conditions</i> table.....	5
• Changed "H" to "Z" in Output Y column of Function Table	9
Changes from Revision AB (March 2014) to Revision AC (April 2014)	Page
• Updated Handling Ratings table.	4
• Added Thermal Information table.	5
• Added Typical Characteristics.	7
• Added Application and Implementation section.	10
• Added Power Supply Recommendations section.	11
Changes from Revision AA (July 2013) to Revision AB (February 2014)	Page
• Updated Features.....	1
• Added Applications.....	1
• Added Device Information table.....	1
• Added Pin Functions table.	3
• Moved T _{stg} to Handling Ratings table.....	4
Changes from Revision Z (November 2012) to Revision AA (July 2013)	Page
• Extended maximum temperature operating range from 85°C to 125°C.....	5

5 Pin Configuration and Functions



Pin Functions

NAME	PIN					DESCRIPTION
	DBV, DCK, DRL	DRY, DSF	DPW	YZP	YZV	
NC	1	1, 5	1	A1, B2	–	Not connected
A	2	2	2	B1	A1	Input
GND	3	3	3	C1	B1	Ground
Y	4	4	4	C2	B2	Output
V _{CC}	5	6	5	A2	A2	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾ ⁽³⁾	-0.5	6.5	V
I _{IK}	Input clamp current		-50	mA
				V _I < 0
I _{OK}	Output clamp current		-50	mA
				V _O < 0
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _{stg}	Storage temperature range	-65	150	°C
T _J	Junction temperature range		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			MIN	MAX	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	5.5	V
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3 V		16	
				24	
		V _{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V _{CC} = 3.3 V ± 0.3 V		10	
		V _{CC} = 5 V ± 0.5 V		5	
T _A	Operating free-air temperature	DSBGA package	–40	85	°C
		All other packages	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G07						UNIT	
	DBV	DCK	DRL	DRY	YZP	DPW		
	5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	4 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	229	278	243	439	130	340	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	164	93	78	277	54	215	
R _{θJB}	Junction-to-board thermal resistance	62	65	78	271	51	294	
ψ _{JT}	Junction-to-top characterization parameter	44	2	10	84	1	41	
ψ _{JB}	Junction-to-board characterization parameter	62	64	77	271	50	294	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	–	–	–	–	–	250	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	–40°C TO 85°C		–40°C TO 125°C RECOMMENDED		UNIT
			TYP ⁽¹⁾	MAX	TYP	MAX	
V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V	0.1		0.1		V
	I _{OL} = 4 mA	1.65 V	0.45		0.45		
	I _{OL} = 8 mA	2.3 V	0.3		0.3		
	I _{OL} = 16 mA	3 V	0.4		0.4		
	I _{OL} = 24 mA		0.55		0.55		
	I _{OL} = 32 mA	4.5 V	0.55		0.55		
I _I	A input V _I = 5.5 V or GND	0 to 5.5 V	±5		±5		μA
I _{off}	V _I or V _O = 5.5 V	0	±10		±10		μA
I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V	10		10		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500		500		μA
C _i	V _I = V _{CC} or GND	3.3 V	4		4		pF
C _o	V _O = V _{CC} or GND	3.3 V	5		5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics, –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 85°C								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	2.4	8.3	1	5.5	1.5	4.2	1	3.5	ns

6.7 Switching Characteristics, –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

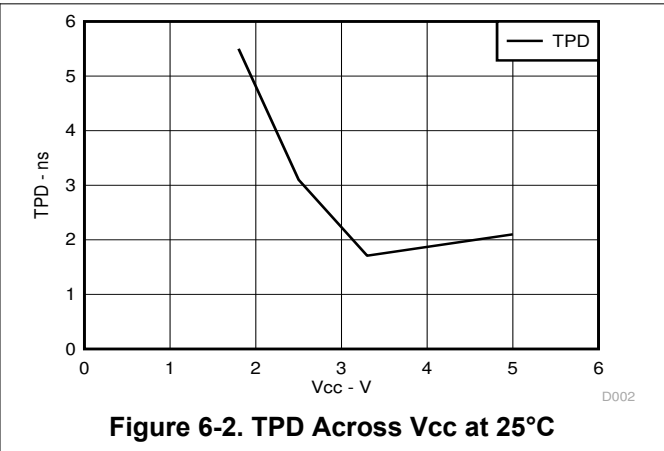
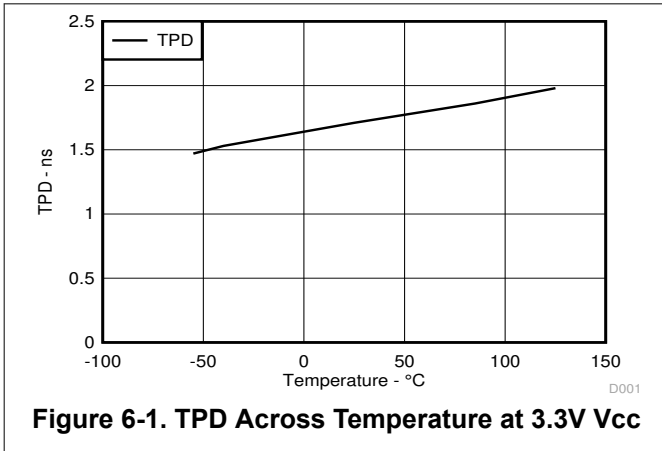
PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 125°C RECOMMENDED								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	2.4	8.6	1	6	1.5	4.7	1	4	ns

6.8 Operating Characteristics

T_A = 25°C

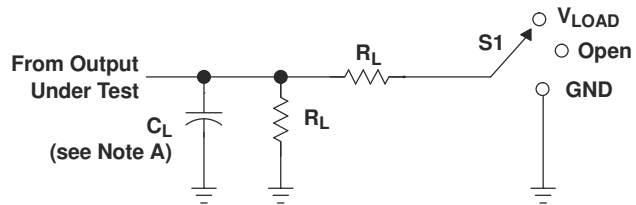
PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
		TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance f = 10 MHz	3	3	4	6	pF

6.9 Typical Characteristics



7 Parameter Measurement Information

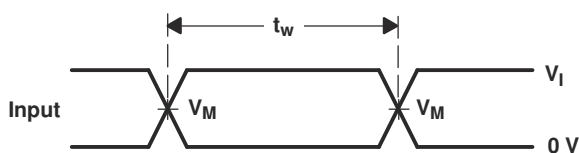
7.1 (Open Drain)



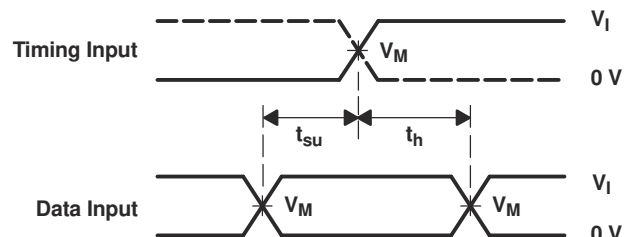
LOAD CIRCUIT

TEST	S1
t_{pZL} (see Notes E and F)	V_{LOAD}
t_{pLZ} (see Notes E and G)	V_{LOAD}
t_{pHZ}/t_{pZH}	V_{LOAD}

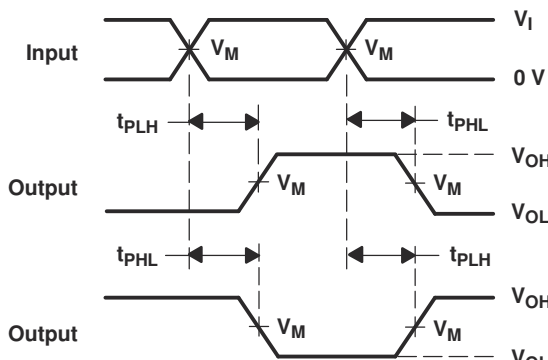
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



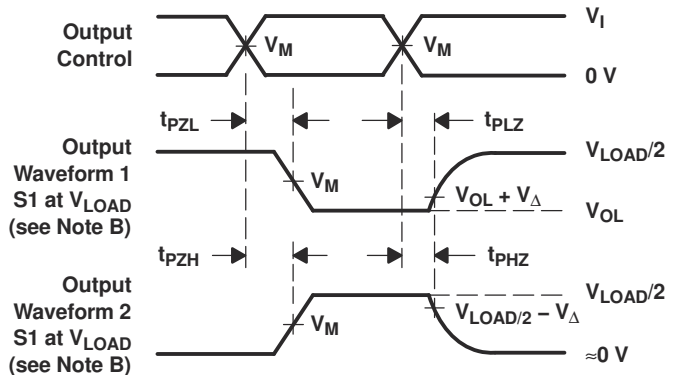
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - F. t_{pZL} is measured at V_M .
 - G. t_{pLZ} is measured at $V_{OL} + V_{\Delta}$.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

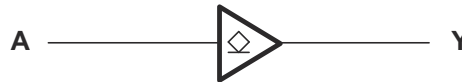
8 Detailed Description

8.1 Overview

The SN74LVC1G07 device contains one open-drain buffer with a maximum sink current of 32 mA. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. The DPW 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs and outputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

8.4 Device Functional Modes

Function Table

INPUT A	OUTPUT Y
L	L
H	Z

9 Application and Implementation

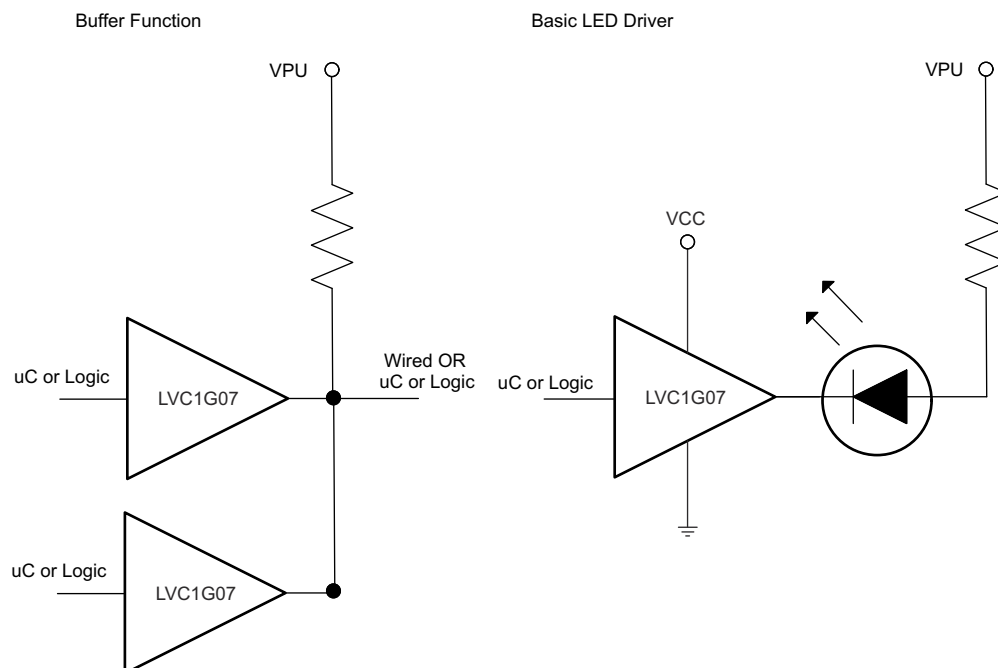
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G07 is a high drive CMOS device that can be used to implement a high output drive buffer, such as an LED application. It can sink 32 mA of current at 4.5 V making it ideal for high drive and wired-OR/AND functions. It is good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate up/down to V_{CC} .

9.2 Typical Application



9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it may drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

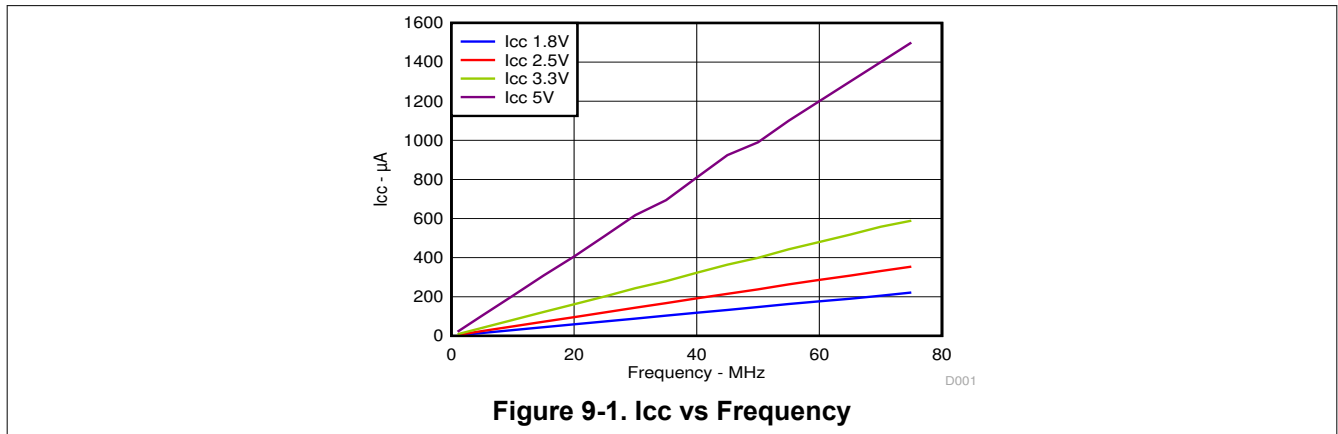
1. Recommended Input Conditions

- Rise time and fall time specs. See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
- Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
- Inputs are over-voltage tolerant allowing them to go as high as $(V_I \text{ max})$ in the [Recommended Operating Conditions](#) table at any valid V_{CC} .

2. Recommend Output Conditions

- Load currents should not exceed $(I_O \text{ max})$ per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
- Outputs should not be pulled above 5.5 V.

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

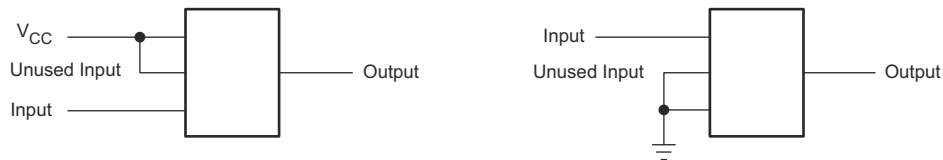
Each V_{cc} pin should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for devices with a single supply. If there are multiple V_{cc} pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to Gnd or V_{cc}, whichever is more convenient.

11.2 Layout Example



12 Device and Documentation Support

12.1 Trademarks

All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G07DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C075, C07F, C07J, C07K, C07R, C 07T) (C07H, C07P, C07S)	Samples
SN74LVC1G07DBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F	Samples
SN74LVC1G07DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F	Samples
SN74LVC1G07DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C075, C07F, C07J, C07K, C07R) (C07H, C07P, C07S)	Samples
SN74LVC1G07DBVTE4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F	Samples
SN74LVC1G07DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C07F	Samples
SN74LVC1G07DCK3	ACTIVE	SC70	DCK	5	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	(CVF, CVZ)	Samples
SN74LVC1G07DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT) (CVH, CVP, CVS)	Samples
SN74LVC1G07DCKRE4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT) (CVH, CVP, CVS)	Samples
SN74LVC1G07DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT) (CVH, CVP, CVS)	Samples
SN74LVC1G07DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT) CVH	Samples
SN74LVC1G07DCKTE4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT) CVH	Samples
SN74LVC1G07DCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CV5, CVF, CVK, CV R, CVT)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										CVH	
SN74LVC1G07DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L4	Samples
SN74LVC1G07DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CV7, CVR)	Samples
SN74LVC1G07DRLRG4	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CV7, CVR)	Samples
SN74LVC1G07DRY2	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV	Samples
SN74LVC1G07DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV	Samples
SN74LVC1G07DRYRG4	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV	Samples
SN74LVC1G07DSF2	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV	Samples
SN74LVC1G07DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV	Samples
SN74LVC1G07YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CV7, CVN)	Samples
SN74LVC1G07YZVR	ACTIVE	DSBGA	YZV	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CV N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G07 :

- Automotive: [SN74LVC1G07-Q1](#)
- Enhanced Product: [SN74LVC1G07-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

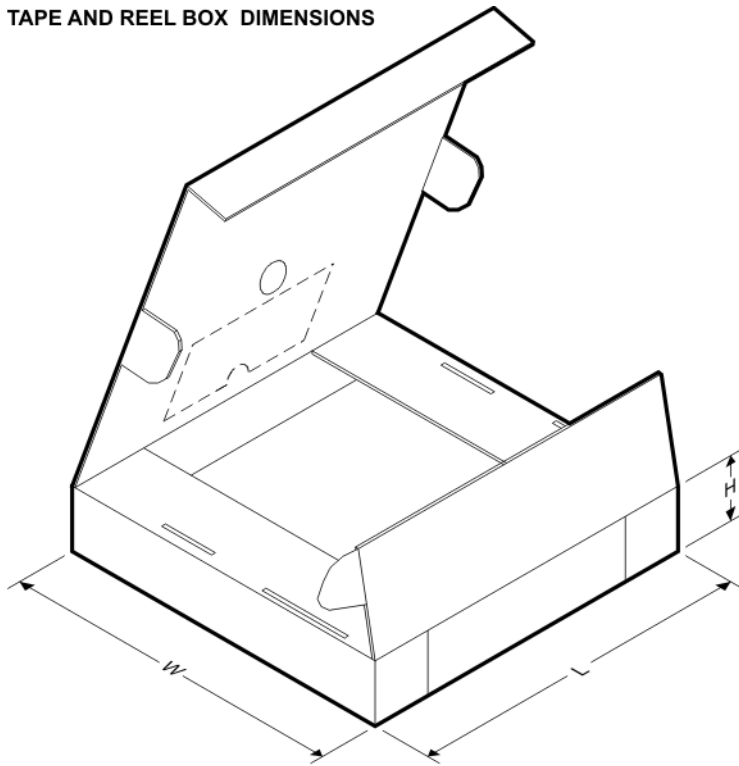
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G07DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G07DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G07DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G07DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G07DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G07DRLR	SOT-5X3	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G07DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G07DRY2	SON	DRY	6	5000	180.0	8.4	1.65	1.2	0.7	4.0	8.0	Q3
SN74LVC1G07DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G07DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74LVC1G07DSF2	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q3
SN74LVC1G07DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74LVC1G07DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G07YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G07YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G07DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G07DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G07DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G07DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G07DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LVC1G07DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G07DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G07DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G07DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G07DRLR	SOT-5X3	DRL	5	4000	184.0	184.0	19.0
SN74LVC1G07DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G07DRY2	SON	DRY	6	5000	202.0	201.0	28.0
SN74LVC1G07DRYR	SON	DRY	6	5000	203.0	203.0	35.0
SN74LVC1G07DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G07DSF2	SON	DSF	6	5000	202.0	201.0	28.0
SN74LVC1G07DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74LVC1G07DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G07YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G07YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

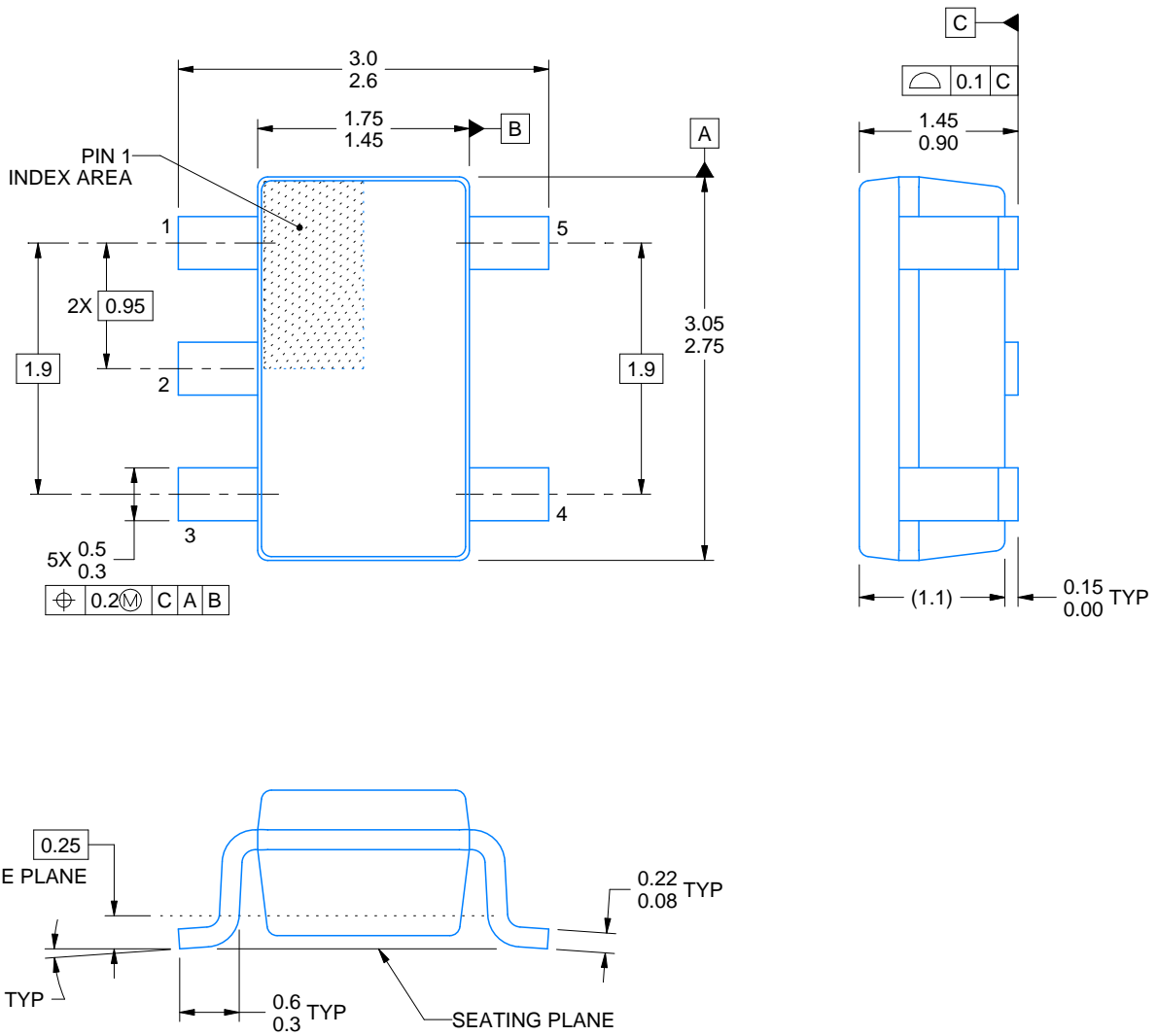
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

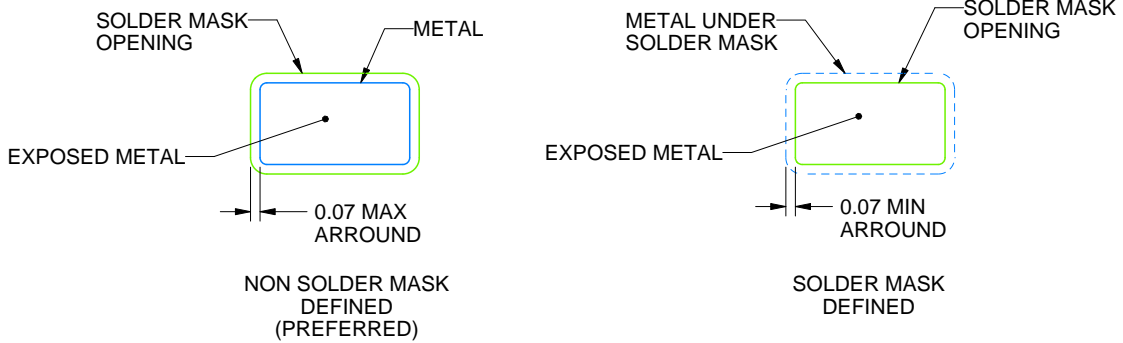
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

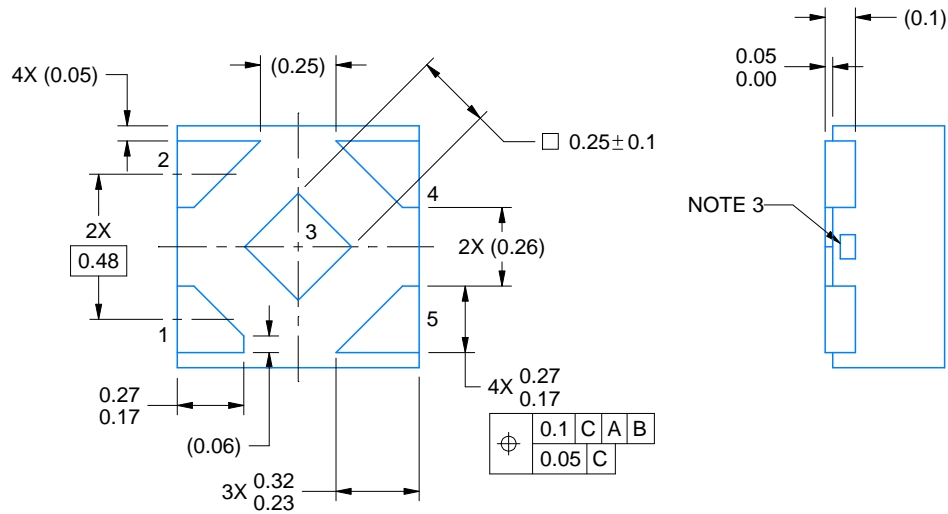
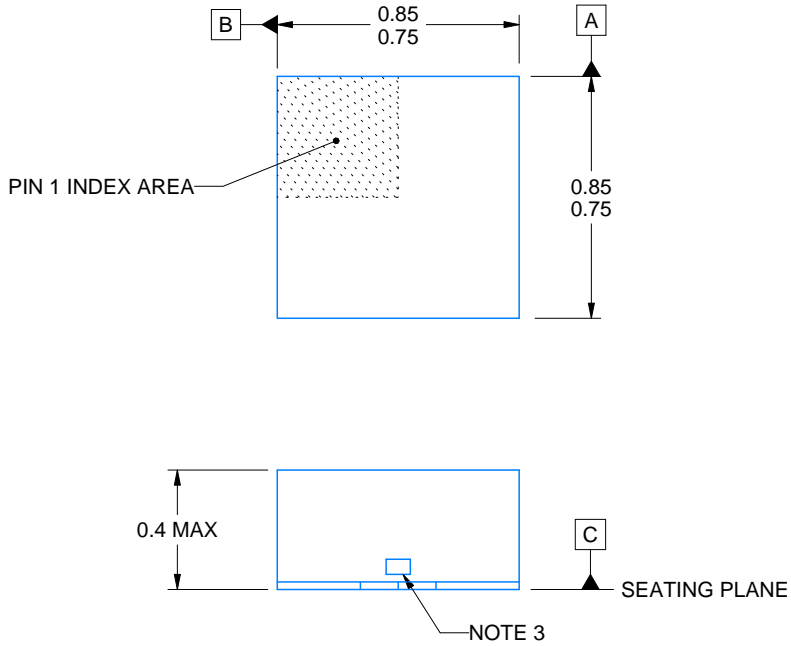
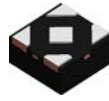
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/B 09/2017

NOTES:

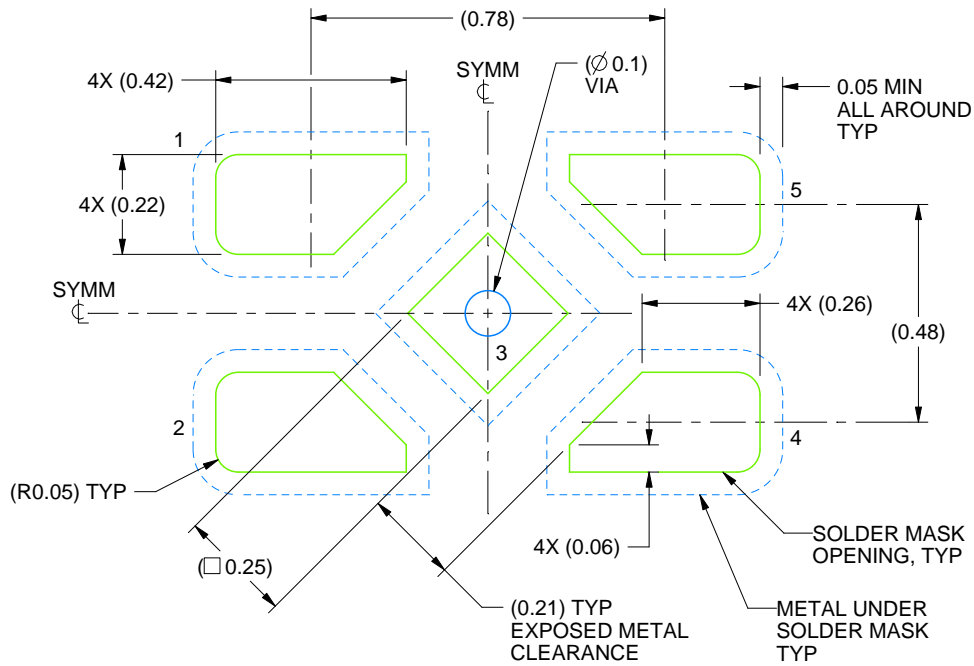
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/B 09/2017

NOTES: (continued)

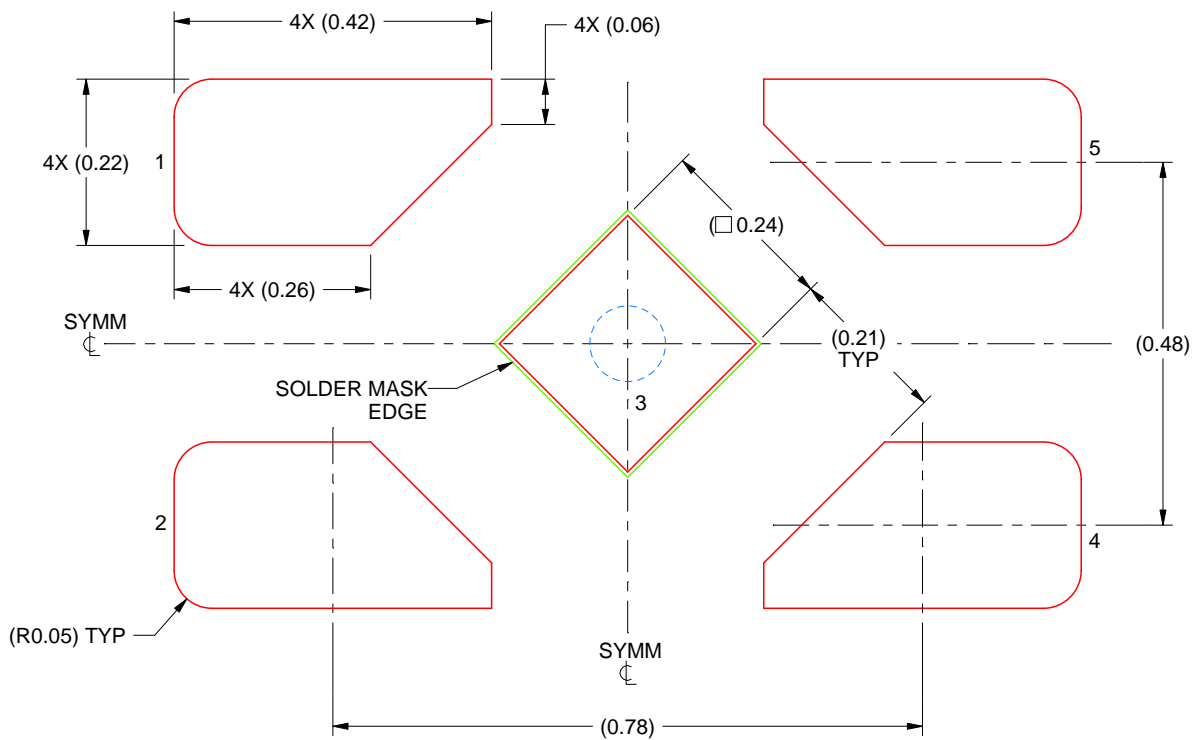
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4223102/B 09/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

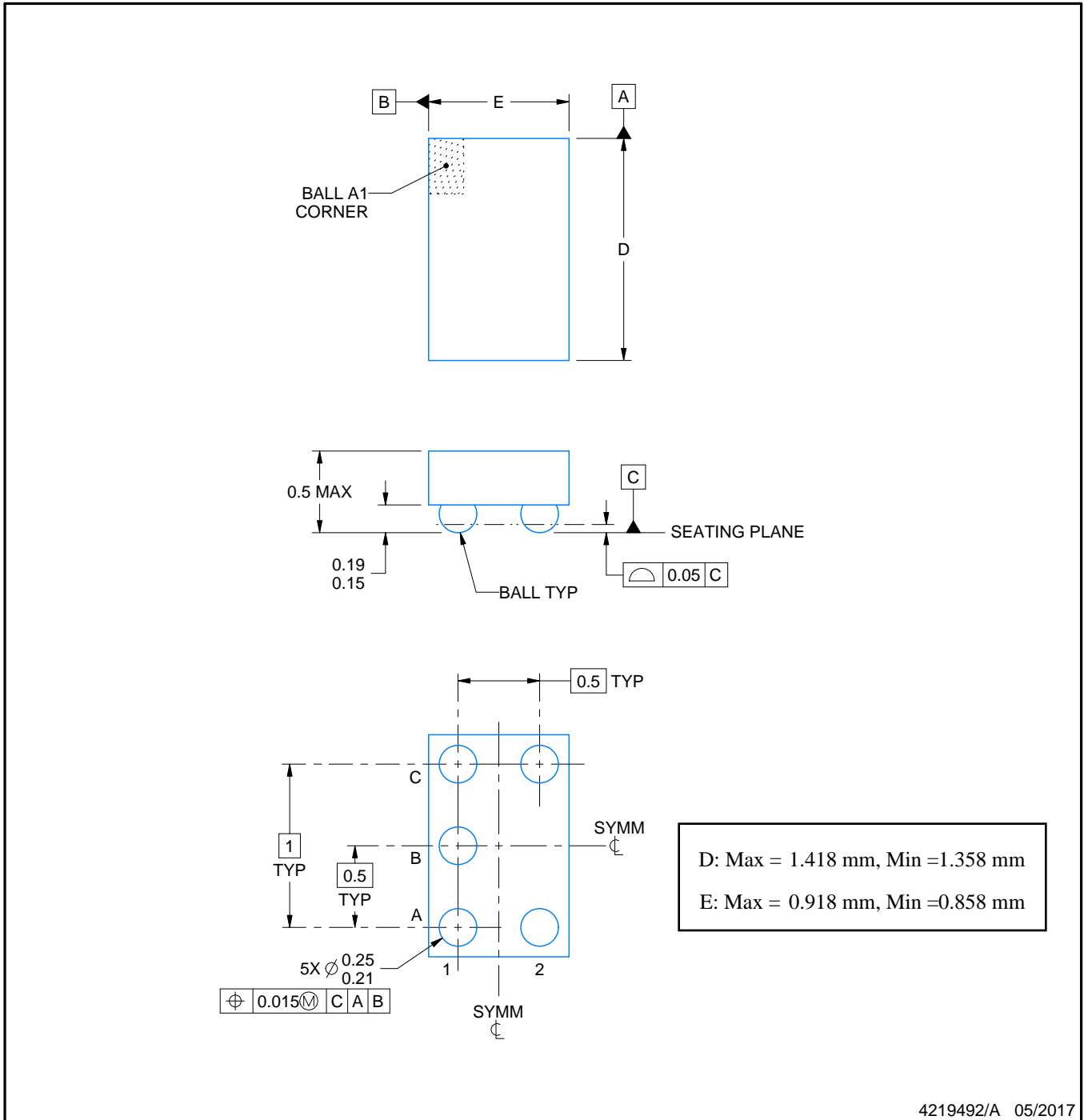
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

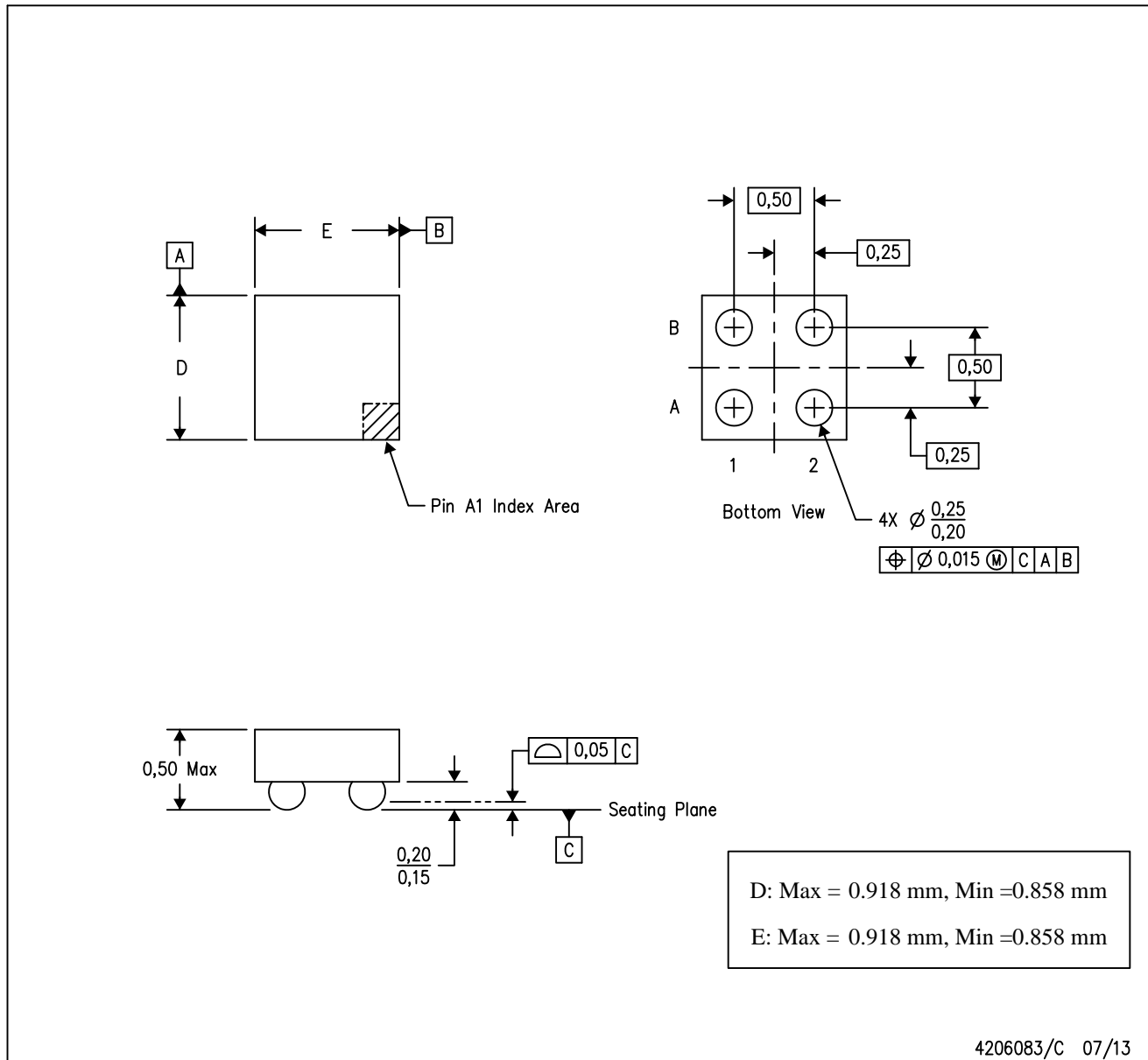
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



4206083/C 07/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.



4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

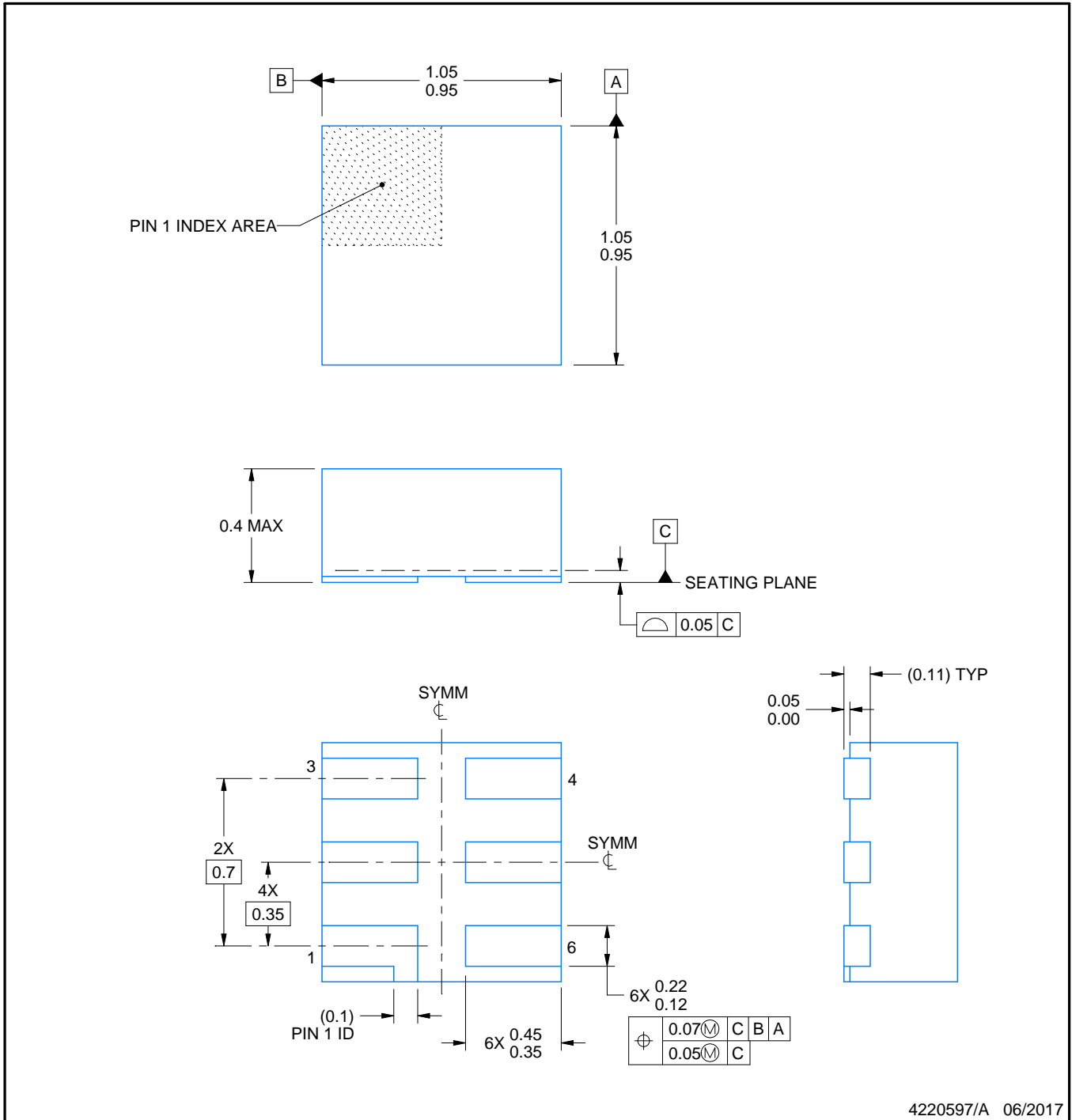


DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/A 06/2017

NOTES:

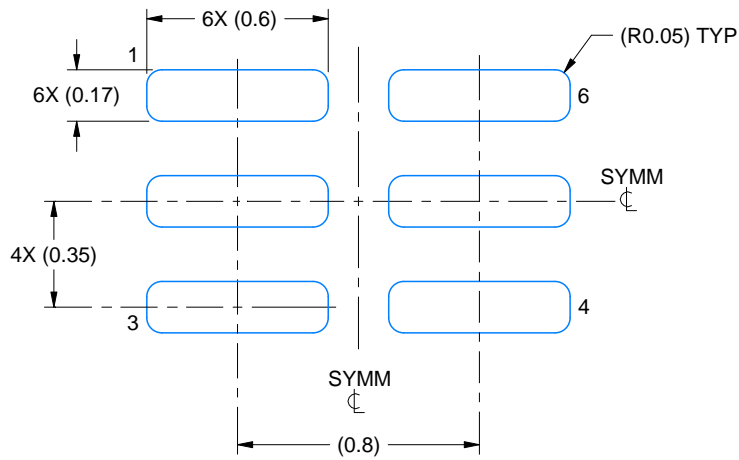
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

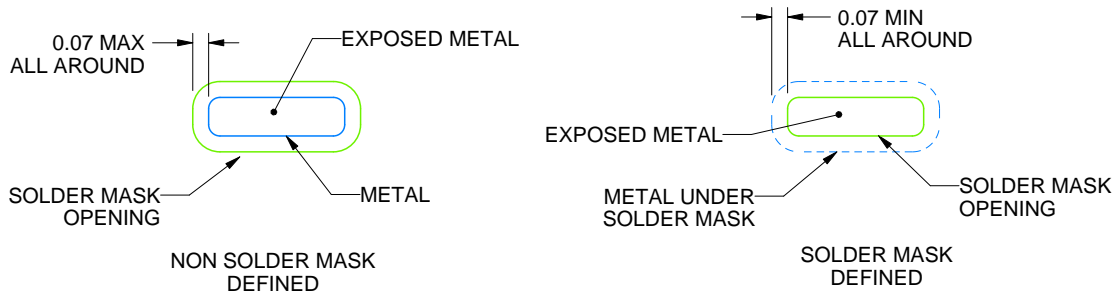
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

DRY0006A



PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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