MCP601/2/3/4

2.7V to 5.5V Single-Supply CMOS Op Amps

Features

- Single-Supply: 2.7V to 5.5V
- Rail-to-Rail Output
- Input Range Includes Ground
- Gain Bandwidth Product: 2.8 MHz (typ.)
- Unity-Gain Stable
- Low Quiescent Current: 230 µA/amplifier (typ.)
- Chip Select ($\overline{CS}$): **MCP603 only**
- Temperature Ranges:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
- Available in Single, Dual and Quad

Typical Applications

- Portable Equipment
- A/D Converter Driver
- Photo Diode Pre-amp
- Analog Filters
- Data Acquisition
- Notebooks and PDAs
- Sensor Interface

Available Tools

- SPICE Macro Models at www.microchip.com
- FilterLab® Software at www.microchip.com

Description

The Microchip Technology Inc. MCP601/2/3/4 family of low-power operational amplifiers (op amps) are offered in single (MCP601), single with Chip Select ($\overline{CS}$) (MCP603), dual (MCP602) and quad (MCP604) configurations. These op amps utilize an advanced CMOS technology that provides low bias current, high-speed operation, high open-loop gain and rail-to-rail output swing. This product offering operates with a single supply voltage that can be as low as 2.7V, while drawing 230 µA (typ.) of quiescent current per amplifier. In addition, the common mode input voltage range goes 0.3V below ground, making these amplifiers ideal for single-supply operation.

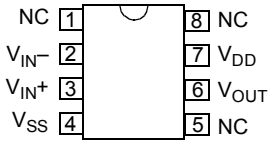
These devices are appropriate for low-power, battery-operated circuits due to the low quiescent current, for A/D convert driver amplifiers because of their wide bandwidth or for anti-aliasing filters by virtue of their low input bias current.

The MCP601, MCP602 and MCP603 are available in standard 8-lead PDIP, SOIC and TSSOP packages. The MCP601 and MCP601R are also available in a standard 5-lead SOT-23 package, while the MCP603 is available in a standard 6-lead SOT-23 package. The MCP604 is offered in standard 14-lead PDIP, SOIC and TSSOP packages.

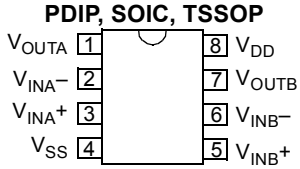
The MCP601/2/3/4 family is available in the Industrial and Extended temperature ranges and has a power supply range of 2.7V to 5.5V.

Package Types

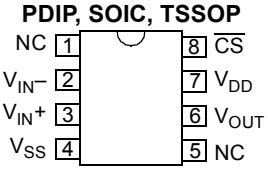
MCP601
PDIP, SOIC, TSSOP



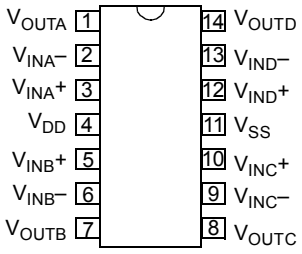
MCP602
PDIP, SOIC, TSSOP



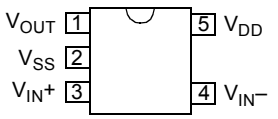
MCP603
PDIP, SOIC, TSSOP



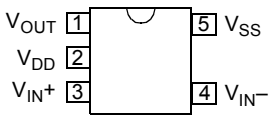
MCP604
PDIP, SOIC, TSSOP



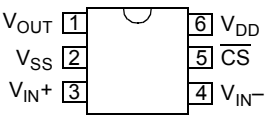
MCP601
SOT23-5



MCP601R
SOT23-5



MCP603
SOT23-6



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} - V_{SS} 7.0V
All inputs and outputs..... V_{SS} - 0.3V to V_{DD} + 0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current.....continuous
Current at Input Pin .....±2 mA
Current at Output and Supply Pins .....±30 mA
Storage temperature .....-65°C to +150°C
Junction temperature .....+150°C
ESD protection on all pins (HBM; MM) ..... ≥ 3 kV; 200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
$V_{IN}+$, $V_{INA}+$, $V_{INB}+$, $V_{INC}+$, $V_{IND}+$	Non-inverting Inputs
$V_{IN}–$, $V_{INA}–$, $V_{INB}–$, $V_{INC}–$, $V_{IND}–$	Inverting Inputs
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
V_{OUT}, V_{OUTA}, V_{OUTB}, V_{OUTC}, V_{OUTD}	Outputs
$\overline{CS}$	Chip Select
NC	No Internal Connection

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$ and R_L = 100 kΩ to $V_{DD}/2$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-2	±0.7	+2	mV	
Industrial Temperature	V_{OS}	-3	±1	+3	mV	T_A = -40°C to +85°C **(Note 1)**
Extended Temperature	V_{OS}	-4.5	±1	+4.5	mV	T_A = -40°C to +125°C **(Note 1)**
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.5	—	µV/°C	T_A = -40°C to +125°C
Power Supply Rejection	PSRR	80	88	—	dB	V_{DD} = 2.7V to 5.5V
Input Current and Impedance						
Input Bias Current	I_B	—	1	—	pA	
Industrial Temperature	I_B	—	20	60	pA	T_A = +85°C **(Note 1)**
Extended Temperature	I_B	—	450	5000	pA	T_A = +125°C **(Note 1)**
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common Mode						
Common Mode Input Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} – 1.2	V	
Common Mode Rejection Ratio	CMRR	75	90	—	dB	V_{DD} = 5.0V, V_{CM} = -0.3V to 3.8V
Open-loop Gain						
DC Open-loop Gain (large signal)	A_{OL}	100	115	—	dB	R_L = 25 kΩ to $V_{DD}/2$, V_{OUT} = 100 mV to V_{DD} – 100 mV
	A_{OL}	95	110	—	dB	R_L = 5 kΩ to $V_{DD}/2$, V_{OUT} = 100 mV to V_{DD} – 100 mV
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} – 20	mV	R_L = 25 kΩ to $V_{DD}/2$, Output overdrive = 0.5V
	V_{OL}, V_{OH}	V_{SS} + 45	—	V_{DD} – 60	mV	R_L = 5 kΩ to $V_{DD}/2$, Output overdrive = 0.5V
Linear Output Voltage Swing	V_{OUT}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 25 kΩ to $V_{DD}/2$, A_{OL} ≥ 100 dB
	V_{OUT}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 5 kΩ to $V_{DD}/2$, A_{OL} ≥ 95 dB
Output Short Circuit Current	I_{SC}	—	±22	—	mA	V_{DD} = 5.5V
	I_{SC}	—	±12	—	mA	V_{DD} = 2.7V
Power Supply						
Supply Voltage	V_{DD}	2.7	—	5.5	V	
Quiescent Current per Amplifier	I_Q	—	230	325	µA	I_O = 0

Note 1: These specifications are not tested in either the SOT-23 or TSSOP packages with date codes older than YYWW = 0408. In these cases, the minimum and maximum values are by design and characterization only.

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, R_L = 100 kΩ to $V_{DD}/2$ and C_L = 50 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Frequency Response						
Gain Bandwidth Product	GBWP	—	2.8	—	MHz	
Phase Margin	PM	—	50	—	°	G = +1 V/V
Step Response						
Slew Rate	SR	—	2.3	—	V/µs	G = +1 V/V
Settling Time (0.01%)	t_{settle}	—	4.5	—	µs	G = +1 V/V, 3.8V step
Noise						
Input Noise Voltage	E_{ni}	—	7	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	29	—	nV/√Hz	f = 1 kHz
	e_{ni}	—	21	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

MCP603 CHIP SELECT CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, R_L = 100 kΩ to $V_{DD}/2$ and C_L = 50 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
DC Characteristics						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	-1.0	—	—	µA	$\overline{CS}$ = 0.2V_{DD}
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.7	2.0	µA	$\overline{CS}$ = V_{DD}
Shutdown V_{SS} current	I_{Q_SHDN}	-2.0	-0.7	—	µA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage in Shutdown	I_{O_SHDN}	—	1	—	nA	
$\overline{CS}$ Threshold Hysteresis	HYST	—	0.3	—	V	Internal switch
Timing						
$\overline{CS}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	3.1	10	µs	$\overline{CS} \le 0.2V_{DD}$, G = +1 V/V
$\overline{CS}$ High to Amplifier Output High-Z Time	t_{OFF}	—	100	—	ns	$\overline{CS} \ge 0.8V_{DD}$, G = +1 V/V, No load.

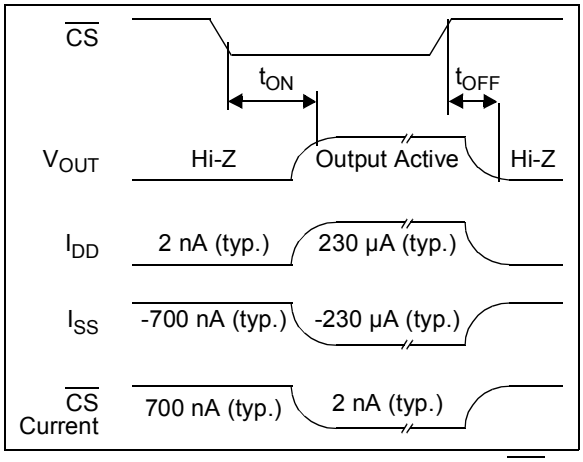


FIGURE 1-1: *MCP603 Chip Select ($\overline{CS}$) Timing Diagram.*

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	Industrial temperature parts
	T_A	-40	—	+125	°C	Extended temperature parts
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 6L-SOT23	θ_{JA}	—	230	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	124	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The Industrial temperature parts operate over this extended range, but with reduced performance. The Extended temperature specs do not apply to Industrial temperature parts. In any case, the internal Junction temperature (T_J) must not exceed the absolute maximum specification of 150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, $V_{OUT} \approx V_{DD}/2$ and C_L = 50 pF.

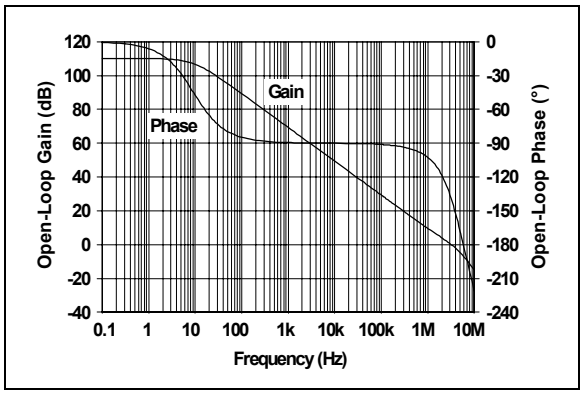


FIGURE 2-1: *Open-Loop Gain, Phase vs. Frequency.*

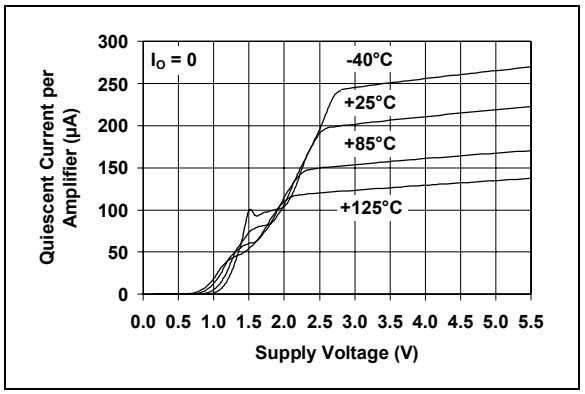


FIGURE 2-4: *Quiescent Current vs. Supply Voltage.*

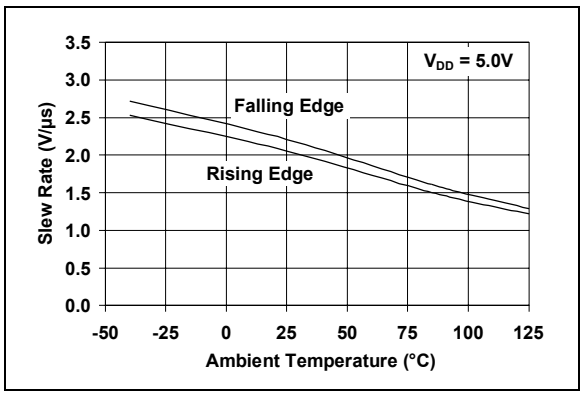


FIGURE 2-2: *Slew Rate vs. Temperature.*

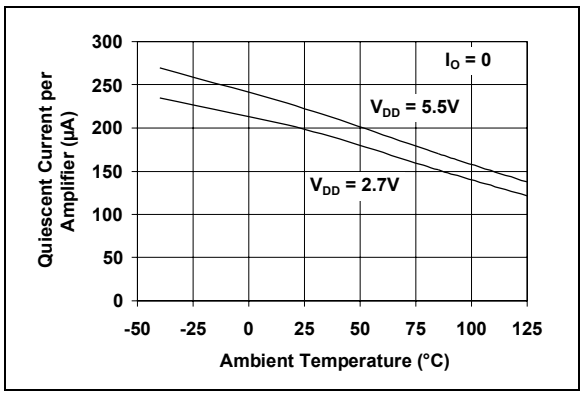


FIGURE 2-5: *Quiescent Current vs. Temperature.*

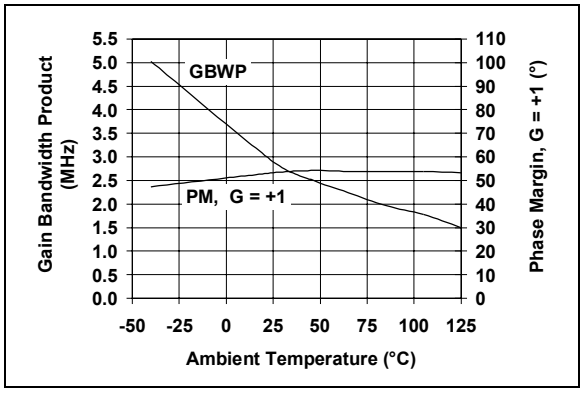


FIGURE 2-3: *Gain Bandwidth Product, Phase Margin vs. Temperature.*

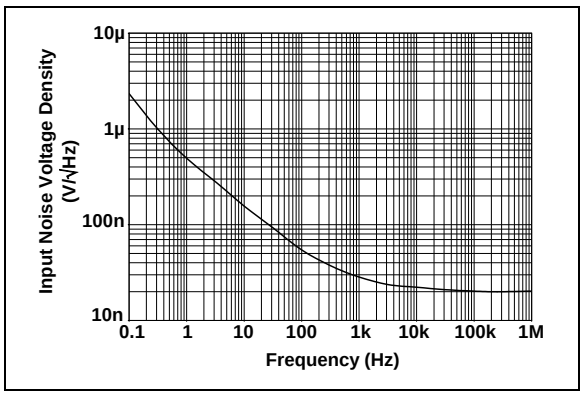


FIGURE 2-6: *Input Noise Voltage Density vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, $V_{OUT} \approx V_{DD}$/2 and C_L = 50 pF.

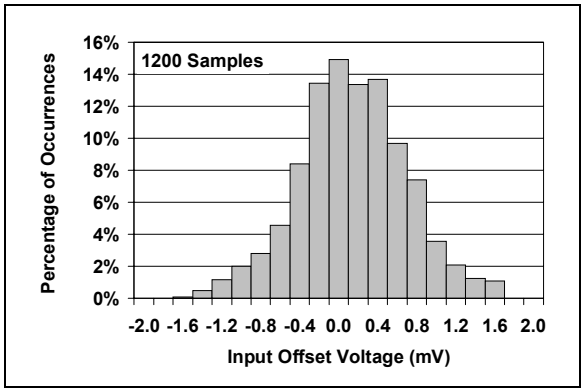


FIGURE 2-7: *Input Offset Voltage.*

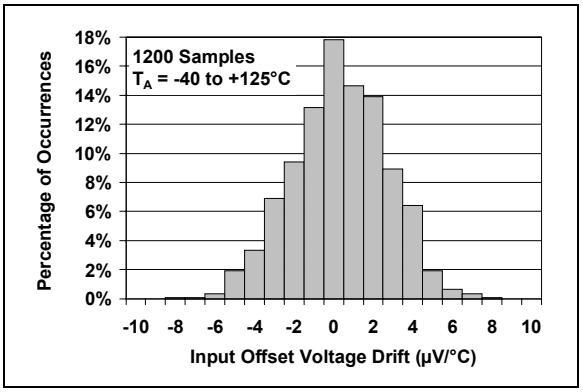


FIGURE 2-10: *Input Offset Voltage Drift.*

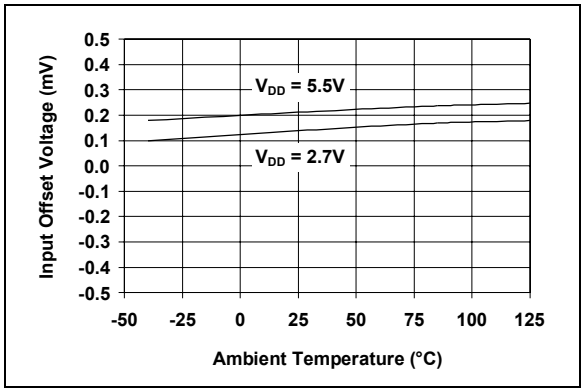


FIGURE 2-8: *Input Offset Voltage vs. Temperature.*

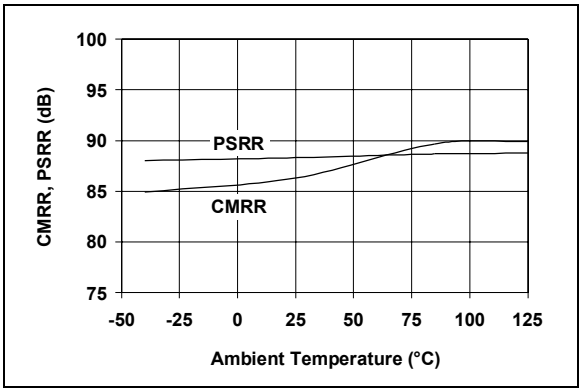


FIGURE 2-11: *CMRR, PSRR vs. Temperature.*

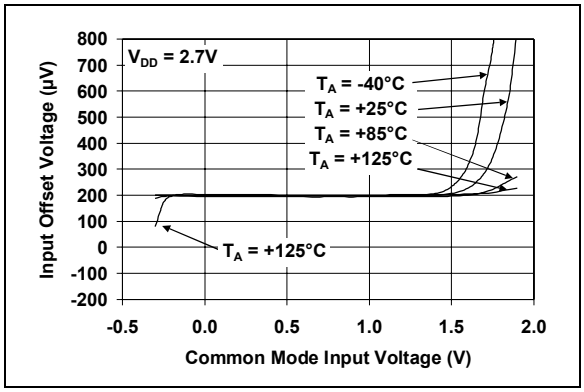


FIGURE 2-9: *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 2.7V.*

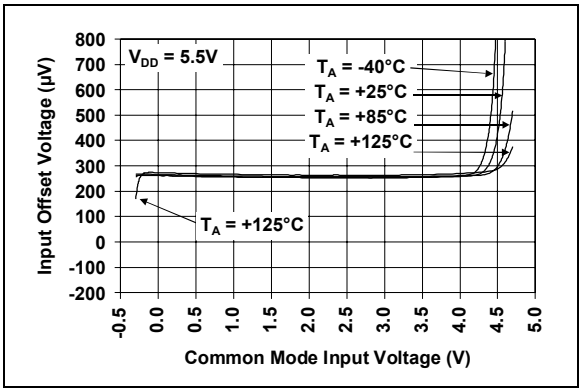


FIGURE 2-12: *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 5.5V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, $V_{OUT} \approx V_{DD}/2$ and C_L = 50 pF.

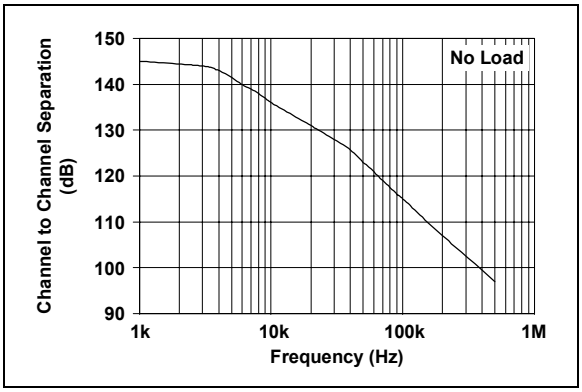


FIGURE 2-13: *Channel-to-Channel Separation vs. Frequency.*

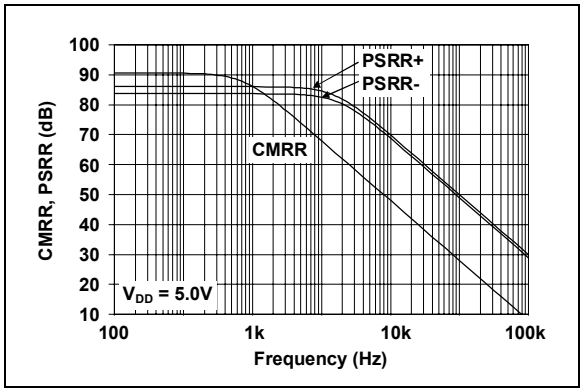


FIGURE 2-16: *CMRR, PSRR vs. Frequency.*

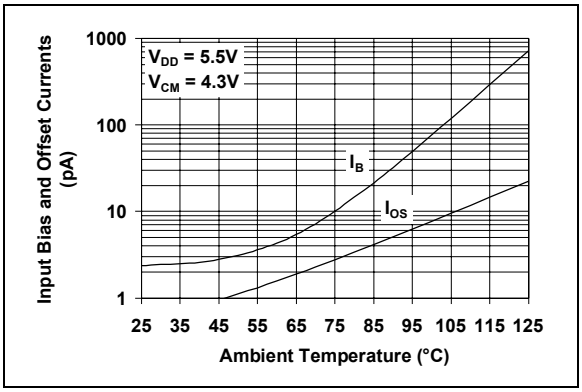


FIGURE 2-14: *Input Bias Current, Input Offset Current vs. Ambient Temperature.*

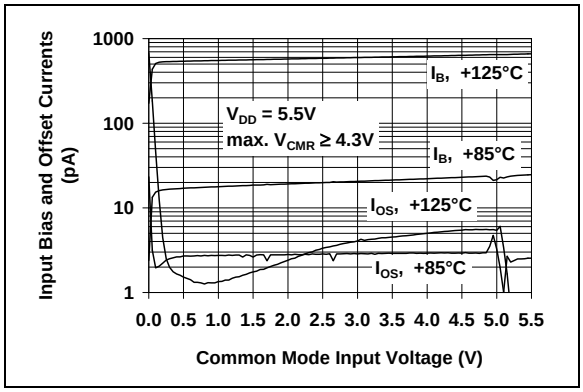


FIGURE 2-17: *Input Bias Current, Input Offset Current vs. Common Mode Input Voltage.*

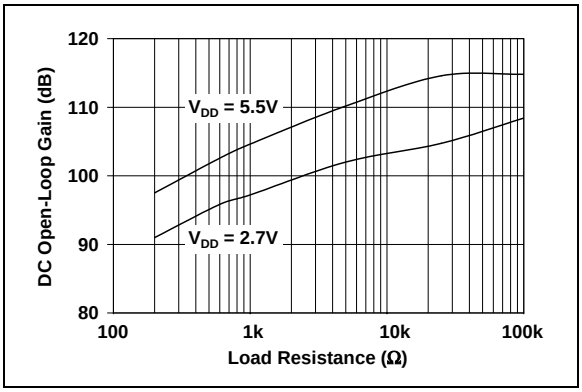


FIGURE 2-15: *DC Open-Loop Gain vs. Load Resistance.*

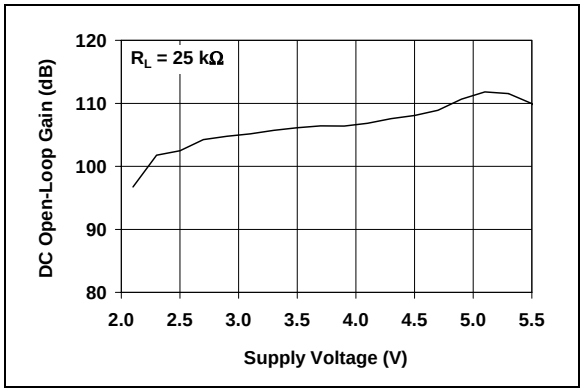


FIGURE 2-18: *DC Open-Loop Gain vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, V_{OUT} ≈ V_{DD}/2 and C_L = 50 pF.

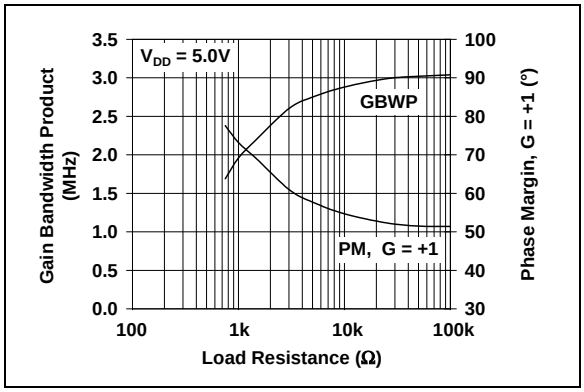


FIGURE 2-19: *Gain Bandwidth Product, Phase Margin vs. Load Resistance.*

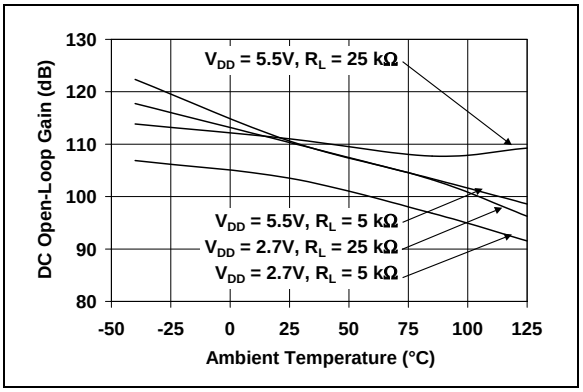


FIGURE 2-22: *DC Open-Loop Gain vs. Temperature.*

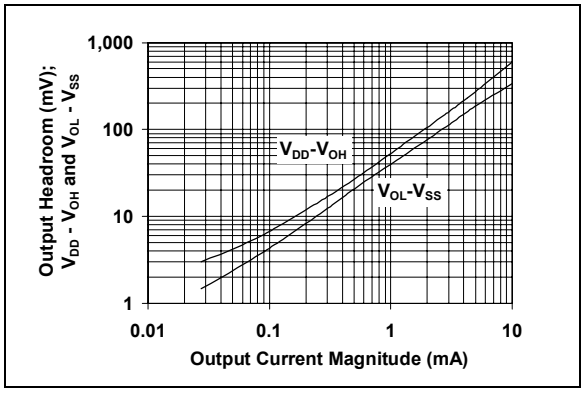


FIGURE 2-20: *Output Voltage Headroom vs. Output Current.*

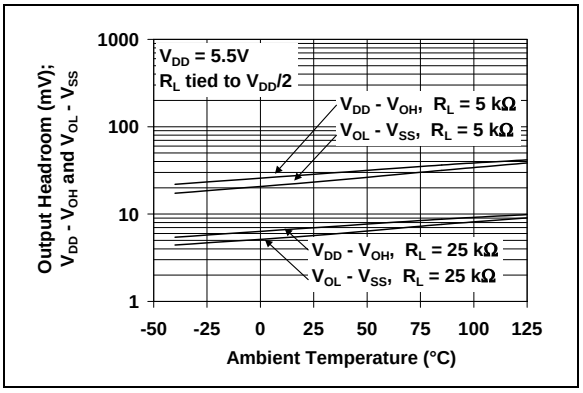


FIGURE 2-23: *Output Voltage Headroom vs. Temperature.*

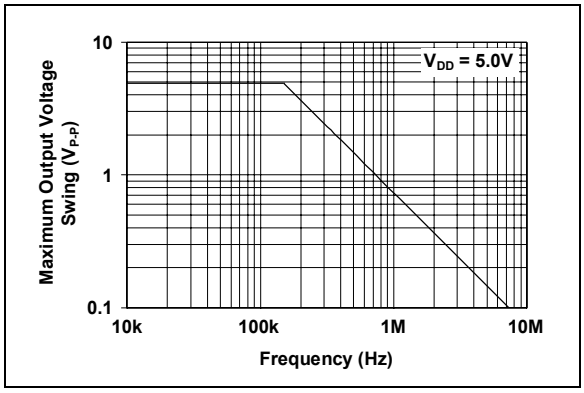


FIGURE 2-21: *Maximum Output Voltage Swing vs. Frequency.*

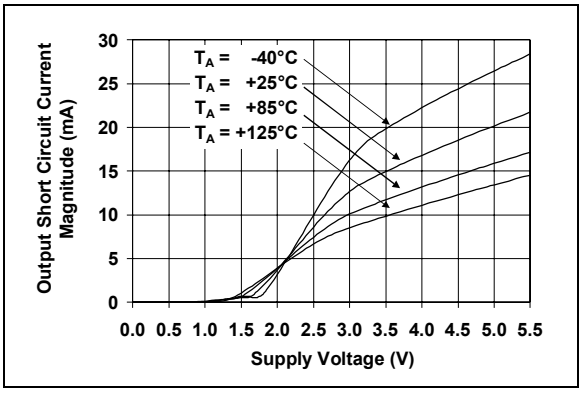


FIGURE 2-24: *Output Short-Circuit Current vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, V_{OUT} ≈ V_{DD}/2 and C_L = 50 pF.

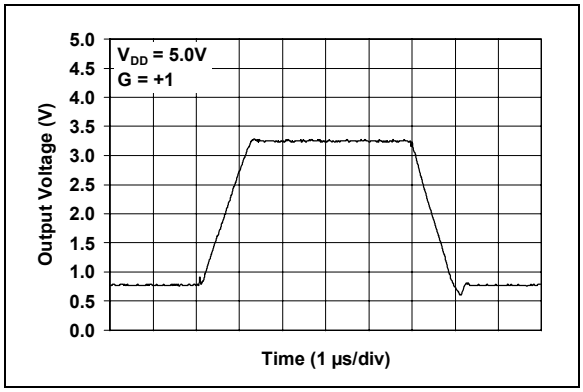


FIGURE 2-25: *Large Signal Non-Inverting Pulse Response.*

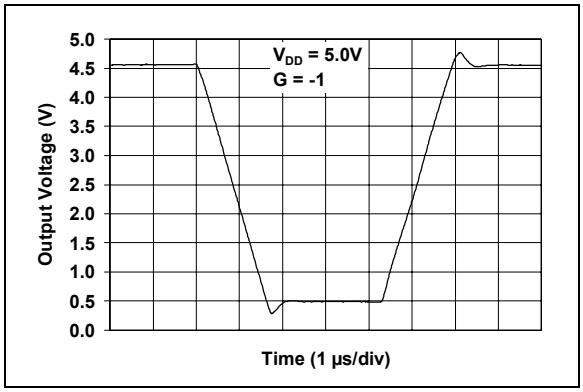


FIGURE 2-28: *Large Signal Inverting Pulse Response.*

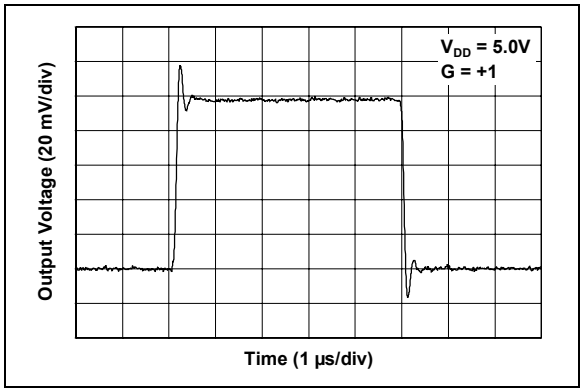


FIGURE 2-26: *Small Signal Non-Inverting Pulse Response.*

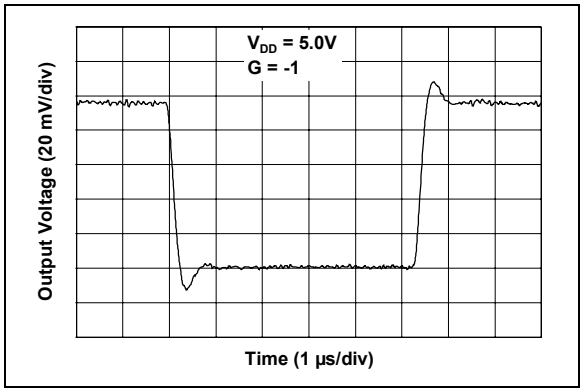


FIGURE 2-29: *Small Signal Inverting Pulse Response.*

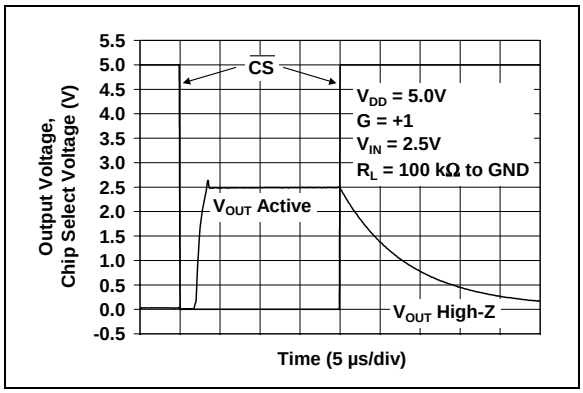


FIGURE 2-27: *Chip Select Timing (MCP603).*

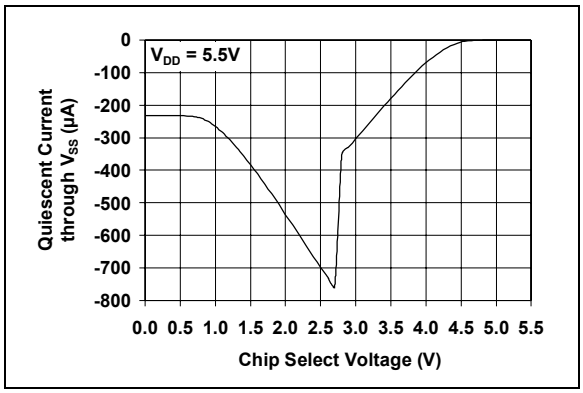


FIGURE 2-30: *Quiescent Current Through V_{SS} vs. Chip Select Voltage (MCP603).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 100 kΩ to V_{DD}/2, V_{OUT} ≈ V_{DD}/2 and C_L = 50 pF.

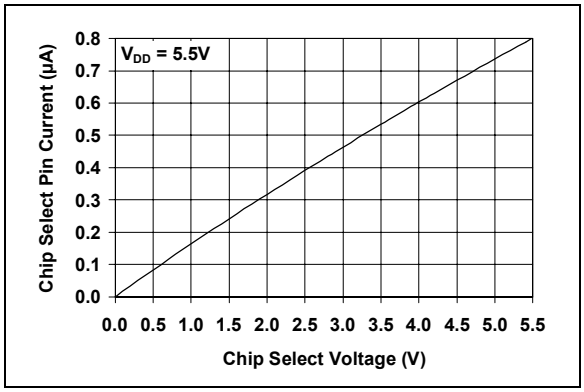


FIGURE 2-31: *Chip Select Pin Input Current vs. Chip Select Voltage.*

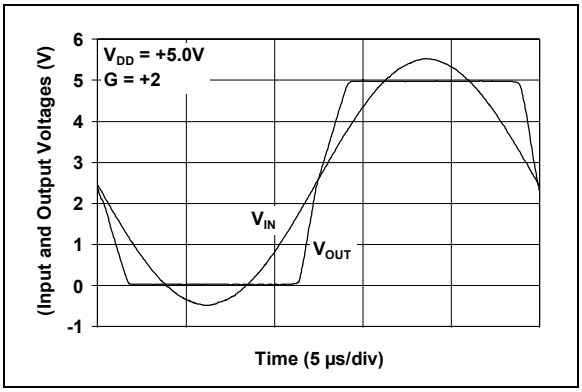


FIGURE 2-33: *The MCP601/2/3/4 family of op amps shows no phase reversal under input overdrive.*

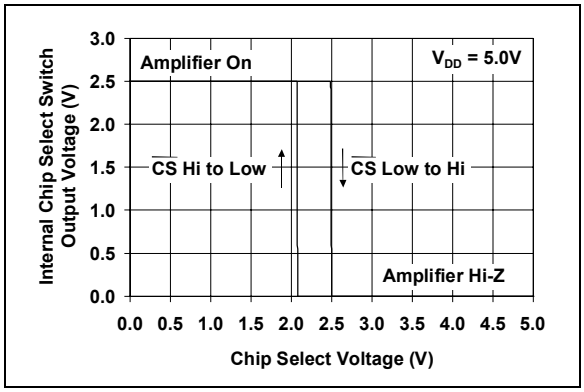


FIGURE 2-32: *Hysteresis of Chip Select's Internal Switch.*

3.0 APPLICATIONS INFORMATION

The MCP601/2/3/4 family of op amps are fabricated on Microchip's state-of-the-art CMOS process. They are unity-gain stable and suitable for a wide range of general purpose applications.

3.1 Input

The MCP601/2/3/4 amplifier family is designed to not exhibit phase reversal when the input pins exceed the supply rails. Figure 2-33 shows an input voltage that exceeds both supplies with no resulting phase inversion.

The Common Mode Input Voltage Range (V_{CMR}) includes ground in single-supply systems (V_{SS}), but does not include V_{DD}. This means that the amplifier input behaves linearly as long as the Common Mode Input Voltage (V_{CM}) is kept within the specified V_{CMR} limits (V_{SS} – 0.3V to V_{DD} – 1.2V at +25°C).

Input voltages that exceed the input voltage range (V_{SS} – 0.3V to V_{DD} – 1.2V at +25°C) can cause excessive current to flow into or out of the input pins. Current beyond ±2 mA may cause reliability problems. Applications that exceed this rating must externally limit the input current with a resistor (R_{IN}), as shown in Figure 3-1.

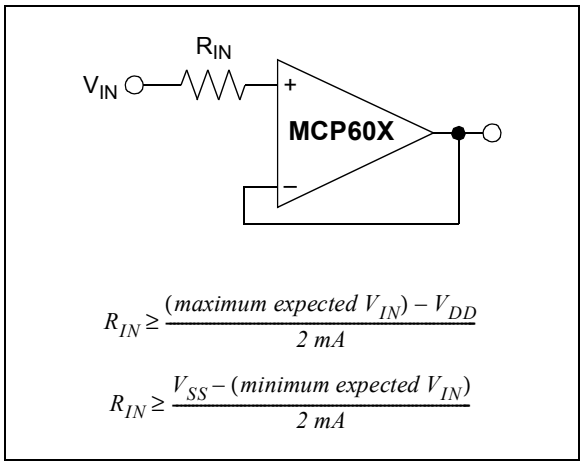


FIGURE 3-1: *R_{IN} limits the current flow into an input pin.*

3.2 Rail-to-Rail Output

There are two specifications that describe the output swing capability of the MCP601/2/3/4 family of op amps. The first specification (Maximum Output Voltage Swing) defines the absolute maximum swing that can be achieved under the specified load conditions. For instance, the output voltage swings to within 15 mV of the negative rail with a 25 kΩ load to $V_{DD}/2$. Figure 2-33 shows how the output voltage is limited when the input goes beyond the linear region of operation.

The second specification that describes the output swing capability of these amplifiers is the Linear Output Voltage Swing. This specification defines the maximum output swing that can be achieved while the amplifier is still operating in its linear region. To verify linear operation in this range, the large signal (DC Open-Loop Gain (A_{OL})) is measured at points 100 mV inside the supply rails. The measurement must exceed the specified gains in the specification table.

3.3 MCP603 Chip Select ($\overline{CS}$)

The MCP603 is a single amplifier with Chip Select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to -0.7 µA (typ.), which is pulled through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. Pulling $\overline{CS}$ low enables the amplifier and, if the $\overline{CS}$ pin is left floating, the amplifier may not operate properly. Figure 1-1 is the Chip Select timing diagram and shows the output voltage, supply currents and $\overline{CS}$ current in response to a $\overline{CS}$ pulse. Figure 2-27 shows the measured output voltage response to a $\overline{CS}$ pulse.

3.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response.

When driving large capacitive loads with these op amps (e.g., > 40 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 3-2) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

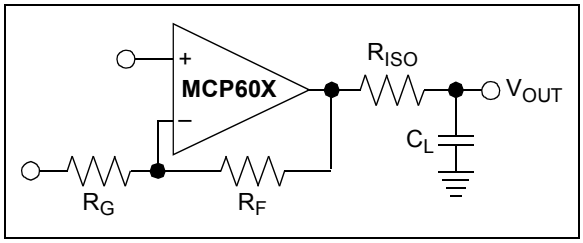


FIGURE 3-2: *Output resistor R_{ISO} stabilizes large capacitive loads.*

Figure 3-3 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N) in order to make it easier to interpret the plot for arbitrary gains. G_N is the circuit's noise gain. For non-inverting gains, G_N and the gain are equal. For inverting gains, G_N = 1 + |Gain| (e.g., -1 V/V gives G_N = +2 V/V).

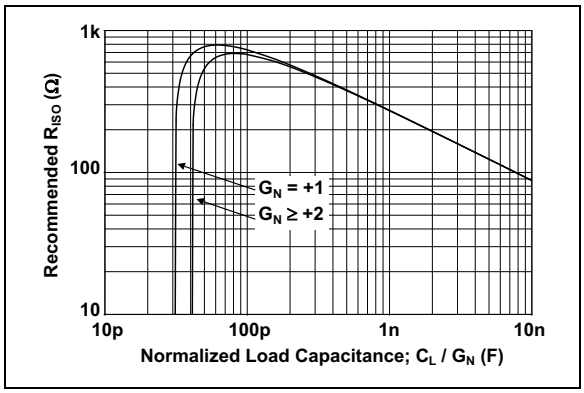


FIGURE 3-3: *Recommended R_{ISO} values for capacitive loads.*

Once you've selected R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot in your circuit. Evaluation on the bench and simulations with the MCP601/2/3/4 SPICE macro model are very helpful. Modify R_{ISO}'s value until the response is reasonable.

3.5 Supply Bypass

With this family of op amps, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other parts.

3.6 PCB Surface Leakage

In applications where low input bias current is critical, printed circuit board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP601/2/3/4 family's bias current at +25°C (1 pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 3-4.

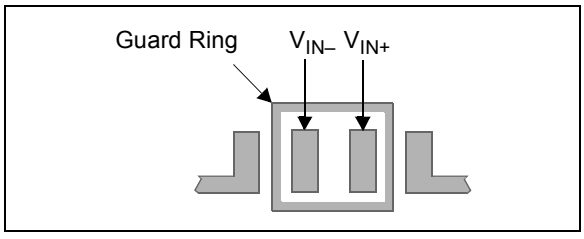


FIGURE 3-4: *Example Guard Ring layout.*

1. Connect the guard ring to the inverting input pin (V_{IN}–) for non-inverting gain amplifiers, including unity-gain buffers. This biases the guard ring to the common mode input voltage.
2. Connect the guard ring to the non-inverting input pin (V_{IN}+) for inverting gain amplifiers and transimpedance amplifiers (converts current to voltage, such as photo detectors). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).

3.7 Typical Applications

3.7.1 ANALOG FILTERS

Figure 3-5 and Figure 3-6 show low-pass, second-order, Butterworth filters with a cutoff frequency of 10 Hz. The filter in Figure 3-5 has a non-inverting gain of +1 V/V, and the filter in Figure 3-6 has an inverting gain of -1 V/V.

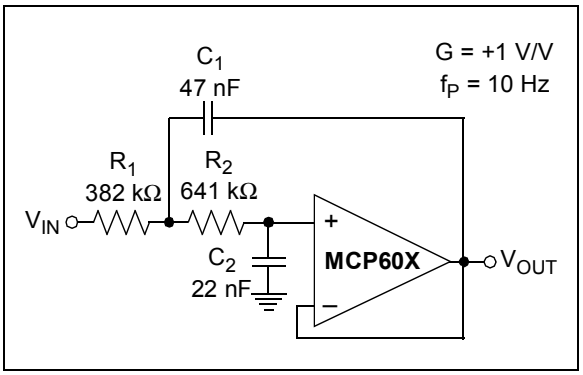


FIGURE 3-5: *Second-Order, Low-Pass Sallen-Key Filter.*

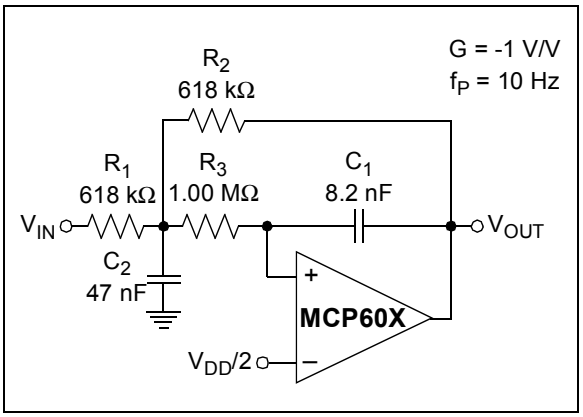


FIGURE 3-6: *Second-Order, Low-Pass Multiple-Feedback Filter.*

The MCP601/2/3/4 family of op amps have low input bias current, which allows the designer to select larger resistor values and smaller capacitor values for these filters. This helps produce a compact PCB layout. These filters, and others, can be designed using Microchip's FilterLab® software.

3.7.2 INSTRUMENTATION AMPLIFIER CIRCUITS

Instrumentation amplifiers have a differential input that subtracts one input voltage from another and rejects common mode signals. These amplifiers also provide a single-ended output voltage.

The three-op amp instrumentation amplifier is illustrated in Figure 3-7. One advantage of this approach is unity-gain operation, while one disadvantage is that the common mode input range is reduced as R_2/R_G gets larger.

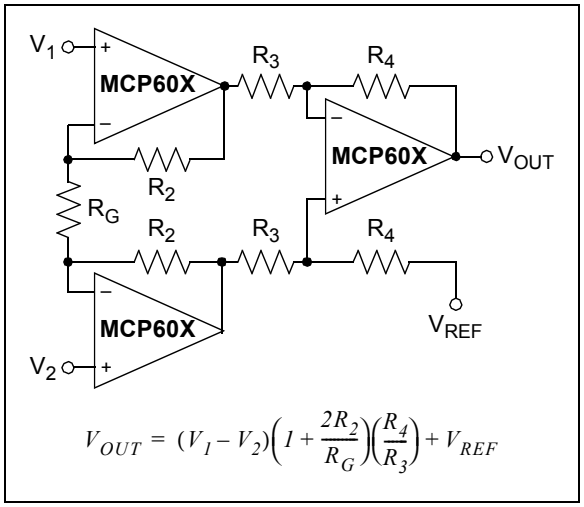


FIGURE 3-7: *Three-Op Amp Instrumentation Amplifier.*

The two-op amp instrumentation amplifier is shown in Figure 3-8. While its power consumption is lower than the three-op amp version, its main drawbacks are that the common mode range is reduced with higher gains and it must be configured in gains of two or higher.

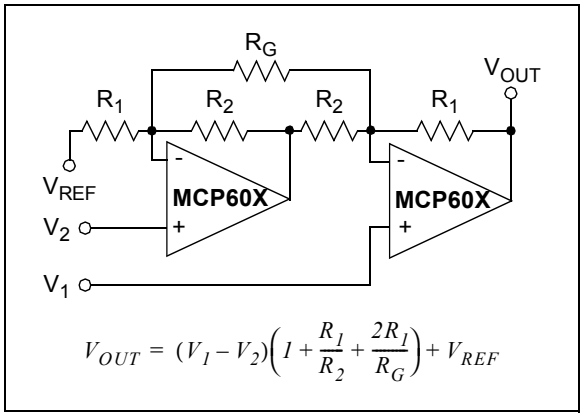


FIGURE 3-8: *Two-Op Amp Instrumentation Amplifier.*

Both instrumentation amplifiers should use a bulk bypass capacitor of at least 1 µF. The CMRR of these amplifiers will be set by both the op amp CMRR and resistor matching.

3.7.3 PHOTO DETECTION

The MCP601/2/3/4 op amps can be used to easily convert the signal from a sensor that produces an output current (such as a photo diode) into a voltage (a transimpedance amplifier). This is implemented with a single resistor (R_2) in the feedback loop of the amplifiers shown in Figure 3-9 and Figure 3-10. The optional capacitor (C_2) sometimes provides stability for these circuits.

A photodiode configured in the Photovoltaic mode has zero voltage potential placed across it (Figure 3-9). In this mode, the light sensitivity and linearity is maximized, making it best suited for precision applications. The key amplifier specifications for this application are: low input bias current, low noise, common mode input voltage range (including ground) and rail-to-rail output.

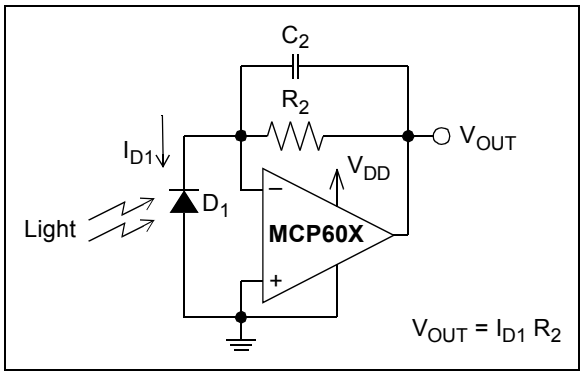


FIGURE 3-9: *Photovoltaic Mode Detector.*

In contrast, a photodiode that is configured in the Photoconductive mode has a reverse bias voltage across the photo-sensing element (Figure 3-10). This decreases the diode capacitance, which facilitates high-speed operation (e.g., high-speed digital communications). The design trade-off is increased diode leakage current and linearity errors. The op amp needs to have a wide Gain Bandwidth Product (GBWP).

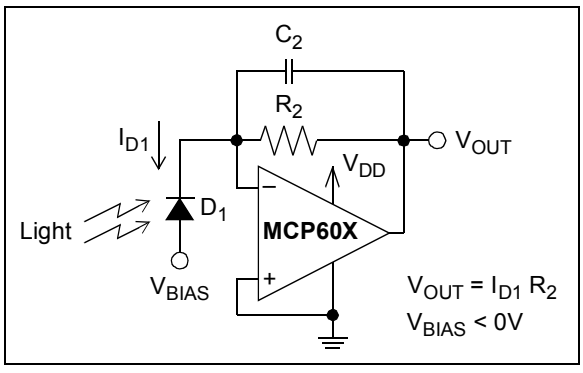


FIGURE 3-10: *Photoconductive Mode Detector.*

4.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP601/2/3/4 family of op amps.

4.1 SPICE Macro Model

The latest SPICE macro model of the MCP601/2/3/4 op amps is available on Microchip's web site at www.microchip.com. This model is intended as an initial design tool that works well in the op amp's linear region of operation at room temperature. See the SPICE model firmware for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specs and plots.

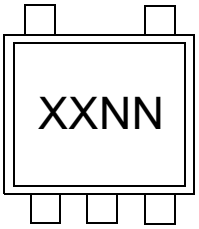
4.2 FilterLab® 2.0

FilterLab® 2.0 is an innovative software tool that simplifies analog active-filter (using op amps) design. Available at no cost from Microchip's web site at www.microchip.com, the FilterLab active-filter software design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.0 PACKAGING INFORMATION

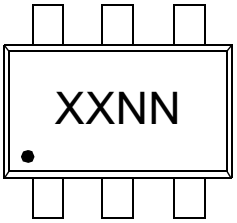
5.1 Package Marking Information

5-Lead SOT-23 **(MCP601 and MCP601R Only)**

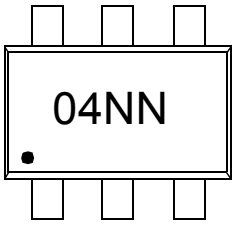


Example:

6-Lead SOT-23A **(MCP603 Only)**



Example:



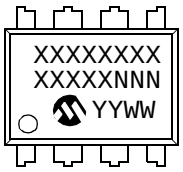
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

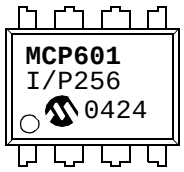
***** Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

Package Marking Information

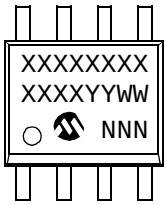
8-Lead PDIP (300 mil)



Example:



8-Lead SOIC (150 mil)



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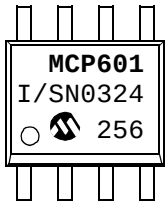
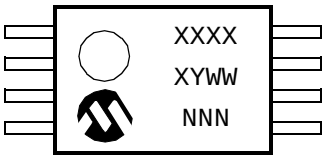


8-Lead TSSOP



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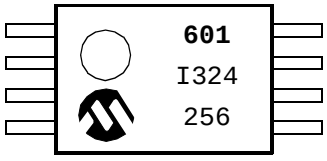
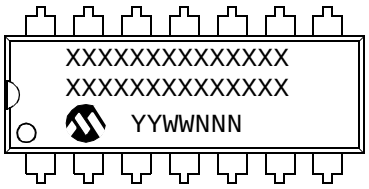
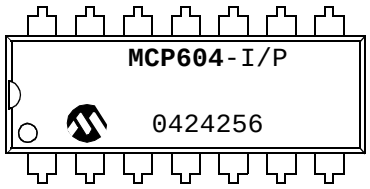


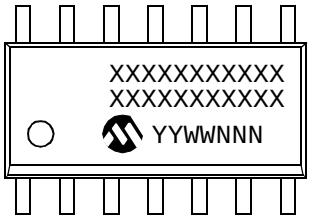
14-Lead PDIP (300 mil) (**MCP604** Only)



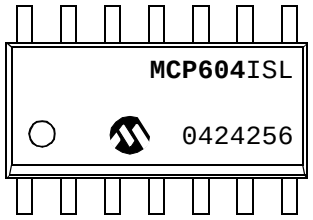
Example:



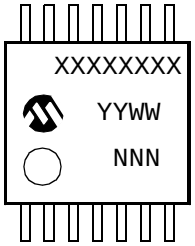
14-Lead SOIC (150 mil) (**MCP604** Only)



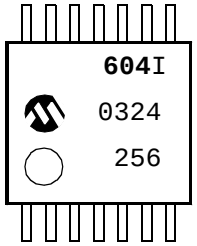
Example:



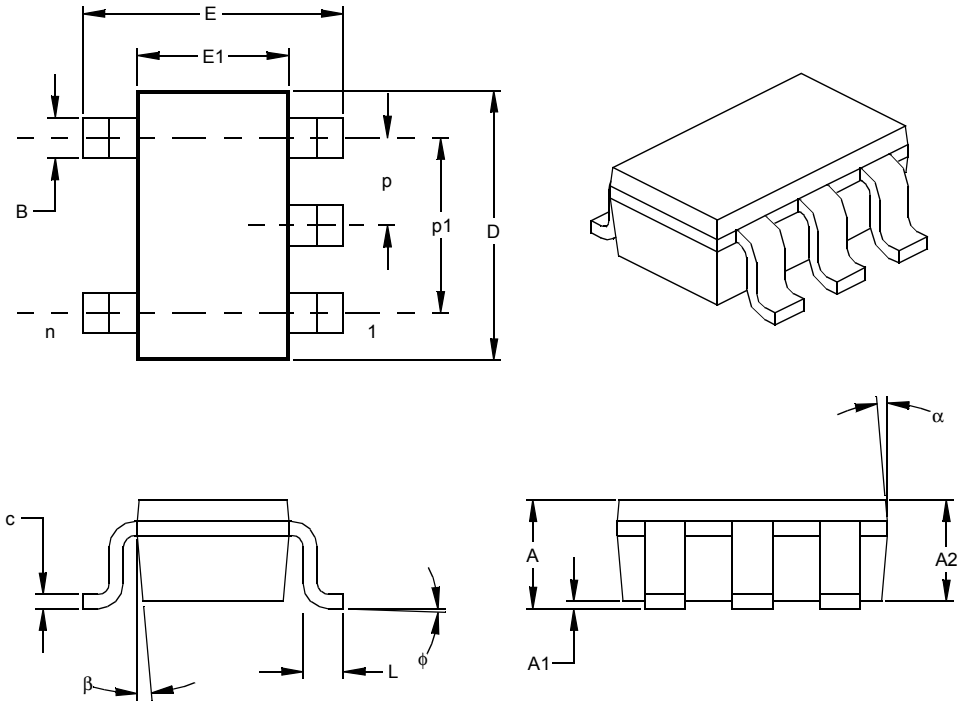
14-Lead TSSOP (4.4mm) (**MCP604** Only)



Example:



5-Lead Plastic Small Outline Transistor (OT) (SOT-23)

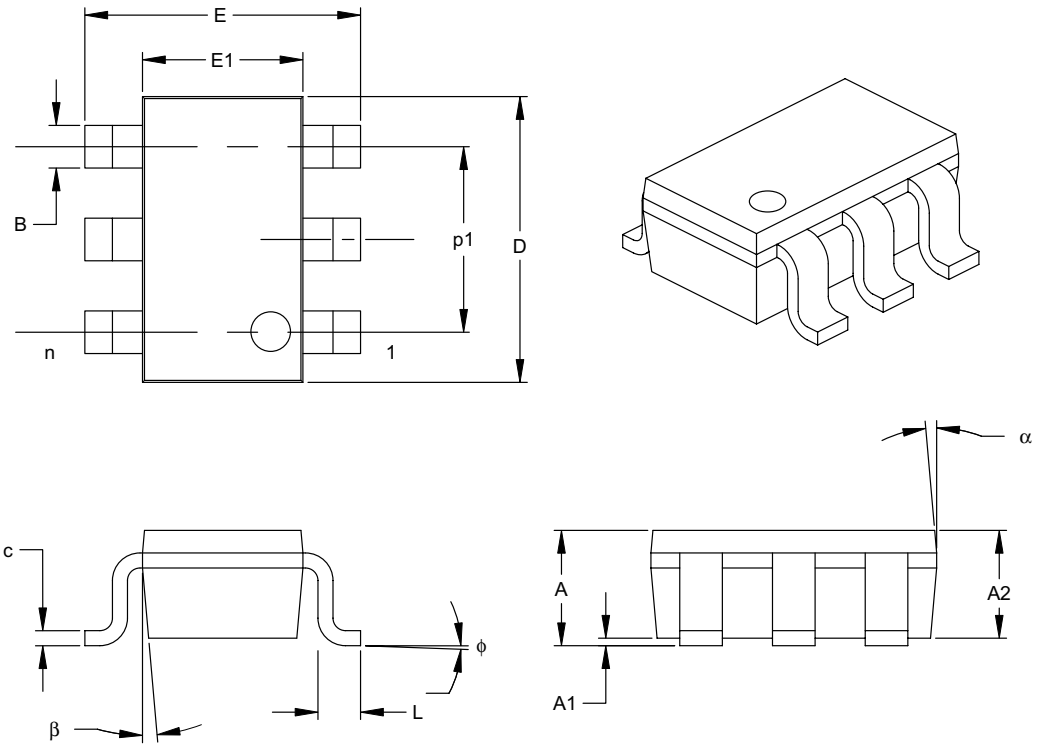


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	ϕ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-178
Drawing No. C04-091

6-Lead Plastic Small Outline Transistor (CH) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		6			6	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

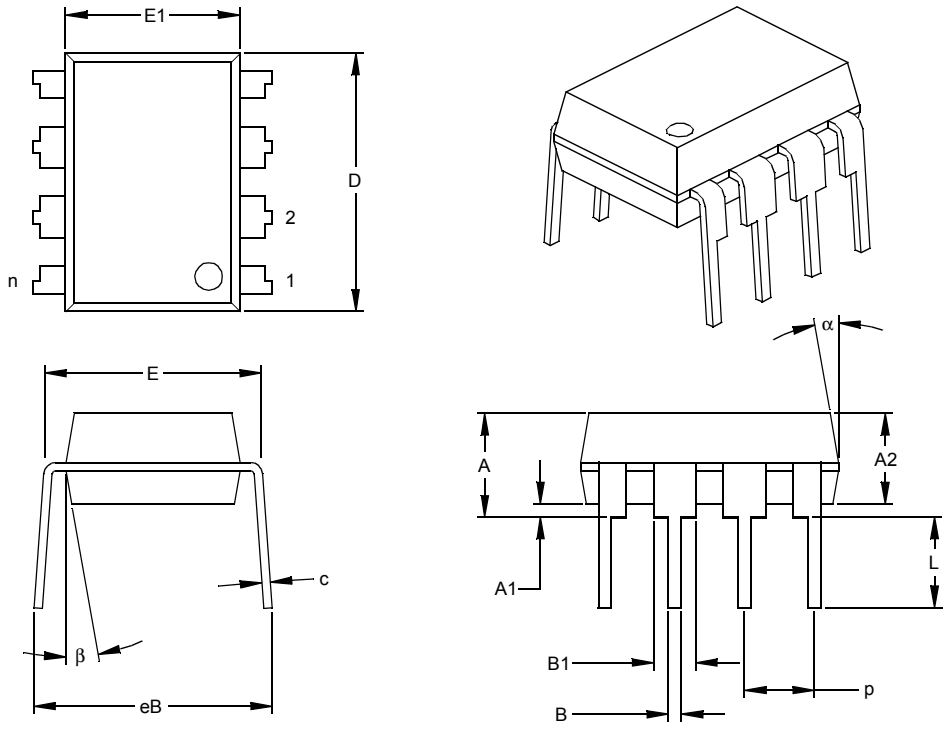
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (formerly EIAJ) equivalent: SC-74A

Drawing No. C04-120

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

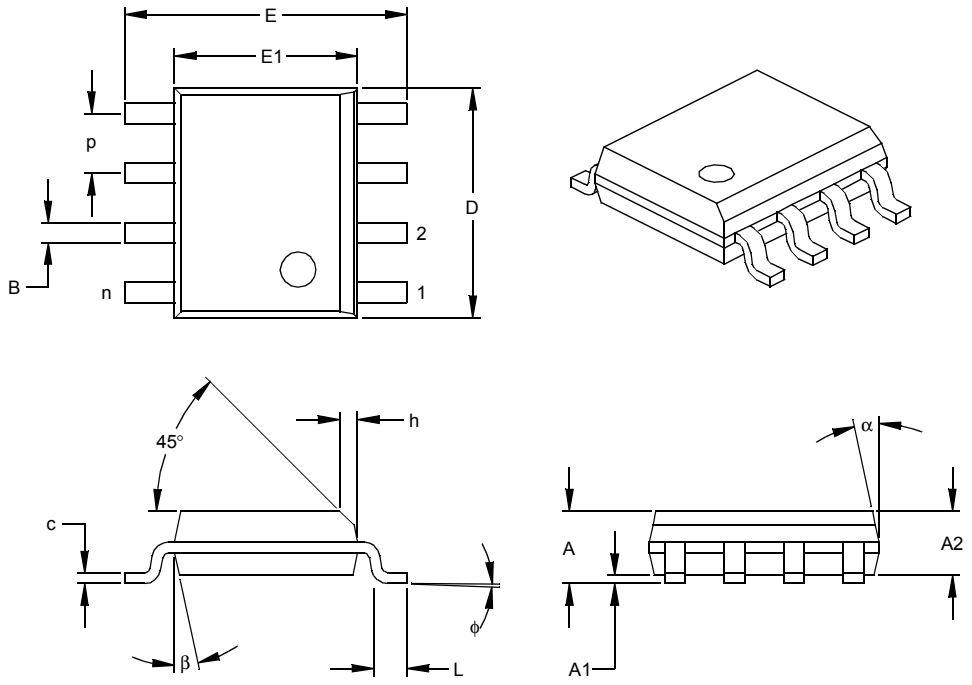


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

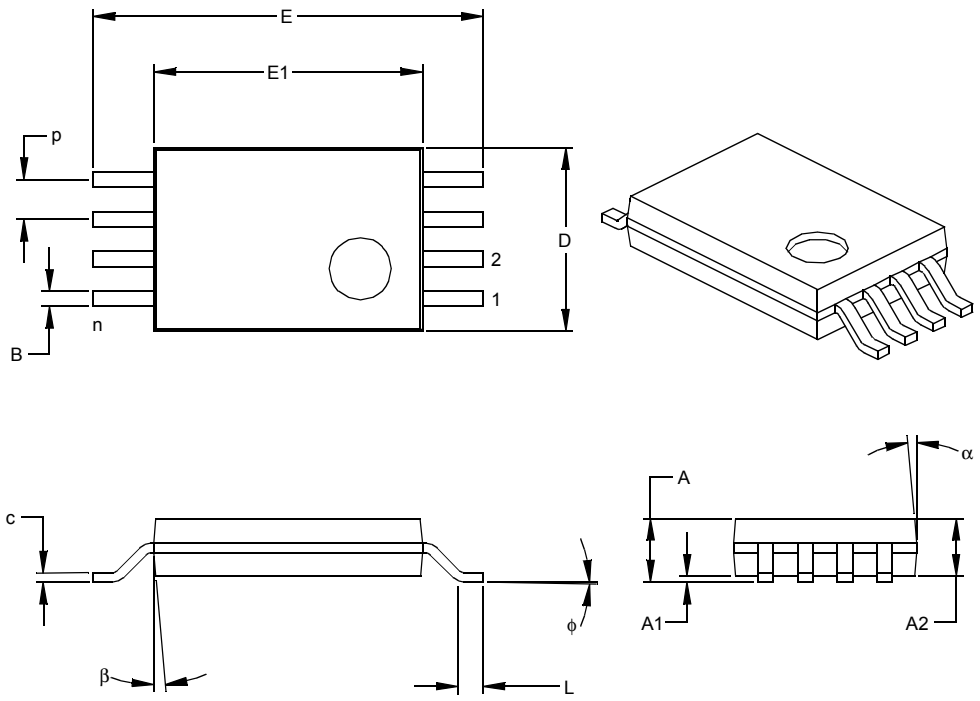


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

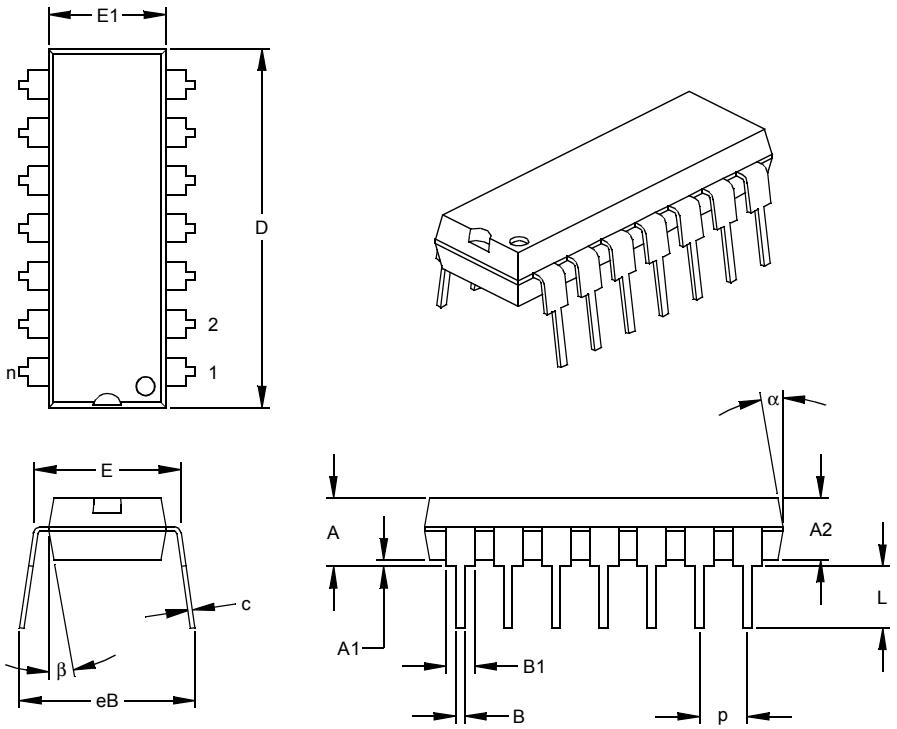


Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

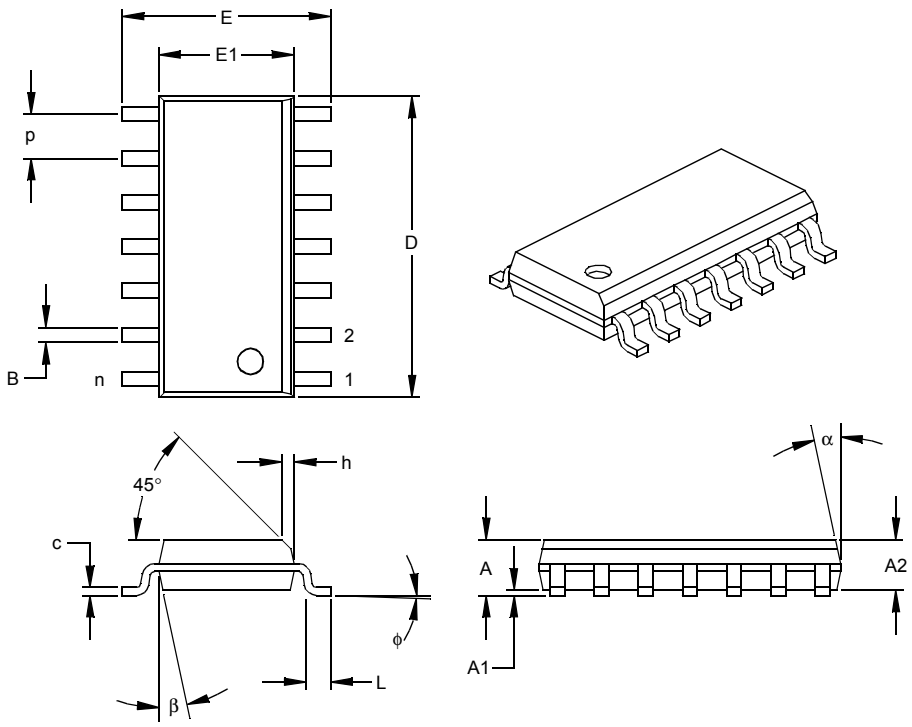
14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

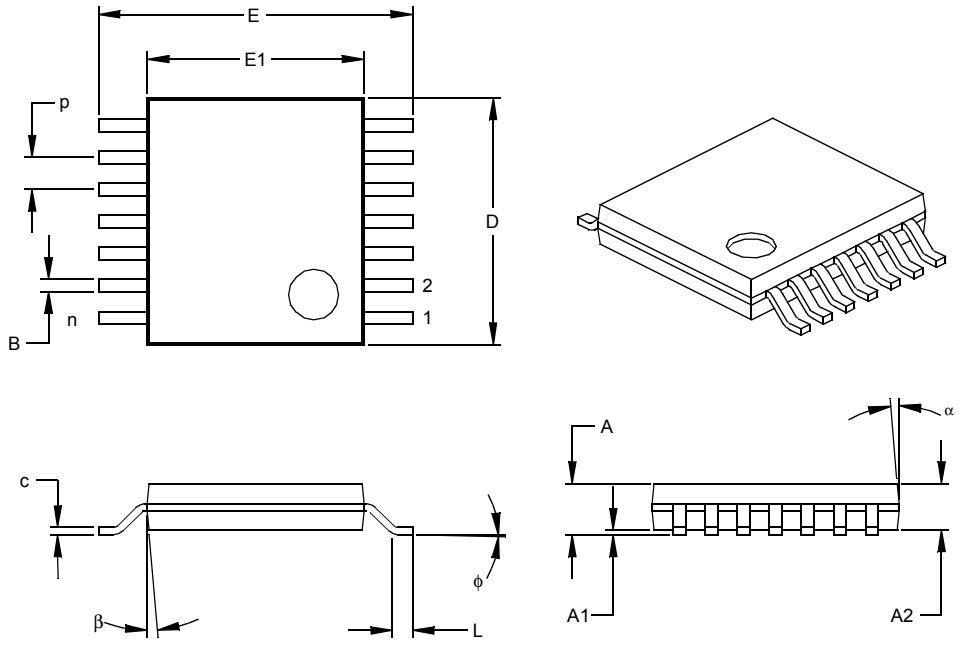


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device	MCP601	Single Op Amp
	MCP601T	Single Op Amp (Tape and Reel for SOT23, SOIC and TSSOP)
	MCP601RT	Single Op Amp (Tape and Reel for SOT23-5)
	MCP602	Dual Op Amp
	MCP602T	Dual Op Amp (Tape and Reel for SOIC and TSSOP)
	MCP603	Single Op Amp with Chip Select
	MCP603T	Single Op Amp with Chip Select (Tape and Reel for SOT23, SOIC and TSSOP)
	MCP604	Quad Op Amp
	MCP604T	Quad Op Amp (Tape and Reel for SOIC and TSSOP)
Temperature Range	I	= -40°C to +85°C
	E	= -40°C to +125°C
Package	OT	= Plastic SOT23, 5-lead **(MCP601 only)**
	CH	= Plastic SOT23, 6-lead **(MCP603 only)**
	P	= Plastic DIP (300 mil Body), 8, 14-lead
	SN	= Plastic SOIC (150 mil Body), 8-lead
	SL	= Plastic SOIC (150 mil Body), 14-lead
	ST	= Plastic TSSOP (4.4mm Body), 8, 14-lead

Examples:

a)	MCP601-I/P:	Single Op Amp, Industrial Temperature, 8LD PDIP package.
b)	MCP601-E/SN:	Single Op Amp, Extended Temperature, 8LD SOIC package.
c)	MCP601T-I/OT:	Tape and Reel, Industrial Temperature, Single Op Amp, 5-LD SOT23 package.
d)	MCP601T-E/ST:	Tape and Reel, Extended Temperature, Single Op Amp, 8LD TSSOP package
e)	MCP601RT-E/OT:	Tape and Reel, Extended Temperature, Single Op Amp, Rotated, 5-LD SOT23 package.
a)	MCP602-I/SN:	Dual Op Amp, Industrial Temperature, 8LD SOIC package.
b)	MCP602-E/P:	Dual Op Amp, Extended Temperature, 8LD PDIP package.
c)	MCP602T-E/ST:	Tape and Reel, Extended Temperature, Dual Op Amp, 8LD TSSOP package.
a)	MCP603-I/SN:	Industrial Temperature, Single Op Amp with Chip Select,8LD SOIC package.
b)	MCP603-E/P:	Extended Temperature, Single Op Amp with Chip Select, 8LD PDIP package.
c)	MCP603T-E/ST:	Tape and Reel, Extended Temperature, Single Op Amp with Chip Select, 8LD TSSOP package.
d)	MCP603T-I/SN:	Tape and Reel, Industrial Temperature, Single Op Amp with Chip Select, 8LD SOIC package.
a)	MCP604-I/P:	Industrial Temperature, Quad Op Amp, 14LD PDIP package.
b)	MCP604-E/SL:	Extended Temperature, Quad Op Amp, 14LD SOIC package.
c)	MCP604T-I/ST:	Tape and Reel, Industrial Temperature, Quad Op Amp, 14LD TSSOP package.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
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