Document Number: MC33742
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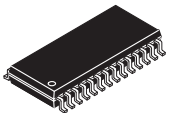
System Basis Chip with Enhanced High Speed CAN Transceiver

33742
33742S

SYSTEM BASIS CHIP



EG SUFFIX (PB-FREE)
98ASB42345B
28-PIN SOICW

EP SUFFIX
(PB-FREE)
98ASA00757D
48-PIN QFN

The 33742 and the 33742S SMARTMOS devices are SPI-controlled System Basis Chips (SBCs), combining many frequently used functions, along with a CAN 2.0-compliant transceiver, used in many automotive electronic control units (ECUs). The 33742 SBC has a fully protected fixed 5.0 V low dropout internal regulator, with current limiting, overtemperature prewarning, and reset. A second 5.0 V regulator can be implemented using external pass PNP bipolar junction pass transistor, driven by the SBC's external V2 sense input and V2 output drive pins.

The SBC has four main operating modes: Normal, Standby, Stop, and Sleep mode. Additionally, there is an internally switched high side power supply output, four wake-up inputs pins, a programmable window watchdog, interrupt, reset, and a SPI module for communication and control. The high speed CAN A and B transceiver is available for intermodule communication.

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33742PEG/R2	-40 °C to 125 °C	28 SOICW
MC33742SPEG/R2		
MC33742PEP/R2		48 QFN

Features

- 1.0 Mbps CAN transceiver bus interface with bus diagnostic capability
- SPI control at frequencies up to 4.0 MHz
- 5.0 V low dropout voltage regulator with current limiting, over-temperature prewarning, and output monitoring and reset
- A second 5.0 V regulator capability using an external series pass transistor
- Normal, Standby, Stop, and Sleep modes of operation with low Sleep and Stop mode current
- A high side switch output driver for controlling external circuitry

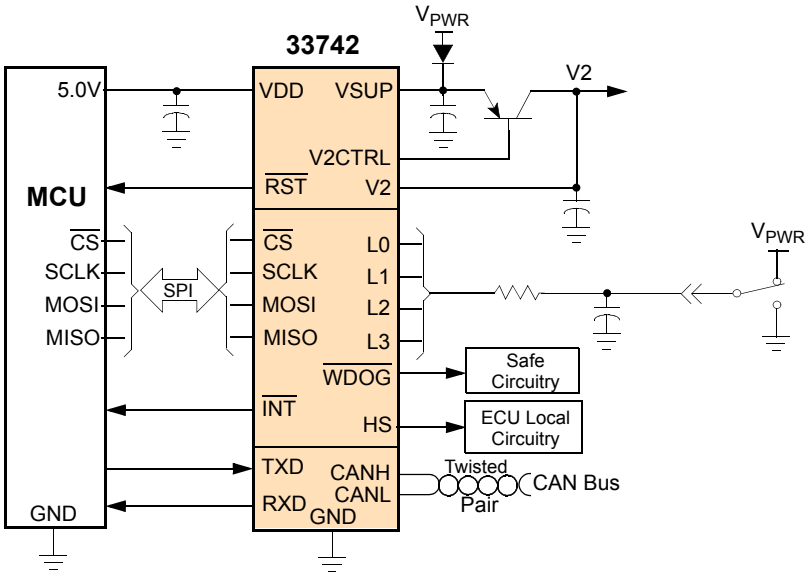


Figure 1. 33742 Simplified Application Diagram

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DEVICE VARIATIONS

Table 1. Device Differences During a Reset Condition

Part No.	Reset Duration	Device Differences	See Page
33742	15 ms (typical)	The duration the $\overline{RST}$ pin is asserted low when the Reset mode is entered after the SBC is powered up, a V_{DD} under-voltage condition is detected, and the watchdog register is not properly triggered.	page 18
33742S	3.5 ms (typical)	The duration the $\overline{RST}$ pin is asserted low when the Reset mode is entered after the SBC is powered up, a V_{DD} under-voltage condition is detected, and the watchdog register is not properly triggered.	page 18

INTERNAL BLOCK DIAGRAM

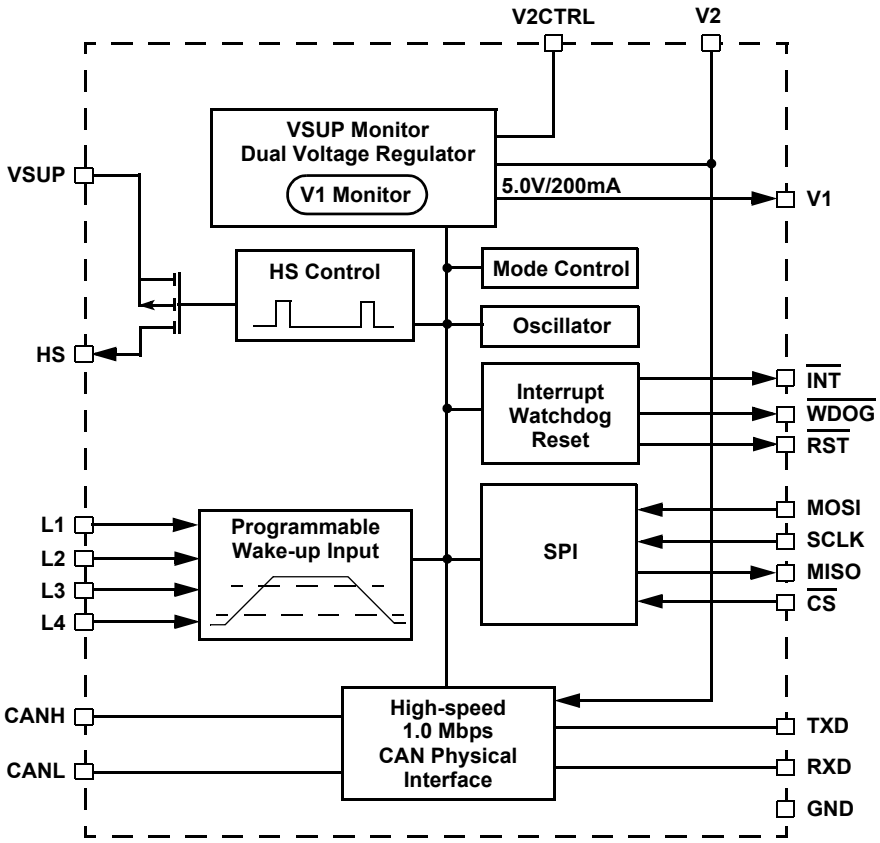


Figure 2. 33742 Simplified Internal Block Diagram

PIN CONNECTIONS

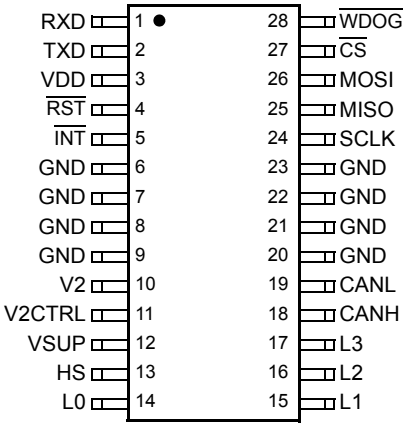


Figure 3. 33742 28-Pin Connections

Table 2. 33742 28-Pin Definitions

A functional description of each pin can be found in the Functional Pin description section beginning on page 22.

Pin	Pin Name	Formal Name	Definition
1	RXD	Receive Data	CAN bus receive data output pin.
2	TXD	Transmit Data	CAN bus transmit data input pin.
3	VDD	Voltage Digital Drain	5.0 V regulator output pin. Supply pin for the MCU.
4	$\overline{\text{RST}}$	Reset Output (Active LOW)	This is the device reset output pin whose main function is to reset the MCU. This pin has an internal -up current source to VDD.
5	$\overline{\text{INT}}$	Interrupt Output (Active LOW)	This output is asserted LOW when an enabled interrupt condition occurs. The output is a push-pull structure.
6–9 20–23	GND	Ground	These device ground pins are internally connected to the package lead frame to provide a 33742-to-PCB thermal path.
10	V2	Voltage Source 2	Sense input for the V2 regulator using an external series pass transistor. V2 is also the internal supply for the CAN transceiver.
11	V2CTRL	Voltage Source 2 Control	Output drive source for the V2 regulator connected to the external series pass transistor.
12	VSUP	Voltage Supply	Supply input pin for the 33742.
13	HS	High Side Output	Output of the internal high side switch. The output current is internally limited to 150 mA.
14–17	L0-L3	Level 0-3 Inputs	Inputs from external switches or from logic circuitry.
18	CANH	CAN High Output	CAN high output pin.
19	CANL	CAN Low Output	CAN low output pin.
24	SCLK	Serial Data Clock	Clock input pin for the Serial Peripheral Interface (SPI).
25	MISO	Master In Slave Out	SPI data sent to the MCU by the 33742. When CS is HIGH, the pin is in the high-impedance state.
26	MOSI	Master Out Slave In	SPI data received by the 33742.
27	$\overline{\text{CS}}$	Chip Select (Active LOW)	The CS input pin is used with the SPI bus to select the 33742. When the CS is asserted LOW, the 33742 is the selected device of the SPI bus.
28	$\overline{\text{WDOG}}$	Watchdog Output (Active LOW)	The WDOG output pin is asserted LOW if the software watchdog is not correctly triggered.

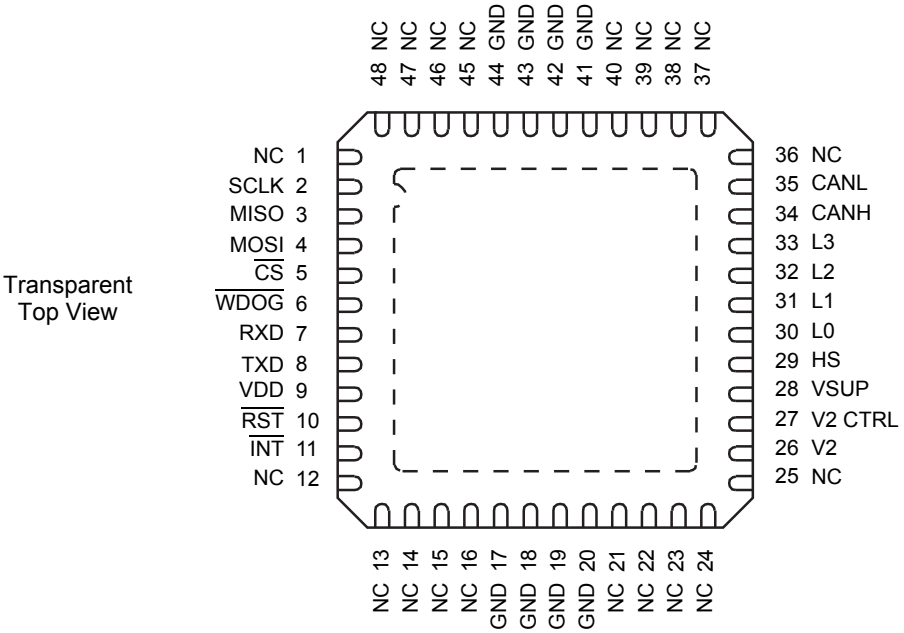


Figure 4. 33742 48-Pin Connections

Table 3. 33742 48-Pin Definitions

A functional description of each pin can be found in the Functional Pin description section beginning on page 22.

Pin	Pin Name	Formal Name	Definition
1, 12-16, 21-25, 36-40, 45-48	NC	No Connect	No connection.
2	SCLK	Serial Data Clock	Clock input pin for the Serial Peripheral Interface (SPI).
3	MISO	Master In Slave Out	SPI data sent to the MCU by the 33742. When CS is HIGH, the pin is in the high-impedance state.
4	MOSI	Master Out Slave In	SPI data received by the 33742.
5	$\overline{CS}$	Chip Select (Active LOW)	The CS input pin is used with the SPI bus to select the 33742. When the CS is asserted LOW, the 33742 is the selected device of the SPI bus.
6	$\overline{WDOG}$	Watchdog Output (Active LOW)	The WDOG output pin is asserted LOW if the software watchdog is not correctly triggered.
7	RXD	Receive Data	CAN bus receive data output pin.
8	TXD	Transmit Data	CAN bus transmit data input pin.
9	VDD	Voltage Digital Drain	5.0 V regulator output pin. Supply pin for the MCU.
10	$\overline{RST}$	Reset Output (Active LOW)	This is the device reset output pin whose main function is to reset the MCU. This pin has an internal pull-up current source to VDD.
11	$\overline{INT}$	Interrupt Output (Active LOW)	This output is asserted LOW when an enabled interrupt condition occurs. The output is a push-pull structure.
17-20 41-44	GND	Ground	These device ground pins are internally connected to the package lead frame to provide a 33742-to-PCB thermal path.

Table 3. 33742 48-Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin description section beginning on page 22.

Pin	Pin Name	Formal Name	Definition
26	V2	Voltage Source 2	Sense input for the V2 regulator using an external series pass transistor. V2 is also the internal supply for the CAN transceiver.
27	V2CTRL	Voltage Source 2 Control	Output drive source for the V2 regulator connected to the external series pass transistor.
28	VSUP	Voltage Supply	Supply input pin for the 33742.
29	HS	High Side Output	Output of the internal high side switch. The output current is internally limited to 150 mA.
30-33	L0-L3	Level 0-3 Inputs	Inputs from external switches or from logic circuitry.
34	CANH	CAN High Output	CAN high output pin.
35	CANL	CAN Low Output	CAN low output pin.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 4. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage at VSUP	V_{SUP}		V
Continuous (Steady-state)		-0.3 to 27	
Transient Voltage (Load Dump)		-0.3 to 40	
Logic Signals (RXD, TXD, MOSI, MISO, $\overline{CS}$, SCLK, $\overline{RST}$, $\overline{WDOG}$, and $\overline{INT}$)	V_{LOG}	-0.3 to V_{DD} + 0.3	V
Output Voltage at VDD	V_{DD}	0.0 to 5.3	V
Output Current at VDD	I_{DD}	Internally Limited	A
HS			
Voltage	V_{HS}	-0.3 to V_{SUP} + 0.3	V
Output Current	I_{HS}	Internally Limited	A
ESD Capability, Human Body Model[1]	V_{ESD1}		V
MC33742 in 28-pin SOIC			
HS, L0, L1, L2, L3, CANH, CANL pins		±4000	
All Other pins		±2000	
MC33742 in 48-pin QFN			
All pins		±2000	
ESD Capability, Machine Model[1]	V_{ESD2}	±200	V
Input Voltage/Current at L0, L1, L2, L3			
DC Input Voltage	V_{DCIN}	-0.3 to 40	V
DC Input Current	I_{DCIN}	±2.0	mA
Transient Input Voltage attached to external circuitry[2]	V_{TRINEC}	±100	V
CANL and CANH			
Continuous Voltage	$V_{CANH/L}$	-27 to 40	V
Continuous Current	$I_{CANH/L}$	200	mA
CANH and CANL Transient Voltage (Load Dump)[3]	$V_{LDH/L}$	40	V
CANH and CANL Transient Voltage[3]	$V_{TRH/L}$	±40	V

Notes

1. Testing done in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω), Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).
2. Testing done in accordance with ISO 7637-1. See Figure 5.
3. Load dump testing done in accordance with ISO 7637-1, Transient test done in accordance with ISO 7637-1. See Figure 6.

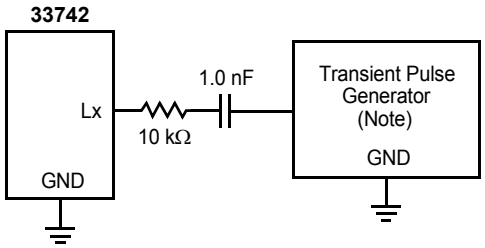
Table 4. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 165	°C
Thermal Resistance	$R_{\theta JG}$	20	°C/W
Thermal Resistance Junction Case (QFN)	R_{TJC}-$R_{\theta JC}$	TBD	°C/W
Power Dissipation[4]	P_D	1.0	W
Peak Package Reflow Temperature During Reflow[6],[7]	T_{PPRT}	Note 7	°C

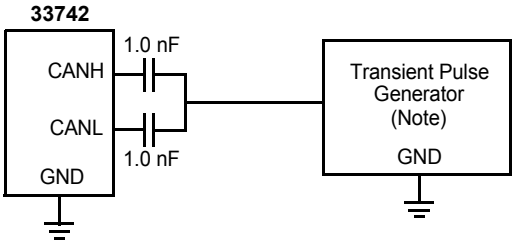
Notes

4. Maximum power dissipation is at 85 °C ambient temperature in free air and with no heatsink, according to JEDEC JESD51-2 and JESD51-3 specifications.
5. The package is not designed for immersion soldering. The maximum soldering time is 10 seconds at 240 °C on any pin. Exceeding the maximum temperature and time limits may cause permanent damage to the device.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.



Note Waveform per ISO 7637-1. Test Pulses 1, 2, 3a, and 3b.

Figure 5. Transient Test Setup for L0:L3 Inputs



Note Waveform per ISO 7637-1. Test Pulses 1, 2, 3a, and 3b.

Figure 6. Transient Test Setup for CANH/CANL

STATIC ELECTRICAL CHARACTERISTICS

Table 5. Static Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT PIN (VSUP)					
Supply Voltage	V_{SUP}				V
Nominal DC Voltage		5.5	—	18	
Extended DC Voltage: Full Functionality[8]		18	—	27	
Extended DC Voltage: Reduced Functionality[9]		4.5	—	5.5	
Load Dump		—	—	40	
Jump Start		—	—	27	
Supply Current in Standby Mode[10] (I_{OUT} at VDD = 40 mA, CAN Recessive or Sleep Mode)	$I_{SUP(STDBY)}$				mA
T_A ≥ 25 °C		—	42	45	
Supply Current in Normal Mode[10] (I_{OUT} at VDD = 40 mA, CAN Recessive or Sleep mode)	$I_{SUP(NORM)}$				mA
T_A ≥ 25 °C		—	42	45	
Supply Current in Sleep Mode[10] (VDD and V2 OFF, CAN in Sleep Mode with CAN Wake-up Disabled[11])	$I_{SUP(SLP-WD)}$				µA
V_{SUP} < 13.5 V, Oscillator Running[12]		—	85	105	
V_{SUP} < 13.5 V, Oscillator Not Running[13]		—	53	80	
V_{SUP} = 18 V, Oscillator Running[12]		—	110	140	
Supply Current in Sleep Mode[10] (V1 and V2 OFF, V_{SUP} < 13.5 V, Oscillator Not Running[13], CAN in Sleep Mode with Wake-up Enabled)	$I_{SUP(SLP-WE)}$				µA
T_A = -40 °C		—	80	—	
T_A = 25 °C		—	65	—	
T_A = 125 °C		—	55	—	
Supply Current in Stop Mode[10] (I_{OUT} at VDD < 2.0 mA, VDD ON, CAN in Sleep Mode with Wake-up Disabled[11])	$I_{SUP(STOP-WD)}$				µA
VSUP < 13.5 V, Oscillator Running[12]		—	—	160	
VSUP < 13.5 V, Oscillator Not Running[13]		—	80	160	
VSUP = 18 V, Oscillator Running[12]		—	100	210	

Notes

8. All functions and modes available and operating: Watchdog, HS turn ON/turn OFF, CAN transceiver operating, L0:L3 inputs operating, normal SPI operation. The 33742 may experience an over-temperature fault.
9. At VDD > 4.0 V, $\overline{RST}$ HIGH if reset 2 selected via SPI. The logic HIGH level will be degraded but the 33742 is functional.
10. Current measured at the VSUP pin.
11. If CAN Module is Sleep-enabled for wake-up, an additional current ($I_{CAN-SLEEP}$) must be added to specified value.
12. Oscillator running means one of the following function is active: Forced Wake-up *or* Cyclic Sense *or* Software Watchdog in Stop mode.
13. Oscillator not running means none of the following functions are active: Forced Wake-up *and* Cyclic Sense *and* Software Watchdog in Stop mode.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT PIN (VSUP) (CONTINUED)					
Supply Current in Stop Mode[14] (I_{OUT} at VDD < 2.0 mA, VDD ON, VSUP < 13.5 V, Oscillator Not Running, CAN in Sleep Mode with Wake-up Enabled)[15]	$I_{SUP(STOP-WE)}$				μA
T_A = -40 °C		—	100	—	
T_A = 25 °C		—	92	—	
T_A = 125 °C		—	80	—	
BATFAIL Flag Internal Threshold	V_{BF}	1.5	3.0	4.0	V
BATFAIL Flag Hysteresis[16]	$V_{BF(HYS)}$	—	1.0	—	V
Battery Fall Early Warning Threshold	$V_{BF(EW)}$				V
In Normal and Standby Modes		5.3	5.8	6.3	
Battery Fall Early Warning Hysteresis	$V_{BF(EW-HYST)}$				V
In Normal and Standby Modes[16]		0.1	0.2	0.3	
OUTPUT PIN (VDD)[17]					
VDD Output Voltage (2.0 mA < I_{V1} < 200 mA)	V_{DDOUT}				V
5.5 V < VSUP < 27 V		4.9	5.0	5.1	
4.5 V < VSUP < 5.5 V		4.0	—	—	
Dropout Voltage	V_{DDDRP1}				V
I_{DD} = 200 mA		—	0.2	0.5	
Dropout Voltage, Limited Output Current and Low V_{SUP}	V_{DDDRP2}				V
I_{DD} = 50 mA, 4.5 V < VSUP		—	0.1	0.25	
Output Current	I_{DD}				mA
Internally Limited		200	285	350	
Thermal Shutdown (Junction)	T_{SD}				°C
Normal or Standby Mode		160	—	200	
Over-temperature Pre-warning (Junction)	T_{PW}				°C
VDDTEMP Bit Set		125	—	160	

Notes

14. Current measured at the VSUP pin.
15. Oscillator not running means none of the following functions are active: Forced Wake-up *and* Cyclic Sense *and* Software Watchdog in Stop mode.
16. Guaranteed by design; it is not production tested.
17. I_{DD} is the total regulator output current. V1 specification with external capacitor. Stability requirement: Capacitance > 47 μF, ESR < 1.3 Ω (tantalum capacitor). In Reset, Normal Request, Normal and Standby modes. Measures with capacitance = 47 μF tantalum.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT PIN (VDD) (CONTINUED)[18]					
Temperature Threshold Difference	T_{SD} - T_{PW}	20	—	40	°C
Reset Threshold Threshold 1, Default Value after Reset, RSTTH Bit Set to Logic [0] Threshold 2, RSTTH Bit Set to Logic [1]	$V_{\overline{RSTTH}}$	 4.5 4.0	 4.6 4.2	 4.7 4.3	V
VDD for Reset Active	V_{DDR}	1.0	—	$V_{\overline{RSTTH}}$	V
Line Regulation (I_{DD} = 10 mA, Capacitance = 47 µF Tantalum at VDD) 9.0 V < V_{SUP} < 18 V 5.5 V < V_{SUP} < 27 V	V_{DDR}	 — —	 5.0 10	 25 25	mV
Load Regulation (Capacitance = 47 µF Tantalum at V1) 1.0 mA < I_{DD} < 200 mA	V_{LD}	 —	 25	 75	mV
Thermal Stability V_{SUP} = 13.5 V, I_{DD} = 100 mA[19]	$V_{THERM-S}$	 —	 30	 50	mV
OUTPUT PIN IN STOP MODE (VDD)[18]					
VDD Output Voltage I_{DD} ≤ 2.0 mA I_{DD} ≤ 10 mA	V_{DDSTOP}	 4.75 4.75	 5.0 5.0	 5.25 5.25	V
I_{DD} Output Current to Wake-up	I_{DDS-WU}	10	17	25	mA
Reset Threshold[18] Threshold 1, Default Value after Reset, RSTTH Bit Set to Logic [0] Threshold 2, RSTTH Bit Set to Logic [1]	$V_{\overline{RST}-STOP}$	 4.5 4.1	 4.6 4.2	 4.7 4.3	V
Line Regulation (Capacitance = 47 µF Tantalum at VDD) 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	$V_{LR-STOP}$	 —	 5.0	 25	mV
Load Regulation (Capacitance = 47 µF Tantalum at V1) 1.0 mA < I_{DD} < 10 mA	$V_{LD-STOP}$	 —	 15	 75	mV

Notes

18. I_{DD} is the total regulator output current. VDD specification with external capacitor. Stability requirement: capacitance > 47 µF, ESR < 1.3 Ω (tantalum capacitor). In Reset, Normal Request, Normal and Standby modes, measures with capacitance = 47 µF tantalum.Selectable by RSTTH bit in SPI Register Reset Control Register (RCR).
19. Guaranteed by characterization and design; it is not production tested.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TRACKING VOLTAGE REGULATOR (V2)[20]					
V2 Output Voltage (Capacitance = 10 µF Tantalum at V2) 2.0 mA ≤ I_{V2} ≤ 200 mA, 5.5 V < V_{SUP} < 27 V	V_2	0.99	1.0	1.01	V_{DD}
I_{V2} Output Current (for Information Only) Depending on External Ballast Transistor	I_{V2}	200	—	—	mA
V2 Control Drive Current Capability[21] Worst Case at T_J = 125 °C	I_{V2CTRL}	0.0	—	10	mA
V2LOW Flag Threshold	V_{2LTH}	3.75	4.0	4.25	V
LOGIC OUTPUT PIN (MISO)[22]					
Low-level Output Voltage I_{OUT} = 1.5 mA	V_{OL}	0.0	—	1.0	V
High-level Output Voltage I_{OUT} = -250 µA	V_{OH}	V_{DD}-0.9	—	V_{DD}	V
Tri-stated MISO Leakage Current 0 V < V_{MISO} < V_{DD}	I_{HZ}	-2.0	—	2.0	µA
LOGIC INPUT PINS (MOSI, SCLK, **$\overline{CS}$**)					
High-level Input Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD} + 0.3	V
Low-level Input Voltage	V_{IL}	-0.3	—	0.3 V_{DD}	V
High-level Input Current on $\overline{CS}$ V_{IN} = 4.0 V	I_{IH}	-100	—	-20	µA
Low-level Input Current on $\overline{CS}$ V_{IN} = 1.0 V	I_{IL}	-100	—	-20	µA
MOSI and SCLK Input Current 0 V < V_{IN} < V_{DD}	I_{IN}	-10	—	10	µA
OUTPUT PIN (RST)[23]					
High-level Output Current 0 V < V_{OUT} < 0.7 V_{DD}	I_{OH}	-300	-250	-150	µA
Low-level Output Voltage I_O = 1.5 mA, 5.5 V < V_{SUP} < 27 V I_O = 0 mA, 1.0 V <V_{SUP} < 5.5 V	V_{OL}	0.0 0.0	— —	0.9 0.9	V
$\overline{RST}$ Pull-down Current V > 0.9 V	I_{PDW}	2.3	—	5.0	mA

Notes
20. V2 specification with external capacitor. Stability requirement: capacitance > 42 µF and ESR < 1.3 Ω (tantalum capacitor), external resistor between base and emitter required. Measurement conditions: ballast transistor MJD32C, capacitance > 10 µF tantalum, 2.2 kΩ resistor between base and emitter of ballast transistor.
21. The guaranteed V2CTRL current capability is 10 mA. No active current limiting is used so the actual available current may be higher.
22. Push-pull structure with tri-state condition ($\overline{CS}$ HIGH).
23. Output pin only. Supply from VDD. Structure switch to ground with pull-up current source.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT PIN ($\overline{\text{WDOG}}$)[24]					
Low-level Output Voltage I_O = 1.5 mA, 1.0 V < V_{SUP} < 27 V	V_{OL}	0.0	—	0.9	V
High-level Output Voltage I_O = -250 µA	V_{OH}	V_{DD}-0.9	—	V_{DD}	V
OUTPUT PIN ($\overline{\text{INT}}$)[24]					
Low-level Output Voltage I_O = 1.5 mA	V_{OL}	0.0	—	0.9	V
High-level Output Voltage I_O = -250 µA	V_{OH}	V_{DD}-0.9	—	V_{DD}	V
OUTPUT PIN (HS)					
Driver Output ON Resistance T_A = 25 °C, I_{OUT} - 150 mA, V_{SUP} > 9.0 V T_A = 125 °C, I_{OUT} - 150 mA, V_{SUP} > 9.0 V T_A = 125 °C, I_{OUT} - 120 mA, 5.5 V < V_{SUP} < 9.0 V	$R_{DS(ON)}$	— — —	2.0 — 3.5	2.5 4.5 5.5	Ω
Output Current Limitation V_{SUP} - V_{HS} > 1.0 V	I_{LIM}	160	—	500	mA
HS Thermal Shutdown	T_{SD}	155	—	190	°C
HS Leakage Current	I_{LEAK}	—	—	10	µA
Output Clamp Voltage I_{OUT} = -10 mA, No Inductive Load Drive Capability	V_{CL}	-1.5	—	-0.3	V
INPUT PINS (L0, L1, L2, AND L3)					
Low-voltage Detection Threshold 5.5 V < V_{SUP} < 6.0 V 6.0 V < V_{SUP} < 18 V 18 V < V_{SUP} < 27 V	V_{THL}	2.0 2.5 2.7	2.5 3.0 3.2	3.0 3.6 3.7	V
High-voltage Detection Threshold 5.5 V < V_{SUP} < 6.0 V 6.0 V < V_{SUP} < 18 V 18 V < V_{SUP} < 27 V	V_{THH}	2.7 3.0 3.5	3.3 4.0 4.2	3.8 4.6 4.7	V
Hysteresis 5.5 V < V_{SUP} < 27 V	V_{HYS}	0.6	—	1.3	V
Input Current -0.2 V < V_{IN} < 40 V	I_{IN}	-10	—	10	µA

Notes
24. Push-pull structure.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CAN TRANSCEIVER CURRENT					
Supply Current of CAN Module					
CAN in Normal mode, Bus Recessive State	I_{RES}	—	1.3	3.0	mA
CAN in Normal mode, Bus Dominant State without Bus Load	I_{DOM}	—	1.5	3.5	mA
CAN in Sleep State, Wake-up Enabled, V2 Regulator OFF	$I_{CAN-SLEEP}$	—	12	24	µA
CAN in Sleep State, Wake-up Disabled, V2 Regulator OFF[25]	I_{DIS}	—	—	1.0	µA
PINS (CANH AND CANL)					
Bus Pin Common Mode Voltage	V_{CM}	-27	—	40	V
Differential Input Voltage (Common Mode Between -3.0 V and 7.0 V)	V_{CANH} - V_{CANL}				mV
Recessive State at RXD		—	—	500	
Dominant State at RXD		900	—	—	
Differential Input Hysteresis (RXD)	V_{HYS}	100	—	—	mV
Input Resistance	R_{IN}				kΩ
28-pin SOIC		5.0	—	100	
48-pin QFN		5.0	—	50	
Differential Input Resistance	R_{IND}	10	—	100	kΩ
CANH Output Voltage	V_{CANH}				V
TXD Dominant State		2.75	—	4.5	
TXD Recessive State		—	—	3.0	
CANL Output Voltage	V_{CANL}				V
TXD Dominant State		0.5	—	2.25	
TXD Recessive State		2.0	—	—	
Differential Output Voltage	Vo_H-Vo_L				
TXD Dominant State		1.5	—	3.0	V
TXD Recessive State		—	—	100	mV
Output Current Capability (Dominant State)					mA
CANH	I_{CANH}	—	—	-35	
CANL	I_{CANL}	35	—	—	
Over-temperature Shutdown	T_{SD}	160	180	—	°C
CANL Over-current Detection[26]					mA
CANL	$I_{CANL/OC}$	60	—	200	
CANH	$I_{CANH/OC}$	-200	—	-60	
CANH and CANL Input Current, Device Supplied (CAN Sleep mode with CAN Wake-up Enabled or Disabled)	I_{CAN1}				µA
V_{CANH}, V_{CANL} from 0 V to 5.0 V		—	3.0	10	
V_{CANH}, V_{CANL} = -2.0 V		-60	-50	—	
V_{CANH}, V_{CANL} = 7.0 V		—	60	75	

Notes
25. Guaranteed by design; it is not production tested.
26. Reported in CAN register. For a description of the contents of the CAN register, refer to CAN Register (CAN) on page 49

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PINS (CANH AND CANL) (CONTINUED)					
CANH and CANL Input Current, Device Unsupplied	I_{CAN2}				µA
V_{CANH}, V_{CANL} = 2.5 V		—	40	100	
V_{CANH}, V_{CANL} = -2.0 V		-60	-50	—	
V_{CANH}, V_{CANL} = 7.0 V		—	190	240	
DIAGNOSTIC INFORMATION (CANH AND CANL)					
CANL to GND Threshold	V_{LG}	—	1.75	—	V
CANH to GND Threshold	V_{HG}	—	1.75	—	V
CANL to VSUP Threshold	V_{LVB}	—	V_{SUP}-2.0	—	V
CANH to VSUP Threshold	V_{HVB}	—	V_{SUP}-2.0	—	V
CANL to VDD Threshold	V_{L5}	—	V_{DD}-0.43	—	V
CANH to VDD Threshold	V_{H5}	—	V_{DD}-0.43	—	V
RXD Weak Pull-down Current Source[27]	I_{RXDW}				µA
RXD Permanent Dominant Failure Condition		—	100	—	
PINS (TXD AND RXD)					
TXD Input High-voltage	V_{IH}	0.7 V_{DD}	—	V_{DD} + 0.4	V
TXD Input Low-voltage	V_{IL}	-0.4	—	0.3 V_{DD}	V
TXD High-level Input Current	I_{IH}				µA
V_{TXD} = V_2		-10	—	10	
TXD Low-level Input Current	I_{IL}				µA
V_{TXD} = 0 V		-150	-100	-50	
RXD Output High Voltage[28]	V_{OH}				V
I_{RXD} = 250 µA		V_{DD} - 1.0	—	—	
RXD Output Low-voltage	V_{OL}				V
I_{RXD} = 1.0 mA		—	—	0.5	

Notes
27. Guaranteed by design; it is not production tested.
28. RXD is a push-pull structure between the V2 pin and GND.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE TIMING (SCLK, $\overline{CS}$, MOSI, MISO)[29]					
SPI Operation Frequency	f_{REQ}	0.25	—	4.0	MHz
SCLK Clock Period	t_{PCLK}	250	—	N/A	ns
SCLK Clock High Time	t_{WSCLKH}	125	—	N/A	ns
SCLK Clock Low Time	t_{WSCLKL}	125	—	N/A	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}	100	—	N/A	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$	t_{LAG}	100	—	N/A	ns
MOSI to Falling Edge of SCLK	t_{SISU}	40	—	N/A	ns
Falling Edge of SCLK to MOSI	t_{SIH}	40	—	N/A	ns
MISO Rise Time[30] C_L = 220 pF	t_{RSO}	—	25	50	ns
MISO Fall Time[30] C_L = 220 pF	t_{FSO}	—	25	50	ns
Time from Falling or Rising Edges of $\overline{CS}$ MISO Low-impedance MISO High-impedance	 t_{SOEN} t_{SODIS}	 — —	 — —	 50 50	ns
Time from Rising Edge of SCLK to MISO Data Valid 0.2 V_{DD} ≤ MISO ≥ 0.8 V_{DD}, C_L = 200 pF	t_{VALID}	—	—	50	ns
STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WDOG}$, $\overline{INT}$)					
Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop mode Activation[31]	$t_{\overline{CS}\text{-STOP}}$	18	—	34	µs
Interrupt Low-level Duration Stop Mode	$t_{\overline{INT}}$	7.0	10	13	µs
Internal Oscillator Frequency[32]	f_{OSC}	—	100	—	kHz

Notes
29. See Figure 7, SPI Timing Diagram, page 20.
30. Not production tested. Guaranteed by design.
31. Not production tested. Guaranteed by design. Detected by V2 OFF.
32. f_{OSC} is indirectly measured (1.0 ms reset) and trimmed.

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WDOG}$, $\overline{INT}$) (CONTINUED)					
Watchdog Period Normal and Standby Modes	$t_{\overline{WDOG}}$				ms
28-pin SOIC					
Period 1		8.58	9.75	10.92	
Period 2		39.6	45	50.4	
Period 3		88	100	112	
Period 4		308	350	392	
48-pin QFN					
Period 1		8.3	9.75	10.92	
Period 2		38.5	45	50.4	
Period 3		86	100	112	
Period 4		300	350	392	
Normal Request Mode Timeout	t_{NRTOUT}				ms
28-pin SOIC		308	350	392	
48-pin QFN		300	350	392	
Watchdog Period Stop Mode	$t_{WD-STOP}$				ms
Period 1		6.82	9.75	12.7	
Period 2		31.5	45	58.5	
Period 3		70	100	130	
Period 4		245	350	455	
Watchdog Period Accuracy	t_{ACC}				%
Normal and Standby Modes		-12	—	12	
Stop Mode		-30	—	30	
Cyclic Sense/FWU Timing Sleep and Stop Modes	t_{CSFWU}				ms
Timing 1		3.22	4.6	5.98	
Timing 2		6.47	9.25	12	
Timing 3		12.9	18.5	24	
Timing 4		25.9	37	48.1	
Timing 5		51.8	74	96.2	
Timing 6		66.8	95.5	124	
Timing 7		134	191	248	
Timing 8		271	388	504	
Cyclic Sense ON Time	t_{ON}				µs
Sleep and Stop modes.		200	350	500	
Cyclic Sense/FWU Timing Accuracy	t_{ACC}				%
Sleep and Stop modes		-30	—	30	

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WDOG}$, $\overline{INT}$) (CONTINUED)					
Delay Between SPI Command and HS Turn ON[33] Normal or Standby mode, V_{SUP} > 9.0 V	t_{S-HSON}	—	—	22	µs
Delay Between SPI Command and HS Turn OFF[33] Normal or Standby mode, V_{SUP} > 9.0 V	$t_{S-HSOFF}$	—	—	22	µs
Delay Between SPI and V2 Turn ON[33] Standby mode	t_{S-V2ON}	9.0	—	22	µs
Delay Between SPI and V2 Turn OFF[33] Normal mode	$t_{S-V2OFF}$	9.0	—	22	µs
Delay Between Normal Request and Normal mode After Watchdog Trigger Command[33] Normal Request mode	t_{S-NR2N}	15	35	70	µs
STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WDOG}$, $\overline{INT}$) (CONTINUED)					
Delay Between SPI and CAN Normal mode[34] Normal mode[35]	t_{S-CAN_N}	—	—	10	µs
Delay Between SPI and CAN Sleep Mode[34] Normal mode [35]	t_{S-CAN_S}	—	—	10	µs
Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ LOW to HIGH) and Device in Normal Request mode (VDD ON and $\overline{RST}$ HIGH) Stop mode	$t_{W-\overline{CS}}$	15	40	90	µs
Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ LOW to HIGH) and First Accepted SPI Command Device in Stop mode After Wake-up	t_{W-SPI}	90	—	N/A	µs
Delay Between $\overline{INT}$ Pulse and First SPI Command Accepted Device in Stop mode After Wake-up	$t_{S-1STSPI}$	20	—	N/A	µs
Delay Between Two SPI Messages Addressing the Same Register	t_{2SPI}	25	—	—	µs
OUTPUT PIN (VDD)					
Reset Delay Time Measured at 50% of Reset Signal	t_D	4.0	—	30	µs
I_{DD} Over-current to Wake-up Deglitcher Time[35]	$t_{IDD-DGLT}$	40	55	75	µs

Notes
33. Delay starts at falling edge of clock cycle #8 of the SPI command and start of “Turn ON” or “Turn OFF” of HS or V2.
34. Delay starts at falling edge of clock cycle #8 of the SPI command and start of “Turn ON” or “Turn OFF” of HS or V2.
35. Guaranteed by design; it is not production tested.

Table 6. Dynamic Electrical Characteristics (continued)

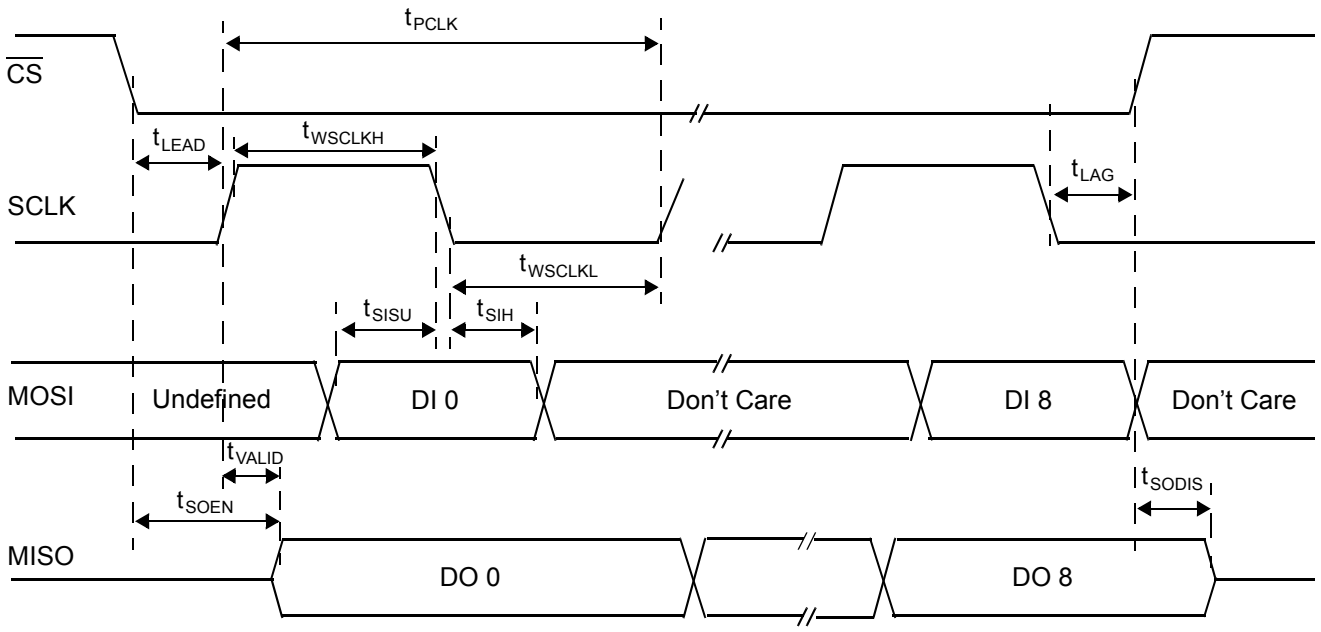
Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40 °C ≤ T_A ≤ 125 °C. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT PIN ($\overline{RST}$)					
Reset Duration After VDD HIGH					ms
33742	$t_{\overline{RST}DUR}$	12	15	18	
33742S	$t_{\overline{RST}DURS}$	3.0	3.5	4.0	
INPUT PINS (L0, L1, L2, AND L3)					
Wake-up Filter Time	t_{WUF}	8.0	20	38	µs
CAN MODULE–SIGNAL EDGE RISE AND FALL TIMES (CANH, CANL)					
Dominant State Timeout	t_{DOUT}	200	360	520	µs
Propagation Loop Delay TXD to RXD (Recessive to Dominant)(36)	t_{LRD}				ns
Slew Rate 3		60	100	210	
Slew Rate 2		70	110	225	
Slew Rate 1		80	130	255	
Slew Rate 0		110	200	310	
Propagation Delay TXD to CAN (Recessive to Dominant)(37)	t_{TRD}				ns
Slew Rate 3		20	65	110	
Slew Rate 2		25	80	150	
Slew Rate 1		35	100	200	
Slew Rate 0		50	160	300	
Propagation Delay CAN to RXD (Recessive to Dominant)(38)	t_{RRD}	10	50	140	ns
Propagation Loop Delay TXD to RXD (Dominant to Recessive)(36)	t_{LDR}				ns
Slew Rate 3		100	150	200	
Slew Rate 2		120	165	220	
Slew Rate 1		140	200	250	
Slew Rate 0		250	340	410	
Propagation Delay TXD to CAN (Dominant to Recessive)(37)	t_{TDR}				ns
Slew Rate 3		60	125	150	
Slew Rate 2		65	150	190	
Slew Rate 1		75	180	250	
Slew Rate 0		200	310	460	
Propagation Delay CAN to RXD (Dominant to Recessive)(38)	t_{RDR}	20	30	60	ns
Non-Differential Slew Rate (CANL or CANH)					V/µs
Slew Rate 3	t_{SL3}	4.0	19	40	
Slew Rate 2	t_{SL2}	3.0	13.5	20	
Slew Rate 1	t_{SL1}	2.0	8.0	15	
Slew Rate 0	t_{SL0}	1.0	5.0	10	
Bus Communication Rate	t_{BUS}	60k	—	1.0M	bps

Notes

36. See Figure 8, page 20.
37. See Figure 9, page 20.
38. See Figure 10, page 21.

TIMING DIAGRAMS



Note Incoming data at MOSI pin is sampled by the 33742 at SCLK falling edge. Outgoing data at MISO pin is set by the 33742 at SCLK rising edge (after t_{VALID} delay time).

Figure 7. SPI Timing Diagram

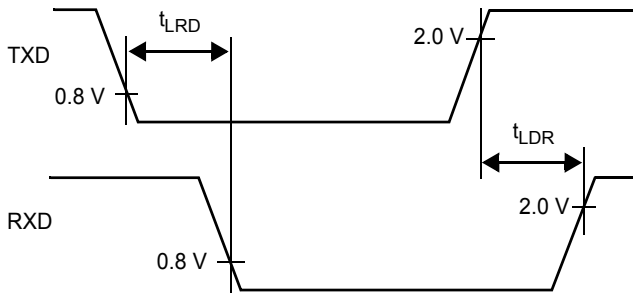
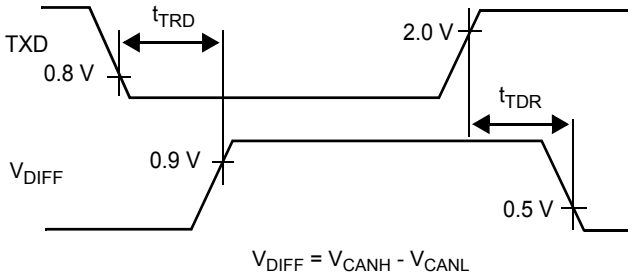


Figure 8. Propagation Loop Delay TXD to RXD



$V_{DIFF} = V_{CANH} - V_{CANL}$

Figure 9. Propagation Delay TXD to CAN

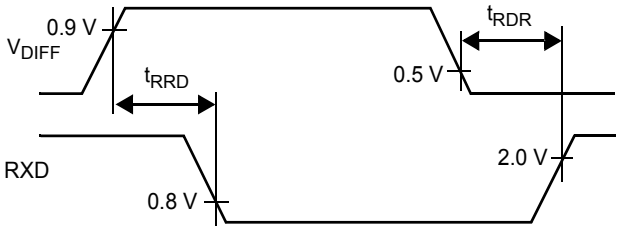


Figure 10. Propagation Delay CAN to RXD

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33742 and the 33742S are system basis chips (SBCs) dedicated to automotive applications. Their functions include the following:

- One fully protected 5.0 V voltage regulator with 200 mA total output current capability available at the VDD pin.
- VDD regulator under-voltage reset function, programmable window or time-out software watchdog function.
- Internal driver (V2) for an external series pass transistor to implement a second 5.0 V voltage regulator.
- Two running modes: Normal and Standby modes set by the system microcontroller.
- Sleep and Stop modes low power operating modes to reduce an application's current consumption while providing a wake-up capability from the CAN interface, L3:L0 wake-up inputs, or from a timer wake-up.
- Programmable wake-up input and cyclic sense wake-ups.
- CAN high-speed physical bus interface with TXD and RXD fault diagnostic capability and enhanced protection features.
- An SPI interface for use in communicating with a MCU and Interrupt outputs to report SBC status, perform diagnostics, and report wake-up events.

FUNCTIONAL PIN DESCRIPTION

RECEIVE AND TRANSMIT DATA (RXD AND TXD)

The RXD and TXD pins (receive data and transmit data pins, respectively) are connected to a microcontroller's CAN protocol handler. TXD is an input and controls the CANH and CANL line state (dominant when TXD is LOW, recessive when TXD is HIGH). RXD is an output and reports the bus state (RXD LOW when CAN bus is dominant, HIGH when CAN bus is recessive). The RXD terminal is a push-pull structure between the V2 pin and GND.

Voltage Digital Drain (VDD)

The VDD pin is the output pin of the 5.0 V internal regulator. It can deliver up to 200 mA. This output is protected against over-current and over-temperature. It includes an over-temperature pre-warning flag, which is set when the internal regulator temperature exceeds 130 °C typical. When the temperature exceeds the over-temperature shutdown (170 °C typical), the regulator is turned off.

VDD includes an under-voltage reset circuitry, which sets the $\overline{\text{RST}}$ pin LOW when VDD is below the under-voltage reset threshold.

RESET OUTPUT ($\overline{\text{RST}}$)

The RESET pin $\overline{\text{RST}}$, is an output that is set LOW when the device is in reset mode. The $\overline{\text{RST}}$ pin is set HIGH when the device is not in reset mode. $\overline{\text{RST}}$ includes an internal pull-up current source. When $\overline{\text{RST}}$ is LOW, the sink current capability is limited, allowing $\overline{\text{RST}}$ to be shorted to 5.0 V for software debug or software download purposes.

INTERRUPT OUTPUT ($\overline{\text{INT}}$)

The Interrupt pin $\overline{\text{INT}}$, is an output that is set LOW when an interrupt occurs. $\overline{\text{INT}}$ is enabled using the Interrupt Register (INTR). When an interrupt occurs, $\overline{\text{INT}}$ stays LOW until the interrupt source is cleared.

$\overline{\text{INT}}$ output also reports a wake-up event by a 10 μs typical pulse when the device is in Stop mode.

VOLTAGE SOURCE 2 (V2)

The V2 pin is the input sense for the V2 regulator. It is connected to the external series pass transistor. V2 is also the 5.0 V supply of the internal CAN interface. It is possible to connect V2 to an external 5.0 V regulator or to the VDD output when no external series pass transistor is used. In this case, the V2CTRL pin must be left open. Refer to Figure 31, SBC Typical Application Schematic, page 57.

VOLTAGE SOURCE 2 CONTROL (V2CTRL)

The V2CTRL pin is the output drive pin for the V2 regulator connected to the external series pass transistor.

VOLTAGE SUPPLY (VSUP)

The VSUP pin is the battery supply input of the device.

HIGH SIDE OUTPUT (HS)

The HS pin is the internal high side driver output. It is internally protected against over-current and over-temperature.

LEVEL 0-3 INPUTS (L0: L3)

The L0:L3 pins can be connected to contact switches or the output of other ICs for external inputs. The input states can be read by SPI. These inputs can be used as wake-up events for the SBC when operating in the Sleep or Stop mode.

CAN HIGH AND CAN LOW OUTPUTS (CANH AND CANL)

The CAN High and CAN Low pins are the interfaces to the CAN bus lines. They are controlled by TXD input level, and the state of CANH and CANL is reported through RXD output. A 60Ω termination resistor is connected between CANH and CANL pins.

SERIAL DATA CLOCK (SCLK)

SCLK is the Serial Data Clock input pin of the serial peripheral interface.

MASTER IN SLAVE OUT (MISO)

MISO is the Master In Slave Out pin of the serial peripheral interface. Data is sent from the SBC to the microcontroller through the MISO pin.

MASTER OUT SLAVE IN (MOSI)

MOSI is the Master Out Slave In pin of the serial peripheral interface. Control data from a microcontroller is received through this pin.

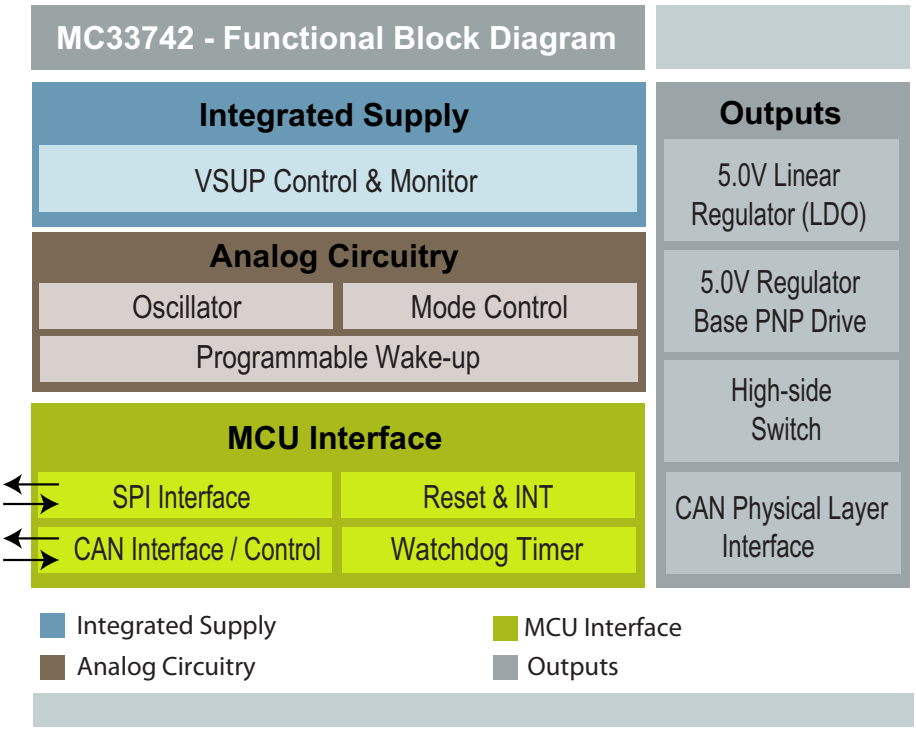
CHIP SELECT ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ is the Chip Select pin of the serial peripheral interface. When this pin is LOW, the SPI port of the device is selected.

WATCHDOG OUTPUT ($\overline{\text{WDOG}}$)

The Watchdog output pin is asserted LOW to flag that the software watchdog has not been properly triggered.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



OUTPUTS

5.0 V LINEAR REGULATOR (LDO)

This low dropout linear regulator (V1) outputs a regulated 5.0 V at 200 mA. The associated monitoring circuit provides detection of under-voltage, over-current, and short-circuit conditions, as well as over-temperature and a reset function.

5.0 V REGULATOR BASE PNP DRIVE

The V2 linear regulator control circuitry provides drive for an external series pass transistor (PNP type). The 5.0 V output tracks the V1 regulator

HIGH SIDE SWITCH

The high switch provides a 2.0 ohm (typ.) RDS_{ON} MOSFET driver connected to the VSUP pin. The output is protected against short-circuit conditions and provides over-temperature shutdown.

CAN PHYSICAL LAYER INTERFACE

This circuitry provides communication between the TXD & RXD pins, from/to the MCU, and the CANL & CANH pins of the CAN physical interface. The various modes of the CAN interface are controlled through the SPI control registers.

INTEGRATED SUPPLY

VSUP CONTROL & MONITOR

This circuitry protects the IC from transient conditions such as vehicle jump-start (27 V) and load dump (40 V). If the V_{SUP} voltage falls below 3.0 V (or a 6.0 V warning interrupt), an under-voltage detection is reported.

ANALOG CIRCUITRY

OSCILLATOR

This circuit is used to generate the internal timings for reset, watchdog, cyclic wake-up, filtering time, etc.

MODE CONTROL

The 4 operating modes of the IC are controlled through the SPI control registers. There are also several special modes possible.

PROGRAMMABLE WAKE-UP

The 4 inputs are used in conjunction with various SPI control register bits to determine the wake-up conditions and the reaction of the IC. They can be connected to contact switches or other ICs.

MCU INTERFACE

SPI INTERFACE

The IC and the MCU communicate using the SPI control and status reporting registers. The clock speed (SCLK) can be as high as 4.0 MHz.

RESET & INT

These 2 outputs notify the MCU when the IC is in reset mode, or when an enabled interrupt condition has occurred.

WATCHDOG TIMER

The timer can be used as a watchdog window or watchdog timeout function. The SPI control register provide the choice as well as the timeout value. When the watchdog timer is not properly serviced by the MCU, an error signal (WDOGN low) and a reset signal (RSTN low) are output.

CAN INTERFACE/CONTROL

The operation of the CAN interface is controlled by the MCU through the use of SPI control register bits.

FUNCTIONAL DEVICE OPERATION

SUPPLY VOLTAGE AT VSUP

The 33742 receives its operating voltage via the VSUP pin. An external diode is needed in series with the VSUP pin and the supply voltage to protect the SBC against negative transients or from a reverse battery situation that can occur in a vehicle application. The 33742 will operate from a supply voltage input as low as 4.5 VDC to as high as 27 VDC. The later voltage is often encountered during a vehicle jump-start.

The VSUP pin can tolerate automotive transient conditions such as load dump to 40 V. The SBC is able to detect when V_{SUP} falls below 3.0 V typical. This under-voltage state is detected and retained in the parts Mode Control Register (MCR) as the BATFAIL bit. This detection capability is available across all operating modes.

Note For a detailed description of all the registers mentioned in this section, refer to the section titled SPI Interface And Register Description beginning on page 46.

The SBC incorporates a V_{SUP} level early warning function, which provides a maskable interrupt if the VSUP voltage level falls below 6.0 V typical. Hysteresis is used to reduce false detections. The early warning function works only in Normal and Standby operation modes. An under-voltage at the VSUP pin is reported in the Input/Output Register (IOR).

VDD REGULATOR

The VDD regulator provides a 5.0 V low dropout voltage capable of supplying up to 200 mA with monitoring circuitry for under-voltage detection and a reset function. The VDD regulator is protected against over-current and short-circuit conditions. It has over-temperature detection and will set warning flags (bit VDDTEMP in the MCR and INTR registers) and has over-temperature shutdown with hysteresis.

V2 REGULATOR

The V2 regulator feature provides for a second 5.0 VDC voltage source The internal V2 circuitry will drive an external series pass transistor, substantially increasing the available supply current. Two pins, the V2 and the V2CTRL, are used to sense and drive the series pass transistor. The output voltage is 5.0 V and tracks the VDD regulator. The MJD32C transistor is recommended for use as the external pass device. Other PNP transistors can be used but depending on the device's gain, an external resistor-capacitor network might be needed. V2 is also the supply voltage for the on-board CAN module. An under-voltage condition for the V2 voltage is reported in the IOR Register (bit V2LOW set to logic [1] if V2 falls below 4.0 V typical).

HS VSUP SWITCH OUTPUT

The HS output is a 2.0 Ω typical switch tied to the VSUP pin. It can power or bias external switches and their associated pull-up or put-downs or other circuitry. An example is biasing a set of switches connected to the L0:L3 wake-up input pins. The HS VSUP output current is limited to 200 mA and is protected against short-circuits conditions and will report an over-temperature shutdown condition (bit HSOT in the IOR register and bit HSOT-V2LOW in the INTR register).

The HS output "on" state is set by the HSON bit in the IOR register. A cyclic mode of operation can be implemented using an internal timer in the Sleep and Stop operating modes. It can also be turned on in Normal or Standby modes to drive loads or supply peripheral components. No internal protection circuitry is provided, however. Dedicated chip protection circuitry is required for inductive load applications. The HS output pin should not go below -0.3 V.

BATTERY FAIL EARLY WARNING

Refer to the previous discussion under the heading, Supply Voltage at VSUP.

INTERNAL CLOCK

The 33742 has an internal clock used to generate all timings (reset, watchdog, cyclic wake-up, filtering time, etc.). There are two on-board oscillators: a higher accuracy (±12 percent) oscillator used in Normal Request, Normal, and Standby modes, and a lower accuracy (±30 percent) oscillator used during Sleep and Stop modes.

OPERATIONAL MODES

INTRODUCTION

The 33742 has four modes of operation, all controllable via the SPI. The modes are Standby, Normal, Stop, and Sleep. An additional temporary mode called Normal Request mode is automatically accessed by the device after reset or wake-up from Stop mode. A Reset mode is also implemented. Special modes and configurations are possible for debug and program microcontroller flash memory.

Table , page 28, offers a summary of the functional modes.

STANDBY MODE

In Standby mode only the VDD regulator is ON. The V2 regulator is turned OFF by disabling the V2CTRL pin. Other functions available are the L0:L3 inputs read through via the SPI and HS output activation.

The CAN interface is not able to send messages. If a CAN message is received, the CANWU bit is set. The watchdog timer is running.

NORMAL MODE

In Normal mode, both the VDD and V2 regulators are in the ON state. All functions are available in this operating mode (watchdog, wake-up input reading through SPI, HS activation, and CAN communication). The watchdog timer is running and must be periodically cleared through SPI.

STOP MODE

The V2 regulator is turned OFF by disabling the V2CTRL pin. The VDD regulator is activated in a special low power mode supplying only a few mA of current. This maintains “keep alive” power for the application’s MCU while the MCU is in a power-saving state (i.e., a MCU’s version of Stop or Wait). In the Stop mode, the supply current available from VSUP pin is very low.

Both parts (the SBC or the MCU) can be awakened from either the 33742 side (for example, cyclic sense, forced wake-up, CAN message, wake-up inputs, and over-current on VDD) or from the MCU side (key wake-up, etc.).

Stop mode is always selected via SPI. In Stop mode, the watchdog software may be either running or not running depending upon selection by SPI (Reset Control Register [RCR], bit WDSTOP). To clear a running watchdog timer, the SBC must be awakened using the $\overline{CS}$ pin (SPI wake-up). In Stop mode, wake-up is identical to that in Sleep mode, with the addition of $\overline{CS}$ and VDD over-current wake-up. Refer to Table , page 28.

SLEEP MODE

In Sleep mode, the VDD and V2 regulators are OFF. Current consumption from the VSUP pin is cut. In Sleep mode, the SBC can be awakened by sensing individual level individual level changes in the L0:L3 inputs, by cyclic checking of the L0:L3 inputs, by the forced wake-up timer, or from the CAN physical interface upon receiving a CAN message. When a wake-up occurs, the SBC goes first into the Reset mode before entering Normal Request mode.

RESET MODE

In the Reset mode, the $\overline{RST}$ pin is LOW and a timer runs for $t_{\overline{RST}DUR}$ time. After $t_{\overline{RST}DUR}$ has elapsed, the 33742 enters the Normal Request operating mode. The Reset mode is entered if a reset condition occurs (VDD LOW, watchdog time-out, or watchdog trigger in a closed window).

NORMAL REQUEST MODE

The Normal Request mode is a temporary operating mode automatically entered by the SBC after the Reset mode or after the 33742 wakes up from the Stop mode.

After a wake-up from the Sleep mode or after a device power-up, the SBC enters the Reset mode prior to entering the Normal Request mode. After a wake-up from the Stop mode, the 33742 enters the Normal Request mode directly.

In Normal Request mode, the VDD regulator is ON, the V2 regulator is OFF, and the $\overline{RST}$ pin is HIGH. As soon as the SBC enters the Normal Request mode, an internal 350ms timer is started (parameter t_{NRTOUT}). During this time, the application’s MCU must address the 33742 via SPI and configure the TIM1 sub register to select the watchdog period. This is required of the SBC to stop the 350 ms watchdog timer and enter the Normal or Standby mode and to set the watchdog timer configuration.

NORMAL REQUEST ENTERED AND NO WATCHDOG CONFIGURATION OCCURS

If the Normal Request mode is entered after the SBC powers up or after a wake-up from Stop mode and no watchdog configuration occurs before the 350 ms time period has expired, the device enters the Reset mode. If no watchdog configuration is performed, the 33742 will cycle from the Normal Request mode to Reset mode to Normal Request mode.

If the Normal Request mode is entered after a wake-up from Sleep mode, and no watchdog configuration occurs while the 33742S is in Normal Request mode, the SBC returns to the Sleep mode.

Table 7. Table of Operations

Mode	Voltage Regulator HS Switch	Wake-up Capabilities (if Enabled)	$\overline{\text{RST}}$ Pin	$\overline{\text{INT}}$ Pin	Watchdog Software	CAN Cell
Normal Request	VDD: ON, V2: OFF, HS: OFF	–	Low for $t_{\overline{\text{RST}}DUR}$ time, then HIGH	–	–	–
Normal	VDD: ON, V2: ON, HS: Controllable	–	Normally HIGH. Active LOW if $\overline{\text{WDOG}}$ or V_{DD} under-voltage occurs	If enabled, signal failure (VDD Pre-warning Temp, CAN, HS)	Running	TXD/RXD
Standby	VDD: ON, V2: OFF, HS: Controllable	–	Same as Normal mode	Same as Normal mode	Running	Low power
Stop	VDD: ON (Limited Current Capability), V2: OFF, HS:OFF or Cyclic Sense	CAN, SPI, L0:L3, Cyclic Sense, Forced Wake-up, I_{DD} Over-current(40)	Normally HIGH. Active LOW if $\overline{\text{WDOG}}$(41) or VDD under-voltage occurs	Signal 33742S wake-up and $I_{DD} > I_{DDS-WU}$ (not maskable)	Running if enabled. Not running if disabled	Low power. Wake-up capability if enabled
Sleep	VDD: OFF, V2: OFF, HS: OFF or Cyclic	CAN, SPI, L0:L3, Cyclic Sense Forced Wake-up	LOW	Not Active	Not running	Low power. Wake-up capability if enabled
Normal Debug(39)	Same as Normal	–	Normally HIGH. Active LOW if VDD under-voltage occurs	Same as Normal	Not running	Same as Normal
Standby Debug(39)	Same as Standby	–	Normally HIGH. Active LOW if VDD under-voltage occurs	Same as Standby	Not running	Same as Standby
Stop Debug(39)	Same as Stop	Same as Stop	Normally HIGH. Active LOW if VDD under-voltage occurs	Same as Stop	Not running	Same as Stop
Flash Programming	Forced externally	–	Not operating	Not operating	Not operating	Not operating

Notes

39. Mode entered via special sequence described under the heading Debug Mode: Hardware and Software Debug with the 33742, beginning on page 34.
40. I_{DD} over-current always enabled.
41. $\overline{\text{WDOG}}$ if enabled.

APPLICATION WAKE-UP FROM THE 33742

When the application is in Stop mode, it can be awakened from the SBC side. When a wake-up condition is detected by the SBC (for example, CAN, wake-up input), the 33742 enters the Normal Request mode and generates an interrupt pulse at the $\overline{\text{INT}}$ pin.

APPLICATION WAKE-UP FROM THE MCU

When the device is in the Stop mode, a wake-up event may come from the system MCU. In this case the MCU selects the device the using a LOW-to-HIGH transition on the 33742 $\overline{CS}$ pin. Then the 33742S goes into Normal Request mode and generates an interrupt pulse at the $\overline{INT}$ pin.

STOP MODE CURRENT MONITOR

If the VDD output current exceeds an internal set threshold (I_{DDS-WU}), the SBC automatically enters the Normal Request mode and generates an interrupt at the $\overline{INT}$ pin. The interrupt is a non-maskable and the INTR register will have no flag set.

INTERRUPT GENERATION WHEN WAKE-UP FROM STOP MODE

When the SBC wakes from Stop mode, it first enters the Normal Request mode before generating a 10 μs typical pulse on the $\overline{INT}$ pin. These are non-maskable interrupts with the wake-up event read through the SPI registers, the CANWU bit in the CAN Register (CANR), or the LCTRx bit in the Wake-up Register (WUR). In case of wake-up from Stop mode over-current situation or from forced wake-up, no bits are set. After the $\overline{INT}$ pulse, the 33742 accepts SPI command after a time delay ($t_{S-1STSPI}$).

WATCHDOG SOFTWARE IN STOP MODE

If the SBC watchdog is enabled, the application must provide a “system ok” response before the end of the 33742 watchdog time. Typically an MCU initiates the wake-up of the 33742 through the SPI wake-up ($\overline{CS}$ activation). The SBC will awaken and jump into the Normal Request mode. The MCU has to configure the 33742 to go to either Normal or Standby mode. The MCU can then decide to return to the Stop mode.

If no MCU wake-up occurs within the watchdog time period, the SBC activates the $\overline{RST}$ pin and jumps into the Normal Request mode. The MCU can then be re-initialized.

STOP MODE ENTER COMMAND

Stop mode is entered at the end of the SPI message at the rising edge of the $\overline{CS}$. (Refer to the $t_{\overline{CS}-STOP}$ data in the Dynamic Electrical Characteristics table on page 16.) Once Stop mode is entered, the SBC can wake up from a VDD regulator over-current detection state. In order to allow time for the MCU to complete the last CPU instruction and enter its low power mode, a deglitcher time of 40 μs typical is implemented.

Figure 11, page 29, depicts the operation of entering the Stop mode.

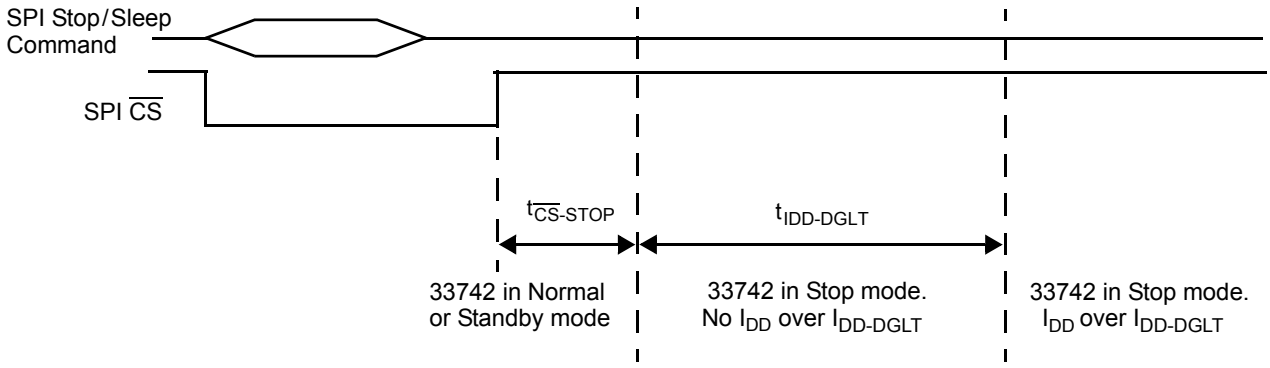


Figure 11. Entering the Stop Mode

WATCHDOG SOFTWARE ($\overline{RST}$ AND $\overline{WDOG}$) (SELECTABLE WATCHDOG WINDOW OR WATCHDOG TIME-OUT)

A watchdog is used in the SBC Normal and Standby modes for monitoring the MCU operation. The watchdog timer may be implemented as either a watchdog window or watchdog timeout, selectable by SPI (TIM1 sub register, bit WDW). Default operation is a watchdog window.

The watchdog period can be set from 10 to 350 ms (TIM1 sub register, bits WDT0 and WDT1). When a watchdog window is selected, the closed window is the first part of the selected period, and the open window is the second part of the period. (Refer to Timing Register (TIM1/2) beginning on page 52.)

The watchdog can only be cleared within the open window time period. Any attempt to clear watchdog in the closed window will generate a reset. The watchdog is cleared addressing the TIM1 sub register using the SPI.

$\overline{\text{RST}}$ PIN DESCRIPTION

A 33742 output is available to perform a reset of the MCU. Reset can happen from:

- V_{DD} Falling Out of Range—If V_{DD} falls below the reset threshold ($V_{\overline{RST}TH}$), the $\overline{\text{RST}}$ pin is pulled LOW until V_{DD} returns to the normal voltage.
- Power-ON Reset—At 33742 power-on or wake-up from Sleep mode, the $\overline{\text{RST}}$ pin is maintained LOW until V_{DD} is within its operation range.
- Watchdog Timeout—If watchdog is not cleared, the 33742 will pull the $\overline{\text{RST}}$ pin LOW for the duration of the reset time ($t_{\overline{RST}DUR}$).

$\overline{\text{RST}}$ AND $\overline{\text{WDOG}}$ OPERATION

Table 8 describes watchdog and reset output modes of operation. $\overline{\text{RST}}$ is activated in the event V_{DD} fall or watchdog is not triggered. $\overline{\text{WDOG}}$ output is active LOW as soon as $\overline{\text{RST}}$ goes LOW and stays LOW as long as the watchdog is not properly reset via SPI. The $\overline{\text{WDOG}}$ output pin is designed as a push-pull structure that can drive off chip components signaling, for instance, errant MCU operation.

Figure 12 illustrates the device behavior in the event the TIM1 register in not properly accessed. In this case, a software reset occurs and the $\overline{\text{WDOG}}$ pin is set LOW until the TIM1 register is properly accessed.

Table 8. Watchdog and Reset Output Operation

Events	$\overline{\text{WDOG}}$ Output	$\overline{\text{RST}}$ Output
Device Power up	LOW to HIGH	LOW to HIGH
V_{DD} Normal, $\overline{\text{WDOG}}$ Properly Triggered	HIGH	HIGH
$V_{DD} < V_{\overline{RST}TH}$	HIGH	LOW
$\overline{\text{WDOG}}$ Timeout Reached	LOW (42)	LOW

Notes

42. $\overline{\text{WDOG}}$ stays LOW until the TIM1 register is properly addressed through SPI.

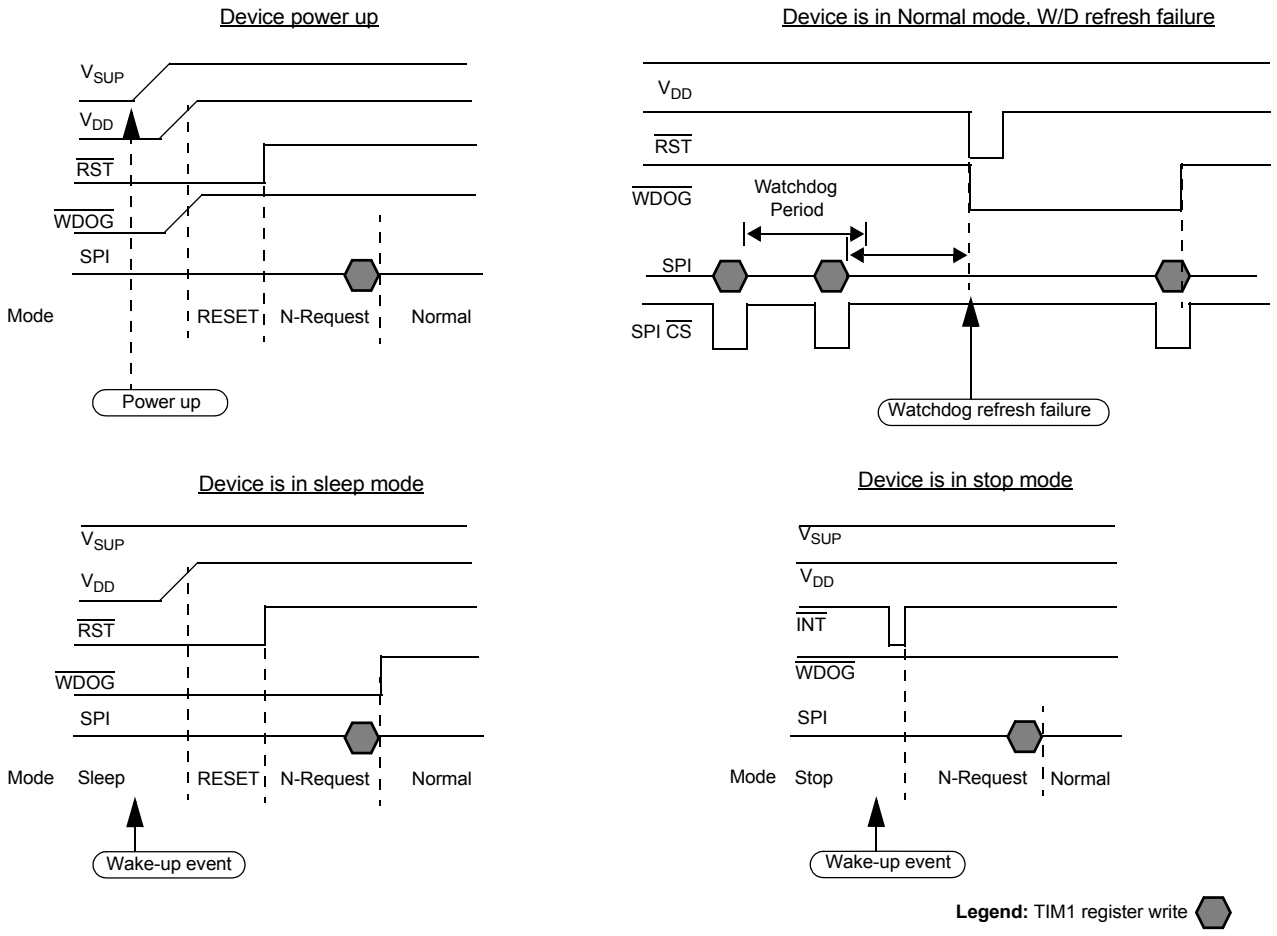


Figure 12. $\overline{\text{RST}}$ and $\overline{\text{WDOG}}$ Output Operation

WAKE-UP CAPABILITIES

Several wake-up capabilities are available to the SBC when it is in Sleep or Stop mode. When a wake-up has occurred, the wake-up event is stored in the Wake-up Register (WUR) or the CAN register and read by the MCU to determine the wake-up source. The wake-up options are selectable through SPI while the 33742 is in Normal or Standby mode and prior to entering low power modes (Sleep or Stop mode). When a wake-up occurs in Sleep mode, the SBC reactivates the VDD supply. It generates an interrupt if a wake-up occurs from Stop mode.

WAKE-UP FROM WAKE-UP INPUTS (L0:L3) WITHOUT CYCLIC SENSE

The wake-up lines are used to determine the state of external switches and if changes occurred to wake up the MCU (in Sleep or Stop modes). The wake-up pins L0:L3 are able to handle up to 40 VDC. The internalize" threshold is 3.0 V typical, and these inputs can be used as an input port expander. The wake-up input states are read through SPI (WUR register).

In order to select and activate direct wake-up from the L0:L3 inputs, the WUR register must be configured with the appropriate level sensitivity. Additionally, the Low Power Control (LPC) Register must be configured with 0xx0 data (bits LX2HS and HSAUTO are set to 0).

The sensitivity of the L0:L3 inputs is selected by the WUR register. Level sensitivity is configured by L0:L3 input pairs: L0 and L1 level sensitivity are configured together, while L2 and L3 are configured together.

CYCLIC SENSE WAKE-UP (CYCLIC SENSE TIMER AND WAKE-UP INPUTS L0:L3)

The 33742 can wake up upon state change of one of the four wake-up input lines (L0:L3). The external pull-up or pull-down resistor of the switches associated with the wake-up input lines can be biased from the HS VSUP switch. The HS switch is activated in Sleep or Stop modes from an internal timer. Cyclic Sense and Forced Wake-up are exclusive states. If Cyclic Sense is enabled, Forced Wake-up cannot be enabled.

In order to select and activate the cyclic sense wake-up from the L0:L3 inputs, the WUR register must be configured with the appropriate level sensitivity and the LPC register must be configured with 1xx1 data (bit LX2HS set at 1 and bit HSAUTO set at 1. The wake-up mode selection (direct or cyclic sense) is valid for all four wake-up inputs.

FORCED WAKE-UP

The SBC can wake-up automatically after a predetermined time spent in Sleep or Stop mode. Cyclic Sense and Forced Wake-up are exclusive. If Forced Wake-up is enabled (FWU bit set to 1 in the LPC register), Cyclic Sense cannot be enabled.

CAN INTERFACE WAKE-UP

The SBC incorporates a high-speed 1.0 Mbps CAN physical interface. It is compatible with ISO 11898-2 standard. The operation of the CAN physical interface is controlled through the SPI. The CAN operating modes are independent of the 33742 operational modes.

The SBC can wake up from a CAN message if the CAN wake-up feature is enabled. Refer to the section titled Logic Commands And Registers beginning on page 46 for details of the wake-up detection.

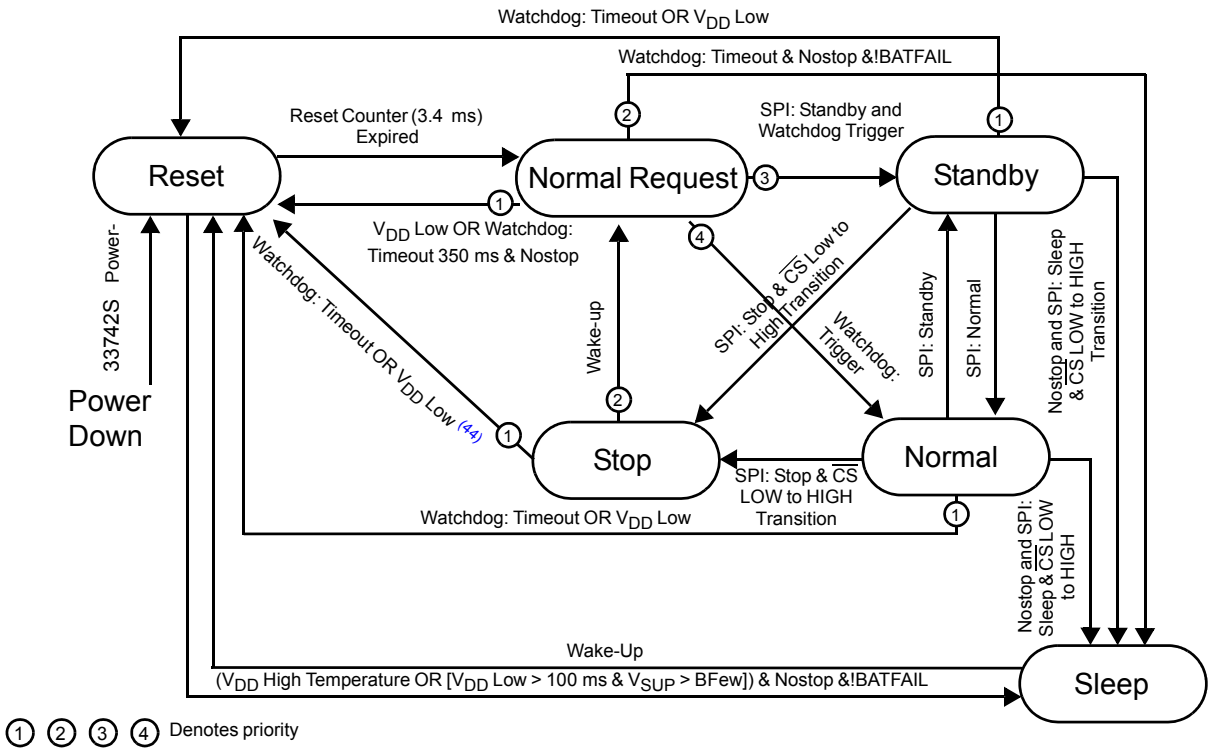
SPI WAKE-UP

The 33742 can be awakened by changes on the $\overline{CS}$ pin in Sleep or Stop modes. Wake-up is detected as a LOW-to-HIGH level transition on the $\overline{CS}$ pin. In the Stop mode, this corresponds to a condition where an MCU and the SBC are both in the Stop mode and when the application wake-up event comes through the MCU.

33742 POWER-UP AND WAKE-UP FROM SLEEP MODE

After device or system power-up, or after the SBC awakens from Sleep mode, the 33742S enters into the Reset mode prior to moving into Normal Request mode.

Figure 13, shows the device state diagram. Figure 14, shows device operation after power-up.



State Machine Description

Nostop = Nostop bit = 1
!Nostop = Nostop bit = 0
BATFAIL = Batfail bit = 1
!BATFAIL = Batfail bit = 0
V_{DD} Over-temperature = V_{DD} thermal shutdown occurs
V_{DD} LOW = V_{DD} below reset threshold
V_{DD} LOW > 100 ms = V_{DD} below reset threshold for more than 100 ms
Watchdog: Trigger = TIM1 subregister write operation
V_{SUP} > BFew = V_{SUP} > Battery Fail Early Warning (6.1 V typical)
Watchdog: Timeout = TIM1 register not written before watchdog timeout period expired, or watchdog written in incorrect time window if watchdog window selected (except Stop mode). In Normal Request mode, timeout is 355 ms p2.2 (350 ms p3) ms.
SPI: Sleep = SPI write command to MCR register, data sleep
SPI: Stop = SPI write command to MCR register, data stop
SPI: Normal = SPI write command to MCR register, data normal
SPI: Standby = SPI write command to MCR register, data standby

Notes
43. These two SPI commands must be sent consecutively in this sequence.
44. If watchdog activated.

Figure 13. SBC State Diagram (Not Valid in Debug Modes)

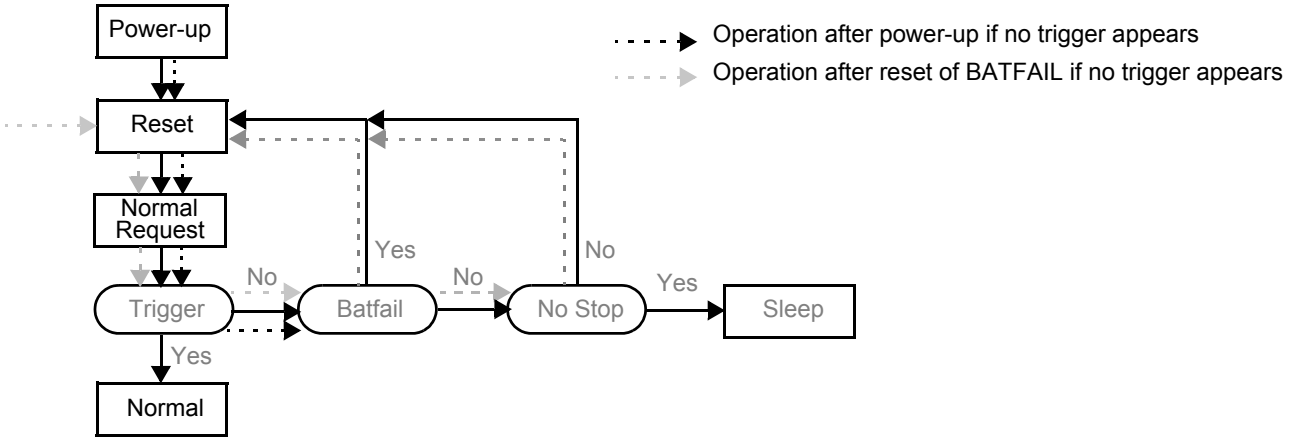


Figure 14. Operation After SBC Power-up

DEBUG MODE: HARDWARE AND SOFTWARE DEBUG WITH THE 33742

When a SBC, and the MCU it serves, is used on the same printed circuit board, both the MCU software and the 33742 operation must be debugged concurrently. The following features permit system debugging by allowing the disabling of the SBC internal software watchdog timer.

DEVICE POWER-UP, RESET PIN CONNECTED TO VDD

The VDD voltage is available when the 33742 power-up but the 33742 will not have received any SPI communication to configure itself. Until set up by the system MCU, the 33742 will generate a reset every 350 ms until the part is configured. To avoid continuous MCU hardware resets, the 33742's RST pin can be connected directly to the VDD pin by a hardware jumper.

DEBUG MODES WITH SOFTWARE WATCHDOG DISABLED THOUGH SPI (NORMAL DEBUG, STANDBY DEBUG, AND STOP DEBUG)

The software configurable watchdog can be disabled through the SPI. To set the watchdog disable while limiting the risk of inadvertently disabling the watchdog timer during normal 33742 operation, it is recommended that the disable be done using the following sequence:

- Step 1–Power down the SBC.
- Step 2–Power up the SBC. This sets the BATFAIL bit, allowing the 33742 to enter Normal Request mode.
- Step 3–Write to the TIM1 sub register to allow the SBC to enter Normal mode.
- Step 4–Write to the MCR register with data 0000. This enables the debug mode. Complete SPI byte is 0001 0000.
- Step 5–Write to the MCR register normal debug. SPI byte is 0001 x101.

  Important While in debug mode, the SBC can be used without having to clear the watchdog on a regular basis to facilitate software and hardware debug.
- Step 6–To leave the debug mode, write 0000 to the MCR register.

At Step 2, the SBC is in Normal Request. Steps 3, 4, and 5 should be completed consecutively and within the 350 ms time period of the Normal Request mode. If not, the 33742 will go into Reset mode and enter Normal Request again.

Figure 15, page 34, illustrates debug mode selection.

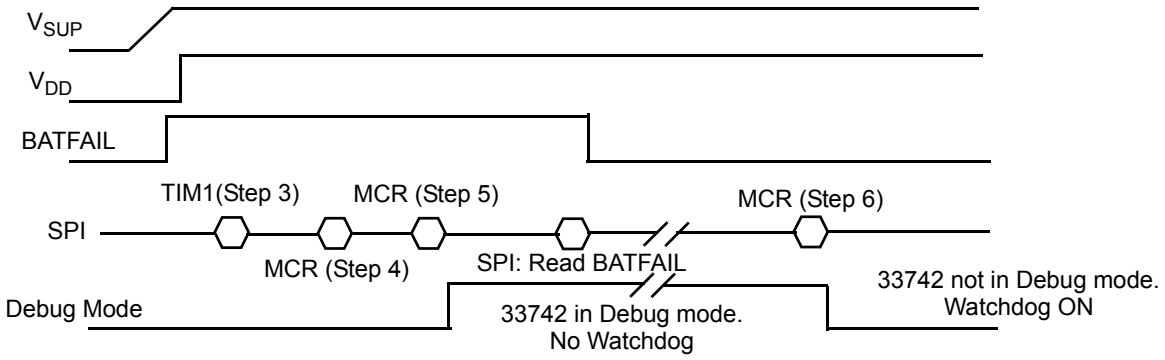


Figure 15. Entering Debug Mode

When the SBC is operating in the debug mode and has been set into Stop Debug or Sleep mode, a wake-up causes the 33742 to enter the Normal Request mode for 350 ms. To avoid having the SBC generate an unwanted reset (enter Reset mode), the next debug mode (Normal Debug or Standby Debug) should be configured within the 350 ms time window of the Normal Request mode.

To avoid entering debug mode after a power-up, first read the BATFAIL bit (MCR read) and write 0000 into the MCR register.

Figures 16 and 17, page 35, show the detailed operation of the SBC once the debug mode has been selected.

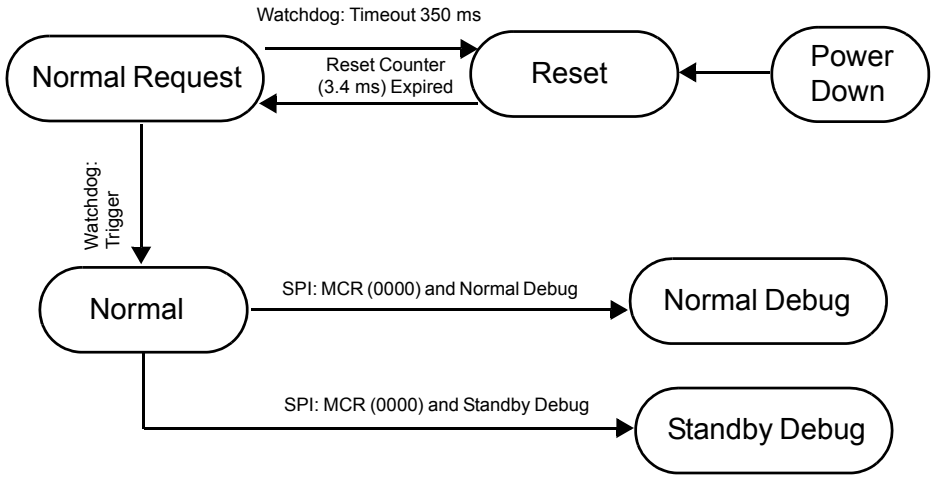
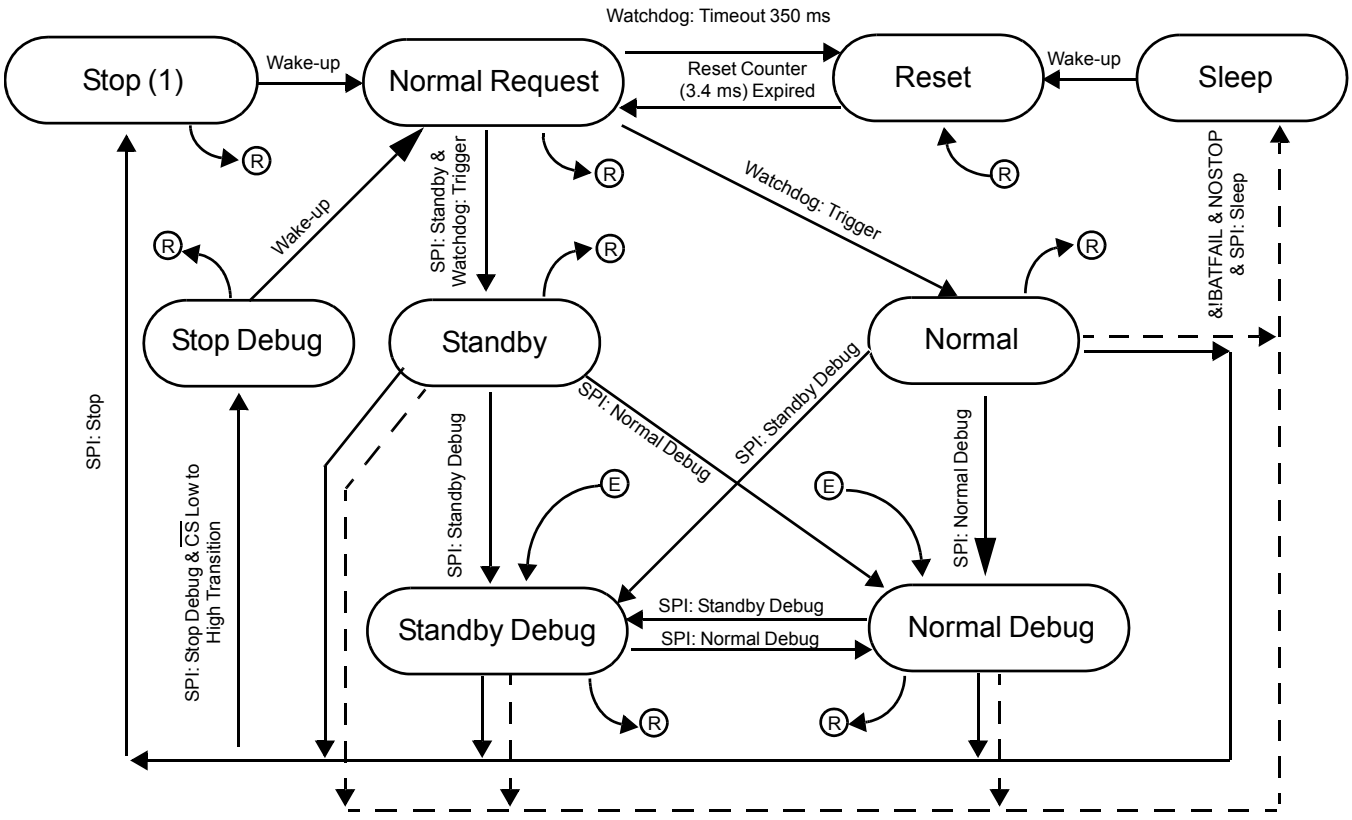


Figure 16. Transitions to Enter Debug Modes



(1) If Stop mode is entered, it is entered without watchdog, no matter the WDSTOP bit.
(E) Debug mode entry point (Step 5 of the Debug mode entering sequence).
(R) Represents transitions to Reset mode due to V1 low.

Figure 17. Simplified 33742S State Diagram in Debug Modes

MCU FLASH PROGRAMMING CONFIGURATION

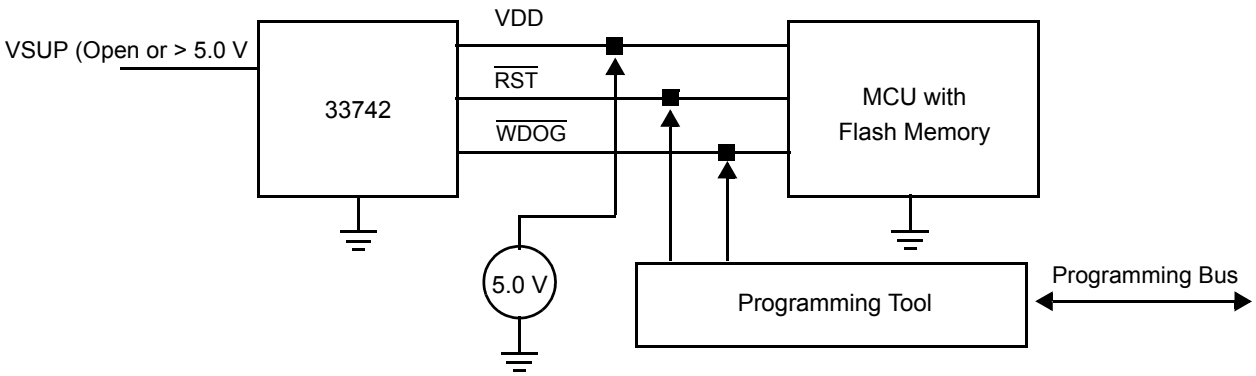
To allow for new software to be loaded into a SBC's MCU NVM or to standalone EEPROM or Flash, the 33742 is capable of having (1) VSUP applied to it to from an external power 5.0 V supply and (2) having the $\overline{RST}$ and the $\overline{WDOG}$ outputs pins eternally forced to 0.0 or 5.0 V without damaging the device.

This allows the SBC to be externally powered and off-board signals to be applied to the reset pins. No functions of the 33742 are operating. Figure 18 illustrates a typical configuration for the connection of programming and debugging tools.

The VSUP should be left open or forced to a value equal to or above V.

The VDD regulator uses an internal pass transistor between VSUP and the VDD output pin. Biasing the VDD output pin with a voltage greater than VDD potential will force current through the body diode of the internal pass transistor to the VSUP pin.

The $\overline{RST}$ pin is periodically pulled LOW for the $t_{\overline{RST}DUR}$ time (device in Reset mode), before being pulled to VDD for 350 ms typical (device in Normal Request mode). During the time reset is LOW, the $\overline{RST}$ pin sinks 5.0 mA maximum (I_{PDW}).



Note External supply and sources applied to VDD, $\overline{RST}$, and $\overline{WDOG}$ test points on application circuit board.

Figure 18. Simplified Schematic for Microcontroller Flash Programming

CAN PHYSICAL INTERFACE

The SBC features a high-speed CAN physical interface for bus communication from 60 kbps up to 1.0 Mbps. Figure 19 is a simplified block diagram of the CAN interface of the 33742.

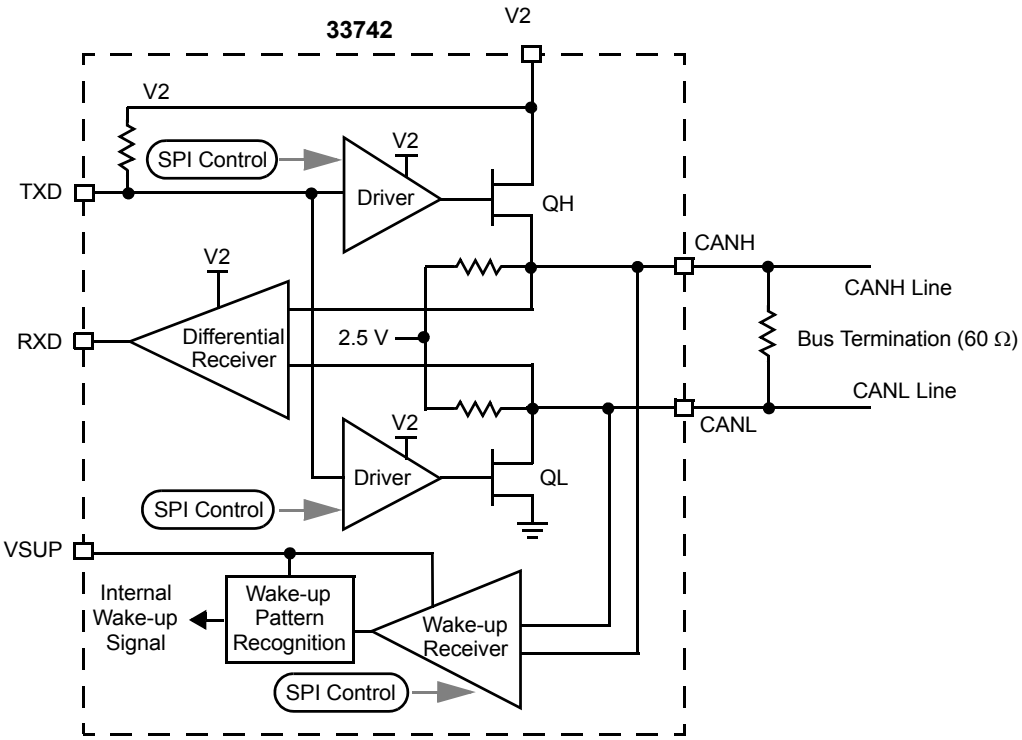


Figure 19. Simplified Block Diagram of CAN Interface

CAN INTERFACE SUPPLY

The supply voltage for the CAN transceiver is the V2 pin. The CAN interface also has a supply path from the external supply line through the VSUP pin. This path is used in CAN Sleep mode to allow wake-up detection.

During CAN communication (transmission and reception), the CAN interface current is sourced from the V2 pin. During CAN low power mode, the current is sourced from the VSUP pin.

MAIN OPERATION MODES DESCRIPTION

The CAN interface of the SBC has two main operating modes: TXRX and Sleep mode. The modes are controlled by the CAN SPI Register. In the TXRX mode, which is used for communication, four different slew rates are available for the user. In the Sleep mode, the user has the option of enabling or disabling the remote CAN wake-up capability.

CAN DRIVER OPERATION IN TXRX MODE

When the CAN interface is in TXRX mode, the driver has two states: recessive or dominant. The driver state is controlled by the TXD pin. The bus state is reported through the RXD pin.

When TXD is HIGH, the driver is set in recessive state, and CANH and CANL lines are biased to the voltage set at V2 divided by 2, or approximately 2.5 V.

When TXD is LOW, the bus is set into dominant state: CANL and CANH drivers are active. CANL is pulled to ground, and CANH is pulled HIGH toward 5.0 V (voltage at V2).

The RXD pin reports the bus state: CANH minus CANL voltage is compared versus an internal threshold (a few hundred millivolts). If CANH minus CANL is below the threshold, the bus is recessive and RXD is set HIGH. If CANH minus CANL is above the threshold, the bus is dominant and RXD is set LOW. This is illustrated in Figure 19.

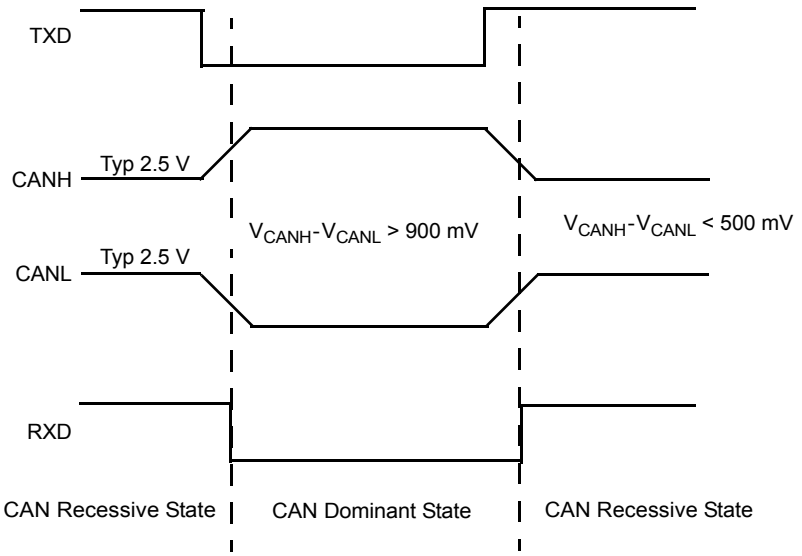


Figure 20. CAN Interface Levels

TXD AND RXD PINS

The TXD pin has an internal pull-up to V2. The state of TXD depends on the V2 status. RXD is a push-pull structure, supplied by V2. When V2 is set at 5.0 V and CAN is TXRX mode, RXD reports bus status. For details, refer to Table , page 28, Table 9, below, and Table 10, page 39.

The TXD pin is a push-pull structure between the V2 pin and GND. The circuitry has a parasitic diode between RXD and V2. It is illustrated in Figure 25. This parasitic diode is reversed biased in normal operation (TXD voltage is lower or equal to V2). In case the TXD voltage is greater than V2, a current will flow into the diode.

If the V2 pin is low (e.g. in sleep mode, or in stop with a ballast transistor), the current leakage at V2 is low enough (10 μA max) to ensure than the RXD pin can be pulled up by an external resistor (i.e. the MCU RXD pin internal pull-up).

The states of the RXD pin in the following Table 9 and 10 is dependant upon external circuitry connected to the V2 and RXD pins.

CAN TXRX MODE AND SLEW RATE SELECTION

The slew rate selection is done via CAN register (refer to Tables 22 through 24 on page 50). Four slew rates are available and control the recessive-to-dominant and dominant-to-recessive transitions. The delay time from TXD pin to CAN bus, from CAN bus to RXD, and from the TXD to RXD loop time is affected by the slew rate selection.

Table 9. CAN Interface/33742S Modes and Pin Status—Operation with Ballast on V2(45)

Mode	CAN Mode (Controlled by SPI)	V2 Voltage	TXD Pin	RXD Pin(46)	CANH/CANL (Disconnected from Other Node)	CAN Communication
Unpowered	–	0.0 V	LOW	LOW	Floating to GND	NO
Reset (with Ballast)	–	0.0 V	LOW	LOW	Floating to GND	NO
Normal Request (with Ballast)	–	0.0 V	LOW	LOW	Floating to GND	NO
Normal	Sleep	5.0 V	0.0 V	5.0 V	Floating to GND	NO
Normal	Normal Slew Rate 0, 1, 2, 3	5.0 V	Internal Pull-up to V2	Report Bus State HIGH if Bus Recessive, LOW if dominant	Bus Recessive CANH = CANL = 2.5 V	YES

Table 9. CAN Interface/33742S Modes and Pin Status—Operation with Ballast on V2[45]

Standby with External Ballast	Normal or Sleep	0.0 V	LOW	LOW	Floating to GND	NO
Sleep	Sleep	0.0 V	LOW	LOW	Floating to GND	NO. Wake-up if enabled
Stop	Sleep	0.0 V	LOW	LOW	Floating to GND	NO. Wake-up if enabled

Notes
45. See also Figure 31, page 57.
46. The state of the RXD pin is dependant upon: 1) the V2 voltage, 2) the external circuitry connected to RXD, (i.e. the MCU RXD pin), and 3) any external pull-up between RXD and the 5.0 V supply.

Table 10. CAN Interface/33742 Modes and Pin Status—Operation without Ballast on V2 [47]

Mode	CAN Mode (Controlled by SPI)	V2 Voltage	TXD Pin	RXD Pin[48]	CANH/CANL (Disconnected from Other Node)	CAN Communication
Unpowered	–	0.0 V	LOW	LOW	Floating to GND	NO
Reset (without Ballast)	–	5.0 V	LOW	LOW	Floating to GND	NO
Normal Request without Ballast. V2 Connected to VDD	–	5.0 V	LOW	5.0 V	Floating to GND	NO
Standby without External Ballast,. V2 connected to VDD	Normal or Sleep	5.0 V	0.0 V	5.0 V	Floating to GND	NO
Normal without External Ballast. V2 Connected to VDD	Normal Slew Rate 0, 1, 2,3	5.0 V	5.0 V	5.0 V	Bus Recessive CANH = CANL = 2.5 V	YES
Normal without External Ballast,. V2 Connected to VDD	Sleep	5.0 V	0.0 V	5.0 V	Floating to GND	NO
Sleep	Sleep	0.0 V	LOW	LOW	Floating to GND	NO. Wake-up if enabled
Stop	Sleep	5.0 V	LOW	LOW	Floating to GND	NO. Wake-up if enabled

Notes
47. See also Figure 36, page 60.
48. The state of the RXD pin is dependant upon: 1) the V2 voltage, 2) the external circuitry connected to RXD, (i.e. the MCU RXD pin), and 3) any external pull-up between RXD and the 5.0 V supply.

CAN SLEEP MODE

The 33742 offers two CAN Sleep modes:

- Sleep mode with CAN wake-up enable: detection of incoming CAN message and SBC wake-up.
- Sleep mode with CAN wake-up disable: no detection of incoming CAN message.

The CAN Sleep modes are set via the CAN SPI register.

In CAN Sleep mode (with wake-up enable or disable), the CAN interface is internally supplied from the VSUP pin. The voltage at V2 pin can be either 5.0 V or turned off. When the CAN is in Sleep mode, the current sourced from V2 is extremely low. In most cases the V2 voltage is off; however, the CAN can be placed into Sleep mode even with 5.0 V applied on V2.

In CAN Sleep mode, the CANH and CANL drivers are disabled, and the receiver is also disabled. CANH and CANL are high-impedance mode to ground.

CAN SIGNALS IN TXRX AND SLEEP MODES

When the CAN interface is set back into TXRX mode by an SPI command, CAN H and CANL are set in recessive level. This is illustrated in Figure 21.

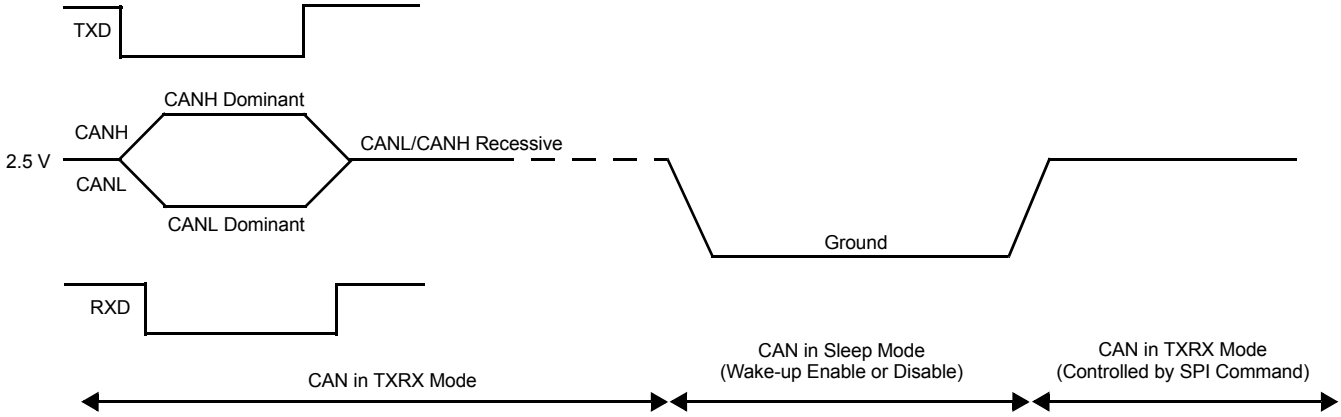


Figure 21. CAN Signals in TXRX and Sleep Modes

CAN IN SLEEP MODE WITH WAKE-UP ENABLE

When the CAN interface is in Sleep mode with wake-up enable, the CAN bus traffic is detected. The CAN bus wake-up is a pattern wake-up.

PATTERN WAKE-UP

In order to wake up the CAN interface, the following criteria must be fulfilled:

- The CAN interface wake-up receiver must receive a series of three consecutive valid dominant pulses, each of which must be longer than 500 ns and shorter than 500 μs.
- The distance between 2 pulses must be lower than 500 μs.
- The three pulses must occur within a time frame of 1.0 ms.

The pattern wake-up of the 33742 CAN interface allow wake-up by any CAN message content.

Figure 22 below illustrates the CAN signals during a CAN bus Sleep state and wake-up sequence.

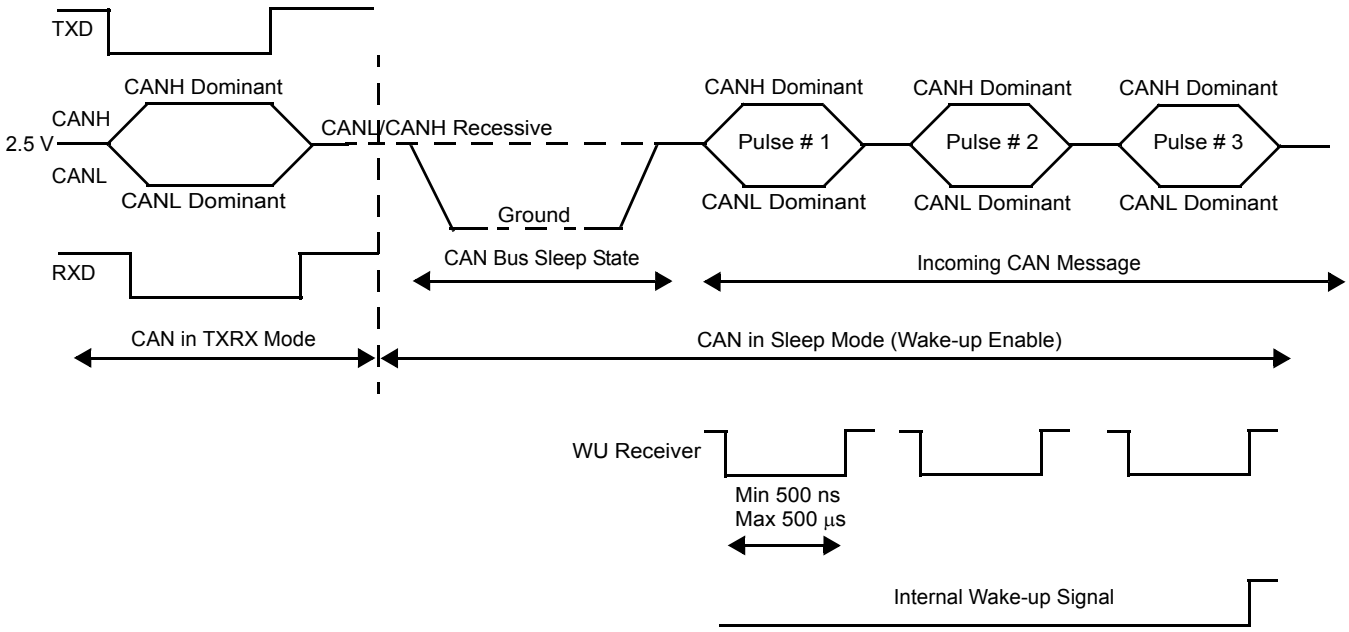


Figure 22. CAN Bus Signal During Can Sleep State and Wake-up Sequence

Figure 23 illustrates how the wake-up signal is generated. First the CAN signal is detected by a low consumption receiver (WU receiver). Then the signal passes through a pulse width filter, which discards the undesired pulses. The pulse must have a width bigger than 0.5 µs and smaller than 500 µs to be accepted. When a pulse is discarded, the pulse counter is reset and no wake-up signal is generated. When a pulse is accepted, the pulse counter is incremented and, after three pulses, the internal wake-up signal is asserted.

Each one of the pulses must be spaced by no more than 500 µs. If not, the counter will be reset and no wake-up signal will be generated. This is accomplished by the wake-up timeout generator. The wake-up cycle is completed (and the wake-up flag reset) when the CAN interface is brought to CAN Normal mode.

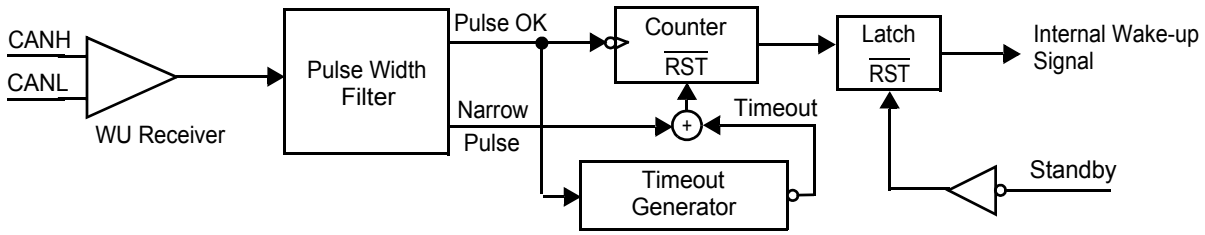


Figure 23. Wake-up Functional Block Diagram

CAN WAKE-UP REPORT

The CAN wake-up reporting depend upon the low power mode the SBC is in.

If the SBC is placed into Sleep mode (VDD and V2 off), the CAN wake-up or any wake-up results in the VDD regulator turning on, leading to turning on the MCU supply and releasing reset. If the 33742 is in Stop mode (V2 off and VDD active), the CAN wake-up or any wake-up is signalled by a pulse on the $\overline{INT}$ output. In addition the CANWU bit is set in the CAN register.

If the SBC is in Normal or Standby mode and the CAN interface is in Sleep mode with wake-up enabled, the CAN wake-up is reported by the CANWU bit in the CAN register.

In the event the SBC is in Normal mode and CAN Sleep mode with wake-up enabled, it is recommended that the user check for the CANWU bit prior to placing the 33742 in Sleep or Stop mode in case bus traffic has occurred while the CAN interface was in Sleep mode.

After a CAN wake-up, a flag is set in the CAN register. Bit CANWU reports the CAN wake-up event while the 33742 was in Sleep or Stop mode. This bit is set until the CAN is in placed by SPI command into TXRX mode and the CAN register can be read.

CAN BUS DIAGNOSTIC

The SBC can diagnose CANH or CANL lines short to GND, shorts to VSUP or VDD.

As illustrated in Figure 24, several single-ended comparators are implemented on the CANH and CANL bus lines. These comparators monitor the bus voltage level in the recessive and dominant states. This information is then managed by a logic circuit to determine if a failure has occurred and to report it. Table 11 indicates the state of the comparators in the event of bus failure and the state of the drivers; that is, whether they are recessive or dominant.

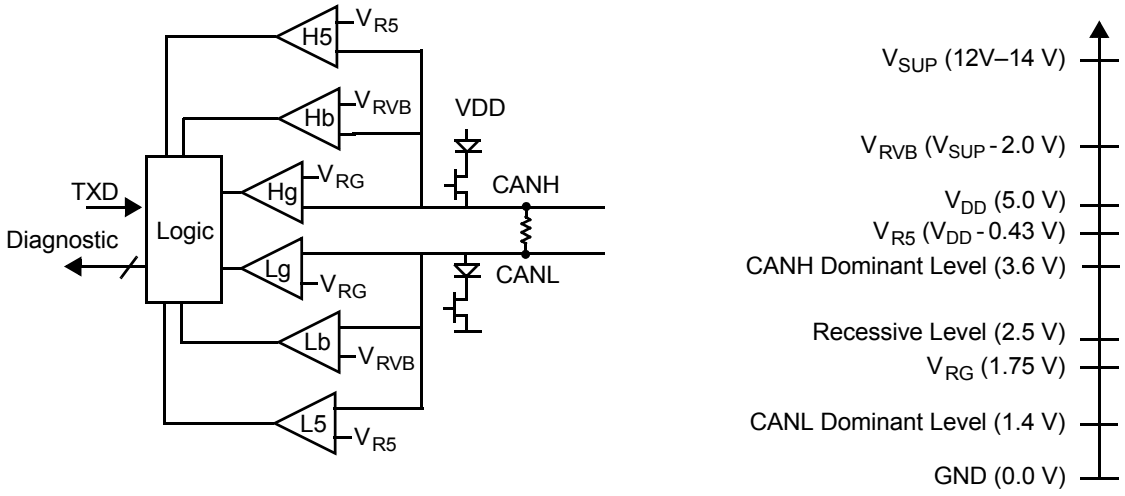


Figure 24. CAN Bus Simplified Structure

Table 11. Short to GND, Short to VSUP, and Short to 5.0 V (VDD) Detection Truth Table

Failure Description	Driver Recessive State		Driver Dominant State	
	Lg (Threshold 1.75 V)	**Hg (Threshold 1.75 V)**	**Lg (Threshold 1.75 V)**	**Hg (Threshold 1.75 V)**
No failure	1	1	0	1
CANL to GND	0	0	0	1
CANH to GND	0	0	0	0
	Lb (Threshold V_{SUP}-2.0 V)	**Hb (Threshold V_{SUP}-2.0 V)**	**Lb (Threshold V_{SUP}-2.0 V)**	**Hb (Threshold V_{SUP}-2.0 V)**
No failure	0	0	0	0
CANL to VSUP	1	1	1	1
CANH to VSUP	1	1	0	1
	L5 (Threshold VDD**-0.43 V)**	**H5 (Threshold** VDD**-0.43 V)**	**L5 (Threshold** VDD**-0.43 V)**	**H5 (Threshold** VDD**-0.43 V)**
No failure	0	0	0	0
CANL to V_{DD}	1	1	1	1
CANH to V_{DD}	1	1	0	1

DETECTION PRINCIPLE

In the recessive state, if one of the two bus lines is shorted to GND, VDD, or VSUP, then voltage at the other line follows the shorted line due to bus termination resistance and the high-impedance of the driver. For example, if CANL is shorted to GND, CANL voltage is zero, and CANH voltage, as measured by the Hg comparator, is also close to zero.

In the recessive state the failure detection to GND or VSUP is possible. However, it is impossible to distinguish which bus line, CANL or CANH, is shorted to GND or VSUP. In the dominant state, the complete diagnostic is possible once the driver is turned on.

CAN BUS FAILURE REPORTING

CANL bus line failures (for example, CANL short to GND) is reported in the SPI register TIM1/2. CANH bus line (for example, CANH short to VSUP) is reported in the LPC register.

In addition CAN-F and CAN-UF bits in the CAN register indicate that a CAN bus failure has been detected.

NON-IDENTIFIED AND FULLY IDENTIFIED BUS FAILURES

As indicated in Table 11, page 42, when the bus is in a recessive state it is possible to detect an error condition; however, is it not possible to fully identify the specific error. This is called “non-identified” or “under-acquisition” bus failure. If there is no communication (i.e., bus idle), it is still possible to warn the MCU that the SBC has started to detect a bus failure.

In the CAN register, bits D2 and D1 (CAN-F and CAN-UF, respectively) are used to signal bus failure. Bit D2 reports a bus failure and bit D1 indicates if the failure is identified or not (bit D1 is set to logic [1} if the error is not identified).

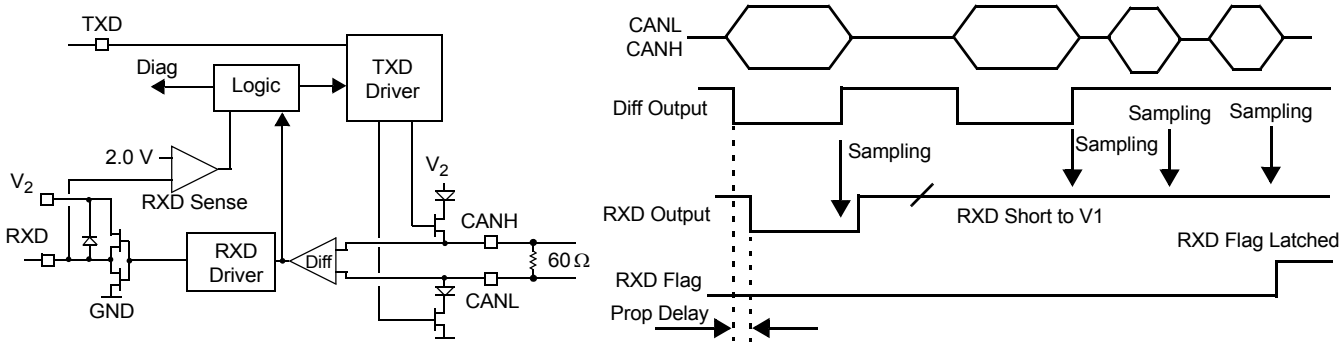
When the detection mechanism is fully operating any bus error will be detected and reported in the TIM1/2 and LPC registers and bit D1 will be reset to logic [0].

NUMBER OF SAMPLES FOR PROPER FAILURE DETECTION

The failure detector requires at least one cycle of recessive and dominant state to properly recognize the bus failure. The error will be fully detected after five cycles of recessive-dominant states. As long as the failure detection circuitry has not detected the same error for five recessive-dominant cycles, the bit “non-identified failure” (CAN-UF) will be set.

RXD PERMANENT RECESSIVE FAILURE

The purpose of this detection mechanism is to diagnose an external hardware failure at the RXD output pin and to ensure that a permanent failure at the RXD pin does not disturb network communication.In the event RXD is shorted to a permanent high level signal (i.e., 5.0 V), the CAN protocol module within the MCU cannot receive any incoming message. Additionally, the CAN protocol module cannot distinguish the bus idle state and could start communication at any time. To prevent this, an RXD failure detection, as illustrated in Figure 25 and explained below, is necessary.



Note The RXD Flag is neither the RXPR bit in the LPC register, nor the CANF bit in the INTR register.

Figure 25. RXD Path and RXD Permanent Recessive Detection Principle

RXD FAILURE DETECTION

The SBC senses the RXD output voltage at each LOW-to-HIGH transition of the differential receiver. Excluding internal propagation delay, RXD output should be LOW when the differential receiver is LOW. In the event RXD is shorted to 5.0 V (e.g.,

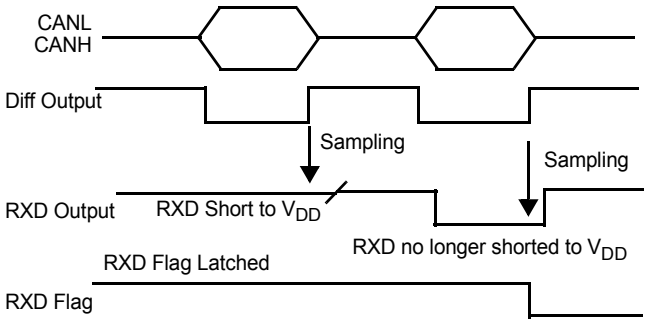
to VDD), RXD will be tied to a high level and the RXD short to 5.0 V can be detected at the next LOW-to-HIGH transition of the differential receiver. Compete detection requires three samples.

When the error is detected, an error flag is latched and the CAN driver is disabled. The error is reported through the SPI register LPC, bit RXPR.

RECOVERY CONDITION

The SBC will try to recover from a bus fault condition by sampling for a correct low level at TXD, as illustrated in Figure 26.

As soon as an RXD permanent recessive is detected, the RXD driver is deactivated and a weak pull-down current source is activated in order to allow recovery conditions. The driver stays disabled until the failure is cleared (RXD no longer permanent recessive) and the bus driver is activated by an SPI register command (write 1 to the CANCLR bit in the CAN register).



Note RXD Flag is neither the RXPR bit in the LPC register nor the CANF bit in INTR register.

Figure 26. RXD Recovery Conditions

TXD PERMANENT DOMINANT FAILURE

PRINCIPLE

In the event TXD is set to a permanent low level, the CAN bus is set into dominant level, and no communication is possible. The SBC has a TXD permanent timeout detector. After timeout, the bus driver is disabled and the bus is released in a recessive state. The TXD permanent dominant failure is reported in the TIM1 register.

RECOVERY

The TXD permanent dominant is used and activated also in case of TXD short to RXD. The recovery condition for TXD permanent dominant (recovery means the reactivation of the CAN drivers) is done by an SPI command and is controlled by the MCU.

The driver stays disabled until the failure is cleared (TXD no longer permanent dominant) and the bus driver is activated by an SPI register command (write logic [1] to CANCLR bit in the CAN register).

TXD TO RXD SHORT CIRCUIT FAILURE

PRINCIPLE

In the event the TXD is shorted to RXD when an incoming CAN message is received, the RXD will be at a LOW. Consequently, the TXD pin is LOW and drives CANH and CANL into the dominant state. The bus is stuck in dominant mode and no further communication is possible.

DETECTION AND RECOVERY

The TXD permanent dominant timeout will be activated and release the CANL and CANH drivers. However, at the next incoming dominant bit, the bus will be stuck again in dominant. In order to avoid this situation, the recovery from a failure (recovery means the reactivation of the CAN drivers) is done by an SPI command and controlled by the MCU.

INTERNAL ERROR OUTPUT FLAGS

There are internal error flags to signal whenever thermal protection is activated or over-current detection occurs on the CANL or CANH pins (THERM-CUR bit). The errors are reported in the CAN register.

DEVICE FAULT OPERATION

Table 12 describes the relationship between device fault or warning and the operation of the VDD, V2, CAN, and HS interface.

Table 12. Fault/Warning

Fault/Warning	VDD	V2	CAN	HS
Battery Fail	Turn OFF	Turn OFF	Turn OFF due to V2. No communication	OFF
VDD Temperature Pre-warning	Warning flag only. Leave as is	No change	No change	No change
VDD Over-temperature	Turn OFF	Turn OFF	Turn OFF due to V2. No communication	OFF
VDD Over-current	VDD regulator enters linear mode. VDD under-voltage reset may occurs. VDD over-temperature Pre-warning or shutdown may occur	Turn OFF if VDD under-voltage reset occurs	If V2 is OFF, turn OFF and no communication	Turn OFF if VDD under-voltage reset occurs
VDD Short-circuit	VDD under-voltage reset occurs. VDD over-temperature Pre-warning or shutdown may occur	Turn OFF	Turn OFF due to V2. No communication	OFF
Watchdog Reset	ON	Turn OFF	Turn OFF due to V2. No communication	OFF
V2LOW (e.g., V2 < 4.0 V)	No change	V2 out of range	Turn OFF due to V2 low	No change
HS Over-temperature	No change	No change	No change	OFF
HS Over-current	No change	No change	No change	HS over-temperature may occur
VSUP LOW	No change	No change	No change	No change
CAN Over-temperature	No change	No change	Disable. As soon as temperature falls, CAN is re-enabled automatically	No change
CAN Over-current	No change	No change	(49)	No change
CANH Short to GND	No change	No change(50)	No communication(51)	No change
CANH Short to VDD	No change	No change	Communication OK	No change
CANH Short to VSUP	No change	No change	Communication OK	No change
CANL Short to GND	No change	No change	Communication OK	No change
CANL Short to VDD	No change	No change	No communication(51)	No change
CANL Short to VSUP	No change	No change	No communication(51)	No change

Notes

49. Refer to descriptions of CANH and CANL short to GND, VDD, and VSUP elsewhere in table.
50. Peak current 150 mA during TXD dominant only. Due to loss of communication, CAN controller reaches bus OFF state. Average current out of V2 is below 10 mA.
51. Over-current might be detected. THERM-CUR bit set in CAN register.

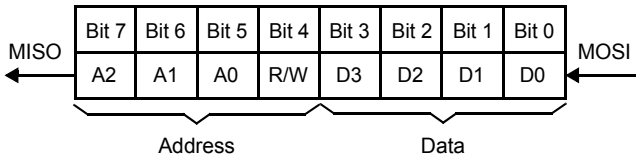
LOGIC COMMANDS AND REGISTERS

SPI INTERFACE AND REGISTER DESCRIPTION

DATA FORMAT DESCRIPTION

Figure 27 illustrates an 8-bit byte corresponding to the 8 bits in a SPI register. The first three bits are used to identify the internal SBC register address. Bit 4 is a read/write bit. The last four bits are data sent from the MCU to the SBC or read back from the 33742 to the MCU.

The state of the MISO has no significance during the write operation. However, during a read operation the final four bits of MISO have meaning; namely, they contain the content of the accessed register.



Note Read operation: R/W bit = logic [0]
Write operation: R/W = logic [1]

Figure 27. Data Format Description.

Table 13. Possible Reset Conditions

Condition	Name	Definition
33742 Reset	POR	Power-ON Reset
33742 Mode Transition	NR2R	Normal Request to Reset mode
	NR2N	Normal Request to Normal mode
	NR2STB	Normal Request to Standby mode
	N2R	Normal to Reset mode
	STB2R	Standby to Reset mode
	STO2R	Stop to Reset mode
	STO2NR	Stop to Normal Request
33742 Mode	RESET	33742S in Reset mode

REGISTER DESCRIPTIONS

The following tables in this section describe the SPI register list and register bit meaning. Register reset values are also described, along with the reset condition. A reset condition is the condition causing the bit to be set at the reset value.

Table 14. List of Registers

Register	Address	Formal Name and Link	Comment and Use	
			Write	Read
MCR	$000	Mode Control Register (MCR) on page 48	Selection for Normal, Standby, Sleep, Stop, and Debug modes	BATFAIL, general failure, VDD pre-warning, and Watchdog flag
RCR	$001	Reset Control Register (RCR) on page 49	Configuration for reset voltage level, CAN Sleep and Stop modes	
CAN	$010	CAN Register (CAN) on page 49	CAN slew rate, Sleep and Wake-up enable/disable modes, drive enable after failure	CAN wake-up and CAN failure status bits

Table 14. List of Registers

IOR	$011	Input/Output Register (IOR) on page 50	HS (high side switch) control in Normal and Standby mode	HS over-temperature bit, VSUP, and V2 LOW status
WUR	$100	on page 51	Control of wake-up input polarity	Wake-up input and real time Lx input state
TIM	$101	Timing Register (TIM1/2) on page 52	• TIM1: Watchdog timing control, Watchdog Window (WDW) or Watchdog Timeout (WTO) mode • TIM2: Cyclic Sense and Forced Wake-up timing selection	CANL and TXD failure reporting
LPC	$110	Low Power Control Register (LPC) on page 54	Control HS periodic activation in Sleep and Stop modes, Forced Wake-up mode activation, CAN-INT mode selection	CANH and RXD failure reporting
INTR	$111	Interrupt Register (INTR) on page 56	Enable or Disable of Interrupts	Interrupt source

NOTE: For SPI Operation

In case a low pulse is asserted by the device on the $\overline{RST}$ output pin during a SPI message, the SPI message can be corrupted. An $\overline{RST}$ low pulse is asserted in 2 cases:

Case 1: W/D refresh issue: The MCU does not perform the SPI watchdog refresh command before the expiration of the timeout (in Normal mode or Normal Request mode and if the “Timeout watchdog” option is selected), or the SPI watchdog refresh command is performed in the closed window (in Normal mode and if “Window watchdog” option is selected).

Case 2: V_{DD} undervoltage condition: V_{DD} falls below the V_{DD} undervoltage threshold.

Message corruption means that the targeted register address can be changed, and another register is written. Table 15 shows the various cases and impacts on SPI register address:

Table 15. Possible Corrupted Registers In Case of RST Pulse During SPI Communication

		Resulting Written register				
		Register	**MCR**	**RCR**	**CAN**	**IOR**
		Address	**$000**	**$001**	**$010**	**$011**
Target written register	Register	Address				
	CAN	$010	X			
	IOR	$011		X		
	WUR	$100	X			
	TIM1/2	$101		X		
	LPC	$110	X		X	
	INTR	$111		X		X

Four registers can be corrupted: MCR, RCR, CAN, and IOR registers. As examples:

- write to CAN register can end up as write to MCR register, or
- write to TIM1 register can end up as write to RCR register

To avoid the previously described behavior, it is recommended to write into the MCR, RCR, CAN, and IOR registers with the expected configuration, after each $\overline{RST}$ assertion.

In the application, a $\overline{RST}$ low pulse leads to an MCU reset and a software restart. By applying this recommendation, all registers will be written with the expected configuration.

MODE CONTROL REGISTER (MCR)

Tables 16 through 18 describes the various Mode Control Registers.

Table 16. Mode Control Register

MCR	R/W	D3	D2	D1	D0
$000b	W	–	MCTR2	MCTR1	MCTR0
	R	BATFAIL[52]	VDDTEMP	GFAIL	WDRST
Reset Value	–	–	0	0	0
Reset Condition (Write)[53]	–	–	POR, RESET	POR, RESET	POR, RESET

Notes
52. BATFAIL bit cannot be set by SPI. BATFAIL is set when VSUP falls below 3.0 V.
53. See Table 13 page 46, for definitions of reset conditions

Table 17. Mode Control Register Control Bits

MCTR 2	MCTR 1	MCTR 0	33742S Mode	Description
0	0	0	Enter/Exit Debug Mode	To enter/exit Debug Mode, refer to detailed description in Debug Mode: Hardware and Software Debug with the 33742, page 34.
0	0	1	Normal	–
0	1	0	Standby	–
0	1	1	Stop, Watchdog OFF[54]	–
0	1	1	Stop, Watchdog ON[54]	–
1	0	0	Sleep[55]	–
1	0	1	Normal	No Watchdog running. Debug mode.
1	1	0	Standby	
1	1	1	Stop	

Notes
54. Watchdog ON or OFF depends on RCR bit D3.
55. Before entering Sleep mode, BATFAIL bit in MCR must be previously cleared (MCR read operation), and NOSTOP bit in RCR must be previously set to logic [1].

Table 18. Mode Control Register Status Bits

Name	Logic	Description
BATFAIL	0	VSUP was not below V_{BF}.
	1	VSUP has been below V_{BF}.
VDDTEMP	0	No over-temperature pre-warning.
	1	Temperature pre-warning on VDD regulator (bit latched).
GFAIL	0	No failure.
	1	CAN Failure or HS over-temperature or V2 low.
WDRST	0	No watchdog reset occurred.
	1	Watchdog reset occurred.

RESET CONTROL REGISTER (RCR)

Tables 19 and 20 contain various Reset Control Register information.

Table 19. Reset Control Register

RCR	R/W	D3	D2	D1	D0
$001b	W	WDSTOP	NOSTOP	CAN SLEEP	RSTTH
	R				
Reset Value	–	1	0	0	0
Reset Condition (Write)(56)	–	POR, RESET, STO2NR	POR, NR2N, NR2STB	POR, NR2N, NR2STB	POR

Notes
56. See Table 13 page 46, for definitions of reset conditions.

Table 20. Reset Control Register Control Bits

Name	Logic	Description
WDSTOP	0	No Watchdog in Stop mode.
	1	Watchdog runs in Stop mode.
NOSTOP	0	Device cannot enter Sleep mode.
	1	Sleep mode allowed. Device can enter Sleep mode.
CAN SLEEP	0	CAN Sleep mode disable (despite D0 bit in CAN register).
	1	CAN Sleep mode enabled (in addition to D0 in CAN register).
RSTTH	0	Reset Threshold 1 selected (typ 4.6 V).
	1	Reset Threshold 2 selected (typ 4.2 V).

CAN REGISTER (CAN)

Tables 21 through 24 contain the information on the CAN register. Table 21 describes control of the high-speed CAN module, mode, slew rate, and wake-up.

Table 21. CAN Register

CAN	R/W	D3	D2	D1	D0
$010b	W	CANCLR	SC1	SC0	MODE
	R	CANWU	CAN-F	CAN-UF	THERM-CUR
Reset Value	–	0	0	0	1
Reset Condition (Write)(57)	–	POR	POR	POR	NR2N, STB2N

Notes
57. See Table 13, page 46, for definitions of reset conditions.

Table 22. CANCLR Control Bits

Logic	Description
0	No effect.
1	Re-enables CAN driver after TXD permanent dominant or RXD permanent recessive failure occurred. Failure recovery conditions must occur to re-enable.

HIGH-SPEED CAN TRANSCEIVER MODES

The MODE bit (D0) controls the state of the CAN interface, TXRX or Sleep mode (Table 23). SC0 bit (D1) defines the slew rate when the CAN module is in TXRX, and it controls the wake-up option (wake-up enable or disable) when the CAN module is in Sleep mode.

Table 23. CAN High Speed Transceiver Modes

SC1	SC0	MODE	CAN Mode (Pass 1.1)
0	0	0	CAN TXRX, Slew Rate 0
0	1	0	CAN TXRX, Slew Rate 1
1	0	0	CAN TXRX, Slew Rate 2
1	1	0	CAN TXRX, Slew Rate 3
x	1	1	CAN Sleep and CAN Wake-up Disable
x	0	1	CAN Sleep and CAN Wake-up Enable

x = Don't care.

Table 24. CAN Register Status Bits

Name	Logic	Description
CANWU	0	No CAN wake-up occurred.
	1	CAN wake-up occurred.
CAN-F	0	No CAN failure.
	1	CAN failure[58].
CAN-UF	0	Identified CAN failure[58].
	1	Non-identified CAN failure.
THERM-CUR	0	No over-temperature or over-current on CANH or CANL drivers.
	1	Over-temperature or over-current on CANH or CANL drivers.

Notes
58. Error bits are latched in the CAN register.

INPUT/OUTPUT REGISTER (IOR)

Tables 25 through 27 contain the Input/Output Register information. Table 26 provides information about information HS control in Normal and Standby modes, while Table 27 provides status bit information.

Table 25. Input/Output Register

IOR	R/W	D3	D2	D1	D0
$011b	W	–	HSON	–	–
	R	V2LOW	HSOT	VSUPLOW	DEBUG
Reset Value	–	–	0	–	–
Reset Condition (Write)[59]	–	–	POR	–	–

Notes
59. See Table 13, page 46, for definitions of reset conditions.

Table 26. HSON Control Bits

Logic	HS State
0	HS OFF, in Normal and Standby modes.
1	HS ON, in Normal and Standby modes.(60)

Notes
60. When HS is turned OFF due to an over-temperature condition, it can be turned ON again by setting the appropriate control bit to 1. Error bits are latched in the IOR register.

Table 27. Input/Output Register Status Bits

Name	Logic	Description
V2LOW	0	V_{2LTH} > 4.0V.
	1	V_{2LTH} < 4.0V.
HSOT	0	No HS over-temperature.
	1	HS over-temperature.
VSUPLOW	0	$V_{BF(EW)}$ > 5.8V.
	1	$V_{BF(EW)}$ < 5.8V.
DEBUG	0	SBC not in Debug mode.
	1	SBC accepts command to go to Debug modes (no Watchdog).

WAKE-UP REGISTER (WUR)

Tables 28 through 30 contain the Wake-up Register information. Local wake-up inputs L0:L3 can be used in both Normal and Standby modes as port expander, as well as for waking up the SBC from Sleep or Stop modes (Table 28).

Table 28. Wake-up Register

WUR	R/W	D3	D2	D1	D0
$100b	W	LCTR3	LCTR2	LCTR1	LCTR0
	R	L3WU	L2WU	L1WU	L0WU
Reset Value	–	0	0	0	0
Reset Condition (Write)(61)	–	POR, NR2R, N2R, STB2R, STO2R			

Notes
61. See Table 13, page 46, for definitions of reset conditions.

Wake-up inputs can be configured by pair. L0 and L1 can be configured together, and L1 and L2, and L2 and L3 can be configured together (Table 29).

Table 29. Wake-up Register Control Bits

LCTR3	LCTR2	LCTR1	LCTR0	L0 L1:L1 L2 Config	L2 L3:L3 L4 Config
x	x	0	0	Inputs Disabled	–
x	x	0	1	High Level Sensitive	
x	x	1	0	Low Level Sensitive	
x	x	1	1	Both Level Sensitive	

Table 29. Wake-up Register Control Bits (continued)

0	0	x	x	–	Inputs Disabled
0	1	x	x		High Level Sensitive
1	0	x	x		Low Level Sensitive
1	1	x	x		Both Level Sensitive

x = Don't care.

Table 30. Wake-up Register Status Bits (62)

Name	Logic	Description
L3WU	0 or 1	If bit = 1, wake-up occurred from Sleep or Stop modes; if bit = 0, no wake-up has occurred. When device is in Normal or Standby mode, bit reports the State on Lx pin (LOW or HIGH) (0 = Lx LOW, 1 = Lx HIGH)
L2WU	0 or 1	
L1WU	0 or 1	
L0WU	0 or 1	

Notes

62. WUR status bits have two functions. After SBC wake-up, they indicate the wake-up source; for example, L2WU set at logic [1] if wake-up source is L2 input. After SBC wake-up and once the WUR register has been read, status bits indicate the real-time state of the Lx inputs (1 = Lx is above threshold, 0 = Lx input is below threshold). If after a wake-up from Lx input a watchdog timeout occurs before the first reading of the WUR register, the LxWU bits are reset. This can occur only if the SBC was in Stop mode.

TIMING REGISTER (TIM1/2)

Tables 31 through 35 contain the Timing Register information. The TIM register is composed of two sub registers:

- TIM1—Controls the watchdog timing selection as well as either the watchdog window or the watchdog timeout option (Figure 28 and Figure 29, respectively). TIM1 is selected when bit D3 is 0 (Table 31). Watchdog timing characteristics are described in Table 32.
- TIM2—Selects an appropriate timing for sensing the wake-up circuitry or cyclically supplying devices by switching the HS on or off. TIM2 is selected when bit D3 is 1 (Table 33). Figure 30, page 54, describes HS operation when cyclic sense is selected Cyclic sense timing characteristics are described in Table 35, page 54.

Both subregisters also report the CANL and TXD diagnostics.

Table 31. TIM1 Timing and CANL Failure Diagnostic Register

TIM1	R/W	D3	D2	D1	D0
$101b	W	0	WDW	WDT1	WDT0
	R	CANL2VDD	CANL2BAT	CANL2GND	TXPD
Reset Value	–	–	0	0	0
Reset Condition (Write)(63)	–	–	POR, RESET	POR, RESET	POR, RESET

Notes

63. See Table 13, page 46, for definitions of reset conditions.

Table 32. TIM1 Control Bits

WDW	WDT1	WDT0	Timing (ms typ)	Parameter	Description
0	0	0	9.75	Watchdog Period 1	No Window Watchdog
0	0	1	45	Watchdog Period 2	
0	1	0	100	Watchdog Period 3	
0	1	1	350	Watchdog Period 4	
1	0	0	9.75	Watchdog Period 1	Watchdog Window enabled (Window length is half the Watchdog Timing).
1	0	1	45	Watchdog Period 2	
1	1	0	100	Watchdog Period 3	
1	1	1	350	Watchdog Period 4	

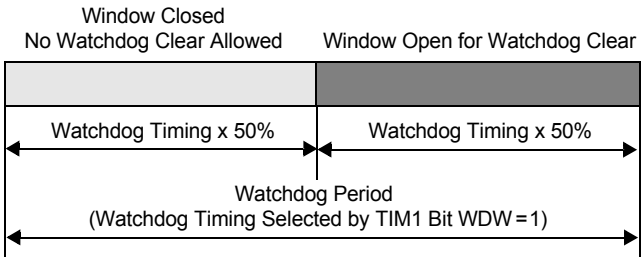


Figure 28. Window Watchdog

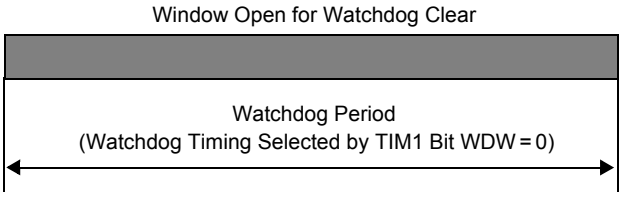


Figure 29. Timeout Watchdog

Table 33. Timing Register Status Bits

Name	Logic	Failure Description
CANL2VDD	0	No CANL short to VDD.
	1	CANL short to VDD.
CANL2BAT	0	No CANL short to VSUP.
	1	CANL short to VSUP.
CANL2GND	0	No CANL short to GND.
	1	CANL short to GND.
TXPD	0	No TXD dominant.
	1	TXD dominant.

Table 34. TIM2 Timing and CANL Failure Diagnostic Register

TIM2	R/W	D3	D2	D1	D0
$101b	W	1	CSP2	CSP1	CSP0
	R	CANL2VDD	CANL2BAT	CANL2GND	TXPD
Reset Value	–	–	0	0	0
Reset Condition (Write)(64)	–	–	POR, RESET	POR, RESET	POR, RESET

Notes
64. See Table 13, page 46, for definitions of reset conditions.

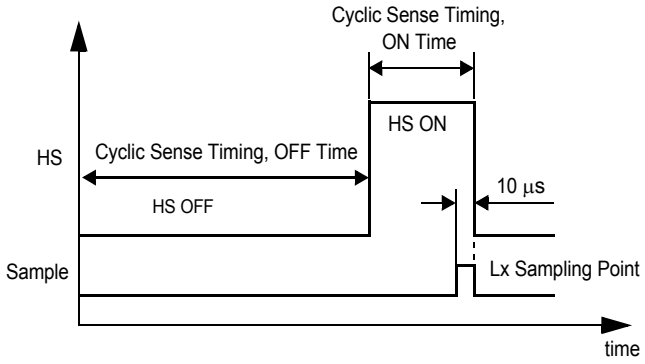


Figure 30. HS Operation When Cyclic Sense Is Selected

Table 35. TIM2 Control Bits

CSP2	CSP1	CSP0	Cyclic Sense Timing (ms)	Parameter
0	0	0	4.6	Cyclic Sense/FWU Timing 1
0	0	1	9.25	Cyclic Sense/FWU Timing 2
0	1	0	18.5	Cyclic Sense/FWU Timing 3
0	1	1	37	Cyclic Sense/FWU Timing 4
1	0	0	74	Cyclic Sense/FWU Timing 5
1	0	1	95.5	Cyclic Sense/FWU Timing 6
1	1	0	191	Cyclic Sense/FWU Timing 7
1	1	1	388	Cyclic Sense/FWU Timing 8

LOW POWER CONTROL REGISTER (LPC)

Tables 36 through 40 contain the Low Power Control Register information. The LPC register controls:

- The state of HS in Stop and Sleep modes (HS permanently OFF or HS cyclic).
- Enable or disable of the forced wake-up function (SBC automatic wake-up after time spent in Sleep or Stop modes; time is defined by the TIM2 sub register).
- Enable or disable the sense of the wake-up inputs (Lx) at the sampling point of the Cyclic Sense period (LX2HS bit). (Refer to Reset Control Register (RCR) on page 49 for details of the LPC register setup required for proper cyclic sense or direct wake-up operation.

The LPC register also reports the CANH and RXD diagnostic.

Table 36. Low Power Control Register

LPC	R/W	D3	D2	D1	D0
$110b	W	LX2HS	FWU	CAN-INT	HSAUTO
	R	CANH2VDD	CANH2BAT	CANH2GND	RXPR
Reset Value	–	0	0	0	0
Reset Condition (Write)(65)	–	POR, NR2R, N2R, STB2R, STO2R	POR, NR2R, N2R, STB2R, STO2R	POR, NR2R, N2R, STB2R, STO2R	POR, NR2R, N2R, STB2R, STO2R

Notes
65. See Table 13, page 46, for definitions of reset conditions.

Table 37. LX2HS Control Bits

Logic	Wake-up Inputs Supplied by HS
0	No.
1	Yes. Lx inputs sensed at sampling point.

Table 38. HSAUTO Control Bits

Logic	Auto-timing HS in Sleep and Stop modes
0	OFF.
1	ON, HS Cyclic, period defined in TIM2 subregister.

Table 39. CAN-INT Control Bits

Logic(66)	Description
0	Interrupt as soon as CAN bus failure detected.
1	Interrupt when CAN bus failure detected and fully identified.

Notes
66. If CAN-INT is at logic [0], any undetermined CAN failure will be latched in the CAN register (bit D1: CAN-UF) and can be accessed by SPI (refer to CAN Register (CAN) on page 49). After reading the CAN register or setting CAN-INT to logic [1], it will be cleared automatically. The existence of CAN-UF always has priority over clearing, meaning that a further undetermined CAN failure does not allow clearing the CAN-UF bit.

Table 40. LPC Status Bits

Name	Logic	Failure Description
CANH2VDD	0	No CANH short to V_{DD}.
	1	CANH short to V_{DD}.
CANH2BAT	0	No CANH short to VSUP.
	1	CANH short to VSUP.
CANH2GND	0	No CANH short to GND.
	1	CANH short to GND.
RXPR	0	No RXD permanent recessive.
	1	RXD permanent recessive.

INTERRUPT REGISTER (INTR)

Tables 41 through 43 contain the Interrupt Register information. The INTR register allows masking or enabling the interrupt source. A read operation identifies the interrupt source. Table 43 provides status bit information. The status bits of the INTR register content are copies of the IOR, CAN, TIM, and LPC registers status content. To clear the Interrupt Register bits, the IOR, CAN, TIM, and/or LPC registers must be cleared (read register) and the recovery condition must occur. Errors bits are latched in the CAN register and the IOR register.

Table 41. Interrupt Register

INTR	R/W	D3	D2	D1	D0
$111b	W	VSUPLOW	HSOT-V2LOW(67)	V1TEMP	CANF
	R	VSUPLOW	HSOT	V1TEMP	CANF
Reset Value	–	0	0	0	0
Reset Condition (Write)(68)	–	POR, RST	POR, RST	POR, RST	POR, RST

Notes
67. If only HSOT-V2LOW interrupt is selected (only bit D2 set in INTR register), reading INTR register bit D2 leads to two possibilities:
1. Bit D2 = 1: Interrupt source is HSOT.
2. Bit D2 = 0: Interrupt source is V2LOW.
HSOT and V2LOW bits status are available in the IOR register.
68. See Table 13, page 46, for definitions of reset conditions.

Table 42. Interrupt Register Control Bits

Name	Description
CANF	Mask bit for CAN failures.
VDDTEMP	Mask bit for VDD medium temperature (pre-warning).
HSOT-V2LOW	Mask bit for HS over-temperature AND V_{2LTH} < 4.0 V.
VSUPLOW	Mask bit for $V_{BF(EW)}$ < 5.8 V.

When the mask bit is set, the $\overline{INT}$ pin goes LOW if the appropriate condition occurs. Upon a wake-up condition from Stop mode due to over-current detection ($I_{DDS-WU1}$ or $I_{DDS-WU2}$), an $\overline{INT}$ pulse is generated; however, INTR register content remains at 0000 (not bit set into the INTR register).

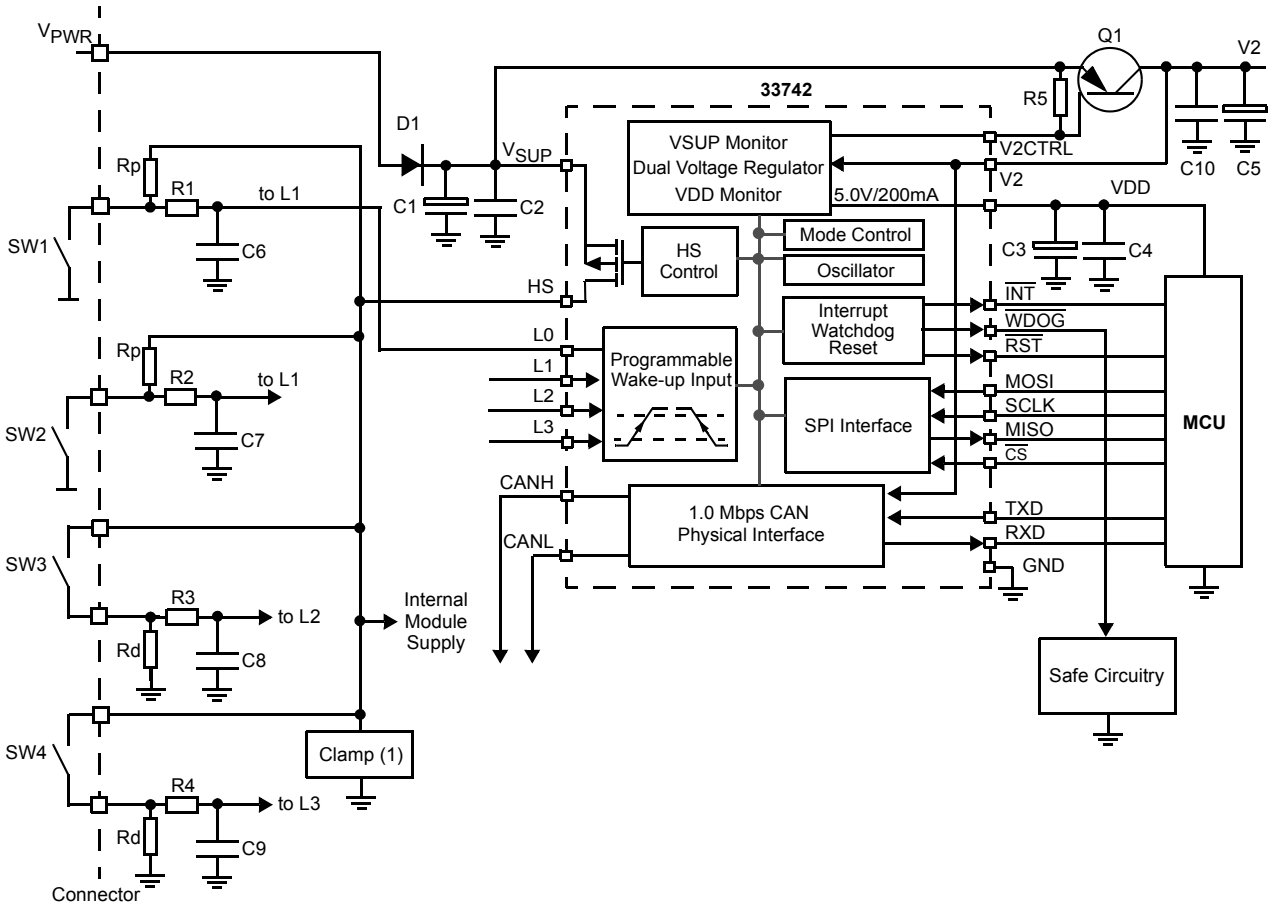
Table 43. Interrupt Register Status Bits

Name	Logic	Description
VSUPLOW	0	No $V_{BF(EW)}$ < 5.8 V.
	1	$V_{BF(EW)}$ < 5.8 V.
HSOT	0	No HS over-temperature.
	1	HS over-temperature.
VDDTEMP	0	No VDD medium temperature (pre-warning).
	1	VDD medium temperature (pre-warning).
CANF	0	No CAN failure.
	1	CAN failure.

TYPICAL APPLICATIONS

SBC POWER SUPPLY

The 33742 is supplied from the battery line. A serial diode is necessary to protect the device against negative transient pulses and from reverse battery. This is illustrated in Figure 31.



Legend
D1: Example: 1N4002 type
Q1: MJD32C
R1, R2, R3, R4: 10kΩ
Rp, Rd: Example: 1.0kΩ depending on switch type.
R5: 2.2 kΩ
C1: 10 μF
C2: 100 nF
C3: 47 μF
C4: 100 nF
C5: 47 μF tantalum or 100 μF chemical
C6, C7, C8, C9, C10: 100 nF
(1) Clamp circuit to ensure max ratings for HS (HS from -0.3V to V_{SUP} + 0.3) are respected.

Figure 31. SBC Typical Application Schematic

VOLTAGE REGULATOR

The SBC contains two 5.0 V regulators: a V1 regulator, fully integrated and protected, and a V2 regulator, which operates with an external ballast transistor.

VDD REGULATOR

The VDD regulator provides 5.0 V output, 2.0% accuracy with current capability of 200 mA max. It requires external decoupling and stabilizing capacitors. The minimum recommended values are as follows:

- C4: 100 nF
- C3: 10 µF < C3 <22 µF, ESR < 1.0 Ω or
- C3: 22 µF < C3 <47 µF, ESR < 5.0 Ω or
- C3: ≥47 µF, ESR < 10 Ω

V2 REGULATOR: OPERATING WITH EXTERNAL BALLAST TRANSISTOR

The V2 regulator is a tracking regulator of the VDD output. Its accuracy relative to VDD is ±1.0%. It requires external decoupling and stabilizing capacitors.

The recommended value are as follows:

- 22 µF, ESR < 5.0 Ω
- 47 µF, ESR < 10 Ω

The V2 pin has two functions: it is a sense input for the V2 regulator and is a 5.0 V power supply input to the CAN interface.

With respect to ballast transistor selection, either PNP or PMOS transistors may be used. A resistor between base and emitter (or source and drain) is necessary to ensure proper operation and optimized performances. Recommended bipolar transistor is MJD32C.

V2 REGULATOR: OPERATION WITHOUT BALLAST TRANSISTOR

The external ballast transistor is optional. If the application does not requires more than the maximum output current capability of the VDD regulator, then the ballast transistor can be omitted. The thermal aspects must be analyzed as well.

The electrical connection is illustrated in Figure 32.

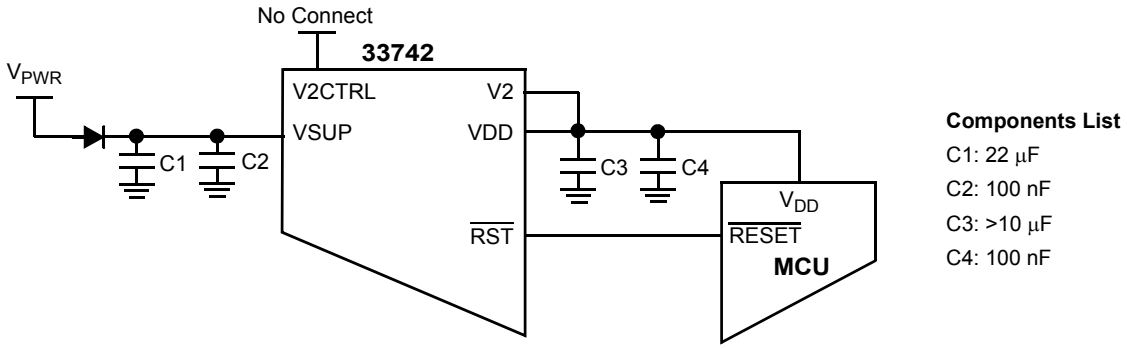


Figure 32. V2 Regulator Electrical Connection

FAILURE ON VDD, WDOG, RESET, AND INT PINS

The paragraphs below describe the behavior of the device and of the INT, RST, and WDOG pins at power-up and under failure of the VDD regulator.

POWER-UP AND SBC ENTERING NORMAL OPERATION

After power-up the 33742 enters Normal Request mode (CAN interface is in TXRX mode): VDD is on and V2 is off.

After 350 ms if no watchdog is written (no TIM1 register write), a reset occurs and the 33742 returns to Normal Request mode. During this sequence WDOG is active (low level).

Once watchdog is written, the 33742 goes to Normal mode: VDD is still on and V2 turns on, WDOG is no longer active, and the RST pin is HIGH. If watchdog is not refreshed, the 33742 generates a reset and returns to Normal Request mode. Figure 33, illustrates the operation.

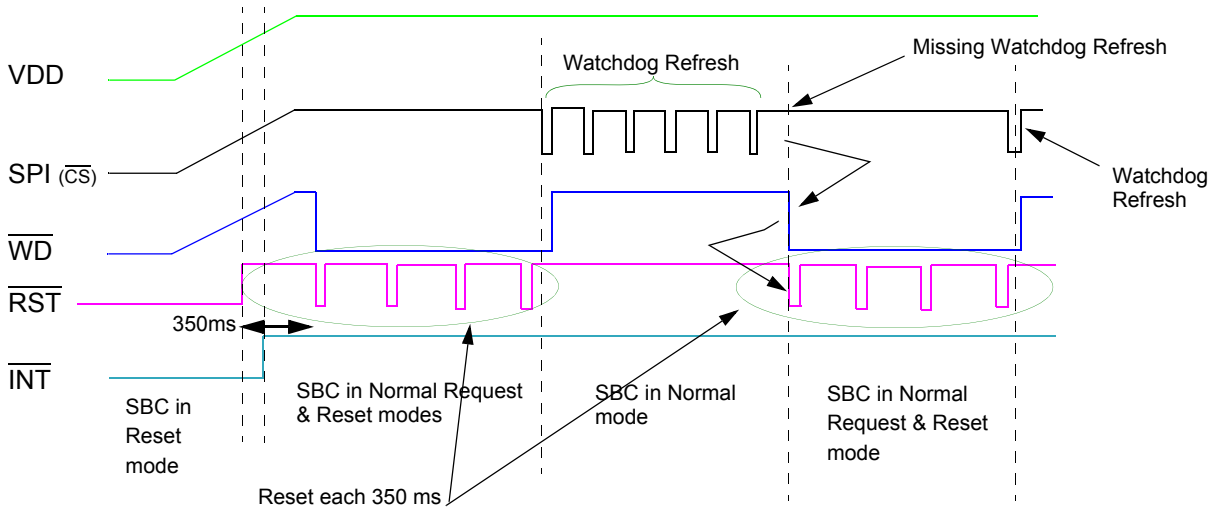


Figure 33. Power up sequence, No W/D write at first

POWER UP AND VDD GOING LOW WITH STOP MODE AS DEFAULT LOW POWER MODE IS SELECTED

The first part of Figure 34 is identical to Figure 33. If VDD is pulled below VDD under-voltage reset (typ 4.6 V), say by an over-current or short-circuit (for instance, short to 4.0 V), and if a low power mode previously selected was Stop mode, the 33742 enters Reset mode ($\overline{RST}$ pin is active). The $\overline{WDOG}$ pin stays HIGH, but the high level (Voh) follows V1 level. The $\overline{INT}$ pin goes LOW.

When the VDD overload condition is removed, the 33742 restarts in Normal Request mode.

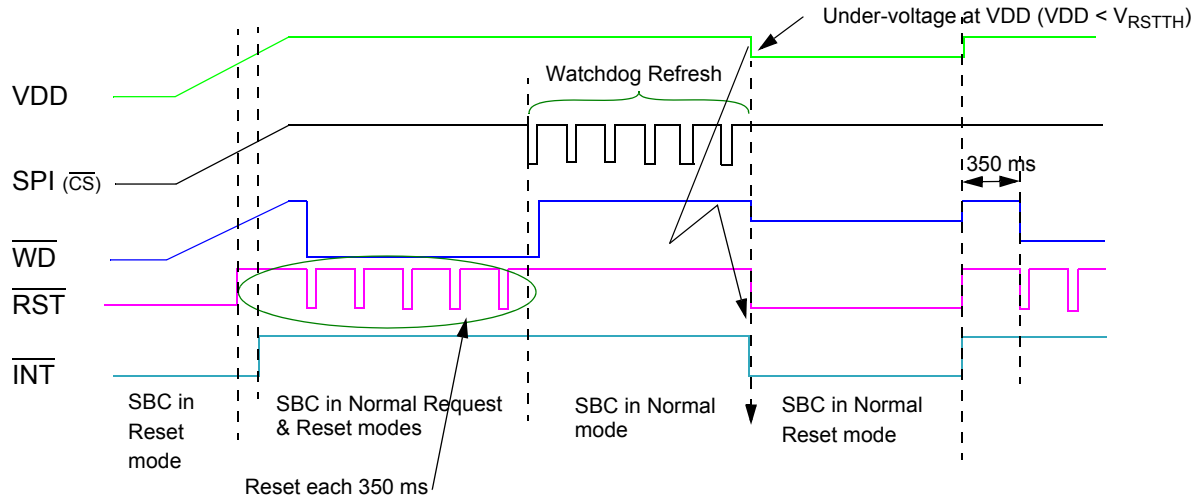


Figure 34. Under-voltage on VDD

POWER-UP AND VDD GOING LOW WITH SLEEP MODE AS DEFAULT LOW POWER MODE IS SELECTED

The first part of Figure 35 is identical to Figure 34. If VDD is pulled below the VDD under-voltage reset (typ 4.6 V), say by an over-current or short-circuit (for instance, short to 4.0 V), and if the low power mode previously selected was Sleep mode and if the BATFAIL flag has been cleared, the 33742 enters in Reset mode for a time period of 100 ms. The WDOG pin stays HIGH, but the high level (VOH) follows VDD level. The RST and INT pins are low. After 100 ms the 33742 goes into Sleep mode, and the VDD and V2 are off.

Figure 35 shows an example wherein VDD is shorted to 4.0 V, and after 100 ms the 33742 enters Sleep mode.

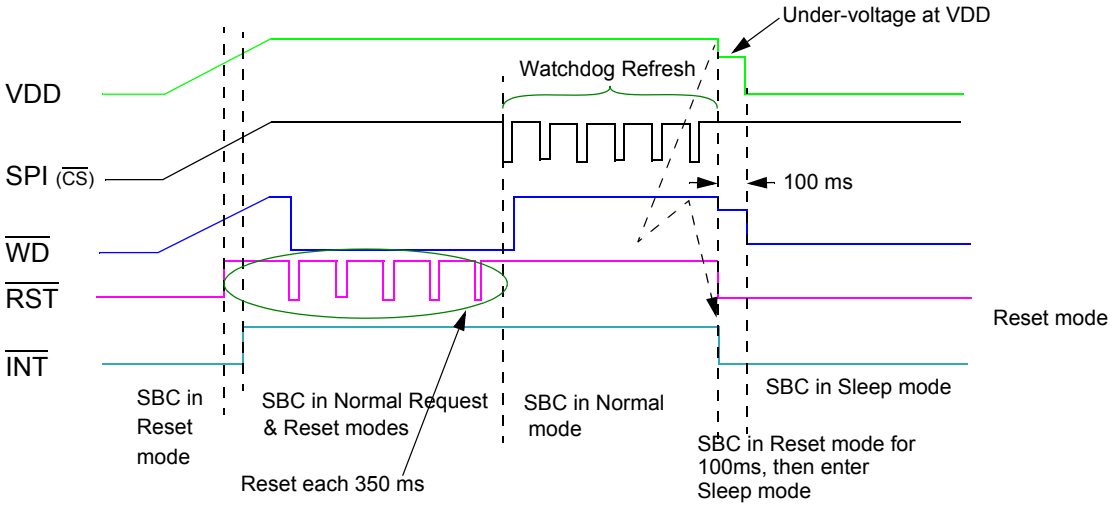
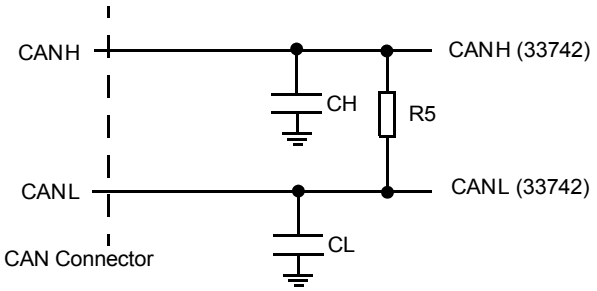
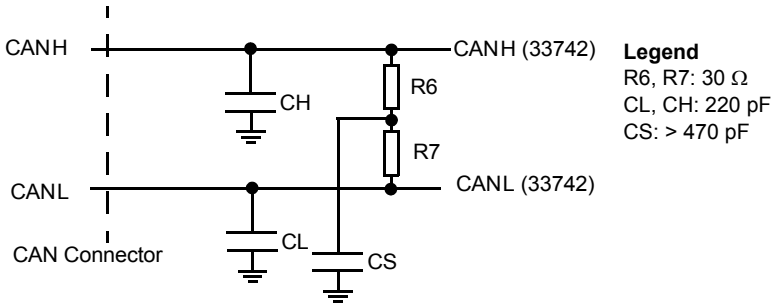


Figure 35. Under-voltage at VDD. Sleep mode selected.



Legend
R5: 60 Ω
CL, CH: 220 pF

Figure 36. CAN Bus Standard Termination



Legend
R6, R7: 30 Ω
CL, CH: 220 pF
CS: > 470 pF

Figure 37. CAN Bus Split Termination

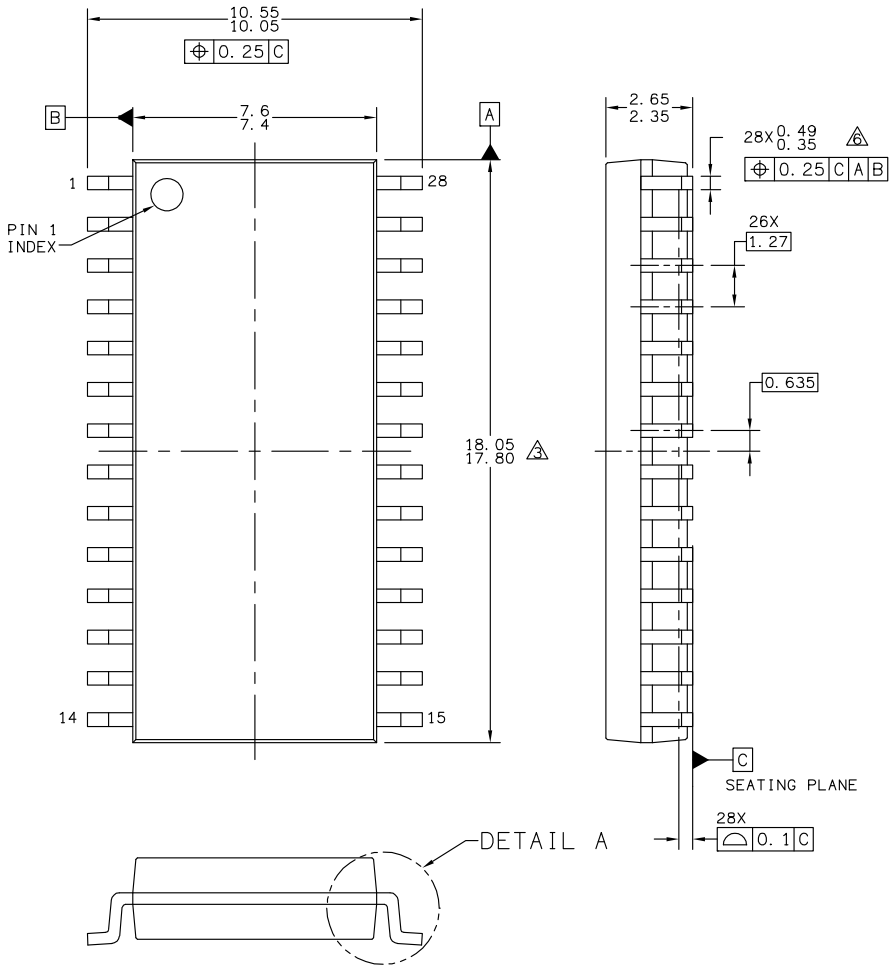
PACKAGING

PACKAGE AND THERMAL CONSIDERATIONS

The 33742 SBC is a standard surface mount 28-pin SOIC wide body. In order to improve the thermal performances of the SOIC package, eight of the 28 pins are internally connected to the package lead frame for heat transfer to the printed circuit board.

PACKAGING DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and perform a keyword search on the 98ASB42345B drawing number below. Dimensions shown are provided for reference ONLY.



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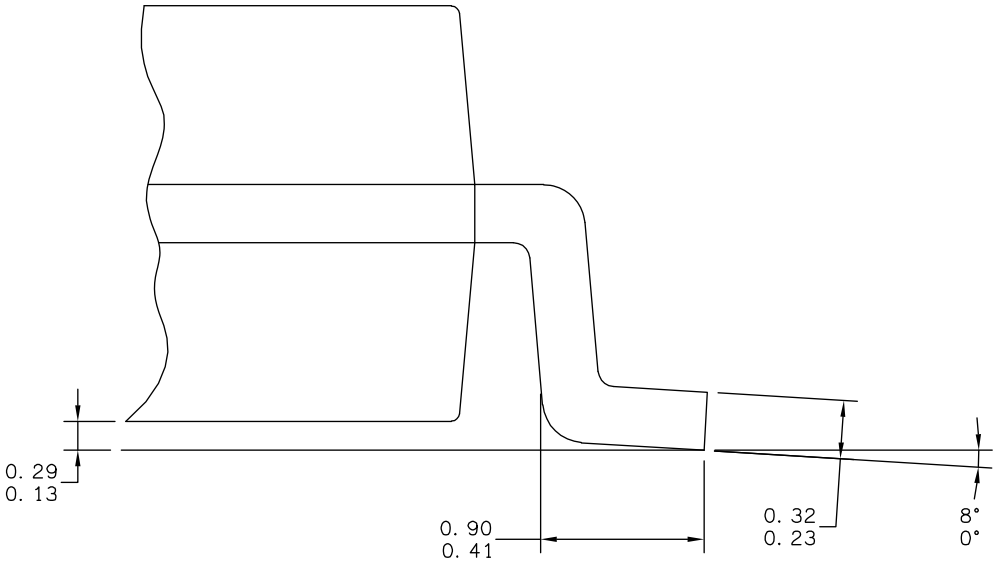
TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	



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TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. 751F–01 THRU –04 OBSOLETE. NEW STANDARD: 751F–05
5. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

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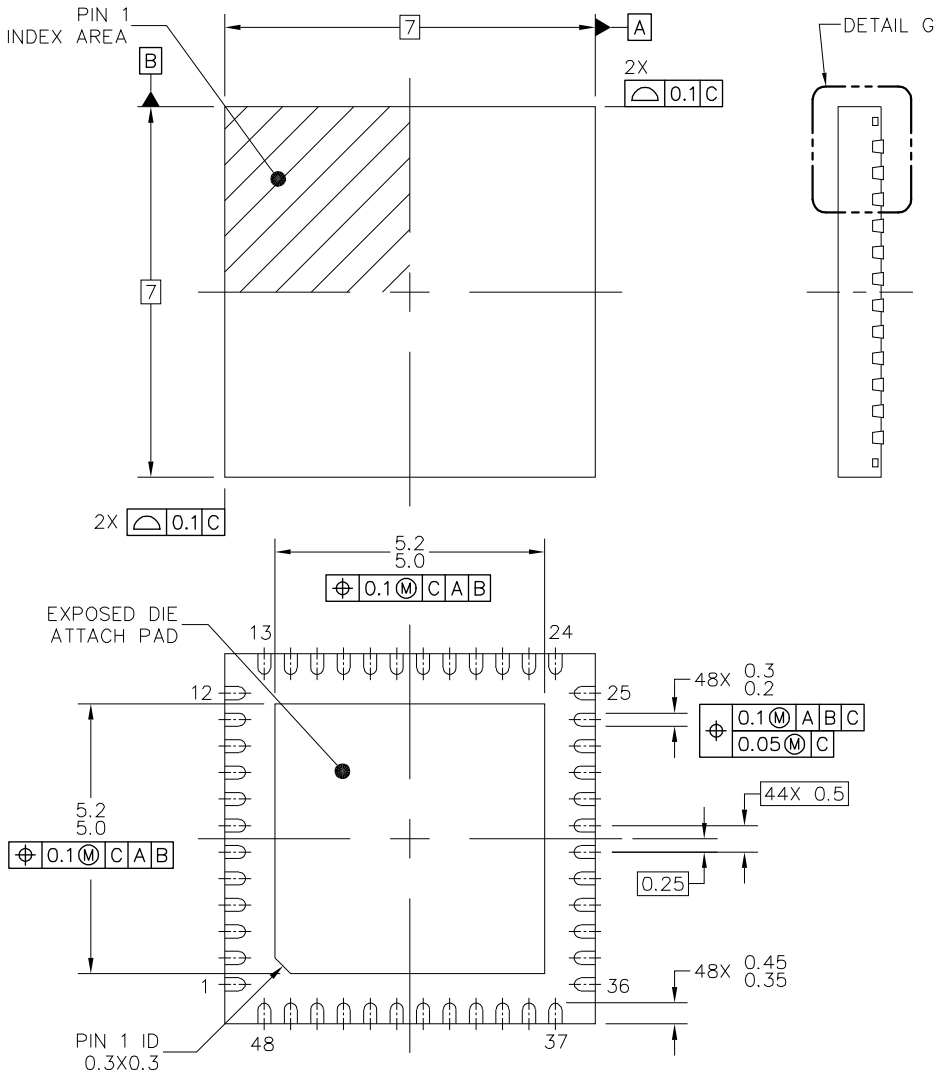
TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F–05	10 MAR 2005
	STANDARD: MS–013AE	

33742



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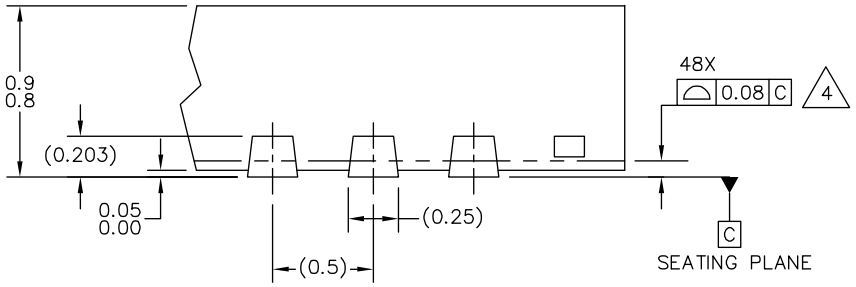
TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00757D	REV: O
	STANDARD: NON-JEDEC	
	28 MAY 2014	



DETAIL G
VIEW ROTATED 90°CW

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TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00757D	REV: O
	STANDARD: NON-JEDEC	
	28 MAY 2014	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH FLAG.
5. MIN METAL GAP SHOULD BE 0.2 MM.

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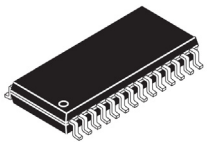
TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL	DOCUMENT NO: 98ASA00757D	REV: O
	STANDARD: NON–JEDEC	
	28 MAY 2014	

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 2.0)

33742SOICW

28-PIN SOICW



EG SUFFIX (PB-FREE)
98ASB42345B
28-PIN SOICW

Note For package dimensions, refer to 98ASB42345B.

Introduction

This thermal addendum is provided as a supplement to the MC33742 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the data sheet.

Packaging and Thermal Considerations

The MC33742 is offered in a 28 pin SOICW exposed pad, single die package. There is a single heat source (P), a single junction temperature (T_J), and thermal resistance ($R_{\theta JA}$).

$$\{ T_J \} = [R_{\theta JA}] \cdot \{ P \}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 44. Thermal Performance Comparison

Thermal Resistance	[°C/W]
$R_{\theta JA}$ (1), (2)	41
$R_{\theta JB}$ (2), (3)	10
$R_{\theta JA}$ (1), (4)	68
$R_{\theta JC}$ (5)	220

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
4. Single layer thermal test board per JEDEC JESD51-3.
5. Thermal resistance between the die junction and the package top surface; cold plate attached to the package top surface and remaining surfaces insulated.

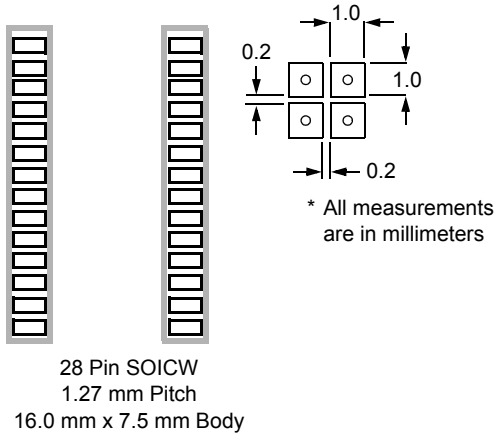


Figure 38. Surface Mount for SOIC Wide Body non-Exposed Pad

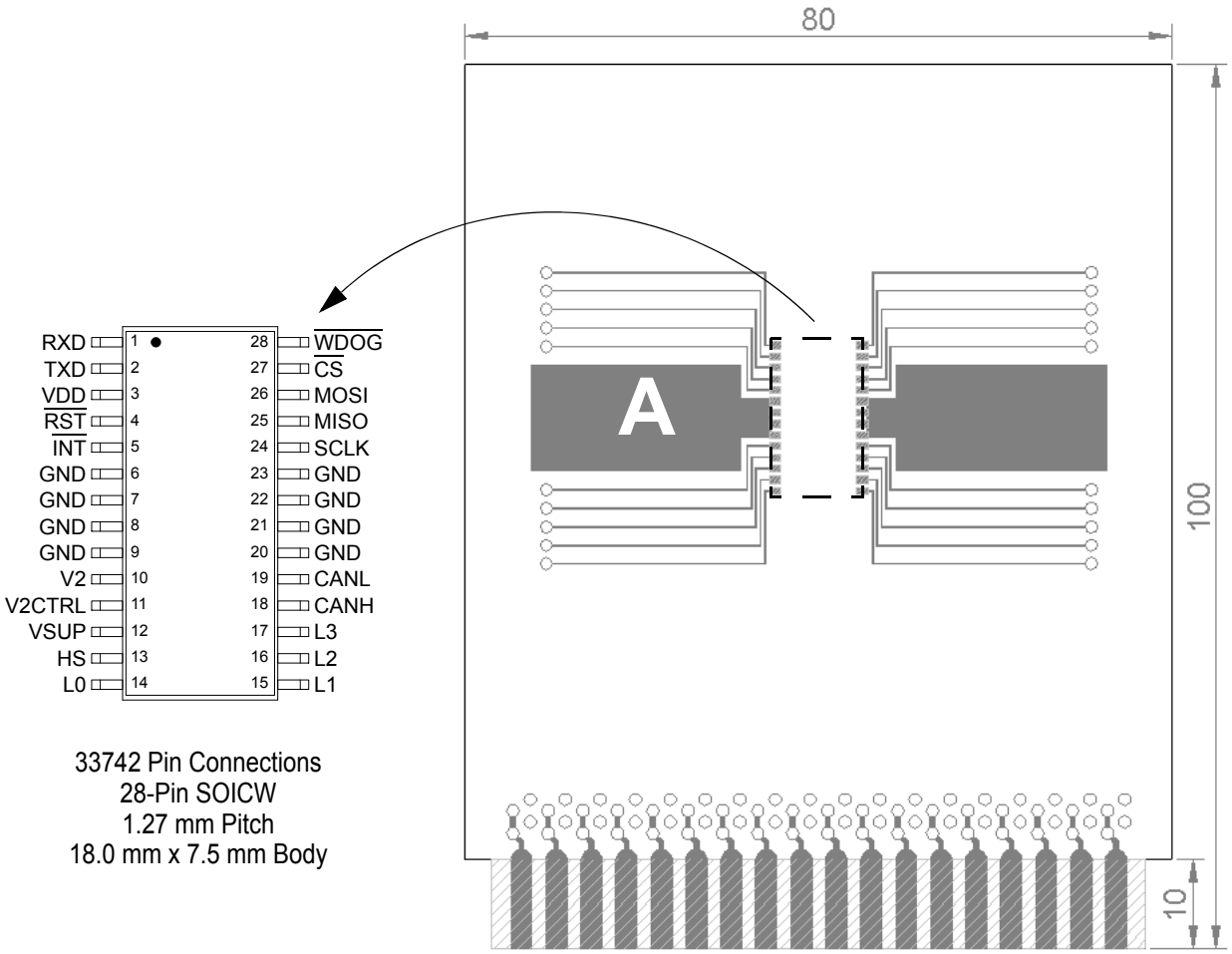


Figure 39. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 45. Thermal Resistance Performance

A [mm²]	$R_{\theta JA}$ [°C/W]
0	68
300	52
600	47

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

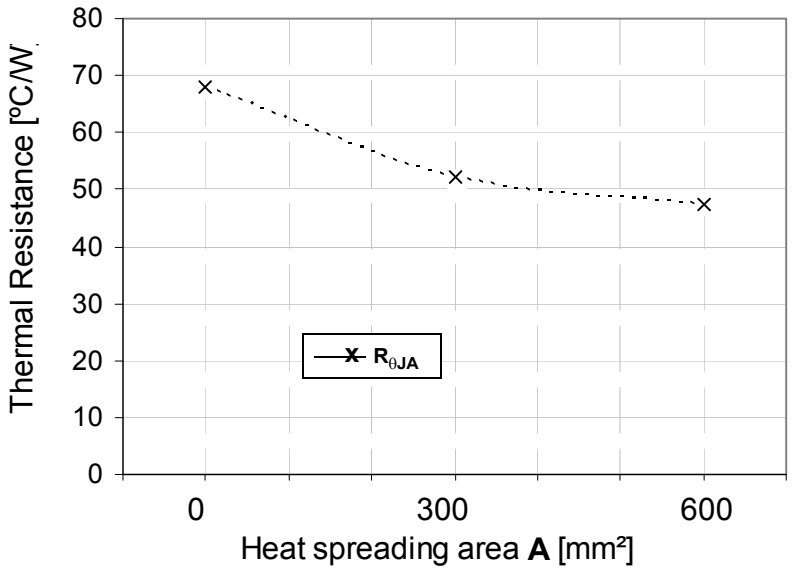


Figure 40. Device on Thermal Test Board $R_{\theta JA}$

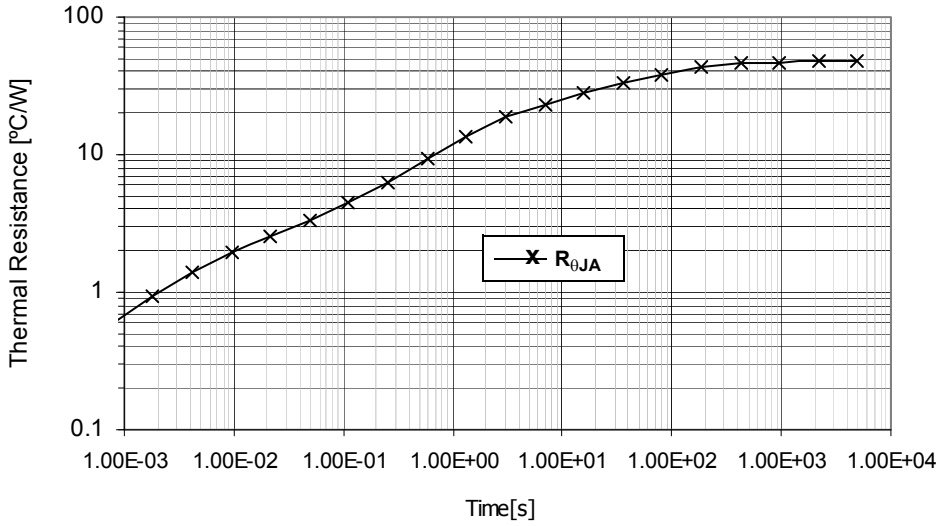


Figure 41. Transient Thermal Resistance $R_{\theta JA}$,
1 W Step response, Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3	2/2006	• Converted to Freescale format • Implemented Revision History page
4	6/2006	• Added Thermal Addendum (Rev. 1.0) • Changed Data Sheet from “Advanced” to “Final”
5	8/2006	• Added MCZ33742EG/R2 and MCZ33742SEG/R2 to the Ordering Information block
6	8/2006	• Replaced label for Logic Inputs to Logic Signals (RXD, TXD, MOSI, MISO, CS, SCLK, RST, WDOG, and INT) on page 7
7	10/2006	• Removed all references to the 54 pin package. • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 7. Added note with instructions from www.freescale.com.
8	2/2007	• Revised () and (), • Restated notes in Maximum Ratings on page 7
9	3/2007	• Text corrections to the included thermal addendum
10	5/2007	• Added EP 48 pin QFN package • Added 98ARH99048A Package drawing • Added PCZ33742EP/R2 to the ordering information
11	6/2008	• Made changes defining RXD as a push-pull structure on page 15, 22, 38, and 39 • Updated figures Figure 12 and Figure 25 • Added provisions of differentiation for 28-pin SOIC and 48-pin QFN for ESD Capability, Human Body Model(1) on page 7, Watchdog Period Normal and Standby Modes on page 17, and Normal Request Mode Timeout on page 17 • Update the Freescale format and style to the current standards • Added the Functional Internal Block Description section • Changed PCZ33742EP/R2 to MC33742EP/R2 in the ordering information
12.0	2/2011	• Added MC33742PEG/R2, MC33742SPEG/R2, and MC33742PEP/R2 to the ordering information
13.0	7/2011	• Updated Freescale form and style • Removed MCZ33742EG/R2, MC33742SDW/R2, MCZ33742SEG/R2, and MCZ33742EP/R2 from the ordering information
14.0	6/2013	• Added a For SPI Operation on page 47 • Updated document properties
15.0	12/2014	• Updated case outline (changed 98ASA10825D to 98ASA00757D) as per PCN 16557

RoHS

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