CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7261
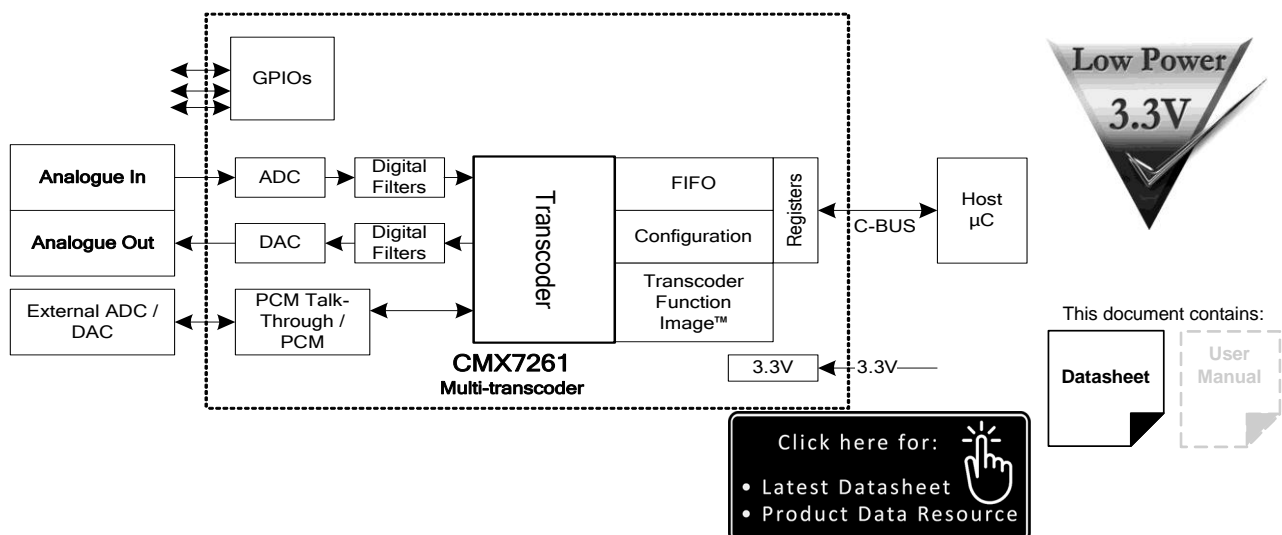# Multi-transcoder

DATASHEET

7261 FI-1.x Multi-transcoder

Features

- Half-duplex operation
- Full-duplex operation
- Multiple codec support:
  - PCM (linear, µ-law, A-law), CVSD and G.729A codecs
- Multiple transcoding support:
  - PCM to CVSD and reverse
  - PCM to G.729A and reverse
  - CVSD to G.729A and reverse
  - PCM µ/A/linear to PCM µ/A/linear transcoder
- No external DSP or codecs required: simply upload Function Image™ (FI)
- Transcoder routing:
  - Choice of input sources – C-BUS transfer to host, external PCM device/codec, analogue audio input
  - Choice of output sources – C-BUS transfer to host, external PCM device/codec, analogue audio output
- Voice activity detection

- C-BUS host serial interface
  - SPI-like with register addressing
  - Read/Write 128-byte FIFOs and data buffers to streamline transfers and relax host service latency
- Auxiliary functions
  - Three GPIOs
  - Analogue input/output gain adjustment
  - Analogue input multiplexer
  - Analogue output multiplexer
- Master/Slave PCM serial interface
  - For external audio CODEC
- Low power 3.3V operation with powersave functions
- Small 64-pin VQFN/LQFP package

Applications

- Half duplex digital radio systems
- Full duplex digital radio systems
- Personal area network voice links
- Privacy-type digital voice communications
- Wireless PBX
- VoIP applications
- Digital Software Defined Radio (SDR)

1   Brief Description

The CMX7261 Multi-transcoder IC is a device supporting multiple speech codecs in a single chip. The CMX7261 is capable of encoding analogue voice into PCM (linear, μ-law or A-law), CVSD or G.729A data formats. It is capable of decoding PCM, CVSD and G.729A back to analogue voice. It can also transcode data between PCM, CVSD and G.729A.

Input and output signals may be passed through the C-BUS interface, the PCM port or the on-chip convertors (ADC/DAC).

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™ data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from a host μC over the C-BUS serial interface or from an external memory device. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

The CMX7261 operates from a 3.3V supply and includes selectable powersaving modes. It is available in a 64-VQFN (Q1) or a 64-LQFP (L9) package.

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

This Data Sheet is the first part of a two-part document.

CONTENTS

Information in this data sheet should not be relied upon for final product design. It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

1.1   History

Version	Changes	Date
9	• Added availability of L9 package	13/3/12
8	• Added analogue input multiplexer. • Updated analogue output multiplexer. • Added differential speaker driver output. • Added single ended analogue input. • Added independent coarse gain control for ANAOUT, MONOUT and SPKR. • Added Reg Done Select register to provide host handshake. • Added programming register to enable/disable GPIO bus-hold function. • Added programming register to enable/disable core voltage regulator. • Updated C-BUS Timing information to show C-BUS usage at 10MHz clock speed.	7/12/11
7	• Advice in section 5.6 greyed out as not implemented in current FI.	22/08/11
6	• Added advice about terminating unconnected GPIO pins in section 5.6	17/08/11
5	• Updated G.729A current consumption figures, to reflect optimisations done on the G.729A algorithm. • Documented the SSOUT0 pin which is used when booting from external serial memory. This pin replaces GPIOD.	27/07/11
4	• Removed the BOOTEN1,2 = 00 reset mechanism as it could be unreliable	08/04/11

3	• Added CVSD 32kbps mode.	08/03/11
	• Added independent fine gain control and fade in/out for both the audio channels, in full duplex mode.	
	• Renamed bit-1 of ANAIN Config - $B0 register to 'ANAIN DrvPwr', in order to differentiate it from bit-11.	
	• Changed anti-alias filter component to a standard value in Fig 7, section 5.3.2.	
	• Removed rows 4 and 8 and deleted the "Activation Block" column in Table 5.	
	• Added DVdd connection to pin 5 in Figure 3.	
2	• Added full duplex operation.	21/01/11
1	• First approved version	20/08/10

2   Block Diagrams

2.1   Half Duplex Transcoder
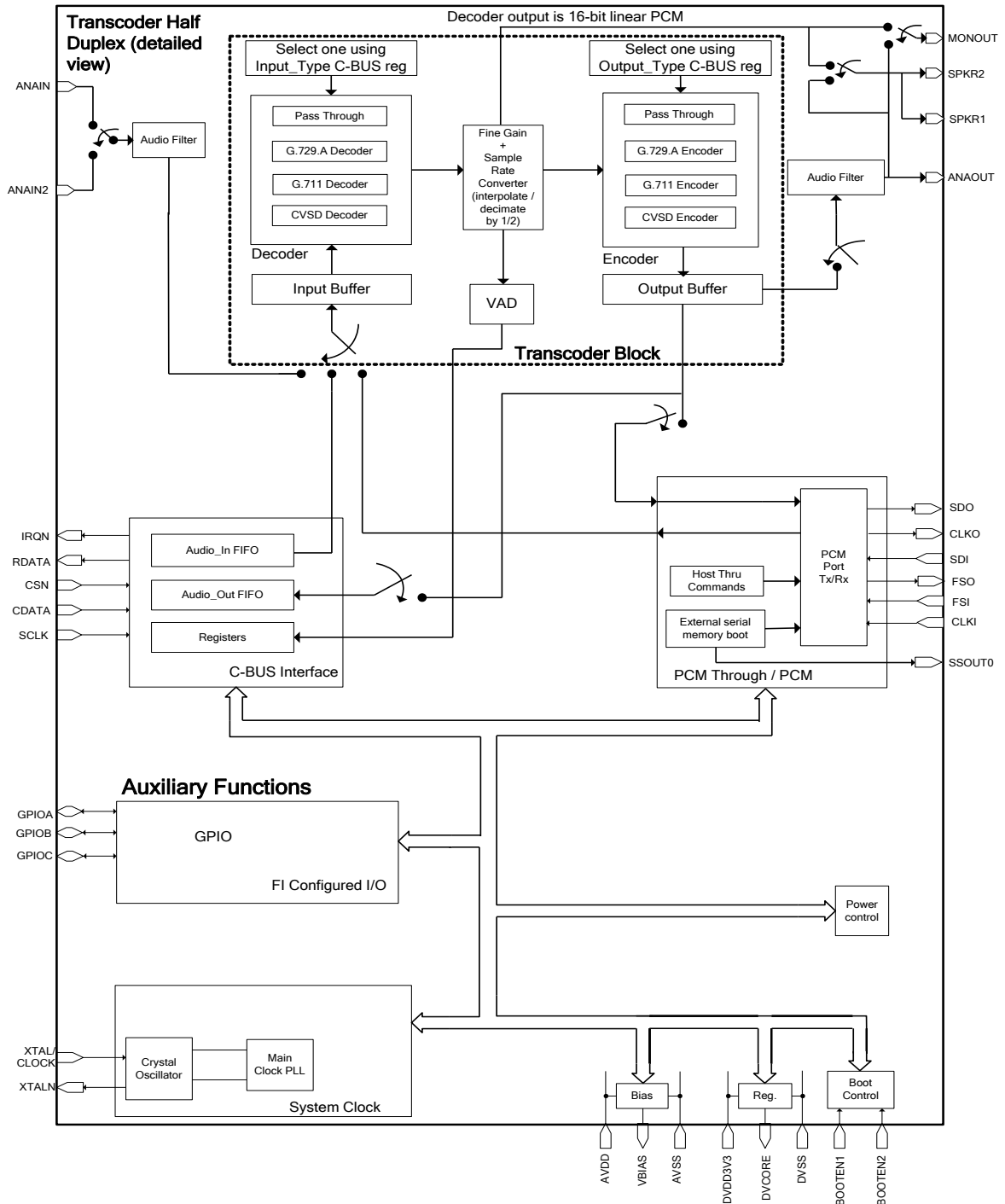
Figure 1 Block Diagram

Figure 1 presents a detailed view of the CMX7261, as used in half duplex mode. In Figure 1, the Decoder, Sample Rate Convertor, Voice Activity Detector (VAD) and the Encoder together form a 'Transcoder

Block'. The CMX7261 contains two such 'Transcoder Blocks' (Figure 1 shows only one of them). In full duplex mode both Transcoder Blocks are used, whereas in half duplex mode only one Transcoder Block is used.

2.2   Full Duplex Transcoder

Figure 2 depicts a block level overview of full duplex transcoding operation. Full duplex operation means that a type of transcoding may be specified on one channel, and the opposite transcoding will then be implemented on a second audio stream.

For example, if channel-1 is set to transcode from CVSD to G.729A, channel-2 will transcode from G.729A to CVSD.
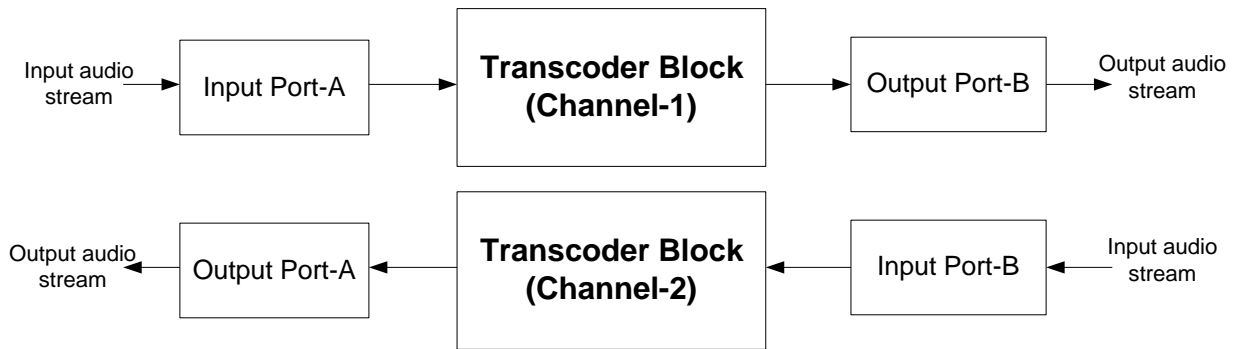
Figure 2 Full Duplex Block Diagram

In full duplex operation, the input and output ports may be specified on one channel and the opposite input and output ports will be used for the second channel.

Table 1 shows the mapping between Input Ports and Output Ports.

Table 1 Input and Output Ports – Full Duplex Mapping

Input Port-A / B	← maps to →	Output Port-A / B
Analogue In		Analogue Out
Audio In FIFO (C-BUS In)		Audio Out FIFO (C-BUS Out)
PCM Port In		PCM Port Out

For example, if channel-1 input port is set to Analogue In and its output port set to Audio Out FIFO, then channel-2 input port will be Audio In FIFO and its output port will be Analogue Out.

3   Pin and Signal List

64-pin Q1/L9	Pin		Signal Description
Pin No.	Name	Type	
1	CLKI	IP	PCM: Serial Clock In.
2	BOOTEN1	IP+PD	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface.
3	BOOTEN2	IP+PD	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface.
4	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
5	DVDD3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the supply pins.
6	GPIOA	BI	General Purpose I/O.
7	RESETN	IP	Logic input used to reset the device (active low).
8	GPIOB	BI	General Purpose I/O.
9	GPIOC	BI	General Purpose I/O.
10	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
11	SPKR2	OP	Single ended output for speaker.
12	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
13	SPKR1VSS	PWR	Negative supply rail (ground) for the on-chip speaker driver circuit.
14	SKPR1P	OP	Low impedance differential driver to the external speaker; 'P' is positive, 'N' is negative. Together these are referred to as the SPKR1 output.
15	SPKR1N	OP	
16	SPKR1VDD	PWR	Positive supply rail for the on-chip speaker driver circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to SPKR1VSS by capacitors mounted close to the device pin.
17	ANAOUTP	OP	Differential outputs for main audio; 'P' is positive, 'N' is negative. Together these are referred to as ANAOUT.
18	ANAOUTN	OP	
19	MONOUTP	OP	Differential outputs for monitor audio; 'P' is positive, 'N' is negative. Together these are referred to as MONOUT.
20	MONOUTN	OP	
21	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits
22	DACREF		DAC reference voltage, connect to AVSS.

64-pin Q1/L9	Pin		Signal Description
Pin No.	Name	Type	
23	ANAIN2P	IP	Input (IP) and feedback (FB) connections to single ended audio input 2. Gain and filtering circuitry can be constructed around these pins. Together these are referred to as ANAIN2.
24	ANAIN2FB	OP	
25	NC	NC	Do not connect.
26	NC	NC	Do not connect.
27	VBIAS	OP	Internally generated bias voltage of approximately AVDD/2. If VBIAS is power saved this pin will present a high impedance to AVDD. This pin must be decoupled to AVSS by a capacitor mounted close to the device pins; no other connections should be made.
28	ANAINP	IP	Differential inputs for main audio; 'P' is positive, 'N' is negative. Together these are referred to as the ANAIN.
29	ANAINN	IP	
30	ADCREF		ADC reference voltage; connect to AVSS.
31	NC	NC	Do not connect.
32	NC	NC	Do not connect.
33	NC	NC	Do not connect.
34	NC	NC	Do not connect.
35	NC	NC	Do not connect.
36	NC	NC	Do not connect.
37	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
38	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits.
39	NC	NC	Do not connect.
40	NC	NC	Do not connect.
41	NC	NC	Do not connect.
42	NC	NC	Do not connect.
43	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
44	DVCORE1	PWR	Digital core supply, nominally 1.8V. By default this will be supplied by an on-chip regulator, although an option is available to use an external regulator. This pin should be decoupled to DVSS by capacitors mounted close to the device pins and connected with a power supply track to DVCORE2. For details see programming register P1.19 in section in 10.1.2 Program Block 1 – Clock Control.

64-pin Q1/L9	Pin		Signal Description
Pin No.	Name	Type	
45	DVDD3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the supply pins.
46	NC	NC	Do not connect.
47	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
48	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
49	XTALN	OP	Output of the on-chip xtal oscillator inverter.
50	XTAL/CLOCK	IP	Input to the oscillator inverter from the xtal circuit or external clock source.
51	NC	NC	Do not connect.
52	NC	NC	Do not connect.
53	SCLK	IP	C-BUS serial clock input from the µC.
54	RDATA	TS OP	3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
55	CDATA	IP	C-BUS serial data input from the µC.
56	CSN	IP	C-BUS chip select input from the µC.
57	IRQN	OP	'wire-Orable' output for connection to the Interrupt Request input of the µC. This output is pulled down to DVSS when active and is high impedance when inactive. An external pull-up resistor is required.
58	DVCORE2	PWR	Digital core supply, nominally 1.8V. Normally this will be supplied by the on-chip regulator, although an option is available to use an external regulator. This pin should be decoupled to DVSS by capacitors mounted close to the device pins and connected with a power supply track to DVCORE1. For details see programming register P1.19 in section in 10.1.2 Program Block 1 – Clock Control.
59	SDO	OP	*While booting FI:* SPI: Master Out Slave In (MOSI). *While running FI:* PCM: Serial Data Out.
60	FSO	OP	PCM: Frame Sync Out.
61	SDI	IP	*While booting FI:* SPI: Master In Slave Out (MISO). *While running FI:* PCM: Serial Data In.
62	SSOUT0	OP	SPI: Slave Select Out 0.
63	CLKO	OP	*While booting FI:* SPI: Serial Clock (SCLK). *While running FI:* PCM: Serial Clock Out.
64	FSI	BI	PCM: Frame Sync In.

Notes: IP = Input (+ PU/PD = internal pull-up / pull-down resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal

3.1   Signal Definitions

Table 2 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
DV_{DD3v3}	DVDD3V3	3.3V positive supply rail for the digital on-chip circuits
DV_{CORE}	DVCORE1, DVCORE2	Power for digital core voltage of approximately 1.8V
AV_{SS}	AVSS	Ground for all analogue circuits

4   PCB Layout Guidelines and Power Supply Decoupling

Digital Ground Plane

CMX7261Q1

Analogue Ground Plane
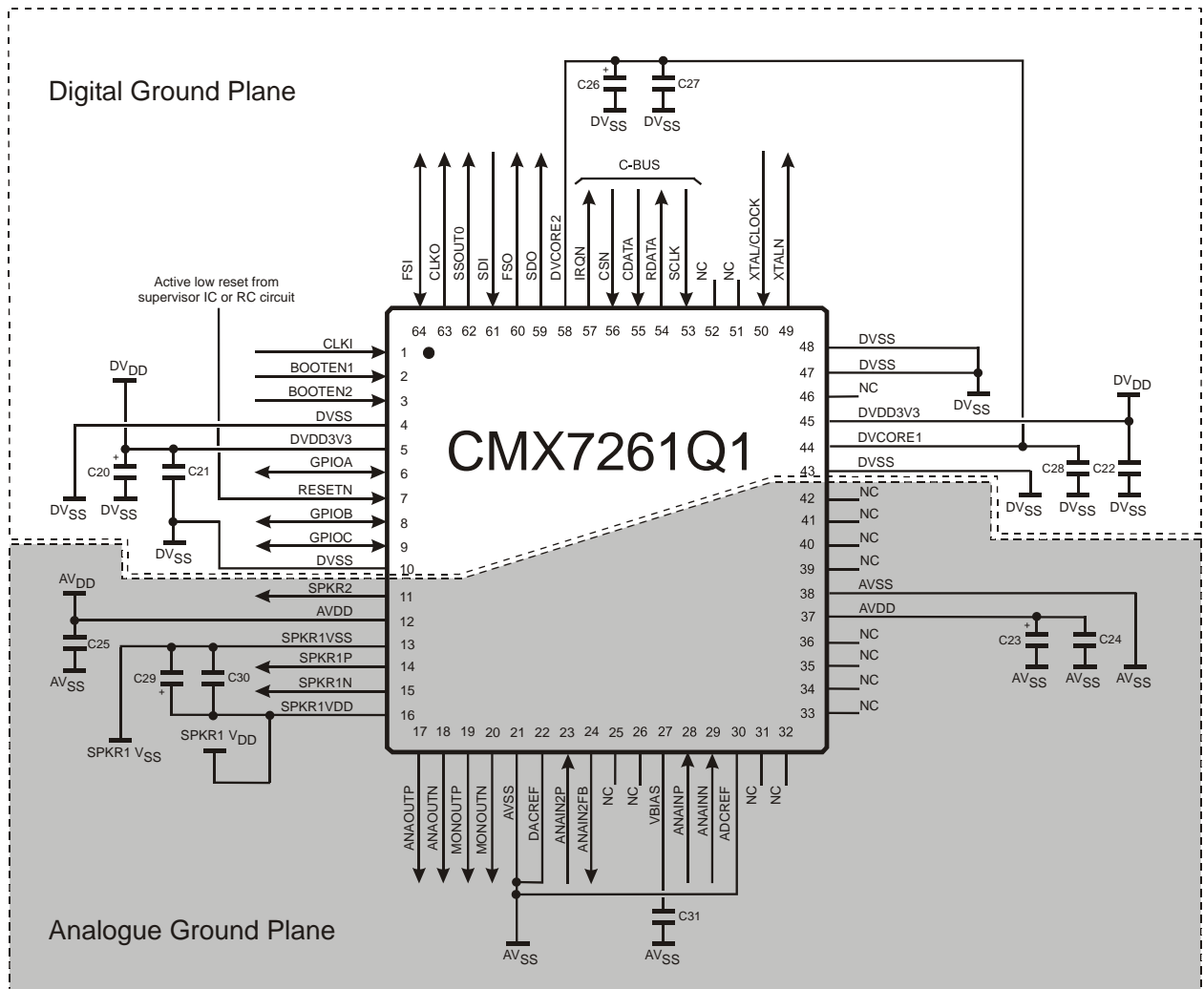
C20	10µF	C26	22µF
C21	10nF	C27	10nF
C22	10nF	C28	10nF
C23	10µF	C29	10µF
C24	10nF	C30	10nF
C25	10nF	C31	100nF

Figure 3 CMX7261 Power Supply and De-coupling

Notes:

To achieve good noise performance, V_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals are very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX7261 area to provide a low impedance connection between the VSS pins and the V_{DD} and V_{BIAS} decoupling capacitors.

5   External Components

5.1   Xtal Interface
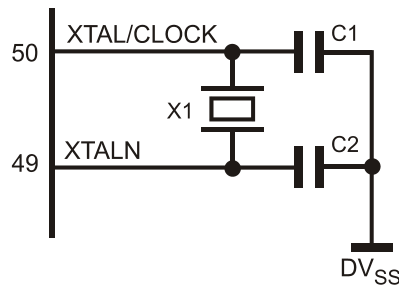
> X1   For frequency range see section 8.1.2 Operating Limits
> C1   22pF Typical
> C2   22pF Typical

Figure 4 Recommended External Components – Xtal Interface

Notes:

- The clock circuit can operate with either a xtal or external clock generator. If using an external clock generator it should be connected to the XTAL/CLOCK pin and the xtal and other components are not required. For external clock generator frequency range see section 8.1.2 Operating Limits. When using an external clock generator the XTAL oscillator circuit may be disabled to save power, see 10.1.2 Program Block 1 – Clock Control for details.

- The tracks between the xtal and the device pins should be as short as possible to achieve maximum stability and best start up performance. It is also important to achieve a low impedance connection between the xtal capacitors and the ground plane.

- The DV_{SS} to the xtal oscillator capacitors C1 and C2 should be of low impedance and preferably be part of the DV_{SS} ground plane to ensure reliable start up. For correct values of capacitors, C1 and C2 refer to the documentation of the xtal used.

5.2   C-BUS Interface
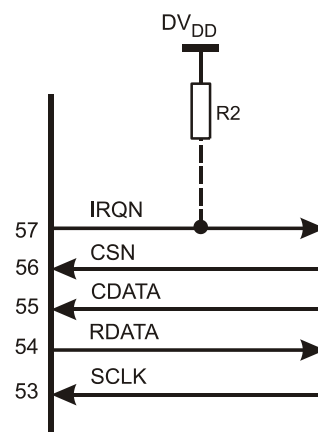
R2   10k - 100kΩ

Figure 5 Recommended External Components – C-BUS Interface

Note: If the IRQN line is connected to other compatible pull-down devices only one pull-up resistor is required on the IRQN node.

5.3 PCM and Serial Port Interface

The CMX7261 can be connected to an external codec using its PCM port. The CMX7261 can also load its FI from an external serial memory. Pins 59, 61 and 63 act as serial port pins whilst booting the FI and as PCM pins whilst the FI is in operation. For more information refer to section 3 Pin and Signal List.

Booting from an external serial memory or connecting with an external codec are both optional.

The schematic in Figure 6 shows the connections required when using an external codec with the CMX7261 as a slave device. The schematic also shows the connections required for interfacing to an external serial memory for FI booting.
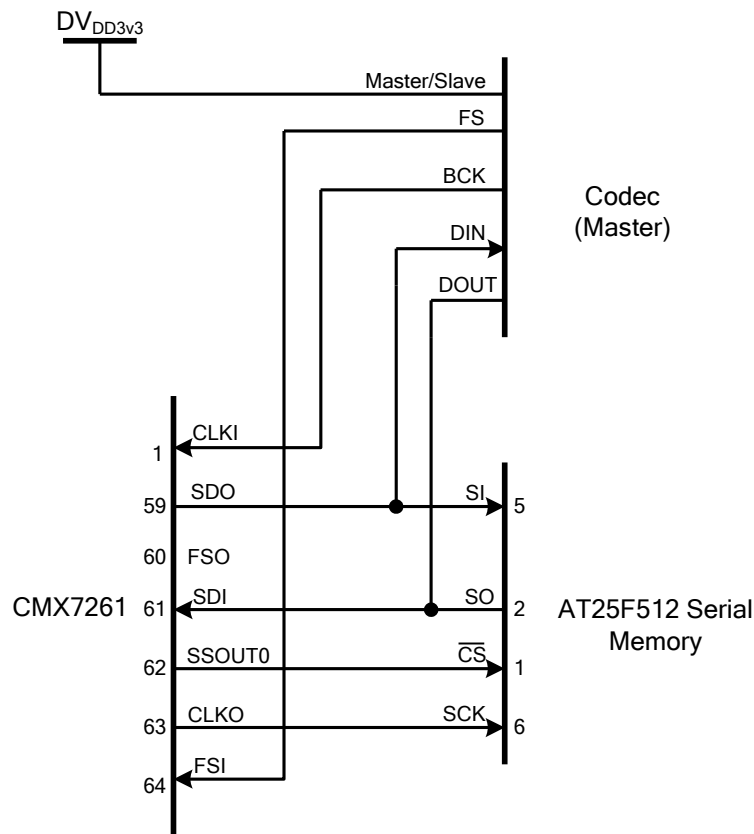
Figure 6 Interfacing the CMX7261 to an External Codec (master) and Serial Memory

The schematic in Figure 7 shows the connections required when using an external codec as a slave device to the CMX7261. The schematic also shows the connections required for interfacing to an external serial memory for FI booting.

Hardware design must ensure that, when booting from external serial memory, no device other than the external serial memory drives the serial port interface pins.
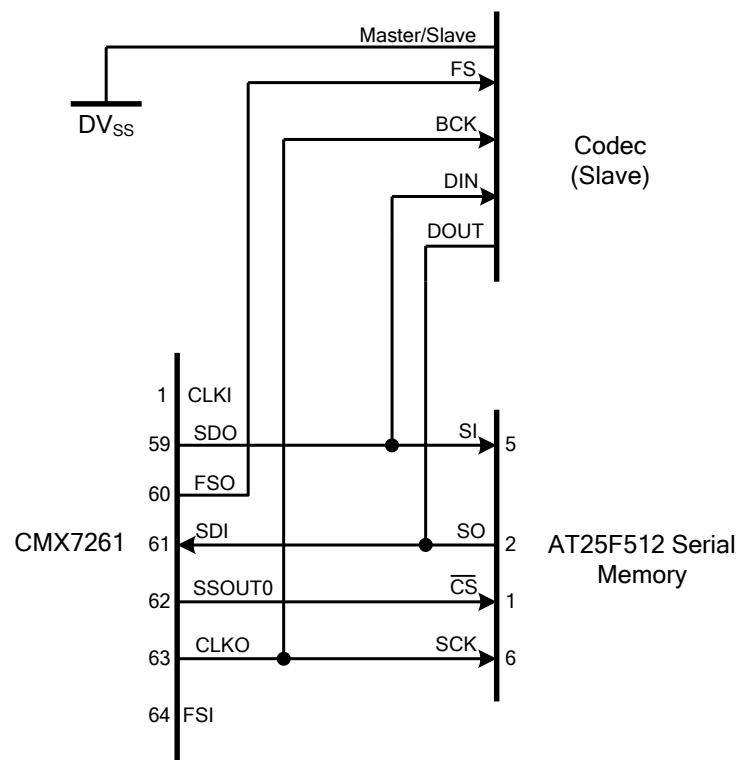
Figure 7 Interfacing the CMX7261 to an External Codec (slave) and Serial Memory

5.4   Audio Output

5.4.1   Audio Output Routing

The CMX7261 has four possible analogue outputs: two differential outputs – ANAOUT and MONOUT, a low impedance differential output speaker driver – SPKR1 and a single ended output – SPKR2, that can drive a headset/earpiece.

The CMX7261's two DACs (Analogue Out DAC and Monitor Out DAC) can output analogue waveforms on any or all of the four outputs (ANAOUT, MONOUT, SPKR1 and SPKR2). Figure 8 Analogue Audio Output Routing, shows the analogue output signal routing and control.
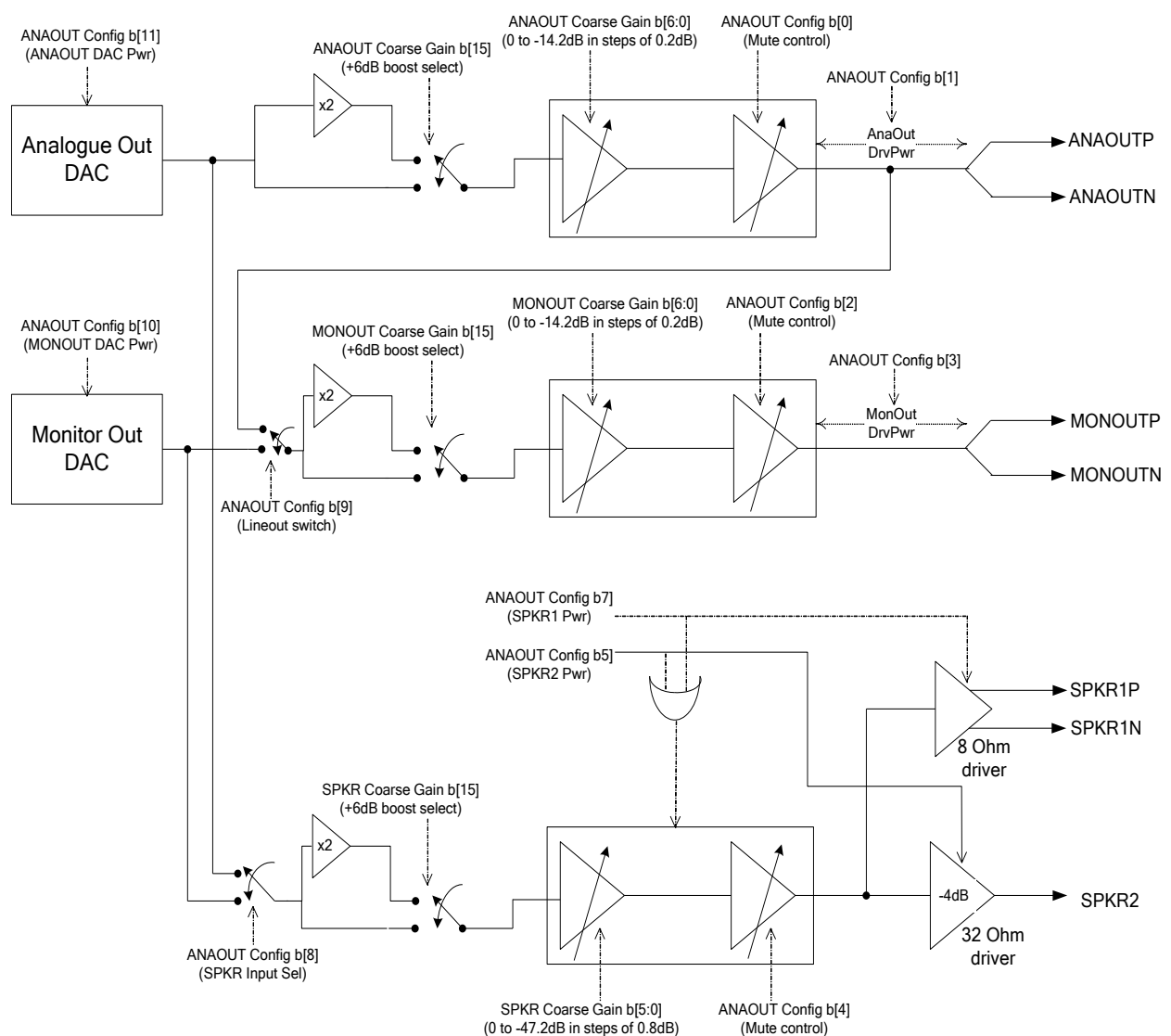
Figure 8 Analogue Audio Output Routing

The registers that control the analogue audio output routing are:
- 9.1.30 ANAOUT Config - $B3 write
- 9.1.31 ANAOUT Coarse Gain - $B4 write
- 9.1.32 MONOUT Coarse Gain - $B5 write
- 9.1.33 SPKR Coarse Gain - $B6 write

NOTE: If lower operating current is desired, it is recommended that unused outputs be powered down using the ANAOUT Config - $B3 write register.

5.4.2   Audio Output Reconstruction Filter
The CMX7261 ANAOUT and MONOUT outputs provide internal reconstruction filtering.
To complete the reconstruction filter, the external RC network shown in
Figure 9 should be used for each of the differential outputs.

The SPKR1 and SPKR2 outputs do not need any external reconstruction filter.
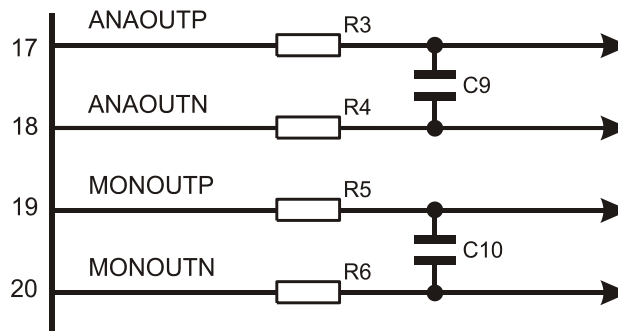
Bandwidth (kHz)	R3-R6 (kOhms)	C9-C10 (pF)
12.5	22	270

Figure 9 Recommended External Components – ANAOUT/MONOUT Reconstruction Filter

The CMX7261 SPKR2 output provides a single ended audio output that can be used to drive an earpiece or headphone, as shown in Figure 10.
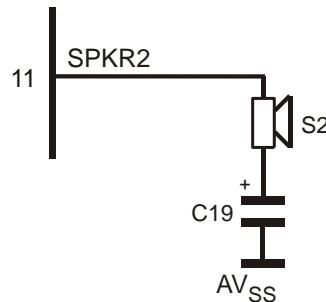
S2   32Ω nominal
C19   100µF

Figure 10 Recommended External Components – Speaker2 Output

The CMX7261 SPKR1 output can be used to drive a speaker as shown in Figure 11.
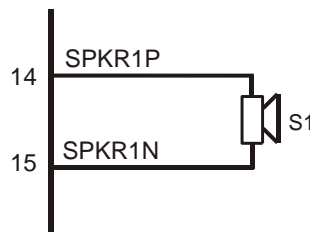
S1   8Ω nominal

Figure 11 Recommended External Components – Speaker1 Output

Care should be taken to avoid shorting any of the speaker outputs to one another or to V_{SS} or V_{DD}. An external RC filter may be added across SPKR1P and SPKR1N pins if clock noise needs further reduction.

5.5   Audio Input

5.5.1   Audio Input Routing

The CMX7261 has two possible analogue inputs: a differential input – ANAIN and a single ended input – ANAIN2.

The CMX7261's ADC can sample any one of the two analogue inputs. Figure 12 shows the analogue input signal routing and control.
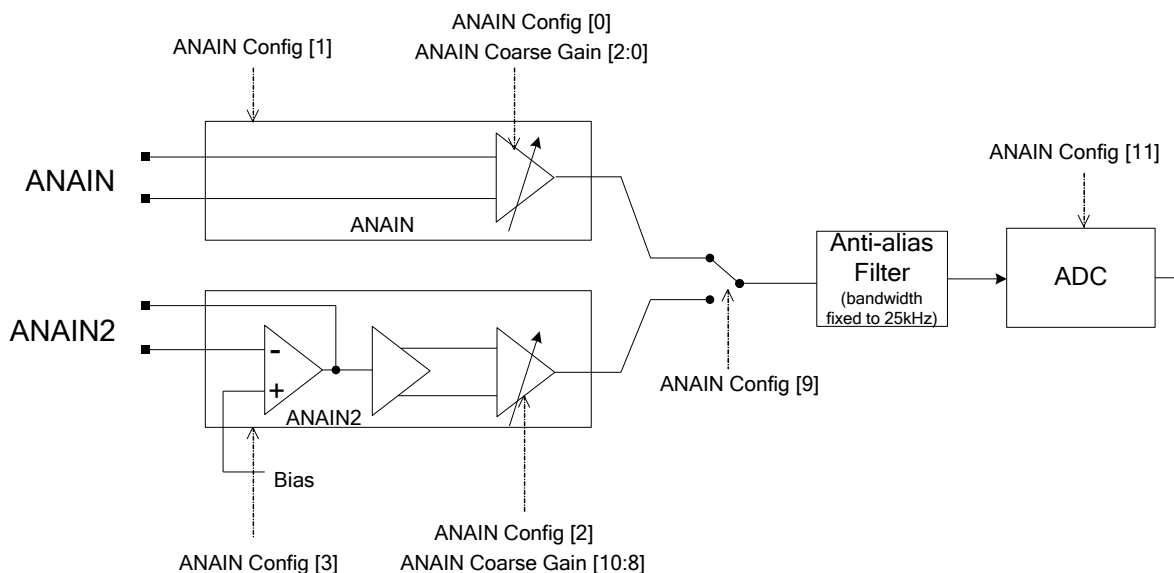
Figure 12 Analogue Audio Input Routing

The registers that control the analogue audio input routing are:
- 9.1.28 ANAIN Config - $B0 write
- 9.1.29 ANAIN Coarse Gain - $B1 write

NOTE: If lower operating current is desired, it is recommended that unused inputs be powered down using the ANAIN Config - $B0 write register.

5.5.2   Differential Audio Input
The device has an antialias filter in the analogue audio input path which should be sufficient for most applications, however, if additional filtering is required it can be done at the input to the device.

The input impedance of the ANAIN pins varies with the input gain setting, see section 8.1.3 Operating Characteristics.

5.5.3   Single-Ended Audio Input Interface
A single ended input can be connected to the CMX7261 using the ANAIN2 pins. Gain and filtering circuitry can be constructed around these pins, as shown in Figure 13.
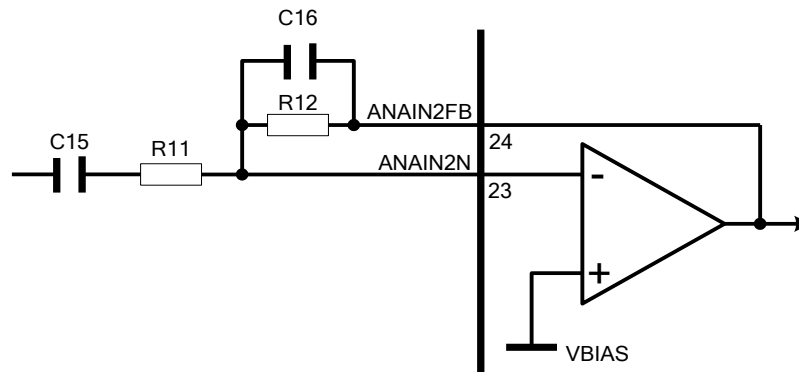
C15   See below
C16   100pF
R11   See below
R12   100kΩ

Figure 13 Recommended External Components – Single-Ended Audio Input Interface

R11 should be selected to provide the required DC gain (assuming C15 is not present) as follows:

$$\left|GAIN_{ANAIN2}\right| = 100k\Omega/R11$$

The gain should be such that the resultant output at the pins is within the input signal range.

C15 should be selected to maintain the lower frequency roll-off of the ANAIN2 input as follows:

$$C15 \geq 0.1\mu F \quad \text{X} \quad \left|GAIN_{ANAIN2}\right|$$

The high frequency cut off $= \left(\dfrac{1}{2\pi.R12.C16}\right)$

The low frequency cut off $= \left(\dfrac{1}{2\pi.R11.C15}\right)$

5.6 GPIO Pins

All GPIO pins are configured as inputs with an internal bus-hold circuit, after the Function Image™ has been loaded. This avoids the need for users to add external termination (pullup/pulldown) resistors onto these inputs. The bus-hold is equivalent to a 75kΩ resistor either pulling up to logic 1 or pulling down to logic 0. As the input is pulled to the opposite logic state by the user, the bus-hold resistor will change, so that it also pulls to the new logic state. The internal bus-hold can be disabled or re-enabled using programming register P1.20 in Program Block 1 – Clock Control.

6   General Description

6.1   CMX7261 Features

The CMX7261 is a multi-transcoder chip that performs encoding and decoding of PCM, CVSD and G.729A, as well as transcoding between these standards. The CMX7261 can be operated either as a half duplex or as a full duplex transcoder. Full duplex operation means that a type of transcoding may be specified on one channel and the opposite transcoding will then be implemented on a second audio stream.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a crystal clock generator, with phase locked loop to enable operation from a range of reference xtal frequencies.

Block diagrams of the device are shown in Figure 1.

Encoder Functions:
- Analogue voice to PCM encoding (µ-law or A-law according to G.711 standard).
- Analogue voice to CVSD encoding.
- Analogue voice to G.729A encoding.
- Input filtering on the input signal – when the signal comes from CMX7261's analogue audio input.

Decoder Functions:
- PCM decoding to analogue voice.
- CVSD decoding to analogue voice.
- G.729A decoding to analogue voice.
- Output filtering on the output signal – when the signal is being sent to CMX7261's analogue audio output.

Transcoder Functions (Half-Duplex):
- PCM to CVSD transcoding.
- PCM to G.729A transcoding.
- G.729A to CVSD transcoding.
- CVSD to G.729A transcoding
- PCM µ / A / linear to PCM µ / A / linear transcoding.
- Transcoding between any of, analogue audio / CVSD / G.729A / G.711 A-law / G.711 µ-law is possible.

Transcoder Functions (Full-Duplex):
- Two separate audio streams (channel-1, channel-2) are processed simultaneously.
- Channel-1 may process audio using a Decoder, Encoder or Transcoder function.
- Channel-2 will process audio in the reverse manner to channel-1. For example, if channel-1 is configured to transcode from CVSD to G.729A, channel-2 will transcode from G.729A to CVSD.

Interface:
- Optimised C-BUS (4-wire, high speed synchronous serial command/data bus) interface to host for control and data transfer, including streaming C-BUS for efficient data transfer.
- Input data can come through the analogue audio input or, C-BUS or from an external PCM device connected to CMX7261's PCM port.
- Output data can be sent to the analogue audio output or, C-BUS or, to an external PCM device connected to CMX7261's PCM port.
- Open drain IRQ to host.
- Three GPIO pins.
- Serial memory or C-BUS (host) boot mode.

6.2   Signal Interfaces

In half duplex mode the transcoder output can be sent to one, any two, or all of the three possible output ports – C-BUS (for transfer to host controller), PCM (for transfer to external DAC) or analogue audio output. In full duplex mode a single output must be selected. The input to the transcoder must come from one of the three input ports – C-BUS (input data from the host controller), PCM (from the external ADC) or analogue audio input.
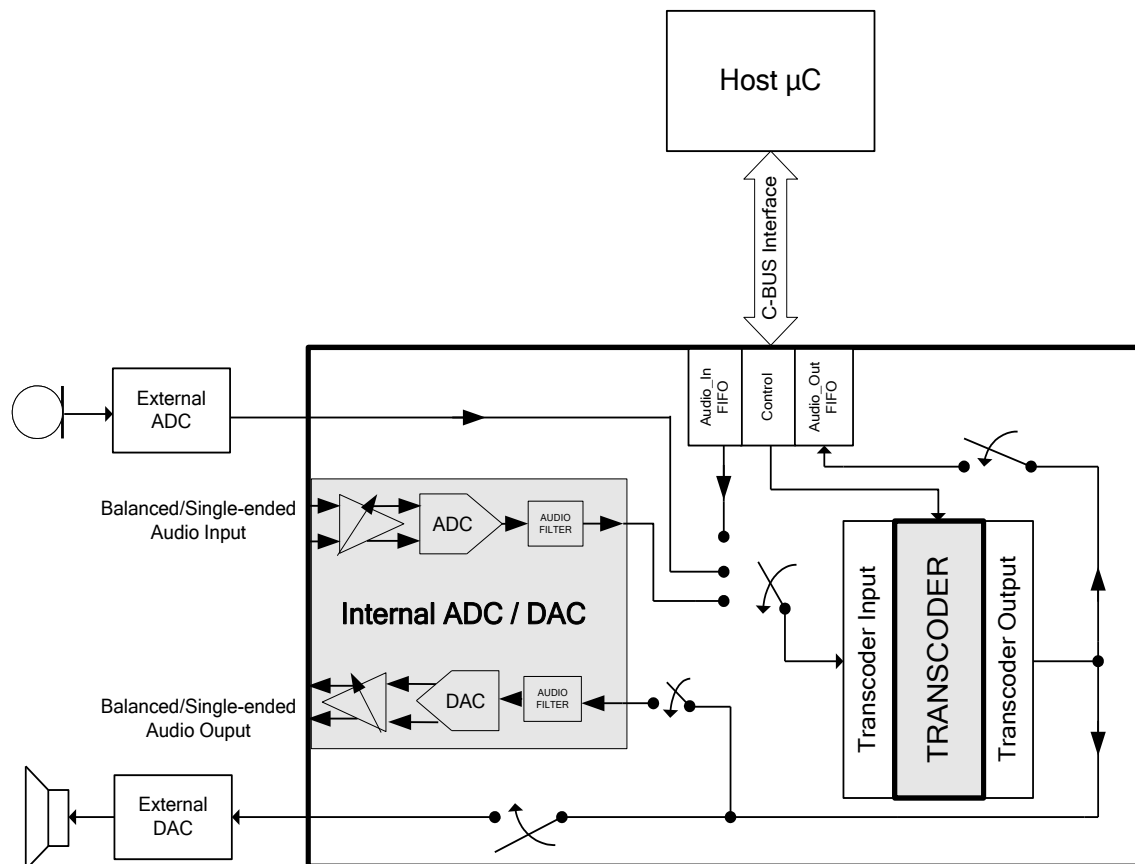
Figure 14 CMX7261 Inputs and Outputs

7   Detailed Descriptions

7.1   Xtal Frequency

The CMX7261 is designed to work with a xtal or an external frequency oscillator within the ranges specified in section 8.1.3. Program Block 1 (see User Manual) and must be loaded with the correct values to ensure that the device will work to specification with the user selected clock frequency. A table of configuration values can be found in Table 6, supporting a sampling rate of 8kHz or 16kHz or 32kHz (32kHz sample rate applies only to CVSD 32kbps mode), for a range of Xtal or external oscillator frequencies.

7.2   Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7261 and the host µC; this interface is compatible with Microwire™, SPI™ and other similar interfaces. Interrupt signals notify the host µC when a change in status has occurred; the µC should read the Status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set, see Interrupt Operation.

7.2.1   C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7261 internal registers and the host µC over the C-BUS serial bus. Single register transactions consist of a single Register Address byte sent from the µC, which may be followed by a data word sent from the µC to be written into one of the CMX7261's Write Only Registers, or a data word read out from one of the CMX7261's Read Only Registers. Streaming C-BUS transactions consist of a single Register Address byte followed by many data bytes being written to or read from the CMX7261. All C-BUS data words are a multiple of 8 bits wide, the width depending on the source or destination register. Note that certain C-BUS transactions require only an address byte to be sent from the µC, no data transfer being required. The operation of the C-BUS is illustrated in Figure 15.

Data sent from the µC on the CDATA (command data) line is clocked into the CMX7261 on the rising edge of the SCLK input. Data sent from the CMX7261 to the µC on the RDATA (reply data) line is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Section 8.2 (C-BUS Timing) gives detailed C-BUS timing requirements.

Note that, due to internal timing constraints, there may be a delay of up to 60µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS single byte command (no data)

Note:
The SCLK line may be high or low at the start and end of each transaction.
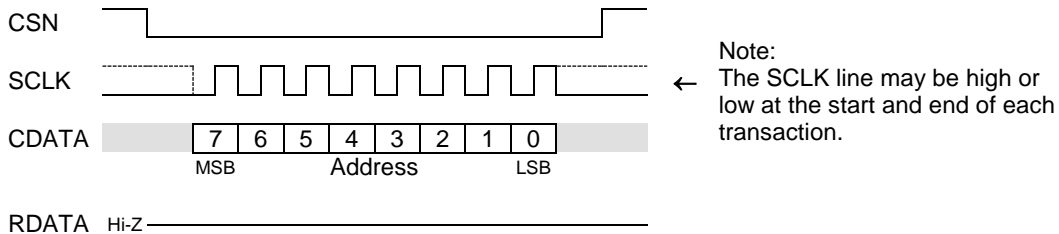
C-BUS n-bit register write
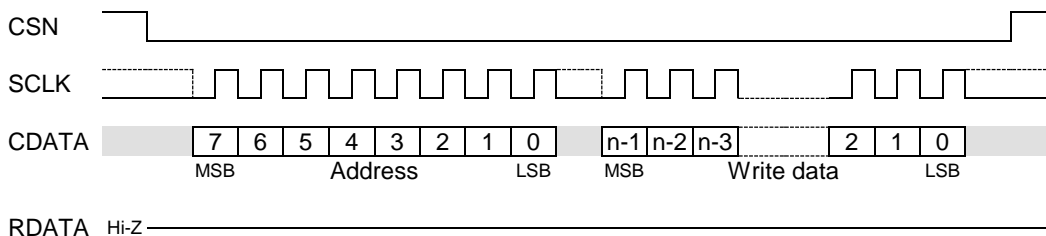
C-BUS n-bit register read
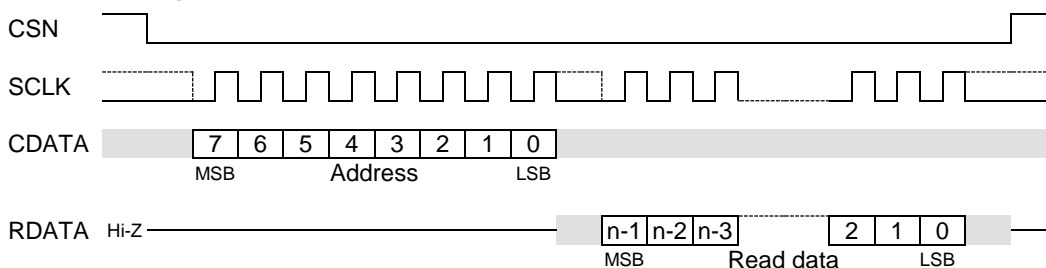
Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 15 Basic C-BUS Transactions

To increase the data bandwidth between the µC and CMX7261, certain of the C-BUS read and write registers are capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 16.

Example of C-BUS data-streaming (8-bit write register)

CSN

SCLK

CDATA | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | ... | 7 6 5 4 3 2 1 0 |
       | Address | First byte | Second byte | | Last byte |

RDATA Hi-Z
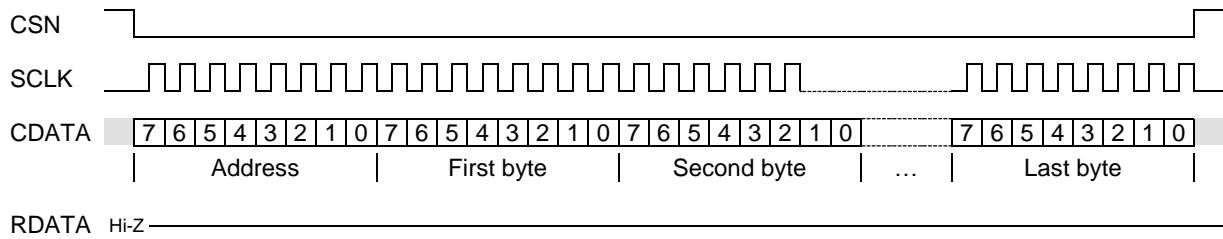
Example of C-BUS data-streaming (8-bit read register)
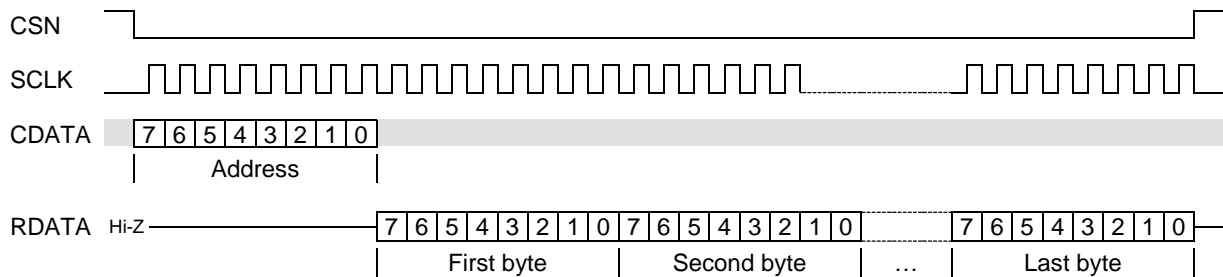
CSN

SCLK

CDATA | 7 6 5 4 3 2 1 0 |
       | Address |

RDATA Hi-Z | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | ... | 7 6 5 4 3 2 1 0 |
                      | First byte | Second byte | | Last byte |

Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 16 C-BUS Data-Streaming Operation

Notes:
1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK can be high or low at the start and end of each C-BUS transaction
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional; the host may insert gaps or concatenate the data as required.

7.3   Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file, which can be included into the host controller software or programmed into an external serial memory. The Function Image™ size can never exceed 128kbytes, although a typical FI will be considerably less than this. Note that the BOOTEN1, 2 pins are only read at power-on, when the RESETN pin goes high, or following a C-BUS General Reset, and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN1, 2 pins are ignored by the CMX7261 until the next power-up or Reset.

The BOOTEN 1, 2 pins are both fitted with internal low current pull-up devices.

For serial memory load operation, BOOTEN2 should be pulled low by connecting it to DV_{SS} either directly or via a 47k resistor (seeTable 3).

Whilst booting, the boot loader will return the checksum of each block loaded in the C-BUS Audio Out FIFO. The checksums can be verified against the published values to ensure that the FI has loaded correctly.

Once the FI has been loaded, the CMX7261 performs these actions:

   (1) The product identification code is reported in the C-BUS Audio Out FIFO
   (2) The FI version code is reported in C-BUS Audio Out FIFO.

Table 3 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS host load	1	1
Reserved	1	0
Serial Memory load	0	1
Reserved	0	0

7.3.1   FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7261 at power-up over the C-BUS interface, using the Audio In FIFO. For Function Image™ load, the FIFO accepts raw 16-bit Function Image™ data (using the Audio In FIFO data word - $49 write register), there is no need for distinction between control and data fields. The BOOTEN 1, 2 pins must be set to the C-BUS load configuration, the CMX7261 powered or Reset, and then data can then be sent directly over the C-BUS to the CMX7261.

If the host detects a brownout, the BOOTEN 1, 2 pins should be set to re-load the FI. A General Reset should then be issued or the RESETN pin used to reset the CMX7261 and the appropriate FI load procedure followed.

Streaming C-BUS may be used to load the Audio In FIFO Data - $48, $49 write register with the Function Image™, and the Audio In FIFO Level - $4B read register used to ensure that the FIFO is not allowed to overflow during the load process.

The download time is limited by the clock frequency of the C-BUS; with a 5MHz SCLK it should take less than 250ms to complete even when loading the largest possible Function Image™.

BOOTEN2 = 1
BOOTEN1 = 1

Power-up or
write General Reset to CMX7261

Use Audio Out FIFO level $4F read register
to wait for 3 device check words to appear in
the Audio Out FIFO - $4D. Read and discard
them.

BOOTEN1 and BOOTEN2 may be
changed once it is clear that the CMX7261
has committed to C-BUS boot - i.e. when
a word has been read from the C-BUS
Audio Input FIFO

Block number **N** = 1

Write Block 1 Length (DB**N**_len) to
Audio In FIFO - $49

Write Start Block N Address (DB**N**_ptr) to
Audio In FIFO - $49

Is Audio In FIFO fill level - $4B, 0?   No

Yes

Write up to "128-FIFO fill level" words to
Audio In FIFO - $49

End of Block?   No

Yes

Read and verify 32-bit checksum words from Audio
Out FIFO - $4D

N = **N**+1

No - load
next block

Is the next block the
activation block?

Yes

Write Start Block **N** Length (ACTIVATE_len) to
Audio In FIFO - $49

Write Start Block **N** Address (ACTIVATE_ptr) to
Audio In FIFO - $49

Poll status register ($7E) until PRG Flag b14 = 1
(FI loaded)

Read the Product ID Code and the FI version code
from the Audio Out FIFO -$4D

CMX7261 is now ready for use

V_{DD}

BOOTEN1

BOOTEN2

Figure 17 FI Loading from Host

7.3.2   FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory by either the host or an external programmer. The serial memory should contain the same data stream as written to the Audio In FIFO shown in Figure 17. The most significant byte of each 16-bit word should be stored first in serial memory.

The serial memory should be interfaced to the CMX7261 using SSOUT0 as the chip select and PCM port pins, which act as an SPI port whilst booting (refer section 3 Pin and Signal List). Section 5.3 PCM and Serial Port Interface, shows the connections required for interfacing the AT25F512 Serial Flash memory with CMX7261.

The CMX7261 needs to have the BOOTEN pins set to serial memory load, and then on power-on, following the RESETN pin becoming high, or following a C-BUS General Reset, the CMX7261 will automatically load the data from the serial memory without intervention from the host controller.
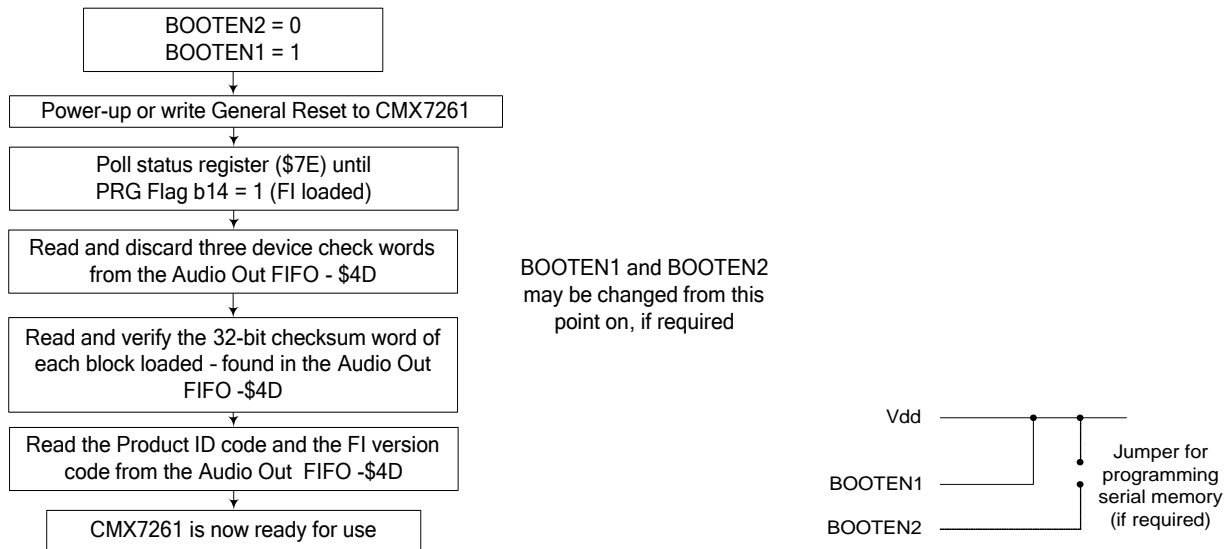
Figure 18 FI Loading from Serial Memory

The CMX7261 has been designed to function with the AT25F512 Serial Flash memory, however other manufacturers' parts may also be suitable. The time taken to load the FI should be less than 500ms even when loading the largest possible Function Image™.

7.4   Coding Formats

This section provides a brief description about the various coding standards handled by the CMX7261. The motivation behind all the voice coding standards described here is to compress analogue voice in order to reduce the bandwidth required to transmit it.

7.4.1   G.711

The G.711 standard is an ITU recommendation for audio companding. The standard specifies coding of linear PCM speech at 8 ksamples/s into logarithmic PCM speech at 8 ksamples/s – a coded data rate of 64 kbits/second.

The general principle behind companding is that for large sample values the exact value of the sample is not that important, so the signal can be quantised without loss of quality. However, when the sample value is small excessive quantisation would lead to poor quality speech. The result is that as the sample amplitude increases less resolution is required and, compared to linear PCM, compression is possible.

There are two variants: µ-law and A-law.

- µ-law is used primarily in North America – codes 14-bit linear PCM to 8-bit logarithmic PCM
- A-law is used in the rest of the world – codes 13-bit linear PCM to 8-bit logarithmic PCM

A single input sample maps onto a single companded sample, with no memory or algorithmic delay. The algorithm is lossy – if linear PCM speech is A-law or µ-law encoded and then decoded back into linear PCM the resulting audio will not be identical sample by sample but should sound similar.

In addition to companding, the G.711 standard specifies that A-law encoded samples should have even bits inverted. This is to provide many 0/1 transitions to assist signal reception when the data is transmitted using a modem. Inverting the even bits is equivalent to XORing the data with 0x55.

The G.711 standard specifies that µ-law encoded samples should be inverted, equivalent to XORing with 0xFF.

7.4.2   G.729A[1]

The G.729 standard is an ITU recommendation for coding of speech signals at 8 ksamples/s using conjugate-structure algebraic-code-excited linear prediction (CS_ACELP) into an 8 kbits/s coded bitstream. G.729 annex A provides a reduced-complexity version at the basic coding rate of 8 kbits/s whilst maintaining compatibility with G.729.

The CS-ACELP coder in the G.729 standard is based on the code-excited linear prediction (CELP) coding model. The G.729.A vocoder operates on speech frames of 10ms corresponding to 80 samples at a sampling rate of 8000samples/s. For every 10ms frame, the speech signal is analysed to extract the parameters of the CELP model (linear prediction filter coefficients, adaptive and fixed-codebook indices and gains). These parameters are encoded and transmitted.

At the decoder, the coded bitstream is used to retrieve the excitation and synthesis filter parameters. The speech is reconstructed by filtering this excitation through the short-term synthesis filter, as shown in Figure 11. The short-term synthesis filter is based on a 10th order linear prediction (LP) filter. The long-term, or pitch synthesis filter is implemented using the so-called adaptive-codebook approach. After computing the reconstructed speech, it is further enhanced by a postfilter.

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[1] CML acknowledges that the device contains an implementation of the G.729 standard, rights to which are held by third parties who may claim and/or be entitled to compensation in connection with their implementation. It is the users' responsibility to obtain any licence that may be required directly from holders of such rights if using G.729 functionality. Licence details are available from Sipro Lab Telecom (www.sipro.com). User hereby waives any right to seek damages or other compensation by way of suit or other action against CML Microsystems Plc in connection with any such standards.
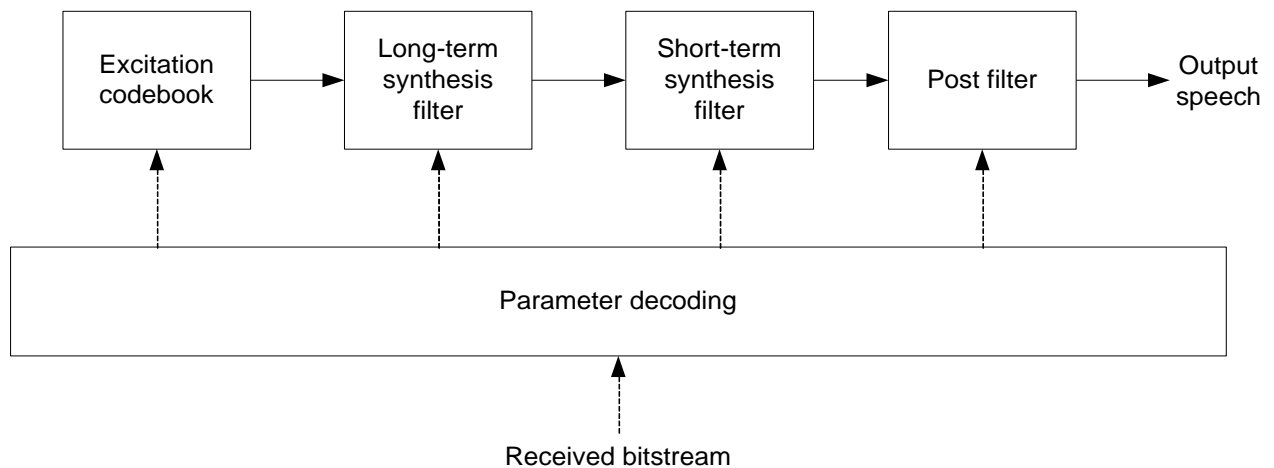
Figure 19 Block Diagram of Conceptual CELP Synthesis Model

A detailed description about the G.729 standard can be found in [1].

7.4.3   CVSD

Continuously variable slope delta modulation (CVSD) is a voice coding technique. It is a delta modulation with variable step size. CVSD encodes at 1 bit per sample, so that audio sampled at 16kHz is encoded at 16kbit/s. Similarly, audio sampled at 32kHz is encoded at 32kbits/sec.

The analogue input signal of a CVSD encoder is first band-limited by the input filter. The encoder maintains a reference sample and a step size. Each band-limited input sample is compared to the reference sample. If the input sample is larger, the encoder emits a 1 bit and adds the step size to the reference sample. If the input sample is smaller, the encoder emits a 0 bit and subtracts the step size from the reference sample.

The encoder also keeps the previous 3 bits of output to determine adjustments to the step size: if the previous 3 bits are all 1s or 0s, the step size is increased; otherwise, the step size is decreased. The adjustment is performed in an exponential manner. The step size is adjusted for every input sample processed. To allow for bit errors to fade out and to allow (re)synchronisation to an ongoing bitstream, the reference sample output is realised as leaky integrator.

A CVSD decoder takes the bitstream emitted from an encoder and replicates the reference sample and step size adjustment functions of the encoder. The reference sample output is band-limited by an output filter. This signal is the reconstructed waveform, and forms the output of the decoder.

When the input to the encoder is silent, the output bitstream should be a pattern of alternating 1s and 0s. Correspondingly, if silence is required as the output from the decoder, the input should be fed with an 'idle pattern' also consisting of alternating 1s and 0s.

Analogue
Input

Input Bandpass Filter

Comparator

Output
Bitstream

3-bit Shift Register

| X | Y | Z |

Output = $X.Y.Z. + \overline{X}.\overline{Y}.\overline{Z}$

Reference Integrator

Pulse Modulator

Step Size Integrator

Figure 20 CVSD Encoder

Input
Bitstream

3-bit Shift Register

| X | Y | Z |

Output = $X.Y.Z. + \overline{X}.\overline{Y}.\overline{Z}$

Reference Integrator

Pulse Modulator

Step Size Integrator

Output Bandpass
Filter

Analogue
Output
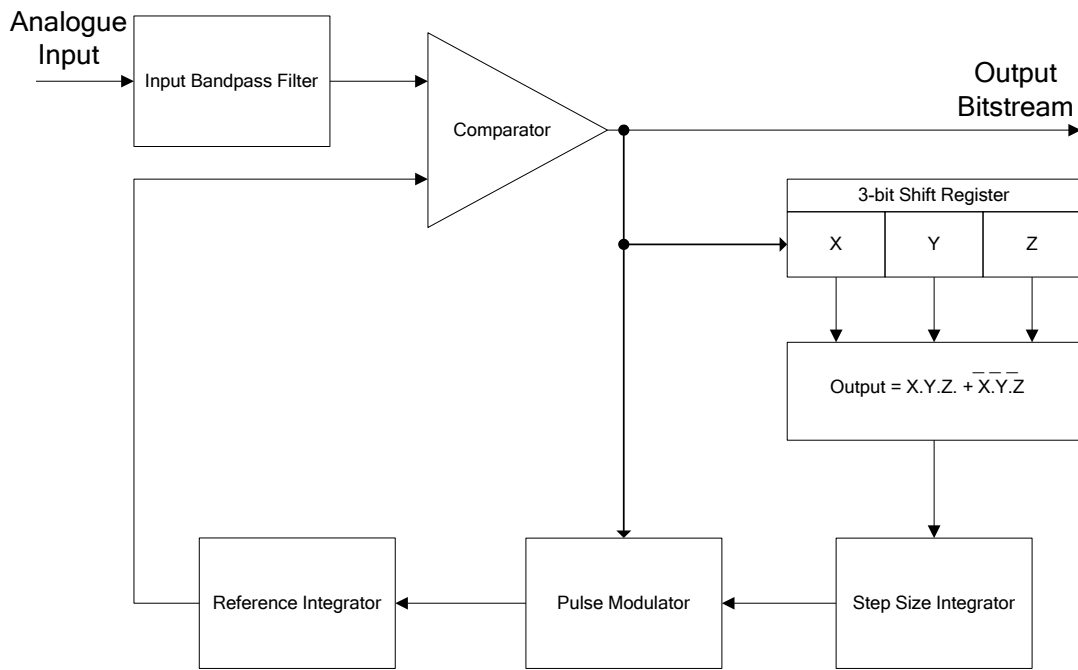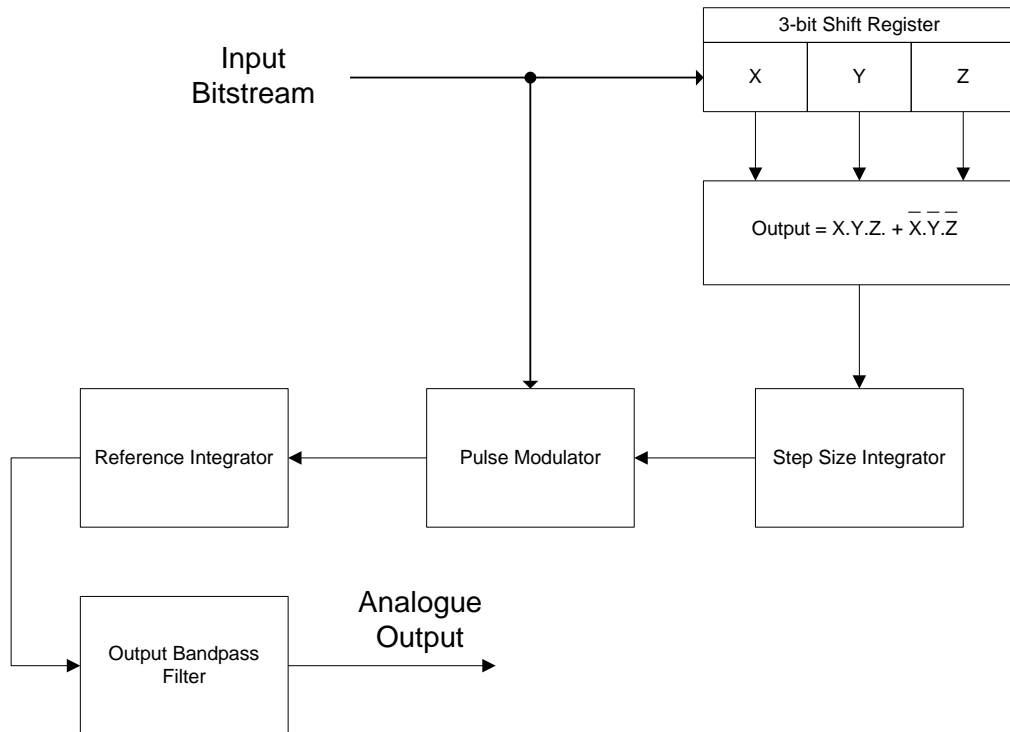
Figure 21 CVSD Decoder

7.5   Transcoding Description

Internally the CMX7261 decodes the input audio to linear PCM before encoding into a desired output format. Once the transcoder is configured, the following steps happen inside the CMX7261:

1. A frame of input audio is first passed through the 'Decoder' block (refer Figure 1 Block Diagram) where it is decoded from the input format configured in the Input Type - $54 write register, to linear PCM. The sample rate converter can optionally interpolate or decimate the output of the decoder by a factor of two. The sample rate converter is necessary when transcoding between modes which have different sampling frequencies. CVSD operates on signals sampled at 16kHz, other compressed formats are intended to operate at an 8kHz sample rate – although linear PCM can work at both rates.
2. The output of the sample rate converter is then passed through the 'Encoder' block (refer Figure 1 Block Diagram) where it is encoded to the output format configured in the Output Type - $56 write register.
3. Optionally the linear PCM output from the Decoder can be monitored using the MONOUT pins. This facility is provided for debug purposes and can be switched off, to conserve power.
4. The output from the sample rate converter is also used by the VAD.

The steps above describe transcoding of a single audio channel. Full duplex mode provides two such audio channels with the limitation that one channel provides the reverse transcoding of the other.

7.5.1   Input and Output Frame Sizes
The input and output frame sizes differ between various transcoding formats, as explained in this section.

G.729A
When decoding a G.729A coded bit stream – a frame of 80-bits will be decoded into 80 linear PCM samples, representing 10ms of audio (at 8kHz sampling rate).
When encoding into a G.729A coded bit stream – a frame of 80 samples representing 10ms of audio (at 8kHz sampling rate) will be encoded into 80 bits (compressed bit stream).

CVSD
When decoding a CVSD coded bit stream – each bit will be decoded into a linear PCM sample, representing 0.0625ms worth of audio (at 16kHz sampling rate).
When encoding into CVSD coded bit stream – each input sample (at 16kHz sampling rate) will be encoded into a single bit.

G.711
When decoding G.711 µ/A-law coded audio – each 8-bit input byte will be decoded into a linear PCM sample representing 0.125ms of audio (at 8kHz sampling rate).
When encoding into G.711 µ/A-law coded audio – each input (at 8kHz sampling rate) will be encoded into an 8-bit sample.

For example:
Transcoding a CVSD coded bit stream into a G.729A coded bitstream.
The CVSD bit stream is first passed through the decoder block, which decodes it to linear PCM samples at 16kHz. This is then passed through the sample rate converter, which decimates it by 2, producing linear PCM samples at 8kHz. The resulting samples are then passed on to the encoder block which encodes 80 samples into 80-bits of G.729A coded bit stream.

7.5.2   Data Transfer Using C-BUS Interface
Audio data can transferred to and from the host via C-BUS Audio In and Audio Out FIFOs, each of which provide efficient streaming C-BUS access. The FIFO fill level can be determined by reading the Audio In and Audio Out FIFO levels and controlled using the FIFO Control - $50 write register. Interrupts may be provided on FIFO fill thresholds being reached, or on every 'N' new samples being read from or written to the respective FIFOs.

Each FIFO word is 16-bits, that can be accessed as one 16-bit word or as two bytes – LSByte and MSByte. Word wide FIFO writes involve writing 16-bit words to the Audio In FIFO data word register using either a single write or a streaming C-BUS. The word written is transferred to the Audio In FIFO and its fill level is updated.

Byte wide FIFO writes involve writing to the Audio In FIFO data byte register using either a single write or a streaming C-BUS. The contents of the Audio In FIFO data byte register are transferred to the Audio In FIFO (with undefined data in the MSByte) and its fill level is updated.

Likewise a word read from the Audio Out FIFO data word read register will return the oldest Audio Out FIFO data word and Audio Out FIFO fill level is updated. Reading the Audio Output data byte register will read the oldest Audio Out FIFO data word, discard the MSByte and return the LSByte. Audio Out FIFO fill level is also updated. In summary:

Operation	Effect
Audio In FIFO Data word Wr	Data word is added to Audio In FIFO. Audio In FIFO fill level is updated.
Audio In FIFO Data byte Wr	Audio In FIFO Data byte written is added to Audio In FIFO and its fill level is updated. The MSByte is a "don't care" byte.
Audio Out FIFO Data word Rd	Oldest Audio Out FIFO data word is removed from FIFO and returned; Audio Out FIFO fill level is updated.
Audio Out FIFO Data byte Rd	Oldest Audio Out FIFO data word is removed from FIFO, its MSByte is discarded and its LSByte is returned. Audio Out FIFO fill level is updated.

Figure 22 shows the C-BUS interface to the Audio In and Audio Out FIFOs.
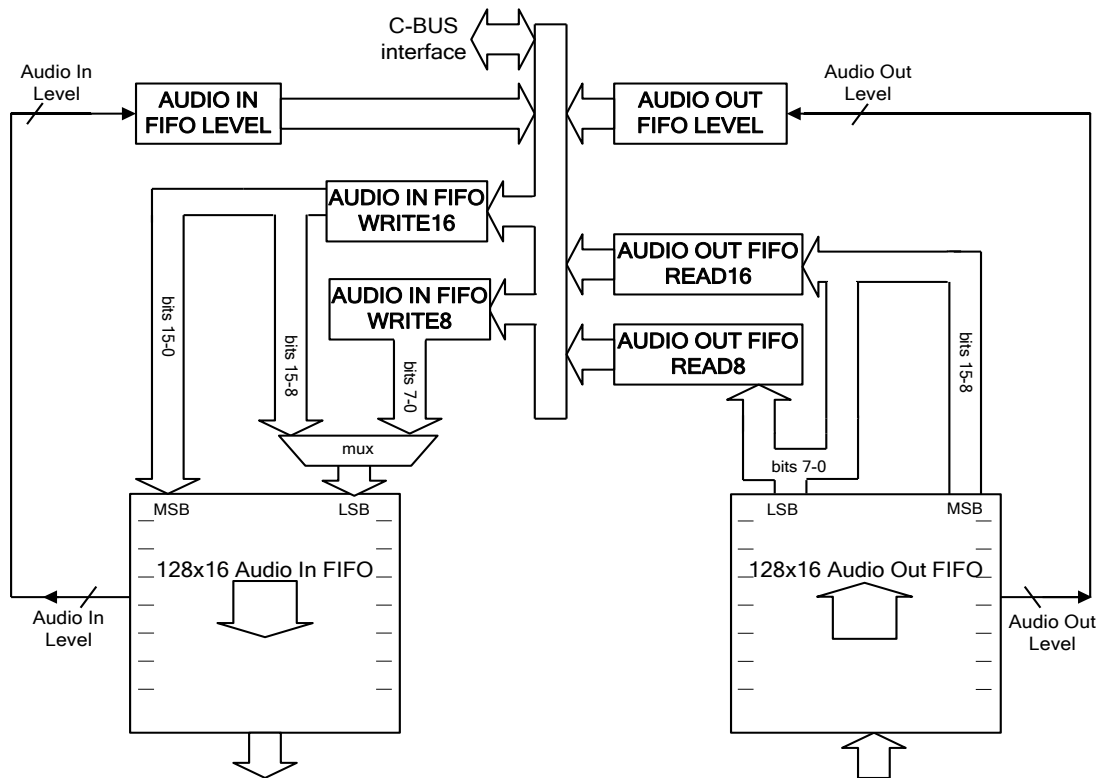
Figure 22 Audio Input and Audio Output FIFOs

The type of input data selected using the Input Type - $54 write register will determine whether the Audio In FIFO write 16 or 8 bit registers should be used for C-BUS audio input. The type of output data selected using the Output Type - $56 write register will determine whether the Audio Out FIFO read 16 or 8 bit registers should be used for C-BUS audio output.

The registers that affect FIFO operation are:
- Audio In FIFO Data - $48, $49 write
- Audio Out FIFO Data - $4C, $4D read
- Audio In FIFO Level - $4B read
- Audio Out FIFO Level - $4F read
- FIFO Control - $50 write.

The remainder of this section explains data transfer to and from the host using the C-BUS interface.

When the input data source is C-BUS:

1. The host must ensure that the Audio In FIFO does not contain audio from previous encoding/decoding operations (see FIFO Control - $50 write register).

2. The Audio Source field in the Mode - $6B write register must be set to indicate that audio input is through the C-BUS interface.

3. The host writes at least a frame of data to the Audio In FIFO (see Audio In FIFO Data - $48, $49 write registers). The frame size varies between different vocoders. The following table gives the frame size for various vocoders that exist in the CMX7261.

Input type	Frame size
Linear PCM	1 linear PCM sample
G.711 μ/A-law	1 G.711 μ/A-law 8 bit sample
CVSD	1 CVSD coded bit
G.729A	80 words (G.729A operates on 80 sample frames). In G.729A packed format, the input (80-bits) is packed into 16-bit words resulting in 5 words representing a G.729A coded frame

4. If the FIFO Control - $50 write register is configured correctly, the host will be interrupted when the Audio In FIFO empties to the level specified by the host. Alternatively, if the host has configured the FIFO Count Interrupt - $51 write register, the host will be interrupted when the CMX7261 has read the specified number of samples from the Audio In FIFO. More data may be loaded into the Audio In FIFO at this stage before data buffered in the CMX7261 runs out, otherwise an under-run will occur.

In typical operation, input data may be written to the Audio In FIFO prior to starting transcoding, enabling the host to create a buffer of data and therefore avoiding risk of the data running out during transcoding.

When the input data source is PCM or the analogue audio input:

In the case where Audio Source is set to external PCM or analogue audio input, the input data from an external PCM codec or the analogue audio input will be loaded into the Input Buffer, without the host having to intervene in the data transfer process.

If the audio source is external PCM/analogue audio input, and the audio destination is C-BUS – the host must read the output data from the C-BUS quickly enough to maintain real-time constraints. Once started the analogue audio input/external PCM will operate at the selected sample rate regardless of the host C-BUS access rate. If the C-BUS Audio Out FIFO is not read quickly enough by the host a data overflow will occur, which the CMX7261 will indicate to the host.

When the output data destination is C-BUS:

1. The host must ensure that the Audio Out FIFO does not contain audio from previous encoding/decoding operations (see FIFO Control - $50 write register).

2. If the host has configured the FIFO Count Interrupt - $51 write register, it waits for the Count_Out interrupt, at which point the host can read a frame of data from the Audio Out FIFO.

3. Alternatively the FIFO Control - $50 write register may be configured to interrupt when the Audio Out FIFO fills to a specified level, and the host may read the Audio Out FIFO when this interrupt occurs.

When the output data destination is PCM or the Analogue audio output:

When the Audio Destination is set to external PCM or analogue audio output, the data in the Output buffer will sent to the external PCM codec or analogue audio output, without the host having to intervene in the data transfer process.

If the audio destination is external PCM/analogue audio output, and the audio source is C-BUS – the host must provide input data to the C-BUS quickly enough to maintain real-time constraints. Once started, the analogue audio output/external PCM will operate at the selected sample rate regardless of the host C-BUS access rate. If the C-BUS Audio In FIFO is not written quickly enough by the host a data underflow will occur, which the CMX7261 will indicate to the host.

In general, Figure 23 describes operation when data is transferred into the CMX7261 using the Audio In FIFO (see Audio In FIFO Data - $48, $49 write registers). Figure 24 describes operation when data is transferred out of the CMX7261 using the Audio Out FIFO (see Audio Out FIFO Data - $4C, $4D read registers).

Specify the audio source and audio destination in the Mode - $6B write register

Specify the input and output data types, in Input Type - $54 write register and Output Type - $56 write registers, respectively

Audio source set to C-BUS?

No → Is audio source set to external PCM source

Yes ↓ (from C-BUS)

Flush Audio_In FIFO

Write at least one frame of input samples to the Audio In FIFO

Start transcoding by setting b0 in the MODE register $6B

Continue writing input frames to the Audio In FIFO

note

Transcoding starts once there is at least one frame of input available in the Audio In FIFO

External PCM source: Yes

Start transcoding by setting b0 in the MODE register $6B

— note —

The host must have configured the external PCM input device before this point. To do this, the host may use the SSP pass thru feature on the CMX7261

The external PCM device should provide input samples

External PCM source: No

Start transcoding by setting b0 in the MODE register $6B

— note →

Audio source set to internal ADC - CMX7261 will automatically configure the internal ADC to produce samples at the correct sampling rate (according to the Input Type specified)

Input samples come from the internal ADC

Figure 23 Input Data Transfer into the CMX7261

```
┌─────────────────────────────────┐
│ Specify the audio source and    │
│ audio destination in the        │
│ Mode - $6B write register       │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│ Specify the input and output    │
│ data types, in Input Type -     │
│ $54 write register and Output   │
│ Type - $56 write registers,     │
│ respectively                    │
└─────────────────────────────────┘
```

Audio destination set to C-BUS? — No → Is audio destination set to external PCM

Yes ↓

Flush Audio_Out FIFO

Start transcoding by setting b0 in the MODE register $6B

Read output frames from the Audio Out FIFO

note — Transcoding starts once there is at least one audio frame available

No ↓ (from external PCM) ; Yes →

Start transcoding by setting b0 in the MODE register $6B

note — The host must have configured the external PCM output device before this point. To do this, the host may use the SSP pass thru feature on the CMX7261

The external PCM device should accept output samples

Start transcoding by setting b0 in the MODE register $6B

note — Audio destination set to internal DAC - CMX7261 will automatically configure the internal DAC to produce samples at the correct sampling rate (according to the Output Type specified)

Output samples are sent to the internal DAC

Figure 24 Output Data Transfer from the CMX7261

7.5.3   Data Formats – Packed and Unpacked

The CMX7261 can accept packed or unpacked data as an input, and provide either as an output. The concept of packing data applies mainly to G.729A, CVSD and G.711 compressed data so, as it is unlikely that these data formats can usefully be transferred through the PCM port, data packing is likely to apply only to data transferred to/from the host using the C-BUS facing FIFOs.

The purpose of standards such as CVSD, G.711 and G.729A is to compress voice in order to conserve the bandwidth required to transmit it. The output of these compression algorithms is a binary bit stream. However, the G.729A standard definition represents a binary-1 and binary-0 using whole 16-bit words - usually $0081 and $007F, respectively. Choosing to represent a single bit using a whole word of 16-bits, nullifies the effect of compression. To avoid this, many applications have come up with their own bit packing standards. Bit packing is defined as grouping bits in the compressed bit stream into bytes or words, or any other conveniently sized chunks.

This section describes the bit packing standards to be used with CMX7261. The CMX7261 is capable of accepting packed data as an input and can output packed data. Though the packed data format is intended for use with C-BUS inputs and outputs, it applies equally well for external PCM inputs and outputs if the external PCM device has some digital logic to pack and unpack data according to the format mentioned in this section.

G.729A – Packed Data
Encoding a G.729A frame compresses 80 words (10ms of audio at 8kHz sampling rate) into 80 bits. In G.729A packed format, groups of 16 bits are packed into data words. Five packed words contain a frame of G.729A coded bits. For data input to the CMX7261, packed words are written to the Audio In FIFO data word register (Audio In FIFO Data - $48, $49 write), in the following order:

1st word written to Audio In FIFO data word write register (beginning of a G.729A frame):

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
G.729A coded bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7	bit8	bit9	bit10	Bit11	bit12	bit13	bit14	bit15

2nd word written to Audio In FIFO data word write register:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit16							...								Bit31

3rd word written to Audio In FIFO data word write register:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit32							...								Bit47

4th word written to Audio In FIFO data word write register:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit-48							...								Bit63

5th word written to Audio In FIFO data word write register (last word in the G.729A frame):

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit64							...								Bit79

G.729A – Unpacked Data
The G.729A standard represents a '1' bit by the word $0081 and '0' bit by the word $007F. In this format, each G.729A frame consists of a frame sync word ($6BC5), followed by a count of number of words in a frame (which is fixed at $0050), followed by eighty words representing the eighty bits of the frame. Unpacked data may be written to the Audio In FIFO data word register (see Audio In FIFO Data - $48, $49 write) in the following format for direct comparison to the G.729A standard.

1st word to be written to Audio In FIFO data word write register

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Frame Sync word - $6BC5															

2nd word to be written to Audio In FIFO data word write register

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Number of bits in the frame - is fixed to $0050 for G.729A															

3rd to 82nd words to be written to Audio In FIFO data word write register

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
$0081 or $007F representing either bit-1 or bit-0 respectively															

CVSD – Packed Data

The packed CVSD data format has 16 CVSD coded bits packed into a 16-bit word, with the most significant bit representing the first (oldest, in time) CVSD bit and the least significant bit contains the last/most recent CVSD bit. If there are less than 16 coded bits available the least significant bits should be padded to fill the 16 bit word. The following diagram shows a packed CVSD word where there are 13 valid CVSD coded bits, and 3 padding bits. The padding bits should consist of alternating 0 and 1 bits.

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Packed CVSD bits													Padding bits		

In order to transfer packed CVSD coded bits as an input, the host writes the packed data words to the Audio In FIFO data word register (Audio In FIFO Data - $48, $49 write). As an output they may be read from the Audio Out FIFO data word register (Audio Out FIFO Data - $4C, $4D read).

CVSD – Unpacked Data

In this case 8 CVSD coded bits are packed into a byte, with the most significant bit representing the first (oldest, in time) CVSD coded bit and the least significant bit containing the last/most recent CVSD coded bit. If there are less than eight coded bits available, the least significant bits should be padded to fill the byte. The following diagram shows a packed CVSD byte where there are 5 valid CVSD coded bits, and 3 padding bits.

B7	B6	B5	B4	B3	B2	B1	B0
CVSD coded bits					Padding bits		

When the host needs to transfer input data in this format, the host writes the CVSD coded bytes to the Audio In FIFO data byte register (Audio In FIFO Data - $48, $49 write). As an output they may be read from the Audio Out FIFO data byte register (Audio Out FIFO Data - $4C, $4D read).

G.711 – Packed Data

G.711 standard µ/A-law audio coding produces an 8-bit output per input sample. A packed data mode results in two bytes being packed into a 16-bit input word. The MSByte of the word will contain the first G.711 coded byte and the LSByte will contain the last/most recent G.711 coded byte, as shown below:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
First/oldest G.711 byte								Last/most recent G.711 byte							

In order to transfer packed G.711 bytes as an input, the host must write the packed data words to Audio In FIFO data word register (Audio In FIFO Data - $48, $49 write).

The G.711 standard describes two processing stages – convert linear PCM to a µ/A-law sample (compression) and then XOR the resulting sample with a mask to ensure that many bit transitions happen within the data (to aid data transmission and reception via a modem). Both packed and unpacked G.711 data may be optionally XORed with a mask as specified by the G.711 standard.

G.711 – Unpacked Data
Single G.711 coded bytes may be written to the Audio In FIFO data byte register (Audio In FIFO Data - $48, $49 write).

B7	B6	B5	B4	B3	B2	B1	B0
G.711 coded byte							

The G.711 standard describes two processing stages – convert linear PCM to a µ/A-law sample (compression) and then XOR the resulting sample with a mask to ensure that many bit transitions happen within the data (to aid data transmission and reception via a modem). Both packed and unpacked G.711 data may be optionally XORed with a mask as specified by the G.711 standard.

Linear PCM Samples
Linear PCM samples are always transferred using one 16-bit word per sample. Input is through the Audio In FIFO data word register (Audio In FIFO Data - $48, $49 write) or the PCM input and output through the Audio Out FIFO data word register (Audio Out FIFO Data - $4C, $4D read), or PCM output. Various input sample formats are possible – the sample resolution may be 13 or 14 bits for example, or the sample may be signed or unsigned. The CMX7261 is capable of processing each of these types of data – specified using the Input Type - $54 write and Output Type - $56 write registers.

7.5.4   Data Formats – 8kHz, 16kHz or 32kHz Sample Rate
The CMX7261 can accept and process signals sampled at either 8kHz, 16kHz or 32kHz sample rates. Dependent on the type of coding or decoding carried out some rates may not be allowed, or some sample rate conversion may be required. The CMX7261 will carry out the necessary sample rate conversion.

Three sample rates are supported because CVSD data is sampled at either 32kHz or 16kHz sample rate, whereas the standard rate specified for G.729A and G.711 data is 8kHz. The CMX7261 is however capable of supporting G.711 with a non-standard sample rate of 8 or 16kHz and linear PCM at 8 or 16kHz.

If the CMX7261 is interfaced to an external CODEC using the PCM port for CVSD coding, and that CODEC is also to be used when coding G.729A speech, there is a problem – if the CODEC runs at 16k samples/sec the sample rate is too fast for G.729A coding, if it runs at 8ksamples/sec it is too slow for CVSD coding. One solution would be to reprogram the CODEC (if this is possible) to change rate when coding in each format, the other is to resample the signal within the CMX7261.

The internal ADC or DAC may be configured to support the appropriate rate when encoding or decoding, to avoid the need for sample rate conversion – for example when encoding CVSD the input sample rate should be 16kHz or 32kHz, as that is what the coding type requires. Examples of sample rate conversion, and appropriate sample rate selection, are given in Figure 25:

A) Example of CVSD encoding - with an external CODEC running at Fs=16kHz

Select PCM port Input, —16k▶ | Decoder: | —16k▶ | Rate Converter: | —16k▶ | Encoder: | Bits Out ▶ Select CVSD Output,
LPCM Fs=16kHz | | Pass Thru | | Pass Thru | | CVSD | | Fs=16kHz
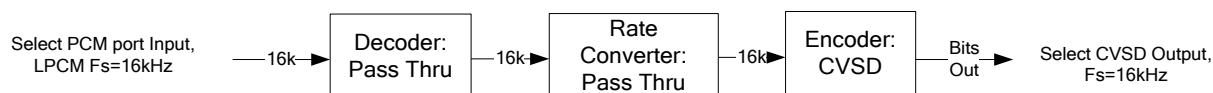
B) Using the same external CODEC as in A), running at Fs=16kHz, but G.729A coding - which must have a sample rate of 8kHz

Select PCM port Input, —16k▶ | Decoder: | —16k▶ | Rate Converter: | —8k▶ | Encoder: | Bits Out ▶ Select G.729A Output,
LPCM Fs=16kHz | | Pass Thru | | Decimate x2 | | G.729A | | Fs=8kHz
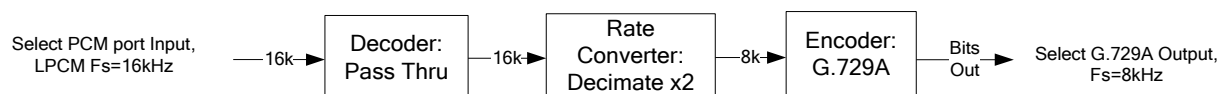
C) Example of G.729A to CVSD transcoding, all using the C-BUS interface

Select C-BUS port Input, Bits In ▶ | Decoder: | —8k▶ | Rate Converter: | —16k▶ | Encoder: | Bits Out ▶ Select CVSD Output,
G.729A Fs=8kHz | | G.729A | | Interpolate x2 | | CVSD | | Fs=16kHz
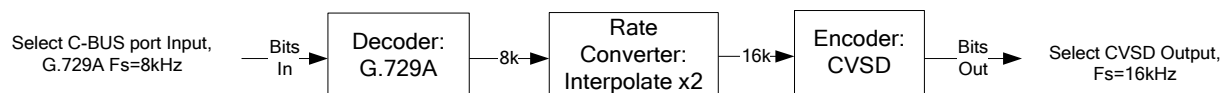
D) Decoding CVSD data using the internal DAC - running at Fs=16kHz

Select C-BUS port Input, —16k▶ | Decoder: | —16k▶ | Rate Converter: | —16k▶ | Encoder: | —16k▶ Select LPCM Output,
CVSD Fs=16kHz | | CVSD | | Pass Thru | | Pass Thru | | Fs=16kHz
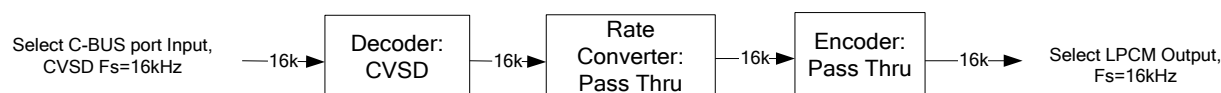
E) G711 A-law encoding using a PCM input running at Fs=16kHz

Select PCM port Input, —16k▶ | Decoder: | —16k▶ | Rate Converter: | —8k▶ | Encoder: | —8k▶ Select G.711 A-law
LPCM Fs=16kHz | | Pass Thru | | Decimate x2 | | G.711 A-law | | Output, Fs=8kHz
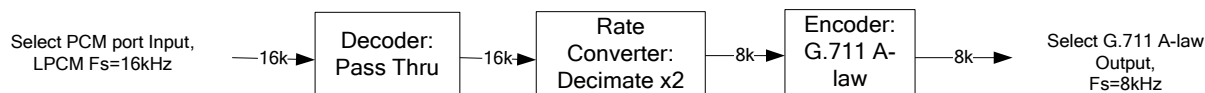
F) Example of G.729A to CVSD (32kbps) transcoding, all using the C-BUS interface

Select C-BUS port Input, Bits In ▶ | Decoder: | —8k▶ | Rate Converter: | —32k▶ | Encoder: | Bits Out ▶ Select CVSD Output,
G.729A Fs=8kHz | | G.729A | | Interpolate x4 | | CVSD | | Fs=32kHz
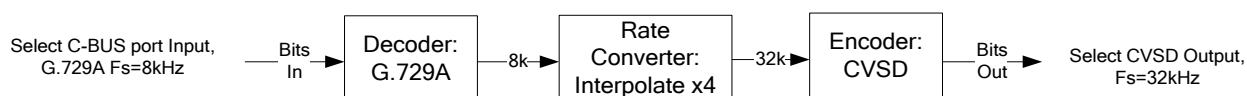
G) Decoding CVSD (32kbps) data using internal DAC - running at Fs=8kHz

Select C-BUS port Input, Bits In ▶ | Decoder: | —32k▶ | Rate Converter: | —8k▶ | Encoder: | Bits Out ▶ Select LPCM Output,
CVSD Fs=32kHz | | CVSD | | Decimate x4 | | Pass Thru | | Fs=8kHz
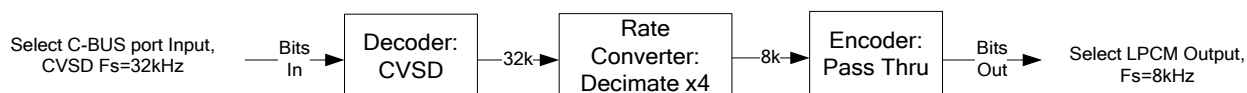
Figure 25 Examples of Sample Rate Conversion

Registers 9.1.9 Input Type - $54 write and 9.1.10 Output Type - $56 write select the input and output sample rate.

7.6   Voice Activity Detection

The CMX7261 has an internal Voice Activity Detection (VAD) block. There are two internal VAD blocks, one each for channel-1 and channel-2. The registers associated with the VAD blocks are:

- 9.1.16 VAD Level Channel-1 - $76 read

- 9.1.17 VAD Level Channel-2 - $77 read

- 9.1.12 VAD Threshold Channel-1- $59 write

- 9.1.13 VAD Threshold Channel-2 - $5A write

- 9.1.18 VAD Signal to Noise Transition Delay Channel-1 - $7A read

- 9.1.19 VAD Signal to Noise Transition Delay Channel-2 - $7B read

- 9.1.20 VAD Noise to Signal Transition Delay Channel-1 - $7C read

- 9.1.21 VAD Noise to Signal Transition Delay Channel-2 - $7D read

The VAD function can be used to detect periods of voice inactivity so that unneeded circuits can be powersaved, improving battery life. Certain coding schemes, such as CVSD, can suffer from added noise (e.g. granular noise) when low level input signals are encoded. The VAD function can minimise this by alerting the host to low level input signals. The host can then take action to quiet the speaker's output by either disabling the speaker, or loading an "idling" pattern into the CMX7261, which will result in a quiet speaker output.

The VAD is implemented using an energy detector consisting of an absolute value function, an integrator and a threshold detector, as shown in Figure 26.
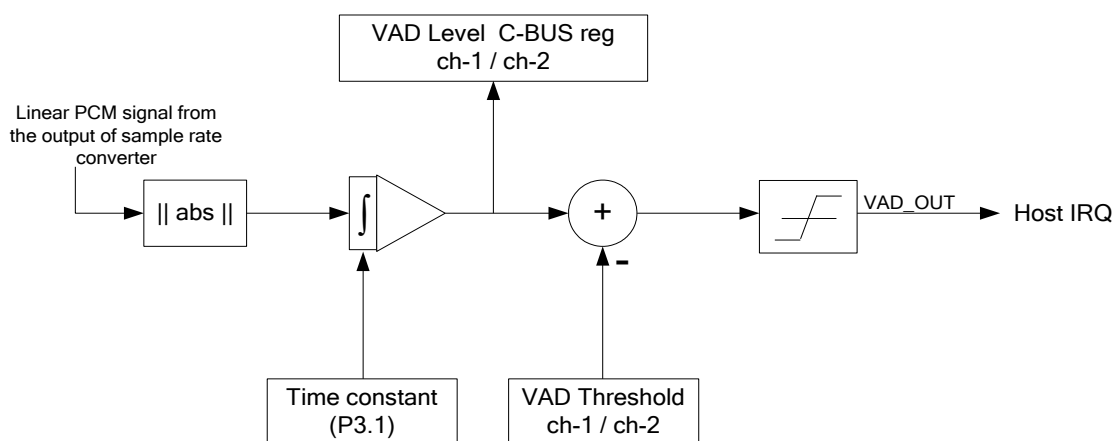
Figure 26 VAD Block Diagram

The linear PCM input to the VAD is rectified and averaged with a leaky integrator. The integrator output is compared to the VAD threshold to derive the VAD_OUT signal.

VAD_OUT = 1 indicates that signal energy greater than the threshold is present.
VAD_OUT = 0 indicates that signal energy is below the threshold.

When the VAD 'trip' threshold has been reached, the amplitude required to clear the VAD state is set internally to half of the 'trip' threshold. For example, if the VAD 'trip' threshold is set to 100mV then the 'clear' threshold will be 50mV. In this case, the signal amplitude must be greater than 100mv for it to be classified as signal and the signal amplitude must fall below 50mv for it to be classified as noise. This hysteresis is provided to minimise chattering and is not user-adjustable. However, the VAD threshold itself is user programmable as explained in the following sections.

The leaky integrator time constants (attack time and decay time) can be programmed using the Program Block 3 – VAD Config. The energy levels detected by the VAD may be read from the VAD Level read registers. This information can be used adaptively to set the detector threshold using the VAD Threshold write registers by observing the energy level of the background noise.

In full duplex mode, the programmed VAD configuration values in Program Block 3 – VAD Config apply to both the channels.

7.6.1   Attack and Decay Time Constant Programming

The attack and decay time constants are configured in the Program Block 3 – VAD Config. The time constants determine the time interval over which the rectified PCM input signal is integrated.

A longer attack/decay time constant will improve reliability by reducing the probability that noise will cause a false positive VAD Out signal but will create a longer time period before the VAD Out signal indicates a change in voice activity.

Typical values for attack and decay time constants are 5ms and 150ms respectively, but optimal values for these time constants are application dependent. The default and recommended values for attack and decay times are 5ms and 100ms, respectively. Program Block 3 – VAD Config, explains how to customise attack and decay times.

7.6.2   Threshold Level Programming

The desired VAD threshold voltage level is programmed into the VAD Threshold register using the following equation:

VAD Threshold register = (Desired RMS voltage of the threshold in V) * 32768 / (DAC full scale reference voltage)

DAC full scale reference voltage is 3,3V.

For example, to compute the required register value for a VAD threshold of 40mV:

VAD Threshold register = 0.04 * 32768/3.3 = 397.188 = $018D

7.6.3   Signal to Noise Hangover

The signal to noise hangover value is configured in the Program Block 3 – VAD Config register dictates the number of consecutive samples that the VAD algorithm has to classify as noise before the VAD output transitions from signal to noise. This prevents pauses in speech being classified as noise. It also helps in avoiding the end parts of a speech segment being classified as noise. The default value for signal to noise hangover is shown in Program Block 3 – VAD Config.

7.6.4   VAD Output Interface

When the CMX7261 outputs transcoded audio to the host, it does so using the output buffer and the active output FIFOs. The VAD signal is derived internally at the point shown in Figure 1 Block Diagram. This results in there being a buffer of samples (or coded bits) between the point at which VAD is calculated and the next item that the host may read from the Audio Out FIFO (or the sample to go into the internal Analogue out port or the PCM interface). This results in the value in the VAD Level register being poorly synchronised to the data that is about to be output.

To provide synchronised VAD information the CMX7261 interrupts the host using the IRQ Status - $7E read register whenever the internal VAD_OUT signal transitions from 0 to 1 or viceversa. Whenever a VAD_OUT 1 to 0 transition causes a host IRQ, the VAD Signal to Noise Transition Delay register will be updated. The VAD Signal to Noise Transition Delay register contains the number of items the host must read from the Audio Out FIFO (or the number of samples that will be output from the Analogue Out or PCM ports) before the signal that caused the VAD_OUT transition from signal (1) to noise (0) is output.

Similarly, on host IRQ, due to VAD_OUT transitioning from 0 to 1, the VAD Noise to Signal Transition Delay register will be updated. The VAD Noise to Signal Transition Delay register contains the number of number of items the host must read from the Audio Out FIFO, (or the number of samples that must be output from the Analogue Out or PCM ports) before the signal which caused the VAD_OUT transition from noise (0) to signal (1) is output.

If more than one output port is enabled, the top nibble of Signal Control - $58 write register is used to select which output port's buffer/FIFO is used when calculating the delays reported in the VAD Signal to Noise Transition Delay / VAD Noise to Signal Transition Delay / registers. This type of VAD reporting mechanism is intended to be used when the output port is C-BUS Audio Out FIFO. However, it will also operate correctly when using Analgoue out or PCM out ports.

7.6.5   VAD Output Level

The signal energy level computed by the VAD algorithm is output in the VAD Level register. During silence periods the VAD Level register may be read to allow the host to adaptively set the detector threshold in the VAD Threshold register for optimal VAD performance.

Care must be taken when reading the VAD Level register because the VAD output level corresponds to the signal being processed internally, not the signal that is available at the output FIFO. Refer to section 7.6.4 for further details.

The following equation can be used to interpret the results contained in the VAD Level register:

VAD output level = (VAD Level register) * (DAC full scale reference value) / 32768

DAC full scale reference voltage is 3.3V.

For example, to compute VAD output level corresponding to a value of $05B9 (1465 decimal) in the VAD Level register:

VAD output level = 1465 * 3.3 / 32768 = 147.54mV

7.7   Device Control

Once the Function Image™ is loaded, the CMX7261 can be set into one of two main modes using the Mode - $6B write register:

- Idle mode – for configuration or low power operation
- Transcode mode – for encoding or decoding or transcoding a single audio channel between analogue/PCM/CVSD/G.729A or G.711 format audio.
- Enc-Dec mode – a test mode which encodes LPCM to a selected compressed audio format and then decodes it again – providing the ability to evaluate audio quality
- Full duplex mode – for encoding, decoding or transcoding one audio channel between analogue/PCM/CVSD/G.729A or G.711 format audio, whilst performing the reverse encoding, decoding or transcoding on a second channel.

These modes are described in the following sections. All control is carried out over the C-BUS interface: either directly to operational registers or, for parameters that are not likely to change during operation, using the Programming Register - $6A write in idle mode.

To conserve power when the device is not actively processing a signal, place the device into idle mode. Additional power saving can be achieved by disabling unused hardware blocks, however, most of the hardware power saving is automatic. Note that the BIAS block must be enabled to allow any of the Analogue Input or Output blocks to function. It is only possible to write to the Programming register whilst in Idle mode. See:

- Programming Register - $6A write
- Mode - $6B write
- Programming Register Operation
- Bias Control - $B7 write.

7.7.1 Normal Operation Overview

In normal operation (after the CMX7261 is configured), the required mode must be selected and correctly formatted data input and read out. This process is carried out by selecting the transcoding type and specifying the input audio source and output audio destination. Such options are required to be configured correctly before transcoding/encoding/decoding can begin.

For continuous transcoding operation, data must be transferred into and out of the CMX7261. Audio transfer into the CMX7261 can be through the analogue audio input, from an external PCM device, or the host can feed in the data using C-BUS interface. Similarly, the transcoded output can be transferred out of the CMX7261 using the analogue audio ouput, or using the PCM interface to an external PCM device or to the host using the C-BUS interface. C-BUS transfers use the Audio In FIFO to transfer data into the CMX7261, and the Audio Out FIFO to transfer data out of the CMX7261. The Status register is used to indicate that the data has been dealt with. The CMX7261 can be configured to interrupt the host on FIFO fill level or when it has read/written a specified number of samples from the Audio In/Out FIFOs.

In the process of transcoding the most significant registers are:

- Mode - $6B write
- IRQ Status - $7E read
- IRQ Enable - $6C write
- Audio In FIFO Data - $48, $49 write
- Audio Out FIFO Data - $4C, $4D read
- Audio In FIFO Level - $4B read
- Audio Out FIFO Level - $4F read

7.7.2 Transcoder Operation

The many CMX7261 features provide significant flexibility however, basic encoding, decoding or transcoding can be carried out easily by just understanding the operation of just a few registers.

Half-duplex transcoder operation is illustrated by Figure 27 and the following detailed example.

Transcode_Process

Flush Audio_In and Audio_Out FIFOs

Specify audio source and audio destination

Note → The host may start writing input data to the specified audio source port

Specify Input type and expected Output type

Start transcoding operation by setting b0 of Mode register $6B

Note → Transcoding starts when there is at least one frame of input data available in the Audio In FIFO

Write the input data frame(s) to the Audio In FIFO

Has the Audio Output FIFO LEVEL or COUNT interrupt occured?

No

Yes

Read the output frame from the Audio Out FIFO

Transcode another frame?

Yes

No

Go to Idle mode

Figure 27 Transcoder Operation Flowchart

Basic Operation (Half-duplex)

Example: The following table explains the process involved in transcoding from G.711 A-law packed input to G.729A packed output when the input comes from Audio In FIFO and the output is sent to the Audio Out FIFO:

Step No.	C-BUS Operation	Action	Description
1	Write $8080 to FIFO Control - $50 write	Flush the audio in and audio out FIFO	To ensure that no data is remaining from any previous transcoding operation
2	Write $0011 to the Input Type - $54 write register	Specify the input data type	Specifies the format of the input data that the CMX7261 expects. In this case, the input data type is specified as G.711 A-law packed data.
3	Write $0010 to the Output Type - $56 write register	Specify the Output data type	Specifies the format of the output data expected from CMX7261. In this case, the expected output data type is specified as G.729A packed data.
4	Write $0110 to the Mode - $6B write register	Specify Audio Source and Audio Destination	Specifies the input and output ports' audio. In this case both are set to C-BUS.
5	Write 80 data bytes (40 writes for packed data) to the Audio In FIFO – see Audio In FIFO Data - $48, $49 write registers	Prime the Input buffer with a frame of data	This provides a buffer of 80 samples (G.729A operates on 80 sample frames) for the CMX7261 to start the transcoding operation on request
6	Write $2805 to the FIFO Count Interrupt - $51 write register	Specify when the host should be interrupted	This tells the CMX7261 to interrupt the host when it has written 5 new data words to the Audio Out FIFO, or read $28 words from the Audio In FIFO In, G.729A packed output mode the 80 bits in a G.729A coded frame will be packed into 5 words. The host will be interrupted when each packed G.729A coded frame is written to the Audio Out FIFO.
7	Write $0111 to the Mode - $6B write register	Start transcoding	Commands the CMX7261 to start the transcoding operation. If there is not enough data in the Input buffer for the specified transcoding mode, the CMX7261 will wait until it has enough data to start transcoding.
8	Check the IRQ Status - $7E read register for bits 2 or 3 – Count_Out or Count_In interrupts	Count_Out: Indicates an output frame is available	The input data has been transcoded into the desired format, and the host can now read a frame of data from the Audio Out FIFO
		Count_In: Indicates that a frame of input data has been read	There is now space for a further 40 words, containing 80 input G.711 sample to be written to the Audio In FIFO. This should be done promptly to ensure uninterrupted transcoding.
9	Continue Transcoding		Repeat steps 8 as required

The procedure described above can be adapted, to achieve different transcoding modes, with different input and output ports. Transcoding from the G.711 A-law packed data to G.729A packed data will continue as long as there is enough input data and the mode bits (b1-0) of Mode - $6B write register has not changed. The registers used for basic operation are:

- Mode - $6B write
- Input Type - $54 write
- Output Type - $56 write
- IRQ Status - $7E read
- Audio In FIFO Data - $48, $49 write
- Audio Out FIFO Data - $4C, $4D read
- FIFO Count Interrupt - $51 write
- FIFO Control - $50 write

Full-duplex operation

Example: The following flowchart and table explains the process involved in transcoding from G.711 A-law packed input to Analogue Audio, for channel-1. In addition, simultaneously transcoding from Analogue Audio to G.711 A-law packed output, for channel-2.

The channel-1 input comes from Audio In FIFO and the output is sent to Analogue Out.

Channel-2 is automatically set to transcode from Analogue Audio to G.711A packed data. Channel-2 input and output ports are automatically set to:

Channel-2 input port   = Analogue In
Channel-2 output port = Audio Out FIFO.

NOTE: In full-duplex operation, multiple output ports cannot be enabled for either channel. Each channel will have only one output port.

Full-duplex transcoder operation is illustrated by Figure 28 and the following detailed example.

```
        ┌─────────────────┐
        │  Full_Duplex    │
        │ Transcode_Process│
        └────────┬────────┘
                 │
    ┌────────────────────────────┐
    │ Flush Audio_In and Audio_Out FIFOs │
    └────────────┬───────────────┘
                 │
    ┌────────────────────────────┐
    │ Specify audio source and audio destination for │
    │ Ch-1, using Mode register $6B │
    └────────────┬───────────────┘
                 │
    ┌────────────────────────────┐
    │ Specify Input Type ($54) and expected Output │
    │ Type ($56) for Ch-1 │
    └────────────┬───────────────┘
                 │
    ┌────────────────────────────┐
    │ Start full-duplex transcoding operation by │
    │ setting b1-b0 of Mode register ($6B), to '11' │
    └────────────┬───────────────┘
                 │
    ┌────────────────────────────┐
    │ Write input data frame(s) to Audio In FIFO │
    │ for Ch-1 and provide Analogue In audio │
    │ input for Ch-2 │
    └────────────┬───────────────┘
```

Automatic internal setting:
Audio Source Ch-2   = Audio Destination Ch-1
Audio Destination Ch-2 = Audio Source Ch-1
NOTE: In full-duplex mode, it is not possible to have multiple output ports enabled for either channel. Each channel will have only one output port.

The host may start writing input data to the Audio In FIFO, if either Ch-1 or Ch-2 is to use the Audio In FIFO as its audio source port.

Automatic internal setting:
Input Type Ch-2 = Output Type Ch-1
Output Type Ch-2 = Input Type Ch-1

The device will automatically start the specified transcoding operation once there is enough data in the Input buffer to process either channel.
If there is not enough input data to process one of the channels, only that channel is stalled. The other channel is processed as normal.

Has the Audio Output FIFO LEVEL or COUNT interrupt occurred? — No

Yes

Read output data for Ch-2 from Audio Out FIFO. Ch-1 output data will be serviced through Analogue Out port

Transcode another frame? — Yes / No

Go to Idle mode

Figure 28 Full duplex Transcoder Operation Flowchart

Step No.	C-BUS Operation	Action	Description
1	Write $8080 to FIFO Control - $50 write	Flush the audio in and audio out FIFO	To ensure that no data is remaining from any previous transcoding operation
2	Write $0011 to the Input Type - $54 write register	Specify the input data type for Ch-1	Specifies the format of the input data that the CMX7261 expects for Ch-1. In this case, the input data type for Ch-1 is specified as G.711 A-law packed data. This action automatically sets the output data type for Ch-2 as G.711 A-law packed data.
3	Write $0004 to the Output Type - $56 write register	Specify the Output data type for Ch-1	Specifies the format of the output data expected from CMX7261 for Ch-1. In this case, the expected output data type is specified as 16-bit linear PCM samples at 8KHz. This action automatically sets the input data type for Ch-2 as 16-bit linear PCM samples at 8KHz.
4	Write $0120 to the Mode - $6B write register	Specify Audio Source and Audio Destination for Ch-1	Specifies the input and output ports for Ch-1. Here input port for Ch-1 is set to Audio In FIFO and output port for Ch-1 is set to Analogue Out. This action automatically sets the input port for Ch-2 to Analogue In and output port for Ch-2 to Audio Out FIFO.
5	Write G.711A packed data words to the Audio In FIFO for Ch-1. Simultaneously, provide Analogue In audio input for Ch-2	Prime the Input buffer with a frame of data, for both Ch-1 and Ch-2	This provides a buffer samples for the CMX7261 to start full-duplex transcoding operation on request.
6	Write $0505 to the FIFO Count Interrupt - $51 write register	Specify when the host should be interrupted	This tells the CMX7261 to interrupt the host when it has written 5 new data words to the Audio Out FIFO, or read 5 words from the Audio In FIFO.
7	Write $0123 to the Mode - $6B write register	Start full-duplex transcoding	Commands the CMX7261 to start full-duplex transcoding operation. If there is not enough data in the Input buffer for either channel, only that channel's processing is stalled. The other channel is processed as normal. The stalled channel's processing resumes when there is enough input data is present for that channel.
8	Check the IRQ Status - $7E read register for bits 2 or 3 – Count_Out or Count_In interrupts	Count_Out:Indicates an output frame is available	The input data has been transcoded into the desired format, and the host can now read a frame of data from the Audio Out FIFO.
		Count_In: Indicates that a frame of input data has been read	There is now space for a further 5 words, of G.711 A-law packed words to be written to the Audio In FIFO. This should be done promptly to ensure uninterrupted transcoding.
9	Continue Transcoding		Repeat steps 8 as required

The procedure described above can be adapted, to achieve different transcoding modes, with different input and output ports. Full-duplex Transcoding from G.711 A-law packed data to analogue audio and vice-versa will continue as long as there is enough input data and the mode bits (b1-0) of the Mode - $6B write register have changed. The registers used for basic operation are:

- Mode - $6B write
- Input Type - $54 write
- Output Type - $56 write
- IRQ Status - $7E read
- Audio In FIFO Data - $48, $49 write
- Audio Out FIFO Data - $4C, $4D read
- FIFO Count Interrupt - $51 write
- FIFO Control - $50 write

7.7.3 Device Configuration (Using the Programming Register)

While in idle mode the Programming register becomes active providing access to the Program Blocks. Program Blocks allow configuration of the CMX7261. Features that can be configured include:

- Configuration of PCM Port rate and word format
- Configuration of the CMX7261 to operate with a non-default XTAL input frequency
- Configuration of the VAD block.

Full details of how to configure these aspects of device operation are given in section 10 in the User Manual.

7.7.4 Device Configuration (Using dedicated registers)

Some device features may be configured using dedicated registers. This allows for configuration outside of idle mode. Configuration of the following features is possible:

- Gain, power saving and muting of the analogue audio output
- Gain, power saving and muting of the analogue audio input
- Gain and muting of any linear PCM output signal
- Gain and muting of any linear PCM input signal.

The registers that allow configuration of these features are:

- ANAIN Coarse Gain - $B1 write
- ANAOUT Coarse Gain - $B4 write
- ANAOUT Config - $B3 write
- ANAIN Config - $B0 write.

7.7.5 Interrupt Operation

The CMX7261 can produce an interrupt output when various events occur. Examples of such events include FIFO fill levels being reached or an output overflow when processing audio data.

Each event has an associated Status register bit and an Interrupt Mask register bit. The interrupt mask register is used to select which status events will trigger an interrupt on the IRQN line. Events can be masked using the IRQ mask bit (bit 15) or individually masked using the Interrupt Mask register. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause an interrupt on the IRQN line. The IRQ bit (bit 15) of the Status register reflects the IRQN line state.

All interrupt flag bits in the Status register are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. See:

- IRQ Status - $7E read
- IRQ Enable - $6C write.

7.7.6   PCM Port

The CMX7261 features a PCM port, which can be used to communicate with an external PCM codec. This can be used as an alternative to the internal ADC and DAC converters. The PCM port can be used for input, output or both, and can be configured for wide range of modes, sample rates and word formats via the programming register. Once configured and enabled, via the mode register, the PCM port operates automatically, transferring data between the CMX7261 and the external PCM codec.

In addition, there is the facility to send configuration or other data words to the external PCM device. There is no facility to read back responses to these configuration words.

See:
- 10.1.3 Program Block 2 – PCM Port Config
- 9.1.22 PCM Talkthrough Data - $63 write

7.8   Signal Level Optimisation

The internal signal processing of the CMX7261 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V supply, the signal range which can be accommodated without distortion is specified in 8.1.3 Operating Characteristics. Signal gain and dc offset can be manipulated as follows:

7.8.1   Audio Output Path Levels

The signals output from ANAOUT and MONOUT have independent gain controls. The Fine Output adjustment has a maximum attenuation of 6dB and no gain, whereas the Coarse Output adjustment has a variable attenuation of up to 14.2dB and 6dB gain.

The ANAOUT and MONOUT signals may be independently inverted. Inversion is achieved by selecting a negative value for the (linear) Fine Output adjustment.

See:

- 9.1.31 ANAOUT Coarse Gain - $B4 write.
- 9.1.31 ANAOUT Config - $B3 write.

7.8.2   Audio Input Path Levels

The Coarse Input has a variable gain of up to +22.4dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the ANAIN pins is specified in section 8.1.3 Operating Characteristics.

A Fine Input level adjustment is provided, although the CMX7261 should operate correctly with the default level selected. Inversion is achieved by selecting a negative value for the (linear) Fine Input gain adjustment.

It should be noted that if the maximum allowable signal input level is exceeded, signal distortion will occur regardless of the internal attenuation.

See:

- 9.1.14 Fine Gain Channel-1 - $5B write.
- 9.1.15 Fine Gain Channel-2 - $5C write.
- 9.1.28 ANAIN Config - $B0 write.
- 9.1.29 ANAIN Coarse Gain - $B1 write.

7.9 C-BUS Register Summary

ADDR. (hex)	Read/ Write	REGISTER	Word Size (bits)	User Manual Page	Section
$01	W	C-BUS RESET	0	69	9.1.2
$48	W	Audio In FIFO Data Byte	8	70	9.1.3
$49	W	Audio In FIFO Data Word	16	70	9.1.3
$4B	R	Audio In FIFO Level	8	70	9.1.4
$4C	R	Audio Out FIFO Data Byte	8	70	9.1.5
$4D	R	Audio Out FIFO Data Word	16	70	9.1.5
$4F	R	Audio Out FIFO Level	8	70	9.1.6
$50	W	FIFO Control	16	71	9.1.7
$51	W	FIFO Count Interrupt	16	71	9.1.8
$54	W	Input Type	16	72	9.1.9
$56	W	Output Type	16	73	9.1.10
$58	W	Signal Control	16	74	9.1.11
$59	W	VAD Threshold Channel-1	16	75	9.1.12
$5A	W	VAD Threshold Channel-2	16	75	9.1.13
$76	R	VAD Level Channel-1	16	76	9.1.16
$77	R	VAD Level Channel-2	16	76	9.1.17
$7A	R	VAD Signal to Noise Transition Delay Ch-1	16	77	9.1.18
$7B	R	VAD Signal to Noise Transition Delay Ch-2	16	77	9.1.19
$7C	R	VAD Noise to Signal Transition Delay Ch-1	16	77	9.1.20
$7D	R	VAD Noise to Signal Transition Delay Ch-2	16	77	9.1.21
$5B	W	Fine Gain Channel-1	16	76	9.1.14
$5C	W	Fine Gain Channel-2	16	76	9.1.15
$63	W	PCM Talkthrough Data	16	77	9.1.22
$64	W	GPIO Control	16	78	9.1.23
$79	R	GPIO Input	16	84	9.1.35
$69	W	Reg Done Select	16	78	9.1.24
$6A	W	Programming Register	16	78	9.1.25
$6B	W	Mode	16	79	9.1.26
$6C	W	IRQ Enable	16	81	9.1.27
$7E	R	IRQ Status	16	85	9.1.36
$7F	R	Mode Register Readback	16	86	9.1.37
$B0	W	ANAIN Config	16	81	9.1.28
$B1	W	ANAIN Coarse Gain	16	82	9.1.29
$B3	W	ANAOUT Config	16	82	9.1.30
$B4	W	ANAOUT Coarse Gain	16	83	9.1.31
$B5	W	MONOUT Coarse Gain	16	83	9.1.32
$B6	W	SPKR Coarse Gain	16	83	9.1.33
$B7	W	Bias Control	16	83	9.1.34

Table 4 C-BUS Registers

All other C-BUS addresses are reserved and must not be accessed.

8   Performance Specification

8.1   Electrical Performance

8.1.1   Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Power Supplies			
DV_{DD} - DV_{SS}	-0.3	4.0	V
DV_{CORE} - DV_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
SPKR1 V_{DD} – SPKR1 V_{SS}	-0.3	4.0	V
Voltage on any pin to V_{SS}	-0.3	IOV_{DD} + 0.3	V
Current into or out of any pin, except power supply pins, SPKR1P and SPKR1N	-20	20	mA
Current into or out of power supply pins, SPKR1P and SPKR1N	-120	120	mA

Q1 Package (64-pin VQFN)	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25ºC		3500	mW
... Derating		35.0	mW/ºC
Storage Temperature	-55	+125	ºC
Operating Temperature	-40	+85	ºC

L9 Package (64-pin LQFP)	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25ºC		1690	mW
... Derating		16.9	mW/ºC
Storage Temperature	-55	+125	ºC
Operating Temperature	-40	+85	ºC

8.1.2   Operating Limits
Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
DV_{DD} - DV_{SS}	3.0	3.3	3.6	V
DV_{CORE} - DV_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
SPKR1 V_{DD} – SPKR1 V_{SS}	3.0	3.3	3.6	V
Operating Temperature	-40	–	+85	°C
Xtal Frequency	4.0	–	12.288	MHz
External Clock Frequency	9.6	–	24.576	MHz

Notes:
> DV_{DD} = AV_{DD} = SPKR1 V_{DD} = "IOV_{DD}"
> DV_{SS} = AV_{SS} = SPKR1 V_{SS} = "V_{SS}"

8.1.3   Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Section 5, External Components.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 9.6MHz$\pm$0.01% (100ppm); Tamb = $-$40°C to +85°C.
$AV_{DD} = DV_{DD}$ = 3.0V to 3.6V.
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

Current consumption figures quoted in this section apply to the device only when loaded with CMX7261 FI-1.3.0.0. Current consumption may vary with Function Image™.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	20				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		-40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	22	-1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current	22	-1.0	–	1.0	µA
V_{BIAS}	21				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	50	–	kΩ

Notes:

20   Characteristics when driving the XTAL/CLK pin with an external clock source.

21   Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Section 5 External Components.

22   Tamb = 25°C, not including any current drawn from the device pins by external circuitry.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		30	15	–	–	ns
'Low' Pulse Width		30	15	–	–	ns
Input Impedance (at 9.6MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
V$_{BIAS}$						
Start-up Time (from powersave)			–	30	–	ms
Single-Ended ANAIN2 Input						
Input Impedance		31	–	> 10	–	MΩ
Input voltage range		34	–	–	20 to 80	%AV$_{DD}$
Load resistance (on pin 24)			47	–	–	kΩ
Amplifier open loop voltage gain						
(I/P = 1mV rms at 100Hz)			–	80	–	dB
Unity gain bandwidth			–	1.0	–	MHz
Differential ANAIN Input						
Input Impedance, enabled		31	10	–	140	kΩ
Input Impedance, muted or powersaved			–	200	–	kΩ
Input Voltage Range		32	–	–	20 to 80	%AV$_{DD}$
Programmable Input Gain Stage						
Gain (at 0dB)		33	-0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		33	-1.0	0	+1.0	dB

Notes:

30   Timing for an external input to the XTAL/CLOCK pin.
31   With no external components connected.
32   Centered about AV$_{DD}$/2; after multiplying by the gain of input circuit (with external components connected).
33   Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.
34   Voltage range at the feedback pin to ensure input buffer does not limit.

AC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
Differential ANAOUT Output					
Power-up to Output Stable	40	–	50	100	µs
ANAOUT Output Coarse Gain Attenuator					
Attenuation (at 0dB)		-0.2	0	+0.2	dB
Cumulative Attenuation Error (w.r.t. attenuation at 0dB)		-0.6	0	+0.6	dB
Output Impedance	41	–	600	–	Ω
Output Voltage Range	43	0.3	–	AV_{DD}-0.3	V
Load Resistance		20	–	–	kΩ
SPKR1 Speaker Output, SPKR2 Earpiece Output					
Power-up to Output Stable	40	–	50	100	µs
SPKR1, SPKR2 Output Coarse Gain Attenuator					
Attenuation (at 0dB)		-0.5	0	0.5	dB
Cumulative Attenuation Error (w.r.t. attenuation at 0dB)		-1.0	0	1.0	dB
Output Power (SPKR1 Outputs)	44	–	–	140	mW
Output Voltage Range (SPKR1 Outputs)	45, 46	0.75	–	$AV_{DD} - 0.75$	V
Output Voltage Range (SPKR2 Outputs)	47	0.5	–	$AV_{DD} - 0.5$	V
Resistance					
SPKR1 Speaker Output	41	8	–	–	Ω
SPKR2 Earpiece Output	41	32	–	–	Ω

Notes:

40   Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

41   Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43   Centered about AV_{DD}/2; with respect to the output driving a 20kΩ load to AV_{DD}/2.

44   Differential power output into a 8Ω load at AV_{DD} = 3.0V.

45   For each output pin.

46   With respect to the outputs driving a differential load of 8Ω.

47   With respect to the output driving a 32Ω load to AV_{DD}/2.

8.1.4   CMX7261: 7261 FI-1.x Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in section 5.

Maximum load on digital outputs = 30pF.

Clock source = 19.2MHz ±0.01% (100ppm) external clock input; Tamb = −40°C to +85°C.

$AV_{DD} = DV_{DD}$ = 3.0V to 3.6V.

Reference signal level = 308mV rms at 1kHz with AV_{DD} = 3.3V

Signal levels track with supply voltage, so scale accordingly.

Signal to Noise Ratio (SNR) in bit rate bandwidth.

Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device only when loaded with 7261FI-1.3.0.0. The use of other Function Images™ can modify the parametric performance of the device. Current consumption may vary with Function Image™.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	50				
Idle mode					
DI_{DD}	51	–	670	–	µA
AI_{DD}	52	–	17	–	µA
Transcoding mode					
G.729A Decoder	53	–	7.7	–	mA
G.729A Encoder	53	–	19.7	–	mA
CVSD Decoder	54	–	4.4	–	mA
CVSD Encoder	55	–	4.5	–	mA
G.711 A-law Encoder	53	–	4.7	–	mA
G.711 A-law Decoder	53	–	4.6	–	mA
Additional current for activating Analogue In port					
DI_{DD}		–	4.4	–	mA
AI_{DD}		–	3.3	–	mA
Additional current for activating Analogue Out port					
DI_{DD}		–	0.3	–	mA
AI_{DD}		–	7.8	–	mA

Notes:

50   Tamb = 25°C, not including any current drawn from the device pins by external circuitry.

51   Using external clock input, XTAL oscillator circuit powered down, and all GPIOs set to output and low using the GPIO Control - $64 write register.

52   All analogue sections are powered down by setting both ANAIN Config - $B0 write and ANAOUT Config - $B3 write registers to 0.

53   Audio source is set to Audio In FIFO, Audio destination is set to Audio Out FIFO in the Mode - $6B write register.
Input rate is set to 8kHz in Input Type - $54 writeregister and Output rate is set to 8kHz in the Output Type - $56 write register.

54   Audio source is set to Audio In FIFO, Audio destination is set to Audio Out FIFO in the Mode - $6B write register.
Input rate is set to 16kHz in Input Type - $54 write register and Output rate is set to 8kHz in the Output Type - $56 write register.

55   Audio source is set to Audio In FIFO, Audio destination is set to Audio Out FIFO in the Mode - $6B write register.
Input rate is set to 8kHz in Input Type - $54 write register and Output rate is set to 16kHz in the Output Type - $56 write register.

8.1.5   CVSD Typical Performance

Figure 29 and Figure 30 show the typical frequency response of the CVSD algorithm. This is the response seen, when an input signal sampled at 8kHz is encoded (into either 16kbps CVSD or 32kbps CVSD) and the encoded bit stream is decoded back to linear PCM signal at a sampling rate of 8kHz. For more details about the operation of CVSD algorithm, refer to section 7.4.3 CVSD.
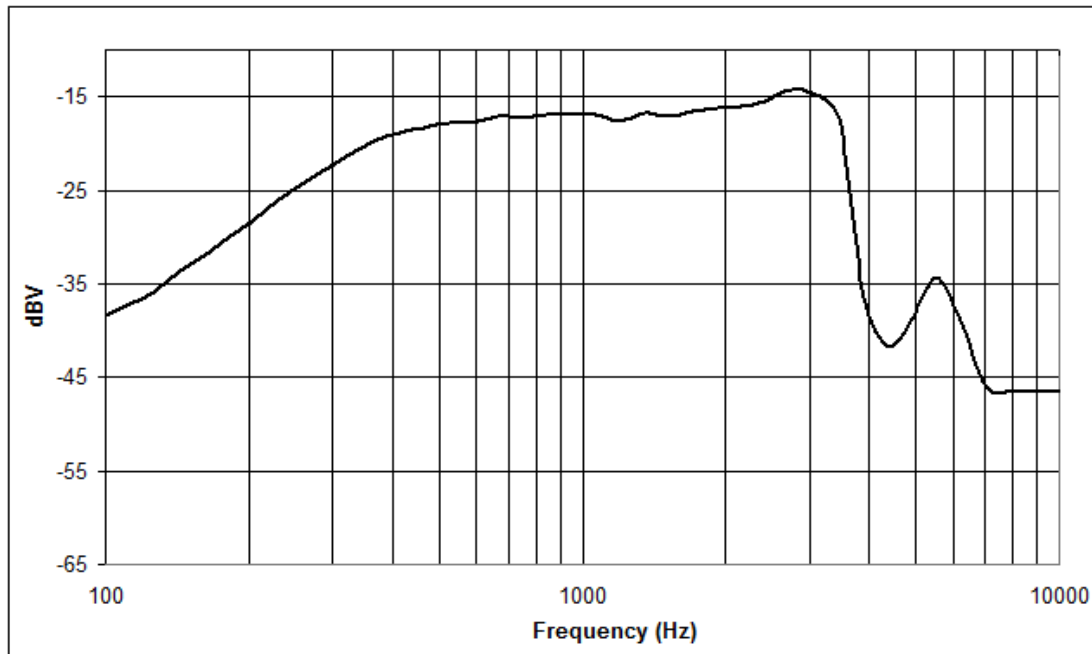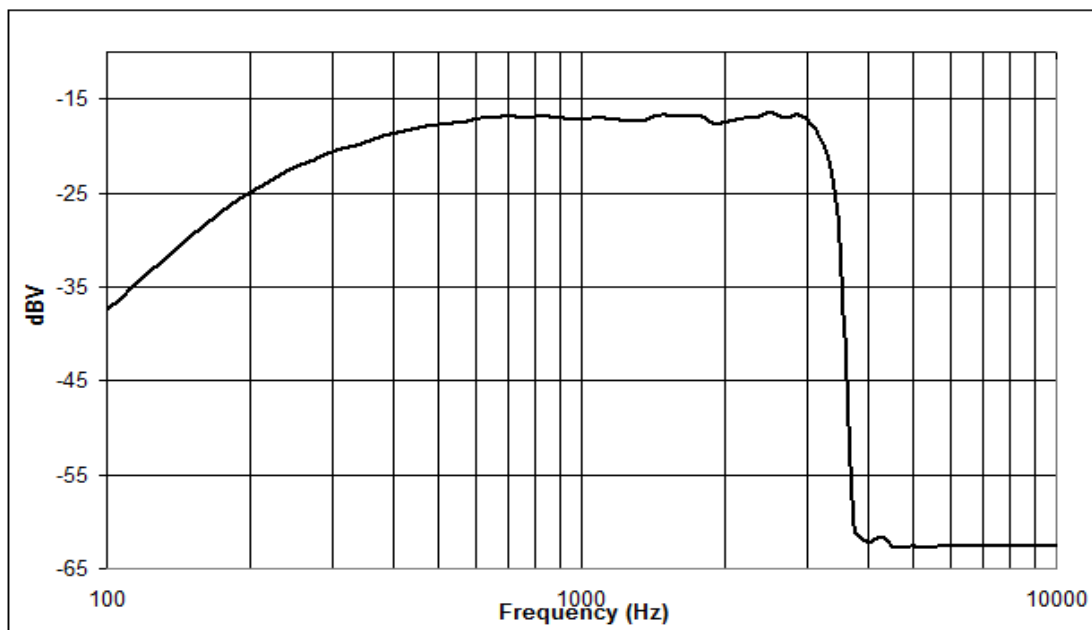

Figure 29 CVSD 16kbps Frequency Response

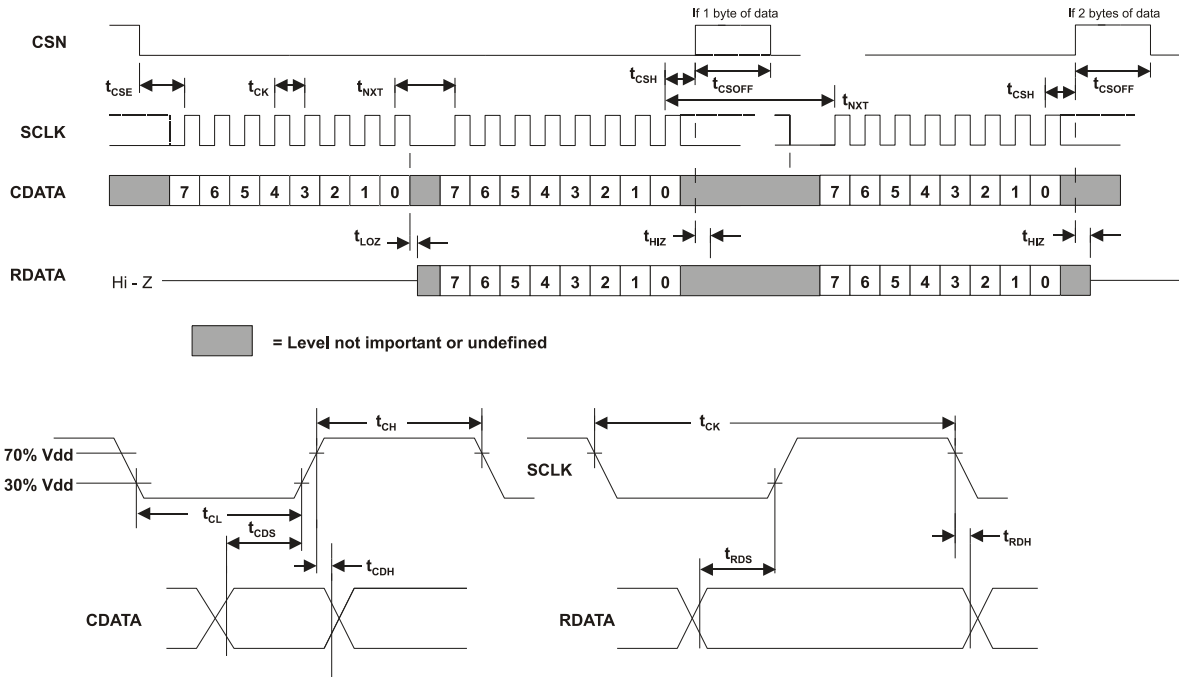**Figure 30 CVSD 32kbps Frequency Response**

8.2   C-BUS Timing

Figure 31 C-BUS Timing

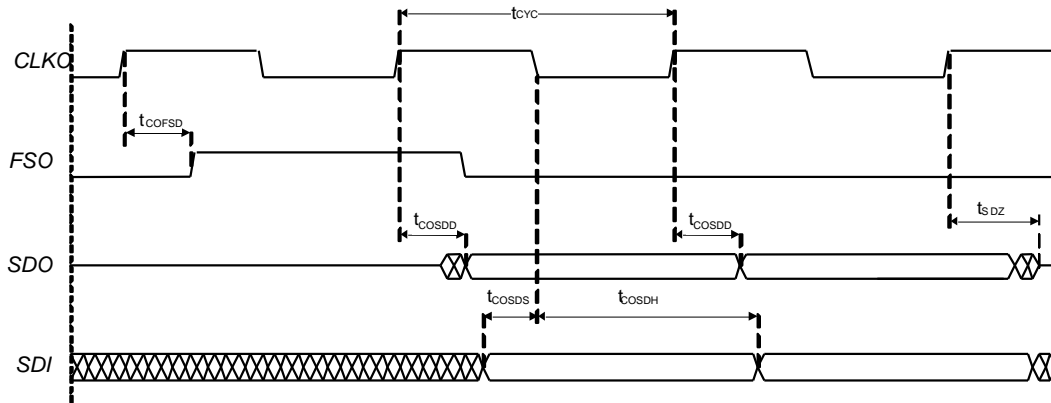| C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA output enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		100	–	–	ns
t_{CK}	SCLK cycle time		100	–	–	ns
t_{CH}	SCLK high time		50	–	–	ns
t_{CL}	SCLK low time		50	–	–	ns
t_{CDS}	CDATA set-up time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA set-up time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes: 1.   Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2.   Data is clocked into the peripheral on the rising SCLK edge.
3.   Commands are acted upon at the end of each command (rising edge of CSN).
4.   To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5.   Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7261 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

8.3   PCM Port Timing

8.3.1   PCM Internal Clock

PCM Master; Internal Clock Generator
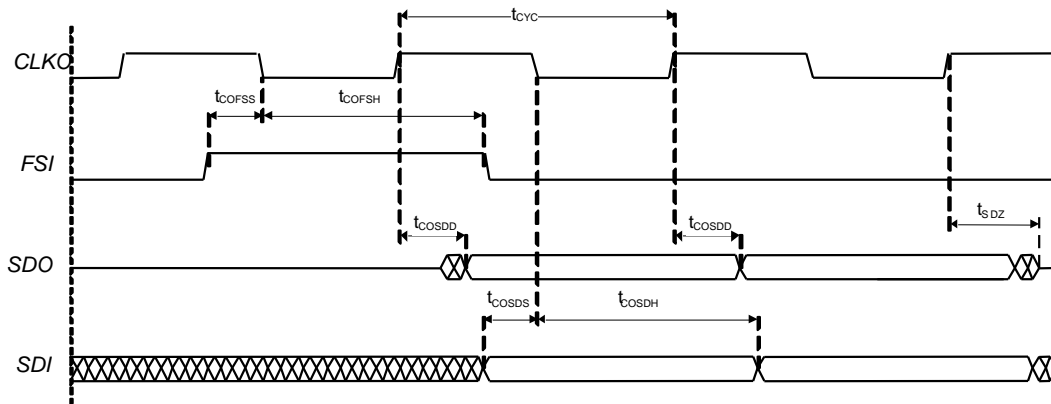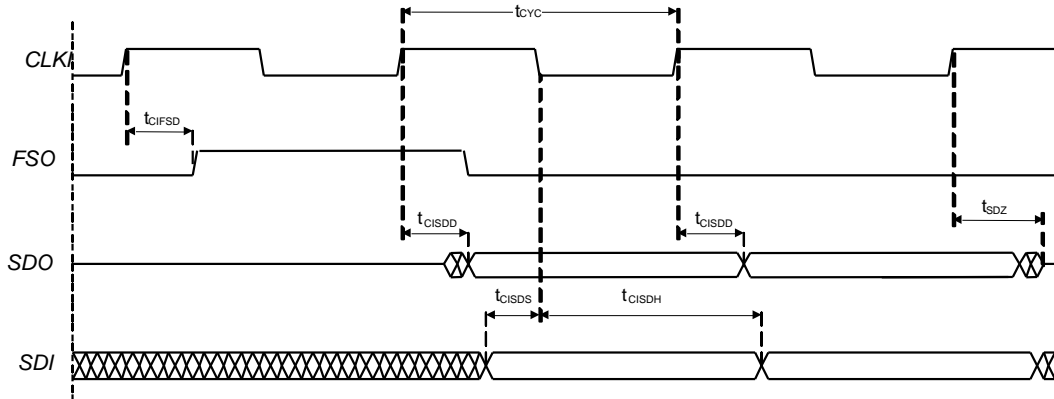
PCM Slave; Internal Clock Generator

Figure 32   PCM Internal Clock Timings

PCM Internal Clock Timings		Notes	Min.	Typ.	Max.	Units
t_{CYC}	CLKO or CLKI cycle time	2	150	-	-	ns
t_{COFSD}	CLKO to FSO delay		-15	0	+15	ns
t_{COSDD}	CLKO to SDO delay		-15	0	+15	ns
t_{COSDS}	CLKO to FSO delay		8	-	-	ns
t_{COSDH}	CLKO to FSO delay		7	-	-	ns
t_{SDZ}	CLKO or CLKI to SDO tristate	1	-14	10	37	ns

8.3.2   PCM External Clock

PCM Master; External Clock Generator
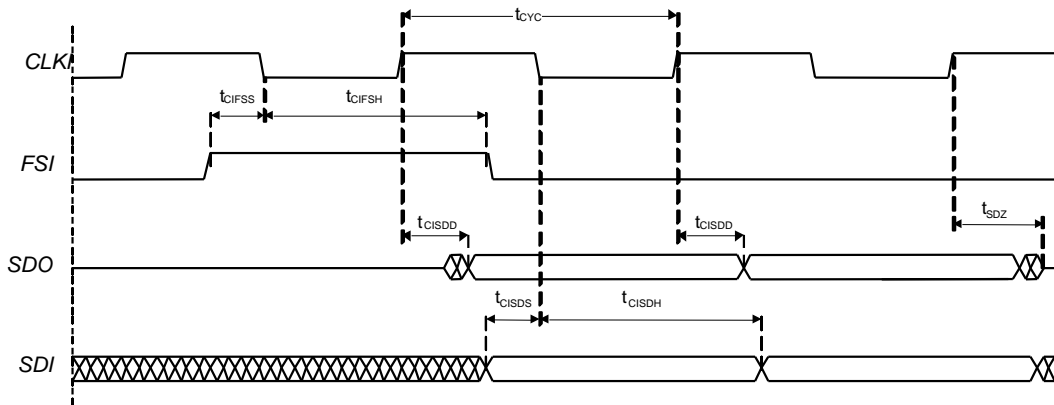

PCM Slave; External Clock Generator

Figure 33   PCM External Clock Timings

PCM External Clock Timings		Notes	Min.	Typ.	Max.	Units
t_{CYC}	CLKO or CLKI cycle time	2	150	-	-	ns
t_{CIFSD}	CLKI to FSO delay		2	0	42	ns
t_{CISDD}	CLKI to SDO delay		2	0	42	ns
t_{CISDS}	CLKI to FSO delay		8	-	-	ns
t_{CISDH}	CLKI to FSO delay		7	-	-	ns
t_{SDZ}	CLKI or CLKO to SDO tristate	1	-14	10	37	ns

8.4   Packaging

DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 34 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7261Q1

DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
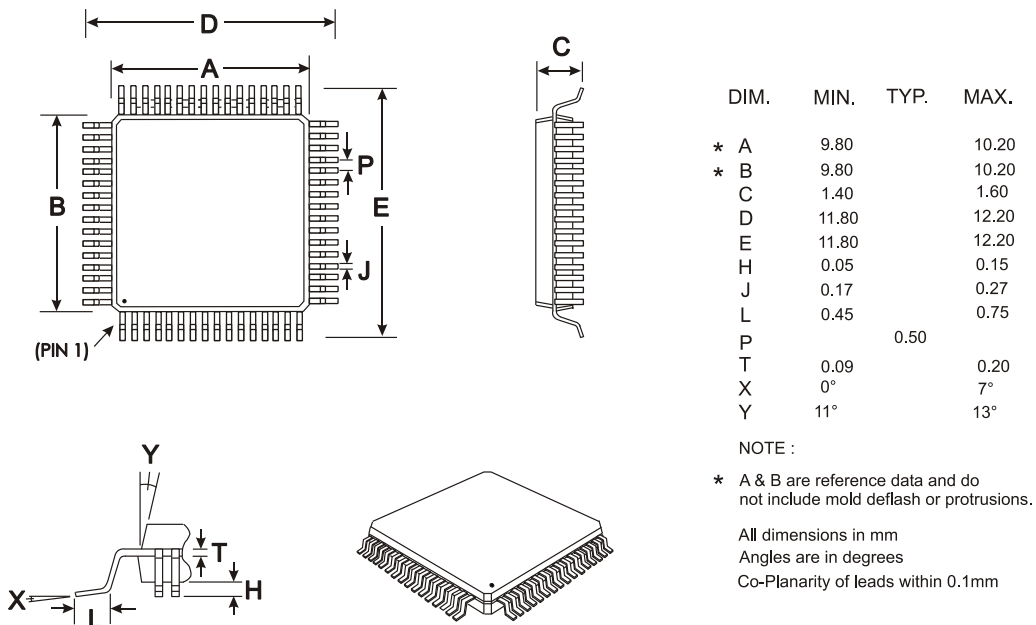Co-Planarity of leads within 0.1mm

Figure 35 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7261L9

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [www.cmlmicro.com].

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