PCA9536 Remote 4-Bit I²C and SMBus I/O Expander With Configuration Registers

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Low Standby Current Consumption of 1 μA Max
- I²C to Parallel Port Expander
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5-V Tolerant I/O Ports
- 400-kHz Fast I²C Bus
- Input/Output Configuration Register
- Polarity Inversion Register
- Internal Power-On Reset
- No Glitch on Power Up
- Power-Up With All Channels Configured as Inputs
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High-Current Drive Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Description

This 4-bit I/O expander for the two-line bidirectional bus (I²C) is designed for 2.3-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I²C interface [serial clock (SCL), serial data (SDA)].

The PCA9536 features 4-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs with a weak pullup to V_{CC}. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. If no signals are applied externally to the PCA9536, the voltage level is 1, or high, because of the internal pullup resistors. The data for each input or output is stored in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

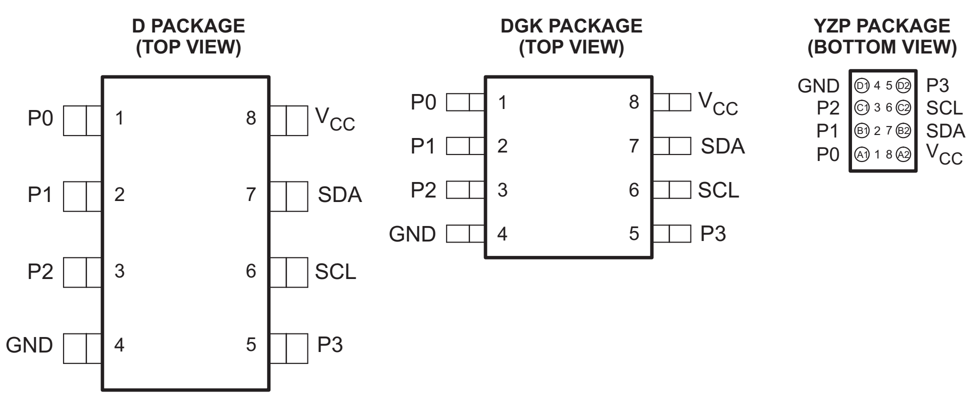
The system master can reset the PCA9536 in the event of a timeout or other improper operation by utilizing the power-on reset feature, which puts the registers in their default state and initializes the I²C/SMBus state machine.

The device's outputs (latched) have high-current drive capability for directly driving LEDs. It has low current consumption.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCA9536	GSBGA (8)	1.90 mm × 0.90 mm
	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



See mechanical drawings for dimensions.

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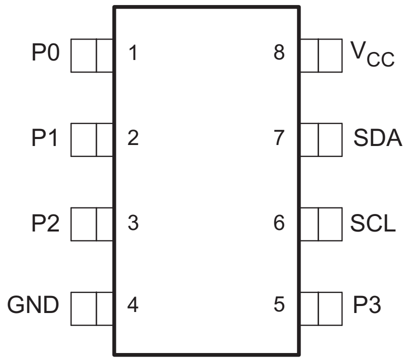
3 Revision History

Changes from Revision F (September 2008) to Revision G **Page**

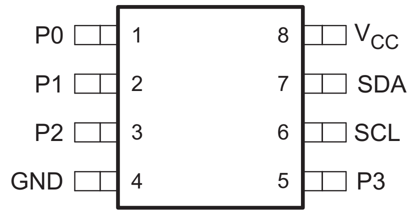
- Added Power-On Reset Errata section. 20

4 Pin Configuration and Functions

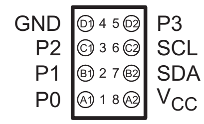
**D PACKAGE
(TOP VIEW)**



**DGK PACKAGE
(TOP VIEW)**



**YZP PACKAGE
(BOTTOM VIEW)**



See mechanical drawings for dimensions.

Pin Functions

NO.	NAME	DESCRIPTION
1	P0	P-port input/output. Push-pull design structure.
2	P1	P-port input/output. Push-pull design structure.
3	P2	P-port input/output. Push-pull design structure.
4	GND	Ground
5	P3	P-port input/output. Push-pull design structure.
6	SCL	Serial clock bus. Connect to V_{CC} through a pullup resistor.
7	SDA	Serial data bus. Connect to V_{CC} through a pullup resistor.
8	V_{CC}	Supply voltage

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range(2)		–0.5	6	V
V_O	Output voltage range(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–200	mA
	Continuous current through V_{CC}			160	
θ_{JA}	Package thermal impedance(3)	D package		97	°C/W
		DGK package		172	
		YZP package		102	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		P3–P0	2	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	$0.3 \times V_{CC}$	V
		P3–P0	–0.5	0.8	
I_{OH}	High-level output current	P3–P0		–10	mA
I_{OL}	Low-level output current	P3–P0		25	mA
T_A	Operating free-air temperature		–40	85	°C

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[(1)]	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	2.3 V to 5.5 V	–1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, I_O = 0	V_{POR}		1.5	1.65	V
V_{OH}	P-port high-level output voltage[(2)]	I_{OH} = –8 mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	4.1			
			4.75 V	4.1			
		I_{OH} = –10 mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	10		mA
	P-port[(3)]	V_{OL} = 0.5 V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	32		
		V_{OL} = 0.7 V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	44		
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	μA
I_{IH}	P-port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	μA
I_{IL}	P-port	V_I = GND	2.3 V to 5.5 V			–100	μA
I_{CC}	Operating mode	$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{scl} = 400 kHz	5.5 V		73	150	μA
			3.6 V		9	50	
			2.7 V		7	30	
		$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{scl} = 100 kHz	5.5 V		14	25	
			3.6 V		9	20	
			2.7 V		6	15	
	Standby mode	V_I = GND, I_O = 0, I/O = inputs, f_{scl} = 0 kHz	5.5 V		225	350	
			3.6 V		175	250	
			2.7 V		125	200	
		$V_I = V_{CC}$, I_O = 0, I/O = inputs, f_{scl} = 0 kHz	5.5 V		0.25	1	
			3.6 V		0.2	0.9	
			2.7 V		0.1	0.8	
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			0.35	mA
		Every LED I/O at V_I = 4.3 V, f_{scl} = 0 kHz	5.5 V			0.4	
C_i	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4	5	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		5	6.5	pF
	P-port				7.5	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be limited externally to a maximum of 25 mA, and the P-port (P3–P0) must be limited to a maximum current of 100 mA.

5.5 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 14)

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency	0	100	0	400	kHz
t_{sch}	I²C clock high time	4		0.6		μs
t_{scl}	I²C clock low time	4.7		1.3		μs
t_{sp}	I²C spike time		50		50	ns
t_{sds}	I²C serial-data setup time	250		100		ns
t_{sdh}	I²C serial-data hold time	0		0		ns
t_{icr}	I²C input rise time		1000	$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I²C input fall time		300	$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I²C output fall time, 10-pF to 400-pF bus		300	$20 + 0.1C_b$ (1)	300	ns
t_{buf}	I²C bus free time between Stop and Start	4.7		1.3		μs
t_{sts}	I²C Start or repeated Start condition setup time	4.7		0.6		μs
t_{sth}	I²C Start or repeated Start condition hold time	4		0.6		μs
t_{sps}	I²C Stop condition setup time	4		0.6		μs
$t_{vd(data)}$	Valid data time, SCL low to SDA output valid		1		0.9	μs
$t_{vd(ack)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1		0.9	μs
C_b	I²C bus capacitive load		400		400	pF

(1) C_b = Total capacitive load of one bus in pF

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 15)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{pv}	Output data valid	SCL	P3–P0		200		200	ns
t_{ps}	Input data setup time	P-port	SCL	100		100		ns
t_{ph}	Input data hold time	P-port	SCL	1		1		μs

5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)

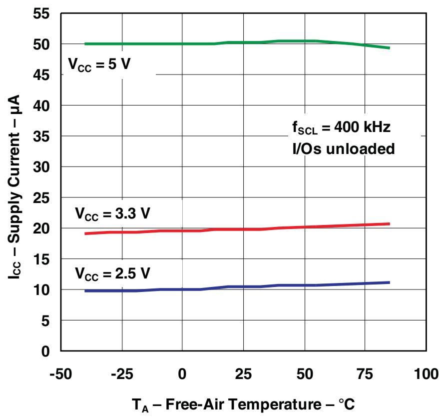


Figure 1. Supply Current vs Temperature

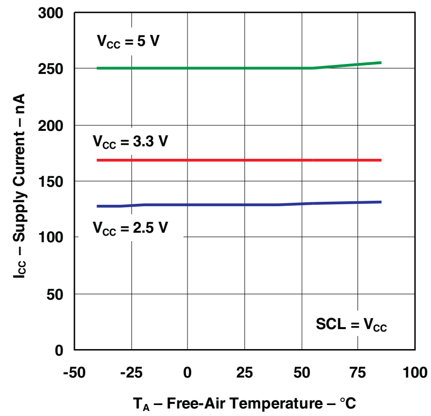


Figure 2. Quiescent Supply Current vs Temperature

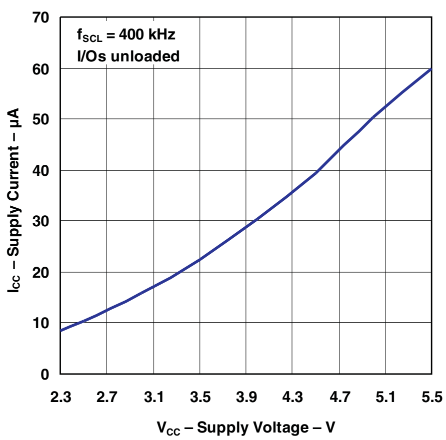


Figure 3. Supply Current vs Supply Voltage

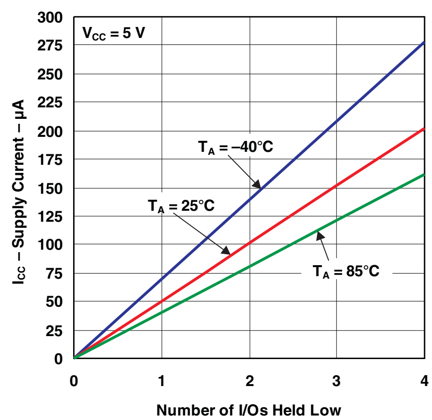


Figure 4. Supply Current vs Number of I/Os Held Low

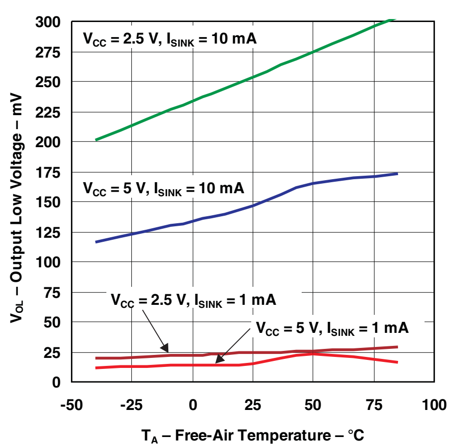


Figure 5. I/O Output Low Voltage vs Temperature

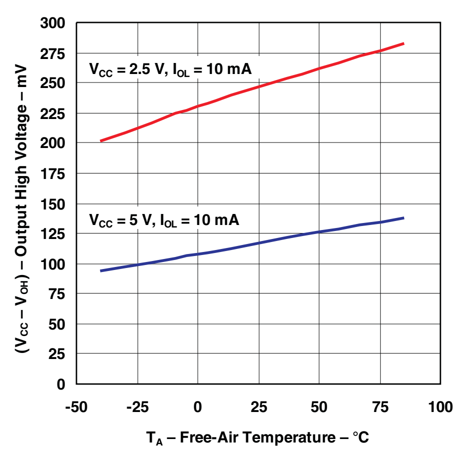


Figure 6. I/O Output High Voltage vs Temperature

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

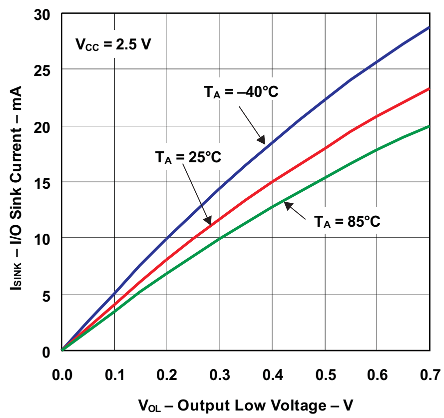


Figure 7. I/O Sink Current vs Output Low Voltage

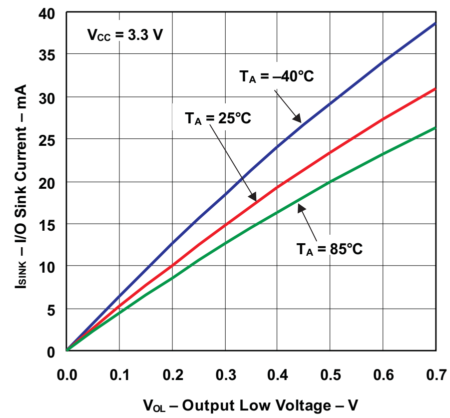


Figure 8. I/O Sink Current vs Output Low Voltage

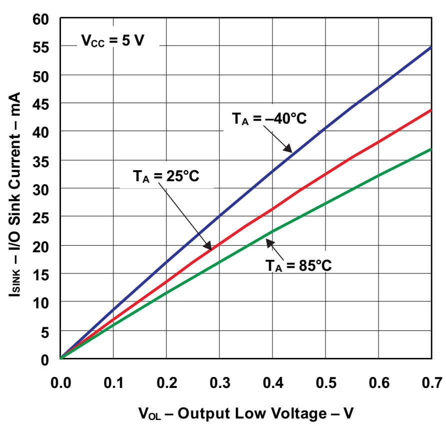


Figure 9. I/O Sink Current vs Output Low Voltage

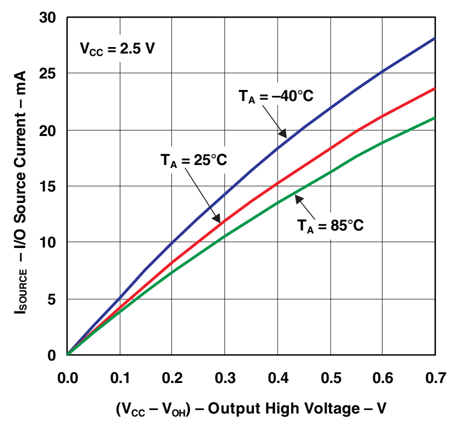


Figure 10. I/O Source Current vs Output High Voltage

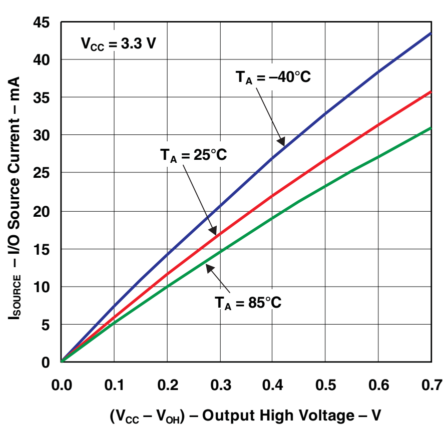


Figure 11. I/O Source Current vs Output High Voltage

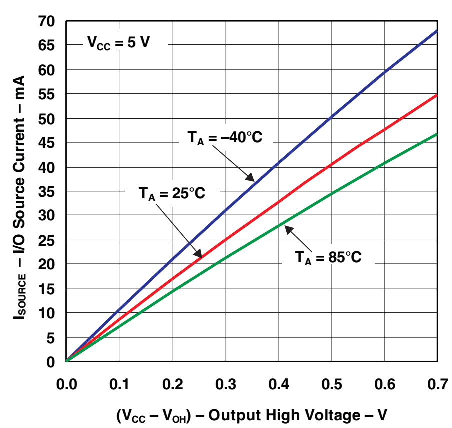


Figure 12. I/O Source Current vs Output High Voltage

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

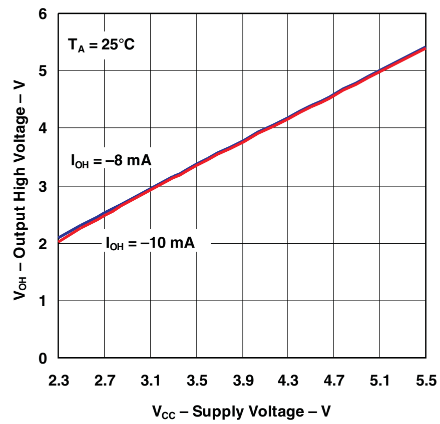
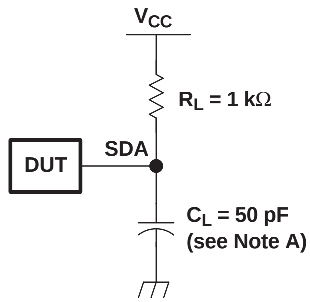
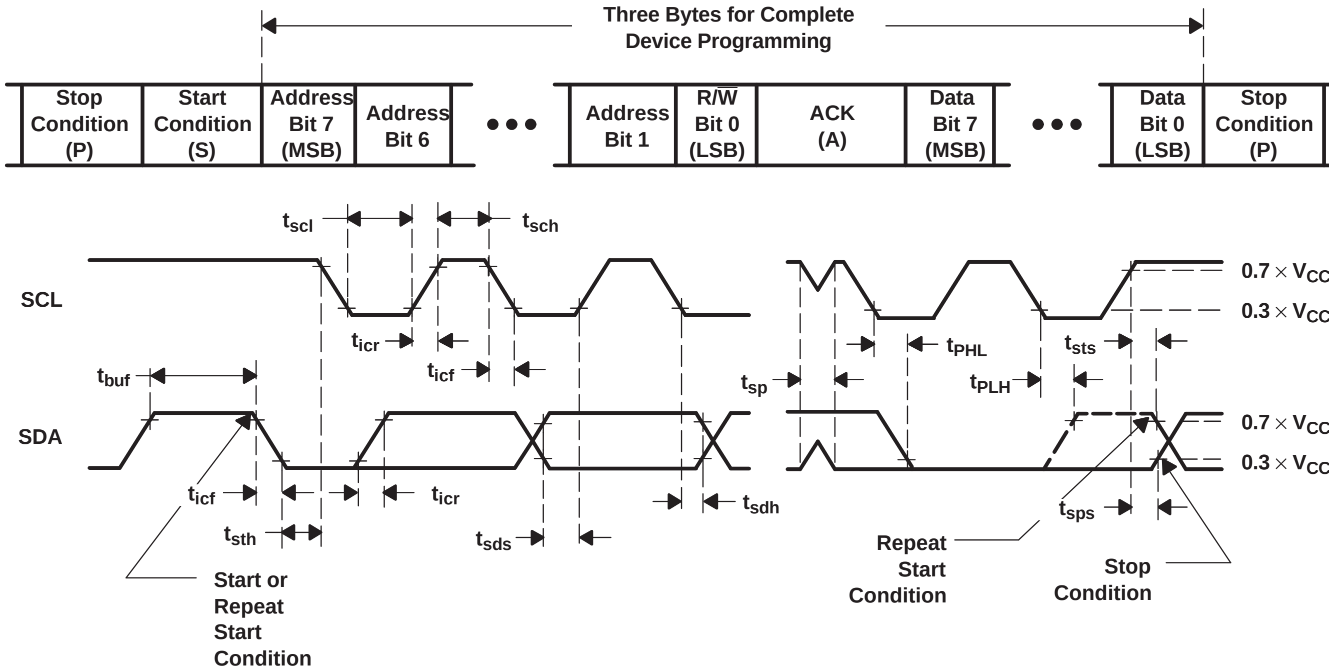


Figure 13. Output High Voltage vs Supply Voltage

6 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

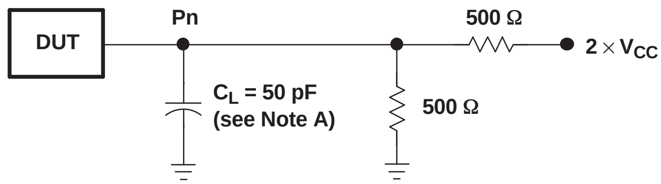
A. C_L include probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

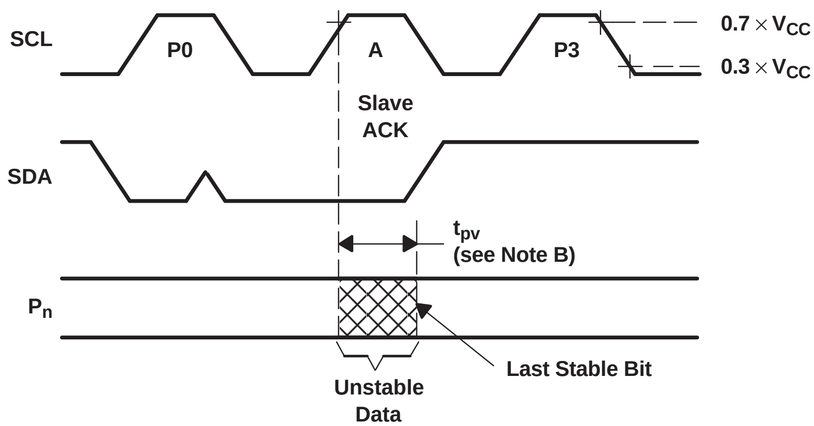
C. All parameters and waveforms are not applicable to all devices.

Figure 14. I^2C Interface Load Circuit and Voltage Waveforms

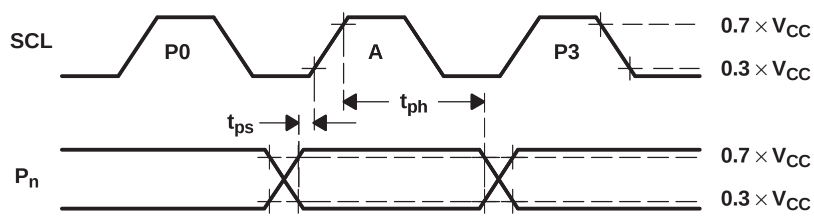
Parameter Measurement Information (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L include probe and jig capacitance.

B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.

C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 15. P-Port Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

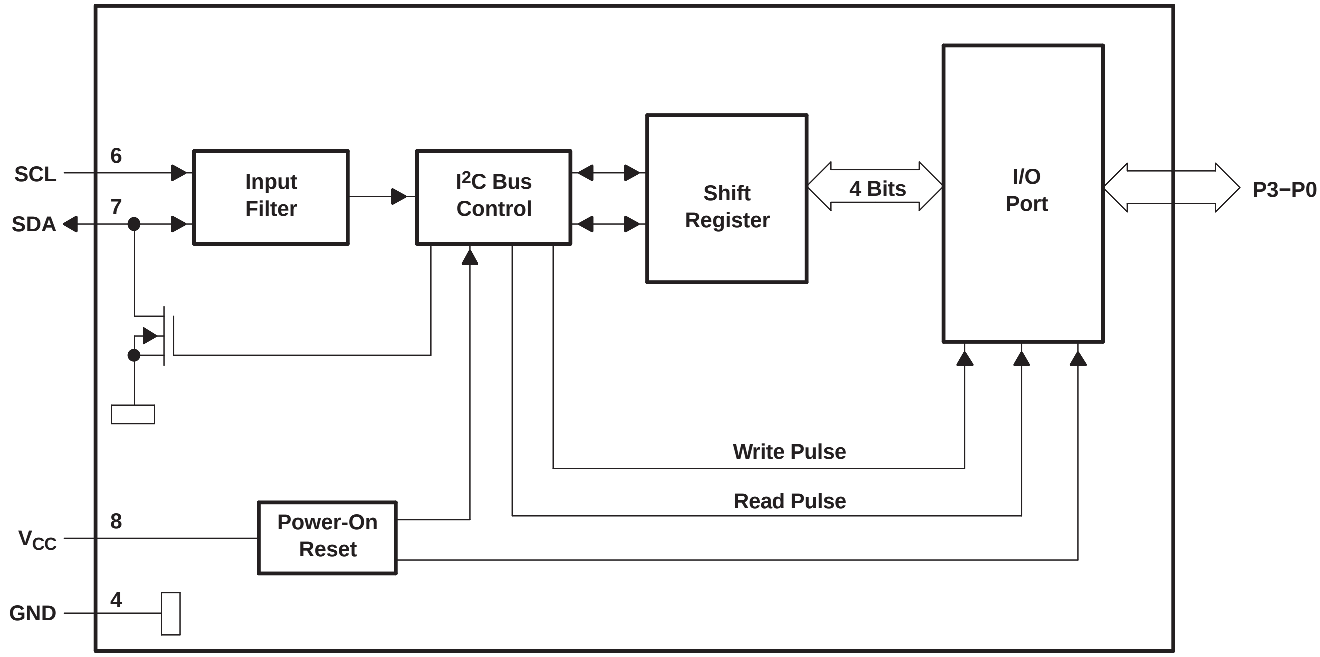


Figure 16. Logic Diagram

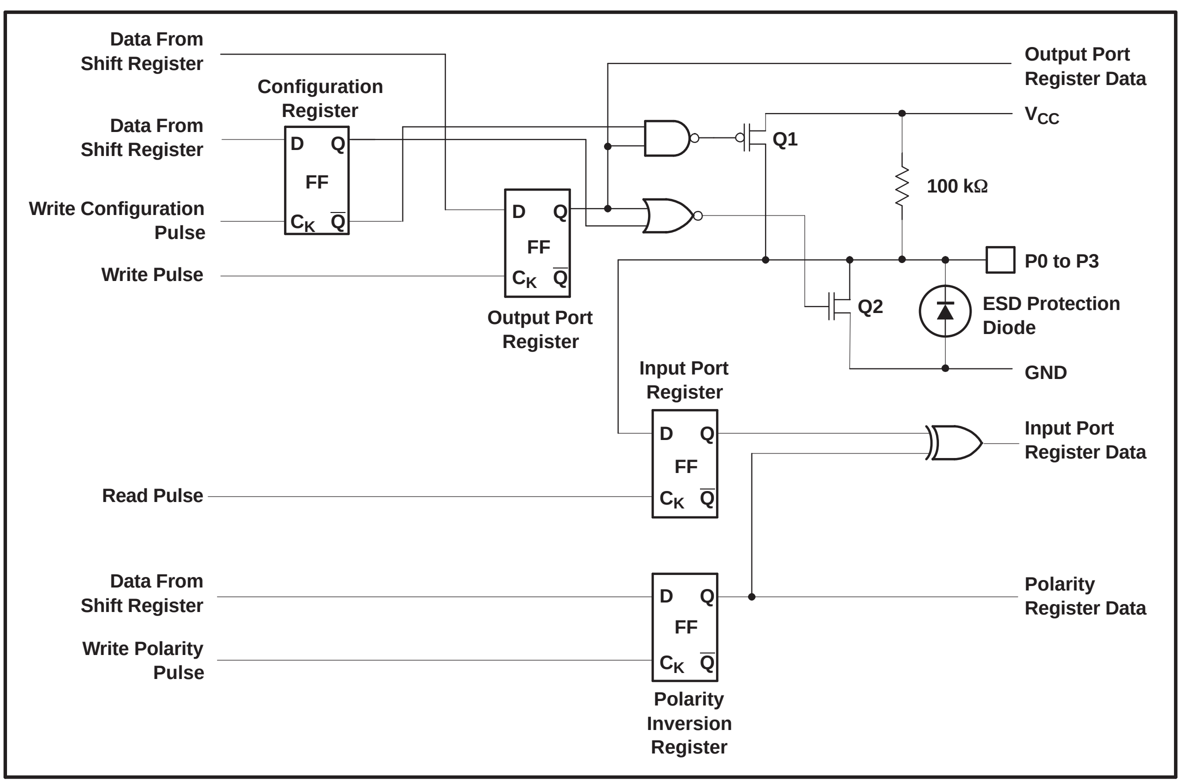


Figure 17. Simplified Schematic Of P0 To P3

7.2 Feature Description

7.2.1 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9536 in a reset condition until V_{CC} has reached V_{POR}. At that time, the reset condition is released and the PCA9536 registers and I^{2}C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

Refer to the *Power-On Reset Errata* section.

7.2.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in Figure 17) are off, creating a high-impedance input with a weak pullup (100 kΩ typ) to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

7.3 Programming

7.3.1 I^{2}C Interface

The bidirectional I^{2}C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^{2}C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 18). After the Start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse.

On the I^{2}C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 19).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 18).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 20). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

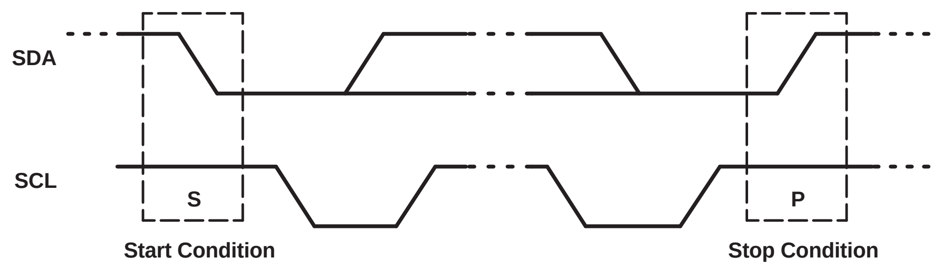


Figure 18. Definition of Start and Stop Conditions

Programming (continued)

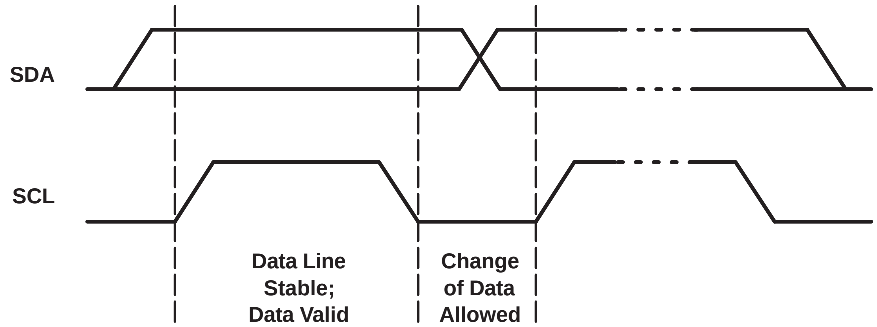


Figure 19. Bit Transfer

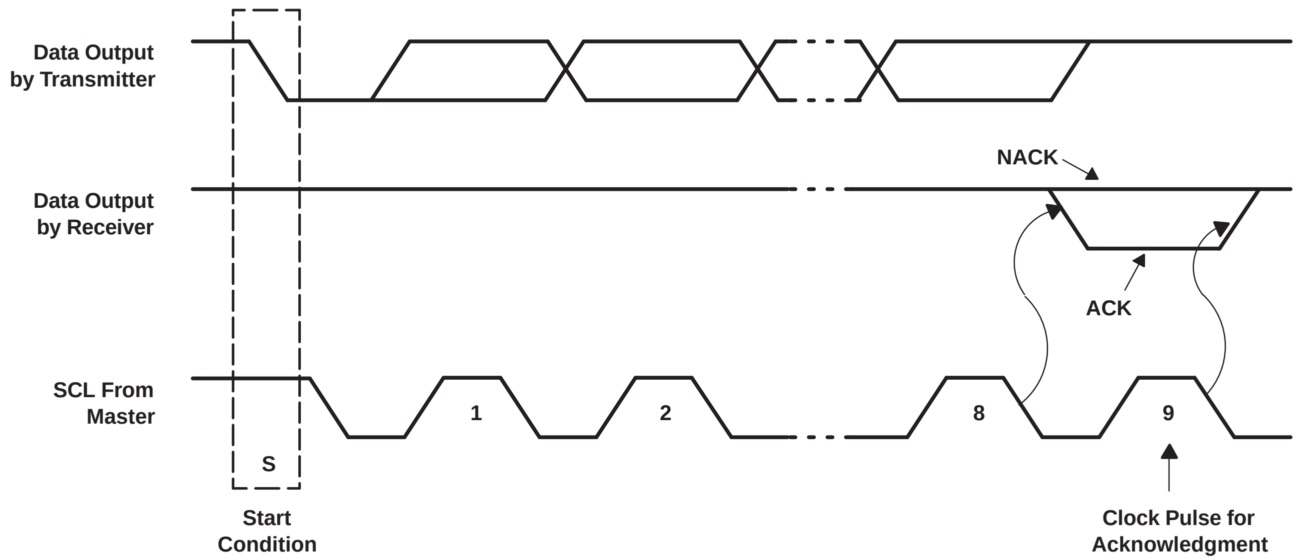


Figure 20. Acknowledgment on the I²C Bus

7.3.2 Register Map

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	H	L	L	L	L	L	H	R/$\overline{W}$
Px I/O data bus	Does not affect operation of the PCA9536				P3	P2	P1	P0
	P7	P6	P5	P4				

7.3.2.1 Device Address

Figure 21 shows the address byte of the PCA9536.

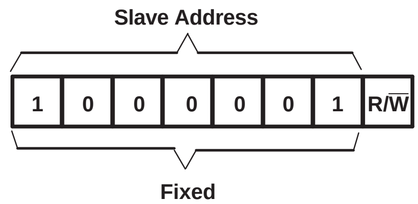


Figure 21. PCA9536 Address

The slave address equates to 65 (decimal) and 41 (hexadecimal).

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

7.3.2.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9536. Two bits of this data byte state the operation (read or write) and the internal register (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

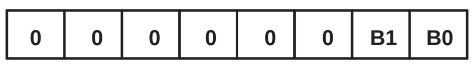


Figure 22. Control Register Bits

Table 2. Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	1111 XXXX
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

7.3.2.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to instruct the I^2C device that the Input Port register will be accessed next.

Table 3. Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
	Not Used							
DEFAULT	1	1	1	1	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 4. Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
	Not Used							
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Table 5. Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
	Not Used							
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 6. Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
	Not Used							
DEFAULT	1	1	1	1	1	1	1	1

7.3.2.4 Bus Transactions

Data is exchanged between the master and PCA9536 through write and read commands.

7.3.2.4.1 Writes

Data is transmitted to the PCA9536 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 21 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission (see Figure 23 and Figure 24).

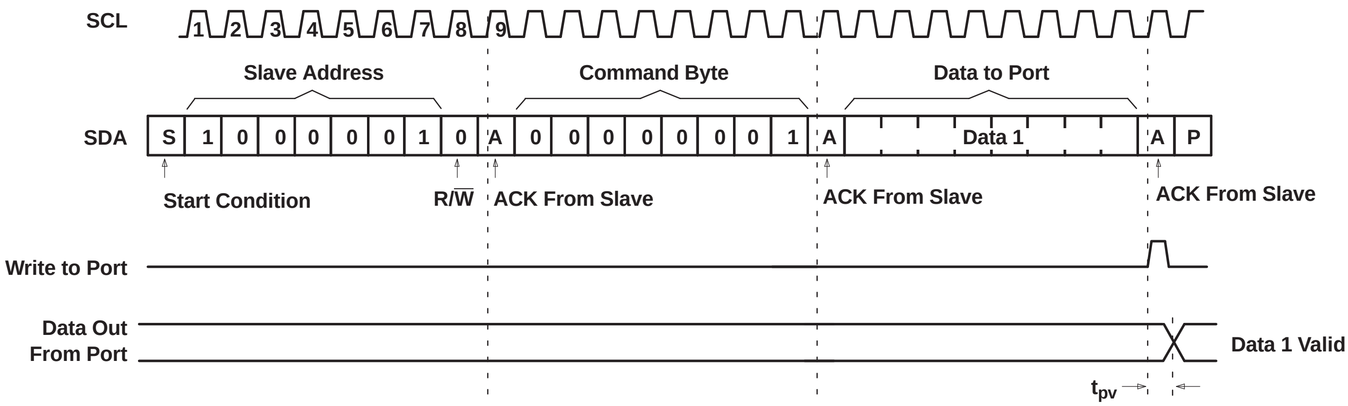


Figure 23. Write to Output Port Register

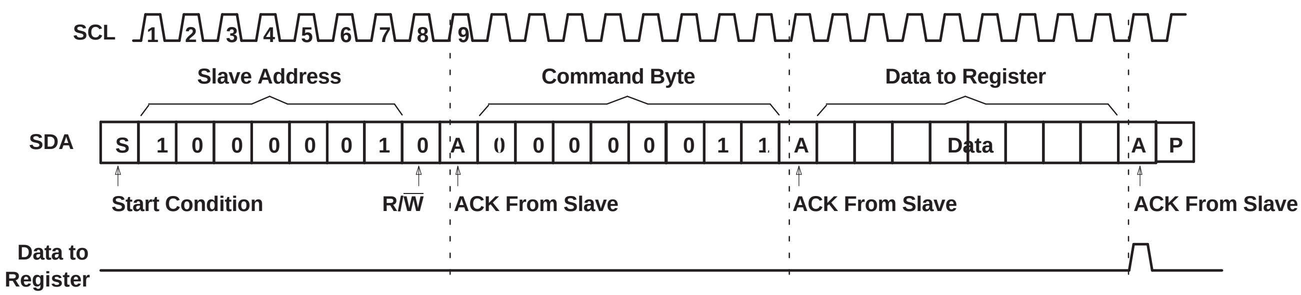


Figure 24. Write to Configuration or Polarity Inversion Registers

7.3.2.4.2 Reads

The bus master first must send the PCA9536 address with the LSB set to a logic 0 (see Figure 21 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9536 (see Figure 25 and Figure 26). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

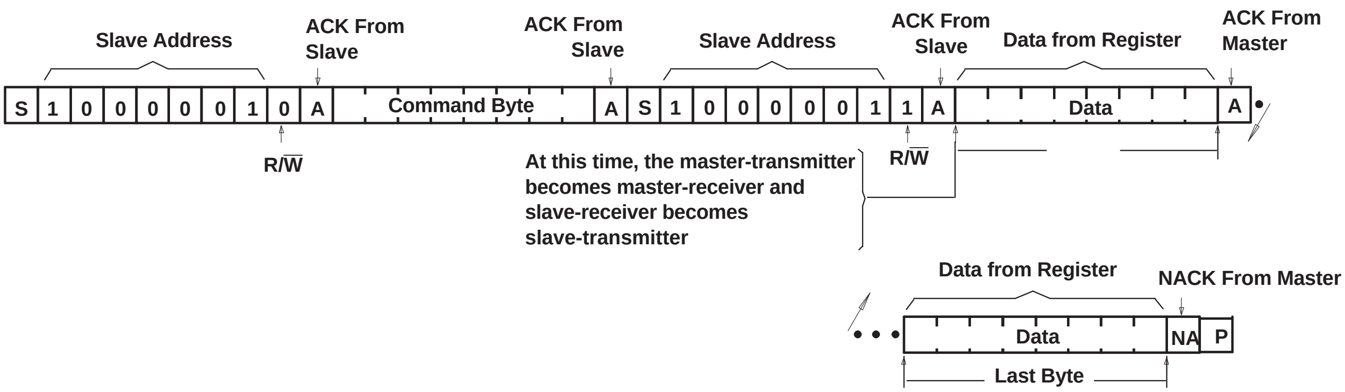
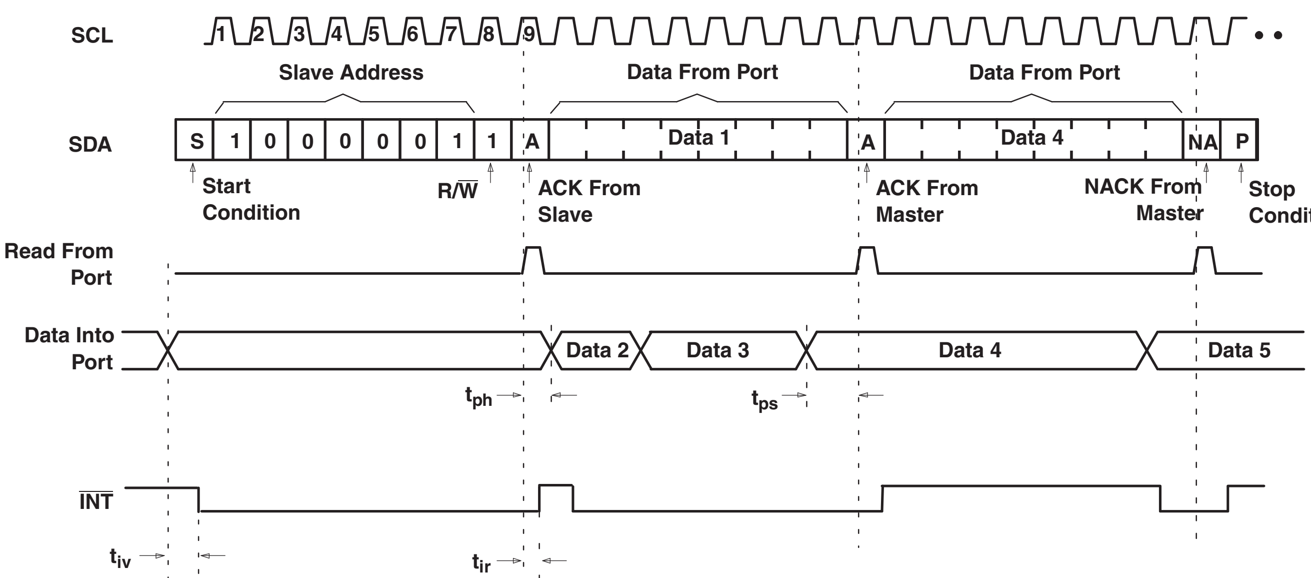


Figure 25. Read From Register



A. This figure assumes that the command byte previously has been programmed with 00h.

B. Transfer of data can be stopped at any moment by a Stop condition.

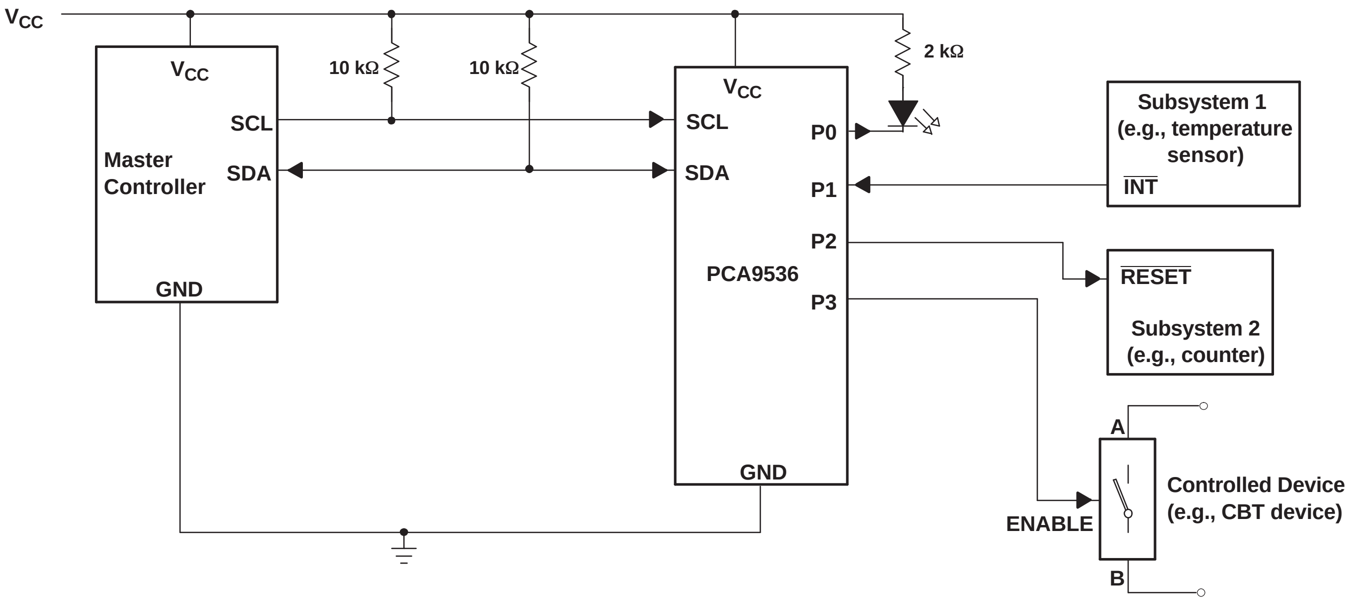
C. This figure eliminates the command byte transfer, a restart, and the slave address call between the initial slave address call and actual data transfer from the P-port (see Figure 25).

Figure 26. Read Input Port Register

8 Application and Implementation

8.1 Typical Application

Figure 27 shows an application in which the PCA9536 can be used.



A. Device address is 10000001.

B. P0, P2, and P3 are configured as outputs.

C. P1 is configured as an input.

Figure 27. Typical Application

8.1.1 Design Requirements

8.1.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor as shown in Figure 27. The LED acts as a diode so, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_{IN} becomes lower than V_{CC} and is specified as ΔI_{CC} in *Electrical Characteristics*.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off. Figure 28 shows a high-value resistor in parallel with the LED. Figure 29 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

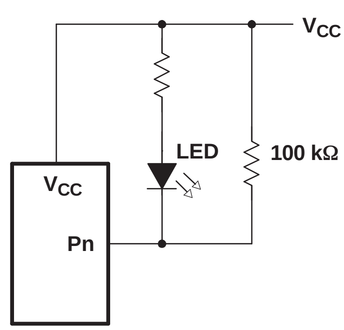


Figure 28. High-Value Resistor in Parallel With the LED

Typical Application (continued)

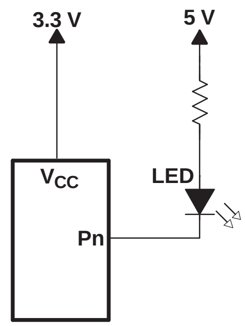
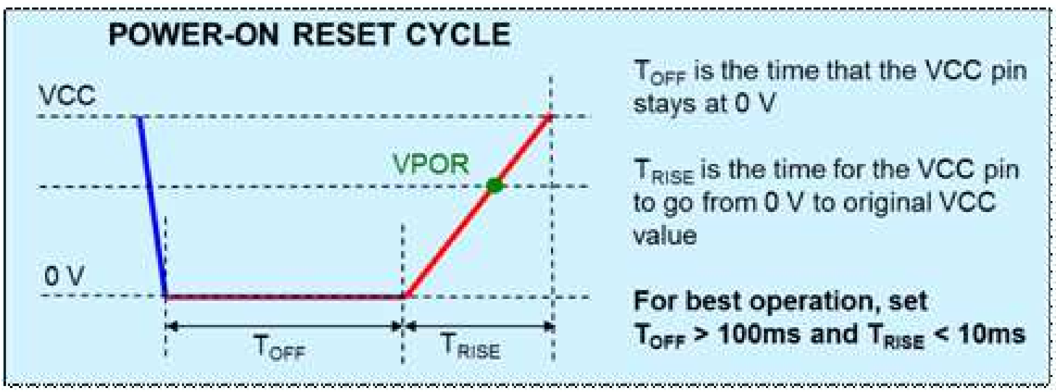


Figure 29. Device Supplied by a Lower Voltage

9 Power Supply Recommendations

9.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.



System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

10 Device and Documentation Support

10.1 Trademarks

NanoFree is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9536D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD536	Samples
PCA9536DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD536	Samples
PCA9536DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(7CF, 7CL)	Samples
PCA9536DGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(7CF, 7CL)	Samples
PCA9536DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD536	Samples
PCA9536DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD536	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

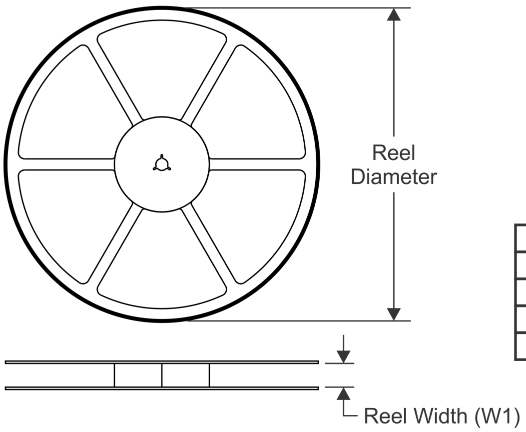
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

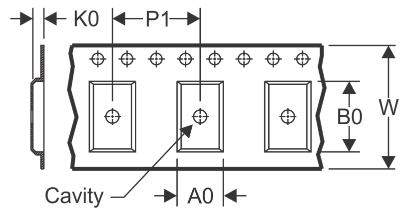
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

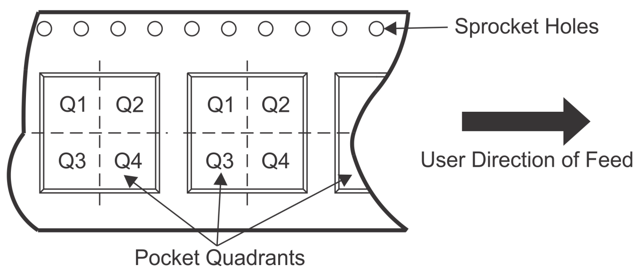


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

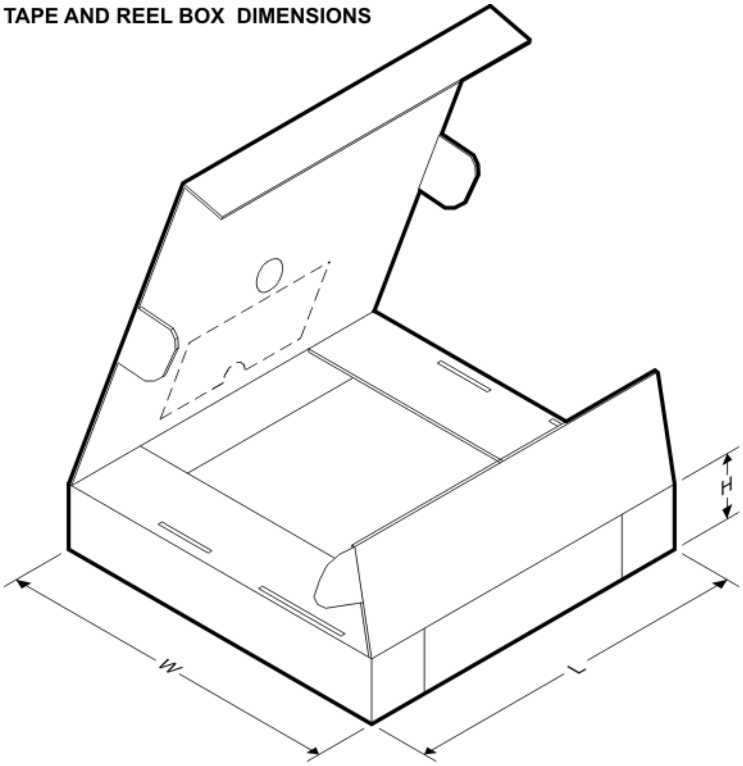
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

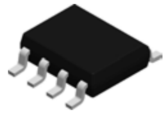
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9536DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PCA9536DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PCA9536DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9536DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
PCA9536DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
PCA9536DR	SOIC	D	8	2500	853.0	449.0	35.0

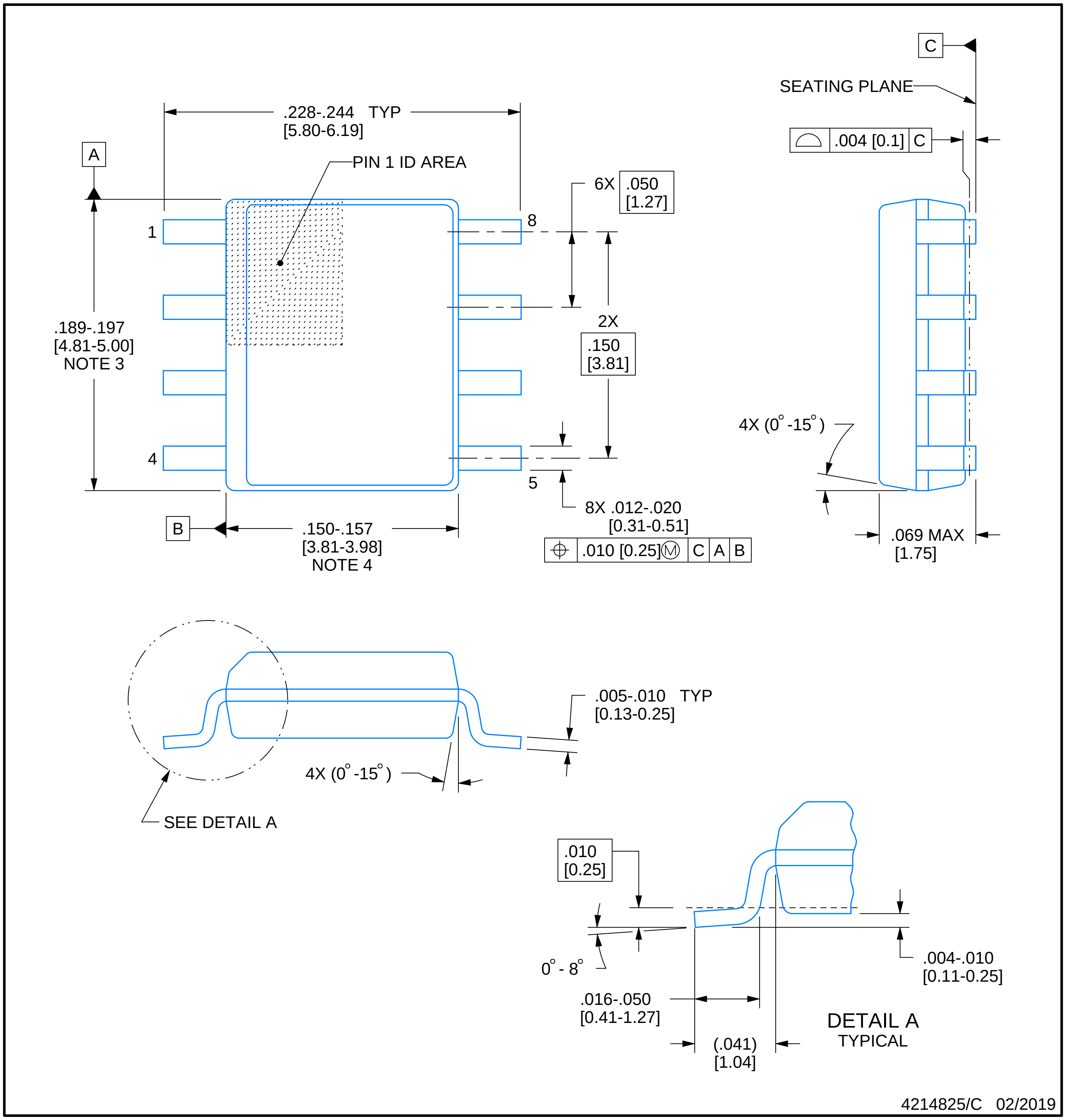


PACKAGE OUTLINE

D0008A

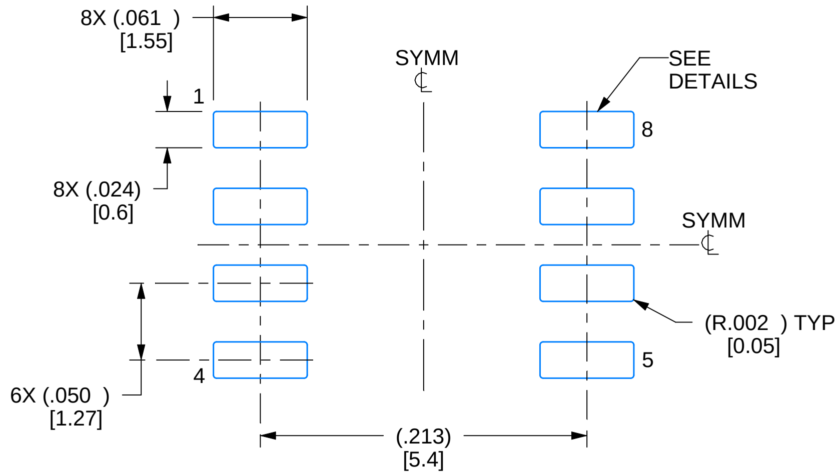
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

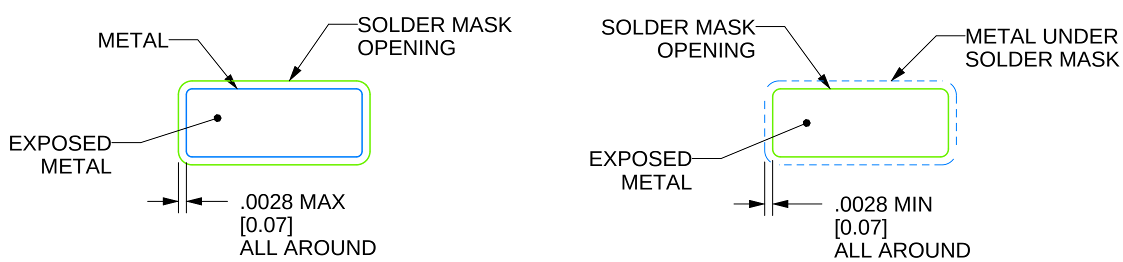


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

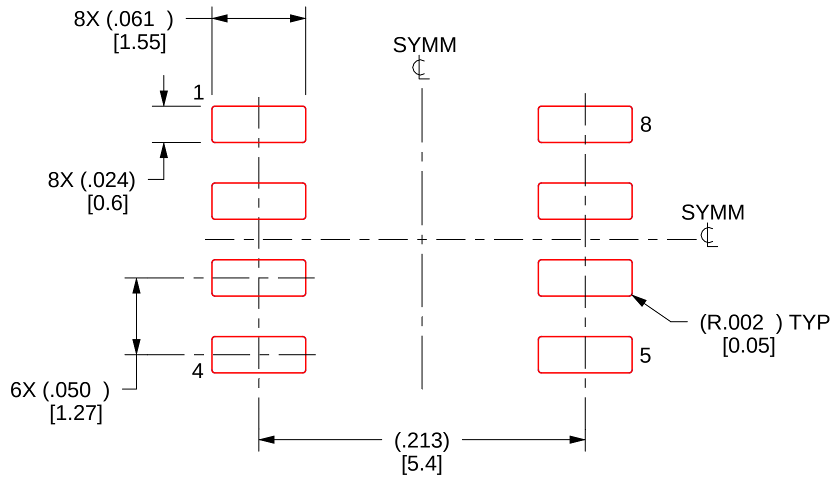
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



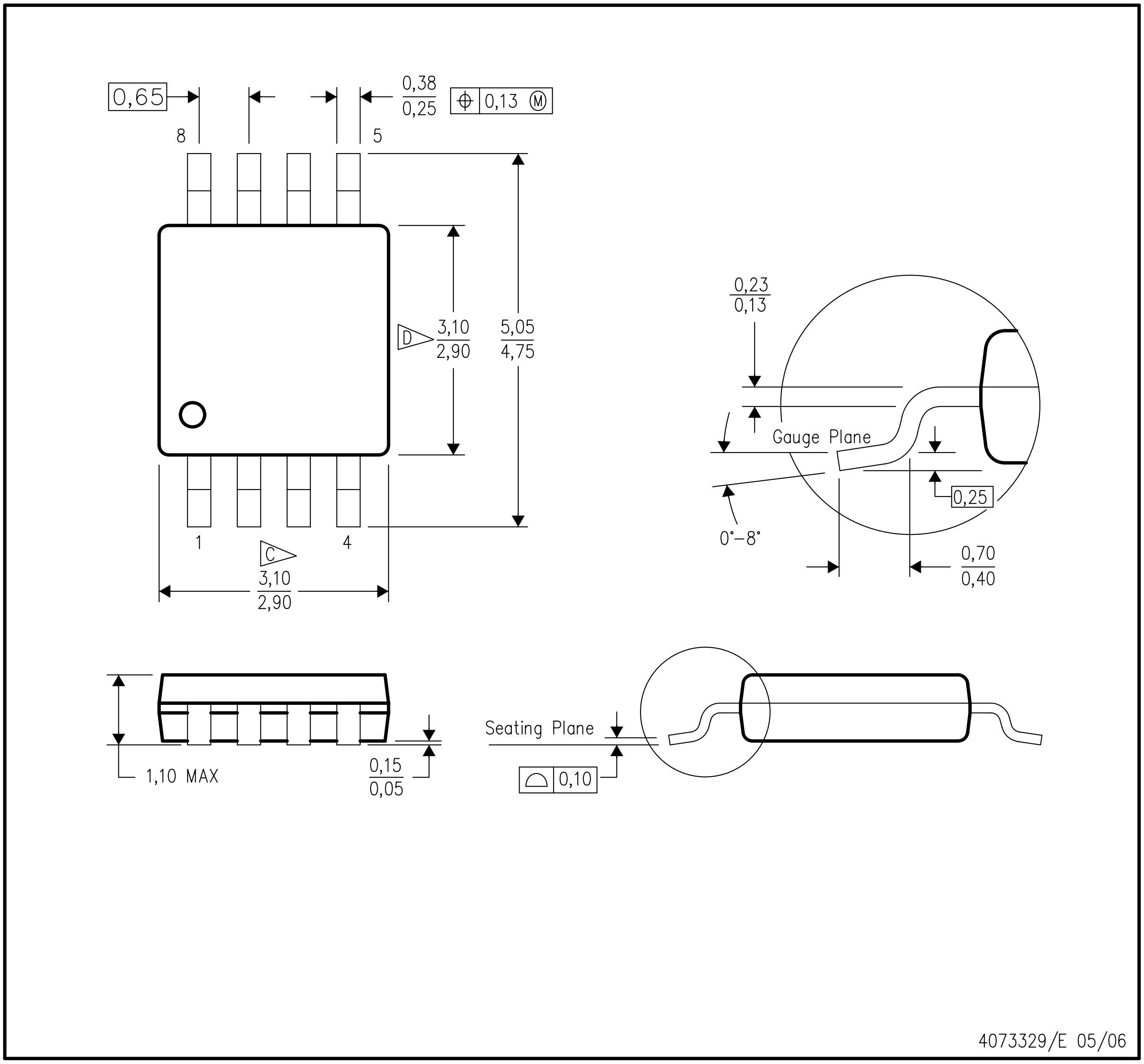
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

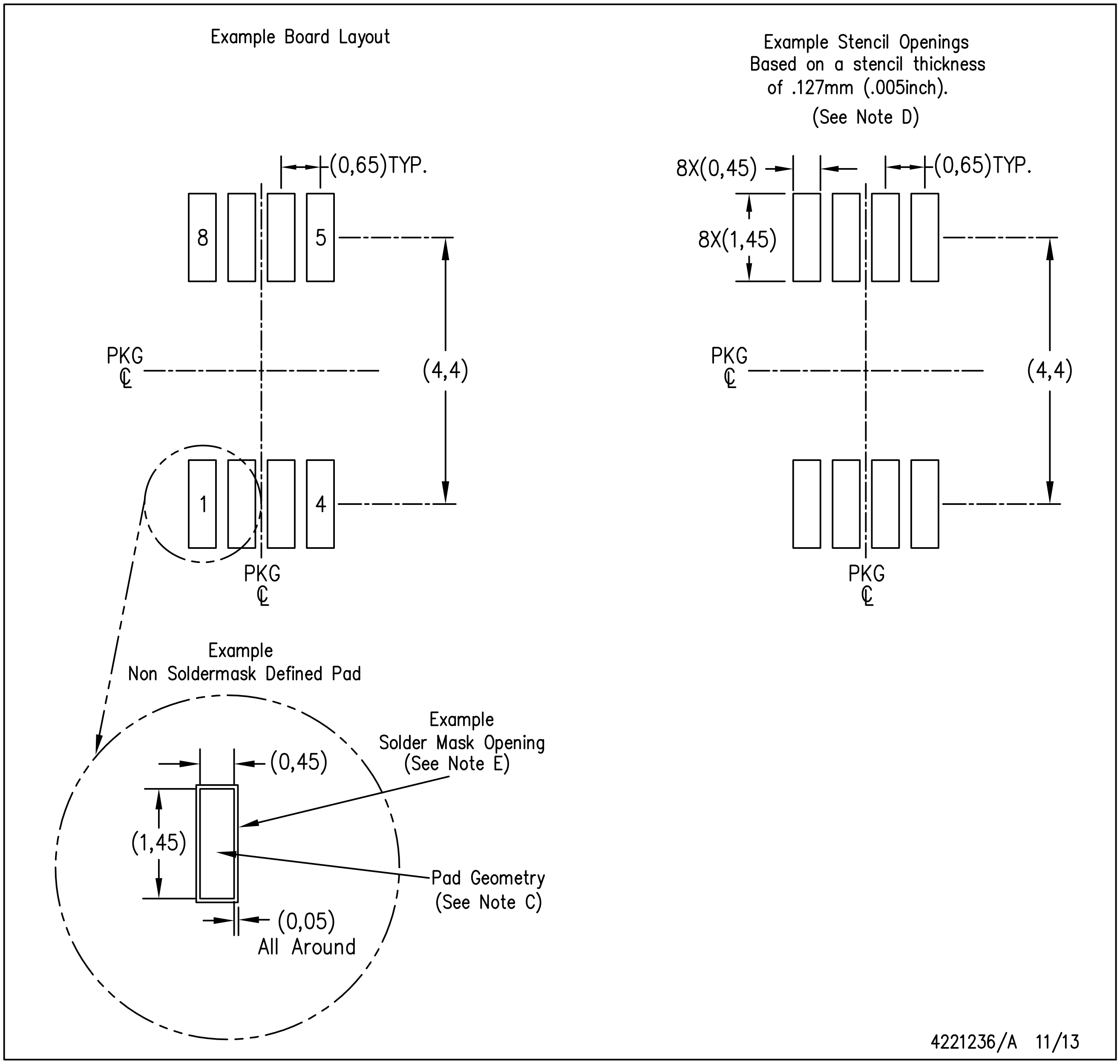
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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