DS125BR820 Low-Power 12.5 Gbps 8-Channel Linear Repeater

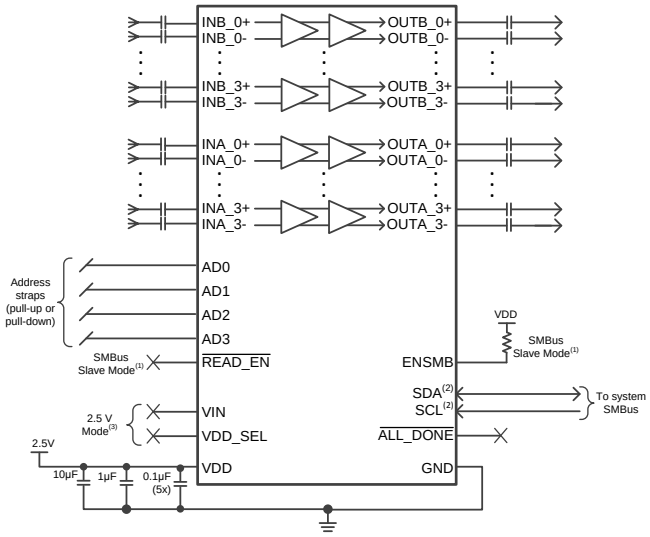
1 Features

- Low 70 mW/Channel (Typ) Power Consumption, with Option to Power Down Unused Channels
- Seamless Link Training Support
- Enables Host ASIC to Meet Front-Port Eye Mask Requirements over Longer Reach
- Advanced Configurable Signal Conditioning I/O
  - Receive CTLE up to 10 dB at 6 GHz
  - Linear Output Driver
  - Variable Output Voltage Range up to 1200 mVp-p
- Programmable via Pin Selection, EEPROM, or SMBus Interface
- Single Supply Voltage: 2.5 V or 3.3 V
- −40°C to 85°C Operating Temperature Range
- Flow-Thru Layout in 10 mm × 5.5 mm 54-Pin Leadless WQFN Package

2 Applications

- Front-Port 40G-CR4/SR4/LR4 Link Extension
- Backplane 40G-KR4 Link Extension
- SAS/SATA/PCIe Link Extension
- Other Proprietary High Speed Interfaces up to 12.5 Gbps

Simplified Functional Block Diagram



(1) Schematic requires different connections for SMBus Master Mode and Pin Mode
(2) SMBus signals need to be pulled up elsewhere in the system.
(3) Schematic requires different connections for 3.3 V mode

3 Description

The DS125BR820 is an extremely low-power high-performance repeater/redriver designed to support eight channels carrying high speed interface up to 12.5 Gbps, such as 40G-CR4, 40G-KR4, SAS/SATA, and PCIe. The receiver's continuous time linear equalizer (CTLE) provides high frequency boost that is programmable from 3 to 10 dB at 6 GHz (12 Gbps) followed by a linear output driver. The CTLE receiver is capable of opening an input eye that is completely closed due to inter symbol interference (ISI) induced by interconnect medium such as board traces or twin axial-copper cables. The programmable equalization maximizes the flexibility of physical placement within the interconnect channel and improves overall channel performance.

When operating in 40G-CR4/KR4, SAS/SATA, and PCIe applications, the DS125BR820 preserves transmit signal characteristics, thereby allowing the host controller and the end point to negotiate transmit equalizer coefficients. This transparency in the link training protocol facilitates system level interoperability and minimizes latency.

The programmable settings can be applied easily via pin control, software (SMBus or I2C), or direct loading from an external EEPROM. In EEPROM mode, the configuration information is automatically loaded on power up, thereby eliminating the need for an external microprocessor or software driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS125BR820	WQFN (54)	10 mm × 5.5 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Block Diagram

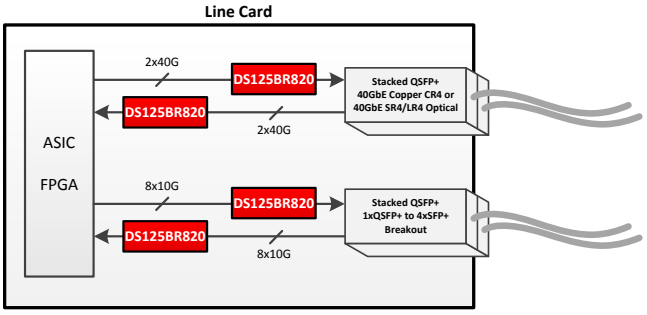


Table of Contents

4 Revision History

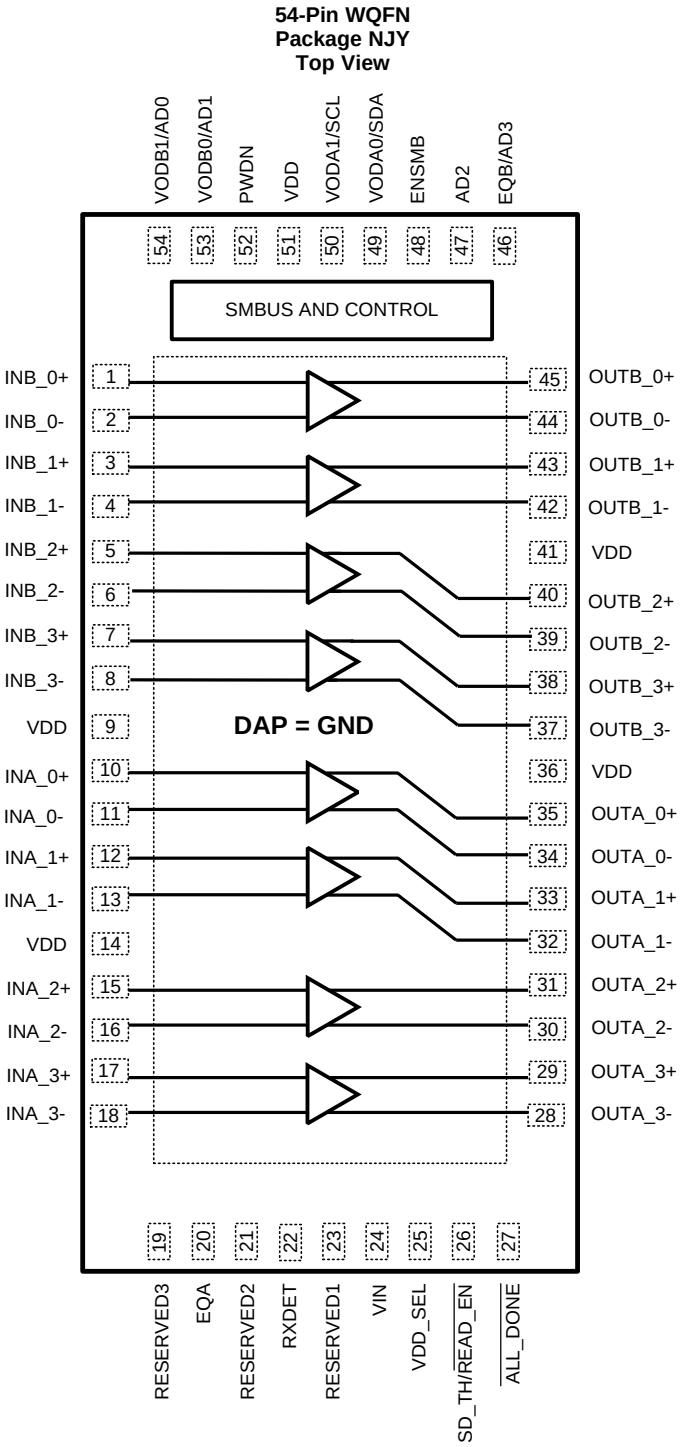
Changes from Revision A (September 2014) to Revision B — **Page**

- Added data type for all differential high speed I/O ... 4
- Changed pin assignment numbers for OUTB_2+/- and OUTB_3+/- to correct typo ... 4
- Changed ENSMB pin type to 4-level LVCMOS per input pin behavior ... 4
- Changed Handling Ratings table to ESD Ratings table ... 7
- Changed register map rows to combine multiple consecutive registers with a value of all zeros and no EEPROM-relevant bits ... 28

Changes from Original (July 2014) to Revision A — **Page**

- Added release of the full document ... 1

5 Pin Configuration and Functions



NOTE: Above 54-lead WQFN graphic is a TOP VIEW, looking down through the package.

Pin Functions[1]

PIN		I/O, TYPE	PIN DESCRIPTION
NAME	NO.		
DIFFERENTIAL HIGH SPEED I/O			
INB_0+, INB_0- , INB_1+, INB_1-, INB_2+, INB_2-, INB_3+, INB_3-	1, 2 3, 4 5, 6 7, 8	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. On-chip 50 Ω termination resistor connects INB_n+ to VDD and INB_n- to VDD depending on the state of RXDET. See Table 2. AC coupling required on high-speed I/O
OUTB_0+, OUTB_0-, OUTB_1+, OUTB_1-, OUTB_2+, OUTB_2-, OUTB_3+, OUTB_3-	45, 44 43, 42 40. 39 38, 37	O, CML	Inverting and non-inverting 50 Ω driver outputs. Compatible with AC coupled CML inputs. AC coupling required on high-speed I/O
INA_0+, INA_0- , INA_1+, INA_1-, INA_2+, INA_2-, INA_3+, INA_3-	10, 11 12, 13 15, 16 17, 18	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. On-chip 50 Ω termination resistor connects INA_n+ to VDD and INA_n- to VDD depending on the state of RXDET. See Table 2. AC coupling required on high-speed I/O
OUTA_0+, OUTA_0-, OUTA_1+, OUTA_1-, OUTA_2+, OUTA_2-, OUTA_3+, OUTA_3-	35, 34 33, 32 31, 30 29, 28	O, CML	Inverting and non-inverting 50 Ω driver outputs. Compatible with AC coupled CML inputs. AC coupling required on high-speed I/O
CONTROL PINS — SHARED (LVCMOS)			
ENSMB	48	I, 4-LEVEL, LVCMOS	System Management Bus (SMBus) Enable Pin Tie 1 kΩ to VDD = Register Access SMBus Slave Mode FLOAT = Read External EEPROM (SMBus Master Mode) Tie 1 kΩ to GND = Pin Mode
ENSMB = 1 (SMBus SLAVE MODE)			
SCL	50	I, LVCMOS, O, OPEN Drain	In SMBus Slave Mode, this pin is the SMBus clock I/O. Clock input or open drain output. External 2 kΩ to 5 kΩ pull-up resistor to VDD or VIN recommended as per SMBus interface standards[2]
SDA	49	I, LVCMOS, O, OPEN Drain	In both SMBus Modes, this pin is the SMBus data I/O. Data input or open drain output. External 2 kΩ to 5 kΩ pull-up resistor to VDD or VIN recommended as per SMBus interface standards[2]
AD0-AD3	54, 53, 47, 46	I, LVCMOS	SMBus Slave Address Inputs. In both SMBus Modes, these pins are the user set SMBus slave address inputs. External 1 kΩ pull-up or pull-down recommended. Note: In Pin Mode, AD2 must be tied via external 1 kΩ to GND.
RESERVED2	21	I, 4-LEVEL, LVCMOS	Reserved For applications requiring Signal Detect status register read-back: ● Leave Pin 21 floating. ● Write Reg 0x08[2] = 1 if Pin 21 is floating. Otherwise, tie Pin 21 via external 1 kΩ to GND (External 1 kΩ to VDD is also acceptable).
RESERVED3	19	I, 4-LEVEL, LVCMOS	Reserved This input may be left floating, tied via 1 kΩ to VDD, or tied via 1 kΩ to GND.

(1) LVCMOS inputs without the “Float” conditions must be driven to a logic low or high at all times or operation is not ensured.
Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.
For 3.3 V mode operation, VIN pin input = 3.3 V and the logic "1" or "high" reference for the 4-level input is 3.3 V.
For 2.5 V mode operation, VDD pin output= 2.5 V and the logic "1" or "high" reference for the 4-level input is 2.5 V.
(2) SCL and SDA pins can be tied either to 3.3 V or 2.5 V, regardless of whether the device is operating in 2.5 V mode or 3.3 V mode.

Pin Functions[1] (continued)

PIN		I/O, TYPE	PIN DESCRIPTION
NAME	NO.		
ENSMB = Float (SMBus MASTER MODE)			
SCL	50	I, LVCMOS, O, OPEN Drain	Clock output when loading EEPROM configuration, reverting to SMBus clock input when EEPROM load is complete (ALL_DONE = 0). External 2 kΩ to 5 kΩ pull-up resistor to VDD or VIN recommended as per SMBus interface standards[2]
SDA	49	I, LVCMOS, O, OPEN Drain	In both SMBus Modes, this pin is the SMBus data I/O. Data input or open drain output. External 2 kΩ to 5 kΩ pull-up resistor to VDD or VIN recommended as per SMBus interface standards[2]
AD0-AD3	54, 53, 47, 46	I, LVCMOS	SMBus Slave Address Inputs. In both SMBus Modes, these pins are the user set SMBus slave address inputs. External 1 kΩ pull-up or pull-down recommended. Note: In Pin Mode, AD2 must be tied via external 1 kΩ to GND.
READ_EN	26	I, LVCMOS	A logic low on this pin starts the load from the external EEPROM[3]. Once EEPROM load is complete (ALL_DONE = 0), this pin functionality remains as READ_EN. It does not revert to an SD_TH input.
RESERVED2	21	I, 4-LEVEL, LVCMOS	Reserved For applications requiring Signal Detect status register read-back: ● Leave Pin 21 floating. ● Write Reg 0x08[2] = 1 if Pin 21 is floating. Otherwise, tie Pin 21 via external 1 kΩ to GND (External 1 kΩ to VDD is also acceptable).
RESERVED3	19	I, 4-LEVEL, LVCMOS	Reserved This input may be left floating, tied via 1 kΩ to VDD, or tied via 1 kΩ to GND.
ENSMB = 0 (PIN MODE)			
EQA EQB	20 46	I, 4-LEVEL, LVCMOS	EQA and EQB pins control the level of equalization for the A-channels and B-channels, respectively. The pins are defined as EQA and EQB only when ENSMB is de-asserted (low). Each of the four A-channels have the same level unless controlled by the SMBus control registers. Likewise, each of the four B-channels have the same level unless controlled by the SMBus control registers. When the device operates in Slave or Master Mode, the SMBus registers independently control each lane, and the EQB pin is converted to an AD3 input. See Table 4.
VODB0 VODB1	53 54	I, 4-LEVEL, LVCMOS	VODB[1:0] controls the output amplitude of the B-channels. The pins are defined as VODB[1:0] only when ENSMB is de-asserted (low). Each of the four B-channels have the same level unless controlled by the SMBus control registers. When the device operates in Slave or Master Mode, the SMBus registers provide independent control of each lane, and VODB[1:0] pins are converted to AD0, AD1 inputs. See Table 5.
VODA0 VODA1	49 50	I, 4-LEVEL, LVCMOS	VODA[1:0] controls the output amplitude of the A-channels. The pins are defined as VODA[1:0] only when ENSMB is de-asserted (low). Each of the four A-channels have the same level unless controlled by the SMBus control registers. When the device operates in Slave or Master Mode, the SMBus registers provide independent control of each lane and the VODA[1:0] pins are converted to SCL and SDA. See Table 5.
AD2	47	I, LVCMOS	Reserved in Pin Mode (ENSMB = 0) This input must be tied via external 1 kΩ to GND.
SD_TH	26	I, 4-LEVEL, LVCMOS	Controls the internal Signal Detect Status Threshold value when in Pin Mode and SMBus Slave Mode. This pin is to be used for system debugging only. See Table 3 for more information. For final designs, input can be left floating, tied via 1 kΩ to VDD, or tied via 1 kΩ to GND.
RESERVED2	21	I, 4-LEVEL, LVCMOS	Reserved Tie via external 1 kΩ to GND (External 1 kΩ to VDD is also acceptable).
RESERVED3	19	I, 4-LEVEL, LVCMOS	Reserved This input must be tied via external 1 kΩ to GND.

(3) When READ_EN is low, the device attempts to load EEPROM. If EEPROM cannot be loaded successfully, for example due to an invalid or blank hex file, the DS125BR820 hangs indefinitely in an unknown state. ALL_DONE pin remains high in this situation.

Pin Functions[1] (continued)

PIN		I/O, TYPE	PIN DESCRIPTION
NAME	NO.		
CONTROL PINS — BOTH PIN AND SMBUS MODES (LVCMOS)			
RXDET	22	I, 4-LEVEL, LVCMOS	The RXDET pin controls the input enable function. Depending on the input level, a 50 Ω or >50 kΩ termination to the power rail is enabled. Pull up pin to VDD (2.5 V mode) or VIN (3.3 V mode) through 1 kΩ resistor to provide a 50 Ω termination to the power rail for normal operation. See Table 2.
RESERVED1	23	I, 4-LEVEL, LVCMOS	Reserved This input must be left floating.
VDD_SEL	25	I, FLOAT	Controls the internal regulator Float = 2.5 V mode Tie to GND = 3.3 V mode
PWDN	52	I, LVCMOS	Tie High = Low power - Power Down Tie to GND = Normal Operation See Table 2.
$\overline{\text{ALL\_DONE}}$	27	O, LVCMOS	Valid Register Load Status Output HIGH = External EEPROM load failed or incomplete LOW = External EEPROM load passed
POWER			
VIN	24	Power	In 3.3 V mode, feed 3.3 V to VIN In 2.5 V mode, leave floating.
VDD	9, 14, 36, 41, 51	Power	Power Supply for CML and Analog Pins 2.5 V mode, connect to 2.5 V 3.3 V mode, connect 0.1 µF cap to each VDD Pin and GND See *Power Supply Recommendations* for proper power supply decoupling .
GND	DAP	Power	Ground pad (DAP - die attach pad).

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (VDD to GND, 2.5 V Mode)	-0.5	+2.75	V
Supply Voltage (VIN to GND, 3.3 V Mode)	-0.5	+4.0	V
LVCMOS Input/Output Voltage	-0.5	+4.0	V
CML Input Voltage	-0.5	VDD + 0.5	V
CML Input Current	-30	+30	mA
Storage temperature, T_{stg}	-40	125	°C
Lead Temperature Range Soldering (4 sec.)(2), T_{solder}		260	°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are ensured for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.
(2) For soldering specifications, see application note SNOA549.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±4000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (2.5 V mode)(1)	2.375	2.5	2.625	V
Supply Voltage (3.3 V mode)(1)	3.0	3.3	3.6	V
Ambient Temperature	-40		+85	°C
SMBus (SDA, SCL)			3.6	V
Supply Noise up to 50 MHz(2)		100		mVp-p

(1) DC plus AC power should not exceed these limits.
(2) Allowed supply noise (mVp-p sine wave) under typical conditions.

6.4 Thermal Information

THERMAL METRIC(1)		NJY 54 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.6	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	10.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	4.4	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	4.3	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{DD}	Current Consumption, 2.5 V Mode	EQ = Level 4, VOD = Level 6 RXDET = 1, PWDN = 0		220	280	mA
	Current Consumption, 3.3 V Mode	EQ = Level 4, VOD = Level 6 RXDET = 1, PWDN = 0		220	280	mA
	Power Down Current Consumption	PWDN = 1		14	27	mA
V_{DD}	Integrated LDO Regulator	V_{IN} = 3.0 - 3.6 V	2.375	2.5	2.625	V
LVCMOS / LVTTL DC SPECIFICATIONS						
V_{IH25}	High Level Input Voltage	2.5 V Supply Mode	1.7		V_{DD}	V
V_{IH33}	High Level Input Voltage	3.3 V Supply Mode	1.7		V_{IN}	V
V_{IL}	Low Level Input Voltage		0		0.7	V
V_{OH}	High Level Output Voltage ($\overline{\text{ALL\_DONE}}$ pin)	I_{OH} = −4mA	2.0			V
V_{OL}	Low Level Output Voltage ($\overline{\text{ALL\_DONE}}$ pin)	I_{OL} = 4mA			0.4	V
I_{IH}	Input High Current (PWDN pin)	V_{IN} = 3.6 V, LVCMOS = 3.6 V	-15		+15	µA
I_{IL}	Input Low Current (PWDN pin)	V_{IN} = 3.6 V, LVCMOS = 0 V	-15		+15	µA
4-LEVEL INPUT DC SPECIFICATIONS						
I_{IH}	Input High Current with internal resistors (4–level input pin)	V_{IN} = 3.6 V, LVCMOS = 3.6 V	+20		+150	µA
I_{IL}	Input Low Current with internal resistors (4–level input pin)	V_{IN} = 3.6 V, LVCMOS = 0 V	-160		-40	µA
V_{TH}	Voltage Threshold from Pin Mode Level 0 to R	V_{DD} = 2.5 V (2.5 V supply mode) Internal LDO Disabled See Table 1 for details		0.50		V
	Voltage Threshold from Pin Mode Level R to F			1.25		
	Voltage Threshold from Pin Mode Level F to 1			2.00		
	Voltage Threshold from Pin Mode Level 0 to R	V_{IN} = 3.3 V (3.3 V supply mode) Internal LDO Enabled See Table 1 for details.		0.66		V
	Voltage Threshold from Pin Mode Level R to F			1.65		
	Voltage Threshold from Pin Mode Level F to 1			2.64		
CML RECEIVER INPUTS (IN_n+, IN_n-)						
$Z_{Rx\text{-}DIFF\text{-}DC}$	Rx DC differential mode impedance	Tested at VDD = 2.5 V	80	100	120	Ω
$Z_{Rx\text{-}DC}$	Rx DC single ended impedance	Tested at VDD = 2.5 V	40	50	60	Ω
$RL_{Rx\text{-}DIFF}$	Rx Differential Input return loss	SDD11 10 MHz		-19		dB
		SDD11 2 GHz		-14		
		SDD11 6-11.1 GHz		-8		
$RL_{Rx\text{-}CM}$	Rx Common mode return loss	SCC11 0.05 - 5 GHz		-10		dB
$V_{Rx\text{-}ASSERT\text{-}DIFF\text{-}PP}$	Signal detect assert level for active data signal	SD_TH = F (float), 1010 pattern at 12 Gbps		57		mVp-p
$V_{Rx\text{-}DEASSERT\text{-}DIFF\text{-}PP}$	Signal detect de-assert for inactive signal level	SD_TH = F (float), 1010 pattern at 12 Gbps		44		mVp-p

Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH SPEED OUTPUTS						
$RL_{Tx-DIFF}$	Tx Differential return loss	SDD22 10 MHz - 2 GHz		-15		dB
		SDD22 5.5 GHz		-12		
		SDD22 11.1 GHz		-10		dB
RL_{Tx-CM}	Tx Common mode return loss	SCC22 50 MHz- 2.5 GHz		-8		dB
$Z_{Tx-DIFF-DC}$	DC differential Tx impedance			100		Ω
$I_{Tx-SHORT}$	Transmitter short circuit current limit	Total current when output is shorted to VDD or GND		20		mA
$V_{Tx-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode voltage between Tx+ and Tx-				25	mV
$V_{Tx-DIFF1-PP}$	Output Voltage Differential Swing	Differential measurement with OUT_n+ and OUT_n-, AC-Coupled and terminated by 50 Ω to GND, Inputs AC-Coupled, Measured with 8T Pattern at 12 Gbps(1) VID = 600 mVp-p VOD = Level 6(2)(3)		615		mVp-p
$V_{Tx-DIFF2-PP}$	Output Voltage Differential Swing	Differential measurement with OUT_n+ and OUT_n-, AC-Coupled and terminated by 50 Ω to GND, Inputs AC-Coupled, Measured with 8T Pattern at 12 Gbps(1) VID = 1000 mVp-p VOD = Level 6(2)(3)		950		mVp-p
$V_{Tx-DIFF3-PP}$	Output Voltage Differential Swing	Differential measurement with OUT_n+ and OUT_n-, AC-Coupled and terminated by 50 Ω to GND, Inputs AC-Coupled, Measured with 8T Pattern at 12 Gbps(1) VID = 1200 mVp-p VOD = Level 6(2)(3)		1100		mVp-p
T_{PDEQ}	Differential propagation delay	EQ = Level 1 to Level 4		80		ps
$V_{Tx-CM-AC-P}$	AC common mode voltage	VOD = Level 6, 12 Gbps		20		mV rms
$V_{DISABLE-OUT}$	Tx disable output voltage	Driver disabled via PWDN	-30	1	30	mVp-p
$V_{OOB-IDLE}$	OOB idle output voltage	VID = 0 mVp-p		15		mVp-p
$V_{OOB-OS-DELTA}$	OOB offset delta	OOB pattern, EQ = Level 1 VOD = Level 6		15		mVp-p
$V_{OOB-CM-DELTA}$	OOB common mode delta	OOB pattern, EQ = Level 1 VOD = Level 6		11		mVp-p
$T_{Tx-IDLE-SET-TO-IDLE}$	Time to transition to idle after differential signal	VID = 1.0 Vp-p, 1.5 Gbps		0.70		ns
$T_{Tx-IDLE-TO-DIFF-DATA}$	Time to transition to valid differential signal after idle	VID = 1.0 Vp-p, 1.5 Gbps		0.04		ns

(1) 8T pattern is defined as a 1111111100000000'b pattern bit sequence.
(2) ATE measurements for production are tested at DC.
(3) In 40G-CR4/KR4/SAS/SATA/PCIe applications, the output VOD level is not fixed. It adjusts automatically based on the VID input amplitude level. The output VOD level set by VODA/B[1:0] depends on the VID level and the frequency content. The DS125BR820 repeater is designed to be transparent in this mode, so the Tx-FIR (de-emphasis) is passed to the Rx to support the handshake negotiation link training.

Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ_{ADD}	Additive Random Jitter	Evaluation Module (EVM) Only, FR4, VID = 800 mVp-p, EQ = Level 1 PRBS15, 12 Gbps VOD = Level 6 All other channels active (4)		0.36		ps rms
EQUALIZATION						
DJE1	Residual deterministic jitter at 6 Gbps	5" Differential Stripline, 5mil trace width, FR4, VID = 800 mVp-p, PRBS15, EQ = Level 2, VOD = Level 6		0.06		UIp-p
DJE2	Residual deterministic jitter at 12 Gbps	5" Differential Stripline, 5mil trace width, FR4, VID = 800 mVp-p, PRBS15, EQ = Level 2, VOD = Level 6		0.12		UIp-p

(4) Additive random jitter is given in RMS value by the following equation: $RJ_{ADD} = \sqrt{[(\text{Output Jitter})^2 - (\text{Input Jitter})^2]}$. Typical input jitter for these measurements is 150 fs rms.

6.6 Electrical Characteristics — Serial Bus Interface DC Specifications

Over recommended operating supply and temperature ranges unless other specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		3.6	V
V_{OL}	Output Low Voltage	SDA or SCL, I_{OL} = 1.25 mA	0		0.36	V
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{IH\text{-}Pin}$	Input Leakage Per Device Pin		+20		+150	µA
$I_{IL\text{-}Pin}$	Input Leakage Per Device Pin		-160		-40	µA
C_I	Capacitance for SDA and SCL	See (1)(2)		< 5		pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5 V ± 5% OR 3.3 V ± 10%	Pullup V_{DD} = 3.3 V (1)(2)(3)		2000		Ω
		Pullup V_{DD} = 2.5 V (1)(2)(3)		1000		Ω

(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400 pF.
(3) Maximum termination voltage should be identical to the device supply voltage.

6.7 Serial Bus Interface Timing Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SMB}	Bus Operating Frequency	ENSMB = VDD (Slave Mode)			400	kHz
		ENSMB = FLOAT (Master Mode)	280	400	520	kHz
t_{FALL}	SCL or SDA Fall Time	Read operation RPU = 4.7 kΩ, Cb < 50 pF		60		ns
t_{RISE}	SCL or SDA Rise Time	Read operation RPU = 4.7 kΩ, Cb < 50 pF		140		ns
t_F	Clock/Data Fall Time	See (1)			300	ns
t_R	Clock/Data Rise Time	See (1)			1000	ns
t_{POR}	Time in which a device must be operational after power-on reset	See (1)			500	ms

(1) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

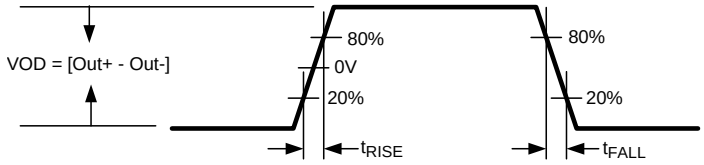


Figure 1. Output Rise And Fall Transition Time

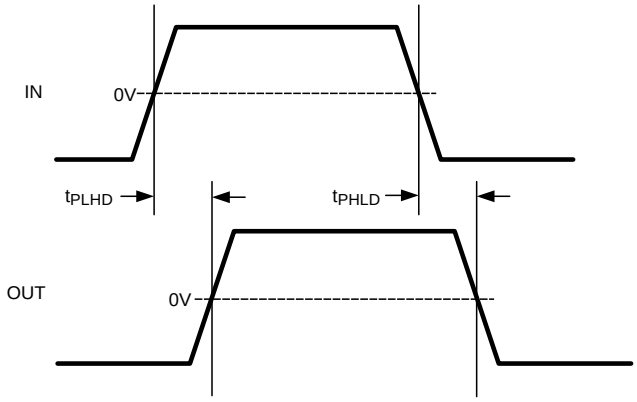


Figure 2. Propagation Delay Timing Diagram

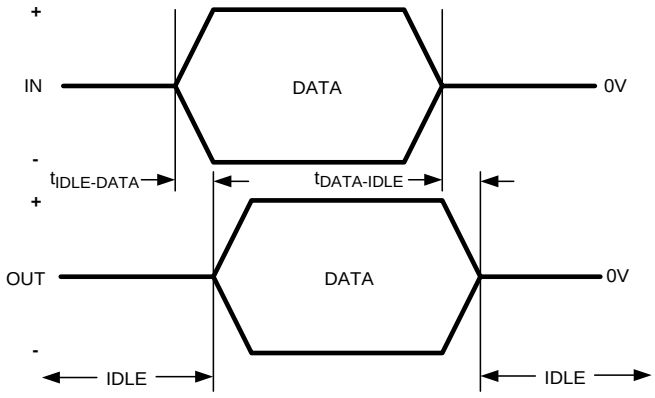


Figure 3. Transmit Idle-Data and Data-Idle Response Time

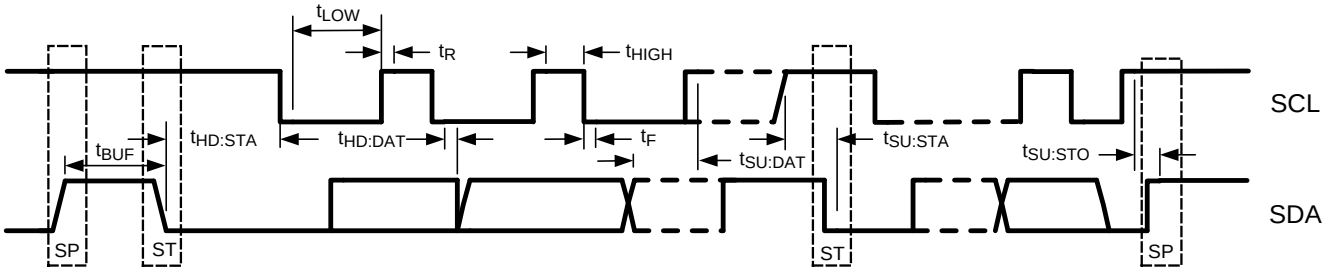
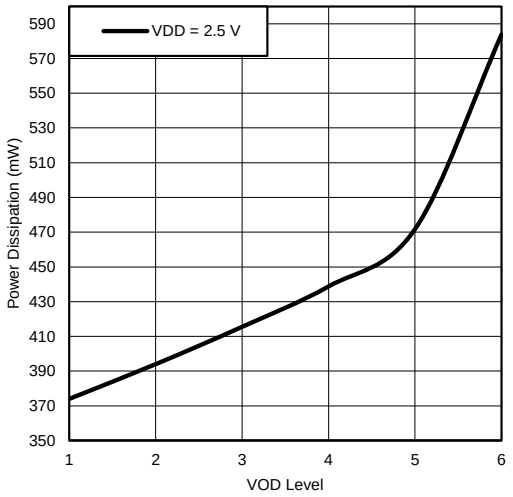


Figure 4. SMBus Timing Parameters

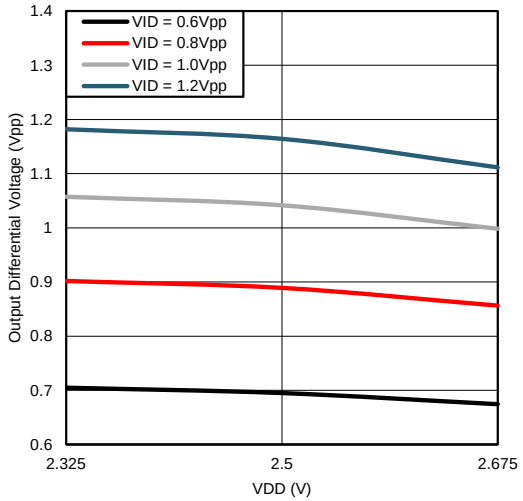
6.8 Typical Characteristics



Test Conditions

EQ	Level 4
VOD_DB	000'b
T	25°C

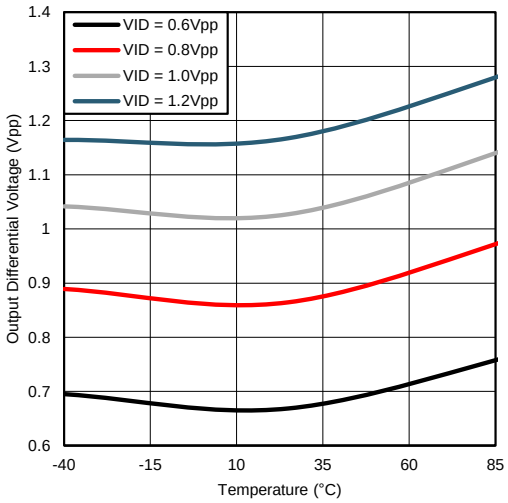
Figure 5. Typical Power Dissipation vs. VOD



Test Conditions

Data Rate, Test Pattern	1.5625 Gbps, 1010 Pattern
VOD	Level 6
EQ	Level 1
T	25°C

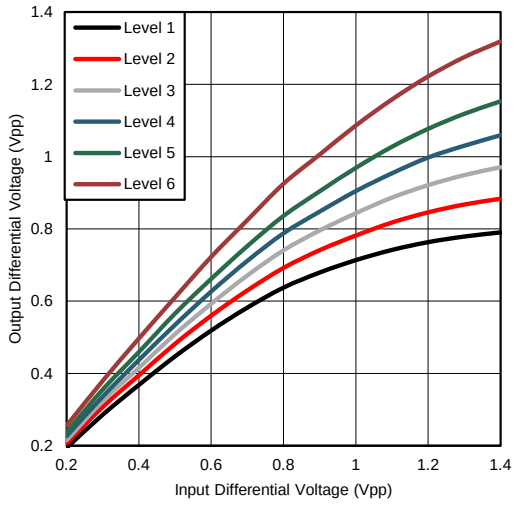
Figure 6. Typical VOD vs. VDD



Test Conditions

Data Rate, Test Pattern	1.5625 Gbps, 1010 Pattern
VOD	Level 6
EQ	Level 1
VDD	2.5 V

Figure 7. Typical VOD vs. Temperature



Test Conditions

Data Rate, Test Pattern	1.5625 Gbps, 1010 Pattern
EQ	Level 1
T	25°C
VDD	2.5 V

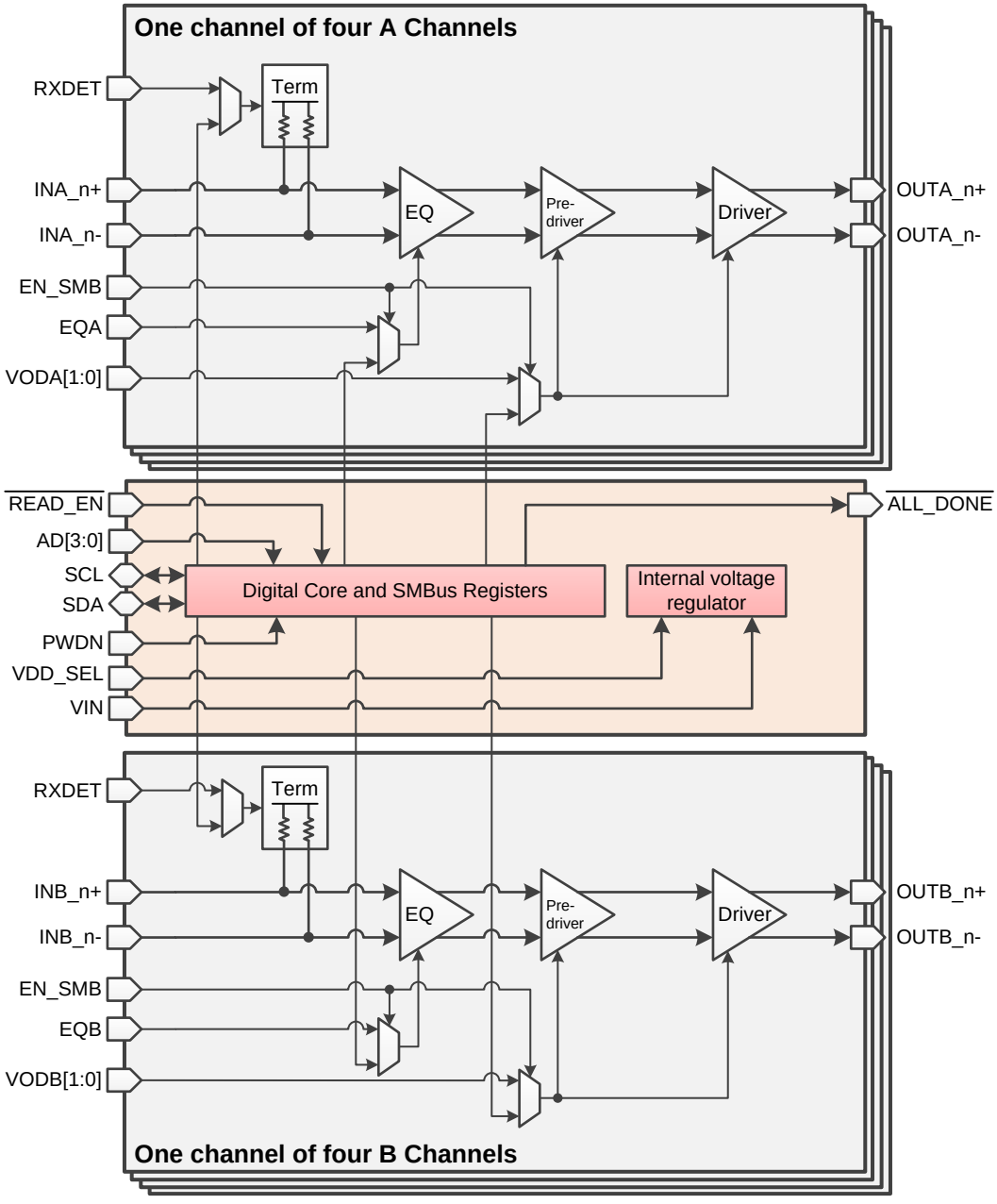
Figure 8. Typical VOD vs. VID

7 Detailed Description

7.1 Overview

The DS125BR820 provides linear equalization for lossy printed circuit board backplanes and balanced cables. The DS125BR820 operates in three modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = Float) to load register information from external EEPROM.

7.2 Functional Block Diagram



Functional Block Diagram (continued)

7.2.1 Functional Datapath Blocks

In an increasing number of high speed applications, transparency between Tx and Rx endpoints is essential to ensure high signal integrity. The DS125BR820 channel datapath uses one input gain stage equalization coupled with a linear driver. This combination provides a high level of transparency, thereby achieving greater drive distance in applications such as 40G-CR4, 40G-KR4, SAS, SATA, and PCIe that require Rx-Tx auto-negotiation and link-training. Refer to the Typical Applications section for more application information regarding recommended settings and placement.

7.3 Feature Description

The 4-level input pins use a resistor divider to help set the four valid control levels and provide a wider range of control settings when ENSMB = 0. There is an internal 30 kΩ pull-up and a 60 kΩ pull-down connected to the package pin. These resistors, together with the external resistor connection, combine to achieve the desired voltage level. By using the 1 kΩ pull-down, 20 kΩ pull-down, no connect, and 1 kΩ pull-up, the optimal voltage levels for each of the four input states are achieved as shown in Table 1.

Table 1. 4–Level Control Pin Settings

		RESULTING PIN VOLTAGE	
LEVEL	SETTING	3.3 V MODE	2.5 V MODE
0	Tie 1 kΩ to GND	0.10 V	0.08 V
R	Tie 20 kΩ to GND	1/3 x V_{IN}	1/3 x V_{DD}
F	Float (leave pin open)	2/3 x V_{IN}	2/3 x V_{DD}
1	Tie 1 kΩ to V_{IN} or V_{DD}	V_{IN} - 0.05 V	V_{DD} - 0.04 V

Typical 4-Level Input Thresholds

- Internal Threshold between 0 and R = 0.2 * V_{IN} or V_{DD}
- Internal Threshold between R and F = 0.5 * V_{IN} or V_{DD}
- Internal Threshold between F and 1 = 0.8 * V_{IN} or V_{DD}

In order to minimize the startup current associated with the integrated 2.5 V regulator, the 1 kΩ pull-up / pull-down resistors are recommended. If several four level inputs require the same setting, it is possible to combine two or more 1 kΩ resistors into a single lower value resistor. As an example, combining two inputs with a single 500 Ω resistor is a valid way to save board space.

7.4 Device Functional Modes

7.4.1 Pin Control Mode:

When in Pin Mode (ENSMB = 0), equalization and VOD (output amplitude) can be selected via pin control for both the A-channels and B-channels per Table 4. The RXDET pin provides either automatic or manual control for input termination (50 Ω or > 50 kΩ to VDD). The receiver electrical signal detect status threshold is adjustable via the SD_TH pin. By setting signal-detect threshold level via the SD_TH pin, status information about a valid signal detect assert/de-assert can be read back via SMBus registers. Pin control mode is ideal in situations where neither MCU or EEPROM is available to access the device via SMBus SDA/SCL lines.

7.4.2 Slave SMBus Mode:

When in Slave SMBus Mode (ENSMB = 1), the VOD (output amplitude), equalization, and termination disable features are all programmable on an individual channel basis, rather than in collective A-channel and B-channel groups. Upon assertion of ENSMB, the EQx and VODx settings are controlled by SMBus immediately. It is important to note that SMBus settings can only be changed from their defaults after asserting Register Enable by setting Reg 0x06[3] = 1. The EQx and VODx pins are subsequently converted to AD0-AD3 SMBus address inputs. The other external control pins (RXDET and SD_TH) remain active unless their respective registers are written to and the appropriate override bit is set. If the user overrides a pin control, the input voltage level of that control pin is ignored until ENSMB is driven low (Pin Mode). In the event that channels are powered down via the PWDN pin, the state of all register settings are not affected.

Device Functional Modes (continued)

Table 2. Rx Detect Settings

PWDN(1) (Pin 52)	RXDET (Pin 22)	SMBus REG Bit[3:2]	INPUT TERMINATION	RECOMMENDED USE	COMMENTS
0	0	00	Hi-Z		Manual Rx-Detect, input is Hi-Z
0	R	01	Pre Detect: Hi-Z Post Detect: 50 Ω	PCIe Only	Auto Rx-Detect, outputs test every 12 ms for 600 ms then stops; termination is Hi-Z until Rx detection; once detected input termination is 50 Ω Reset function by pulsing PWDN high for 5 µs then low again
0	F (Default)	10	Pre Detect: Hi-Z Post Detect: 50 Ω	PCIe Only	Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until Rx detection; once detected input termination is 50 Ω
0	1	11	50 Ω	40G-CR4/SR4/LR4 SAS/SATA	Manual Rx-Detect, input is 50 Ω For 40G-CR4/SR4/LR4/SAS/SATA applications, it is required to use this setting.
1	X	X	Hi-Z		Power Down mode, input is Hi-Z, output drivers are disabled Used to reset Rx-Detect State Machine when held high for 5 µs

(1) In SMBus Slave Mode, the Rx Detect State Machine can be manually reset in software by overriding the device $\overline{\text{PRSNT}}$ function. This is accomplished by setting the Override $\overline{\text{PRSNT}}$ bit (Reg 0x02[7]) and then toggling the $\overline{\text{PRSNT}}$ value bit (Reg 0x02[6]). See Table 9 for more information about resetting the Rx Detect State Machine.

Table 3. Signal Detect Status Threshold Level(1)(2)

LEVEL	SD_TH (Pin 26)	SMBus REG BIT[3:2] and[1:0]	[3:2] ASSERT LEVEL (mVp-p)		[1:0] DE-ASSERT LEVEL (mVp-p)	
			3 Gbps	12 Gbps	3 Gbps	12 Gbps
1	0	10	18	75	14	55
2	R	01	12	40	8	22
3	F (default)	00	15	50	11	37
4	1	11	16	58	12	45

(1) VDD = 2.5 V, 25°C, 11 00 11 00 pattern at 3 Gbps and 101010 pattern at 12 Gbps
(2) Signal detect status threshold sets the value at which a signal detect status is flagged via SMBus Reg 0x0A. Regardless of the threshold level, the output always remains enabled unless manually powered down.

7.4.3 SMBus Master Mode

When in SMBus Master Mode (ENSMB = Float), the VOD (output amplitude), equalization, and termination disable features for multiple devices can be loaded via external EEPROM. By asserting a Float condition on the ENSMB pin, an external EEPROM writes register settings to each device in accordance with its SMBus slave address. The settings programmable by external EEPROM provide only a subset of all the register bits available via SMBus Slave Mode, and the bit-mapping between SMBus Slave Mode registers and Master SMBus registers can be referenced in Table 6. Once the EEPROM successfully finishes loading each device's register settings, the device reverts back to SMBus Slave Mode and releases SDA/SCL control to an external master MCU. If the EEPROM fails to load settings to a particular device, for example due to an invalid or blank hex file, a time-out occurs and the device hangs in an unknown state.

7.5 Signal Conditioning Settings

Equalization and VOD settings accessible via the pin controls are chosen to meet the needs of most high speed applications. These settings can also be controlled via the SMBus registers. Each pin input has a total of four possible voltage level settings. Table 4 and Table 5 show both the Pin Mode and SMBus Mode settings that are used in order to program the equalization and VOD gain for each DS125BR820 channel.

Signal Conditioning Settings (continued)

Table 4. Equalizer Settings(1)(2)

EQUALIZATION BOOST RELATIVE to DC							
LEVEL	EQA(3) EQB	EQ – 8 bits[7:0]	dB at 1.5 GHz	dB at 2.5 GHz	dB at 4 GHz	dB at 5 GHz	dB at 6 GHz
1	0	xxxx xx00 = 0x00	2.1	2.5	2.7	2.9	3.0
2	R	xxxx xx01 = 0x01	4.0	5.1	6.4	6.8	7.4
3	F	xxxx xx10 = 0x02	5.5	7.0	8.3	8.6	8.9
4	1	xxxx xx11 = 0x03	6.8	8.3	9.5	9.6	9.8

(1) Optimal EQ setting should be determined via simulation and prototype verification.
(2) Equalization boost values are inclusive of package loss.
(3) To program EQ Level 1-4 correctly in Pin Mode, RESERVED3 and AD2 pins must be tied via 1 kΩ resistor to GND.

Table 5. Output Voltage Settings(1)

LEVEL	VODA1 VODB1	VODA0 VODB0	VOD - 3 bits[2:0]	VOD_DB - 3 bits[2:0]	VID Vp-p	VOD/VID Ratio(1)
--	--	--	000'b	000'b	1.2	0.57(2)
1	0	0	001'b	000'b	1.2	0.65
2	0	R	010'b	000'b	1.2	0.71
3	0	1	011'b	000'b	1.2	0.77
4	R	F	100'b	000'b	1.2	0.83
5	F	R	101'b	000'b	1.2	0.90
6	1	0	110'b	000'b	1.2	1.00
--	--	--	111'b	000'b	1.2	1.04(2)(3)

(1) For 40G-CR4/KR4/SAS/SATA/PCIe operation, it is important to keep the output amplitude and dynamic range as large as possible. When operating in Pin Mode, it is recommended to use VODA[1:0] = VODB[1:0] = Level 6. In SMBus Mode, it is also recommended to use Level 6 (that is, VOD = 110'b and VOD_DB = 000'b).
(2) These VOD settings are only accessible via SMBus Modes.
(3) VOD = 111'b setting in SMBus Mode is not recommended.

7.6 Programming

The DS125BR820 device supports reading directly from an external EEPROM device by implementing SMBus Master Mode. When using SMBus Master Mode, the DS125BR820 reads directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user must follow these specific guidelines.

- Maximum EEPROM size is 8K (1024 x 8-bit).
- Set ENSMB = Float — enable the SMBus Master Mode.
- The external EEPROM device address byte must be 0xA0 and capable of 1 MHz operation at 2.5 V and 3.3 V supply.
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is 0xB0.

When tying multiple DS125BR820 devices to the SDA and SCL bus, use these guidelines to configure the devices:

- Use SMBus AD[3:0] address bits so that each device can load its configuration from the EEPROM. Example below is for four devices. The first device in the sequence is conventionally address 0xB0, while subsequent devices follow the address order listed below.
  - U1: AD[3:0] = 0000 = 0xB0,
  - U2: AD[3:0] = 0001 = 0xB2,
  - U3: AD[3:0] = 0010 = 0xB4,
  - U4: AD[3:0] = 0011 = 0xB6
- Use a pull-up resistor on SDA and SCL; value = 2 kΩ to 5 kΩ
- Daisy-chain $\overline{\text{READ\_EN}}$ (Pin 26) and $\overline{\text{ALL\_DONE}}$ (Pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
  1. Tie $\overline{\text{READ\_EN}}$ of the first device in the chain (U1) to GND.
  2. Tie $\overline{\text{ALL\_DONE}}$ of U1 to $\overline{\text{READ\_EN}}$ of U2.
  3. Tie $\overline{\text{ALL\_DONE}}$ of U2 to $\overline{\text{READ\_EN}}$ of U3.
  4. Tie $\overline{\text{ALL\_DONE}}$ of U3 to $\overline{\text{READ\_EN}}$ of U4.
  5. Optional: Tie $\overline{\text{ALL\_DONE}}$ output of U4 to a LED to show the devices have been loaded successfully.

Once the $\overline{\text{ALL\_DONE}}$ status pin of the last device is flagged to indicate that all devices sharing the SMBus line have been successfully programmed, control of the SMBus line is released by the repeater and the device reverts back to SMBus Slave Mode. At this point, an external MCU can perform any additional Read or Write operations.

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS125BR820 device. The first three bytes of the EEPROM always contain a base header common and necessary to control initialization of all devices connected to the I2C bus. The CRC enable flag is used to enable or disable CRC checking. If CRC checking is disabled, a fixed pattern (8'hA5) is written/read instead of the CRC byte from the CRC location to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start address in the EEPROM. If the MAP bit is not present, the configuration data start address is assumed to follow the base header directly. Lastly, one bit in the base header is used to indicate whether EEPROM size > 256 bytes. This bit ensures that EEPROM slot addresses are formatted properly as one byte (EEPROM ≤ 256 bytes) or two bytes (EEPROM > 256 bytes) for subsequent address map headers. There are 37 bytes of data for each DS125BR820 device.

```
:20000000000010000000407002FAD4002FAD4002FAD4002FAD409805F5A8005F5A8005F5AD0
:20002000 8005F5A800005454 0000000000000000000000000000000000000000000000F6
:20006000000000000000000000000000000000000000000000000000000000000000000080
:20008000000000000000000000000000000000000000000000000000000000000000000060
:2000A000000000000000000000000000000000000000000000000000000000000000000040
:2000C000000000000000000000000000000000000000000000000000000000000000000020
:2000E000000000000000000000000000000000000000000000000000000000000000000000
:20004000000000000000000000000000000000000000000000000000000000000000000A0
```

Note: The maximum EEPROM size supported is 8 kbits (1024 x 8 bits).

7.6.1 EEPROM Register Map for Single Device

A detailed EEPROM Register Map for a single device is shown in Table 6. For instances where multiple devices are written to EEPROM, the device starting address definitions align starting with Table 6 Byte 0x03.

Table 6. EEPROM Register Map - Single Device With Default Value

EEPROM Address Byte			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description		0x00	CRC_EN	Address Map Present	EEPROM > 256 Bytes	Reserved	DEVICE COUNT[3]	DEVICE COUNT[2]	DEVICE COUNT[1]	DEVICE COUNT[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x01	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x02	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x03	PWDN_CH7	PWDN_CH6	PWDN_CH5	PWDN_CH4	PWDN_CH3	PWDN_CH2	PWDN_CH1	PWDN_CH0
SMBus Register			0x01[7]	0x01[6]	0x01[5]	0x01[4]	0x01[3]	0x01[2]	0x01[1]	0x01[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x04	Reserved	Reserved	Reserved	Reserved	Ovrd_PWDN	Reserved	Reserved	Reserved
SMBus Register			0x02[5]	0x02[4]	0x02[3]	0x02[2]	0x02[0]	0x04[7]	0x04[6]	0x04[5]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x05	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Ovrd_SD_TH	Reserved
SMBus Register			0x04[4]	0x04[3]	0x04[2]	0x04[1]	0x04[0]	0x06[4]	0x08[6]	0x08[5]
Default Value	0x04		0	0	0	0	0	1	0	0
Description		0x06	Reserved	Ovrd_RXDET	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x08[4]	0x08[3]	0x08[2]	0x08[1]	0x08[0]	0x0B[6]	0x0B[5]	0x0B[4]
Default Value	0x07		0	0	0	0	0	1	1	1
Description		0x07	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CH0_RXDET_1	CH0_RXDET_0
SMBus Register			0x0B[3]	0x0B[2]	0x0B[1]	0x0B[0]	0x0E[5]	0x0E[4]	0x0E[3]	0x0E[2]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x08	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CH0_EQ_1	CH0_EQ_0
SMBus Register			0x0F[7]	0x0F[6]	0x0F[5]	0x0F[4]	0x0F[3]	0x0F[2]	0x0F[1]	0x0F[0]
Default Value	0x2F		0	0	1	0	1	1	1	1

Table 6. EEPROM Register Map - Single Device With Default Value (continued)

EEPROM Address Byte			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description		0x09	CH0_SCP	Reserved	Reserved	Reserved	Reserved	CH0_VOD_2	CH0_VOD_1	CH0_VOD_0
SMBus Register			0x10[7]	0x10[6]	0x10[5]	0x10[4]	0x10[3]	0x10[2]	0x10[1]	0x10[0]
Default Value	0xAD		1	0	1	0	1	1	0	1
Description		0x0A	CH0_VOD_DB_2	CH0_VOD_DB_1	CH0_VOD_DB_0	Reserved	CH0_THa_1	CH0_THa_0	CH0_THd_1	CH0_THd_0
SMBus Register			0x11[2]	0x11[1]	0x11[0]	0x12[7]	0x12[3]	0x12[2]	0x12[1]	0x12[0]
Default Value	0x40		0	1	0	0	0	0	0	0
Description		0x0B	Reserved	Reserved	CH1_RXDET_1	CH1_RXDET_0	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x15[5]	0x15[4]	0x15[3]	0x15[2]	0x16[7]	0x16[6]	0x16[5]	0x16[4]
Default Value	0x02		0	0	0	0	0	0	1	0
Description		0x0C	Reserved	Reserved	CH1_EQ_1	CH1_EQ_0	CH1_SCP	Reserved	Reserved	Reserved
SMBus Register			0x16[3]	0x16[2]	0x16[1]	0x16[0]	0x17[7]	0x17[6]	0x17[5]	0x17[4]
Default Value	0xFA		1	1	1	1	1	0	1	0
Description		0x0D	Reserved	CH1_VOD_2	CH1_VOD_1	CH1_VOD_0	CH1_VOD_DB_2	CH1_VOD_DB_1	CH1_VOD_DB_0	Reserved
SMBus Register			0x17[3]	0x17[2]	0x17[1]	0x17[0]	0x18[2]	0x18[1]	0x18[0]	0x19[7]
Default Value	0xD4		1	1	0	1	0	1	0	0
Description		0x0E	CH1_THa_1	CH1_THa_0	CH1_THd_1	CH1_THd_0	Reserved	Reserved	CH2_RXDET_1	CH2_RXDET_0
SMBus Register			0x19[3]	0x19[2]	0x19[1]	0x19[0]	0x1C[5]	0x1C[4]	0x1C[3]	0x1C[2]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x0F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CH2_EQ_1	CH2_EQ_0
SMBus Register			0x1D[7]	0x1D[6]	0x1D[5]	0x1D[4]	0x1D[3]	0x1D[2]	0x1D[1]	0x1D[0]
Default Value	0x2F		0	0	1	0	1	1	1	1
Description		0x10	CH2_SCP	Reserved	Reserved	Reserved	Reserved	CH2_VOD_2	CH2_VOD_1	CH2_VOD_0
SMBus Register			0x1E[7]	0x1E[6]	0x1E[5]	0x1E[4]	0x1E[3]	0x1E[2]	0x1E[1]	0x1E[0]
Default Value	0xAD		1	0	1	0	1	1	0	1

Table 6. EEPROM Register Map - Single Device With Default Value (continued)

EEPROM Address Byte			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description		0x11	CH2_VOD_DB_2	CH2_VOD_DB_1	CH2_VOD_DB_0	Reserved	CH2_THa_1	CH2_THa_0	CH2_THd_1	CH2_THd_0
SMBus Register			0x1F[2]	0x1F[1]	0x1F[0]	0x20[7]	0x20[3]	0x20[2]	0x20[1]	0x20[0]
Default Value	0x40		0	1	0	0	0	0	0	0
Description		0x12	Reserved	Reserved	CH3_RXDET_1	CH3_RXDET_0	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x23[5]	0x23[4]	0x23[3]	0x23[2]	0x24[7]	0x24[6]	0x24[5]	0x24[4]
Default Value	0x02		0	0	0	0	0	0	1	0
Description		0x13	Reserved	Reserved	CH3_EQ_1	CH3_EQ_0	CH3_SCP	Reserved	Reserved	Reserved
SMBus Register			0x24[3]	0x24[2]	0x24[1]	0x24[0]	0x25[7]	0x25[6]	0x25[5]	0x25[4]
Default Value	0xFA		1	1	1	1	1	0	1	0
Description		0x14	Reserved	CH3_VOD_2	CH3_VOD_1	CH3_VOD_0	CH3_VOD_DB_2	CH3_VOD_DB_1	CH3_VOD_DB_0	Reserved
SMBus Register			0x25[3]	0x25[2]	0x25[1]	0x25[0]	0x26[2]	0x26[1]	0x26[0]	0x27[7]
Default Value	0xD4		1	1	0	1	0	1	0	0
Description		0x15	CH3_THa_1	CH3_THa_0	CH3_THd_1	CH3_THd_0	Reserved	hi_idle_SD CH0-3	hi_idle_SD CH4-7	fast_SD CH0-3
SMBus Register			0x27[3]	0x27[2]	0x27[1]	0x27[0]	0x28[6]	0x28[5]	0x28[4]	0x28[3]
Default Value	0x09		0	0	0	0	1	0	0	1
Description		0x16	fast_SD CH4-7	lo_gain_SD CH0-3	lo_gain_SD CH4-7	Reserved	Reserved	CH4_RXDET_1	CH4_RXDET_0	Reserved
SMBus Register			0x28[2]	0x28[1]	0x28[0]	0x2B[5]	0x2B[4]	0x2B[3]	0x2B[2]	0x2C[7]
Default Value	0x80		1	0	0	0	0	0	0	0
Description		0x17	Reserved	Reserved	Reserved	Reserved	Reserved	CH4_EQ_1	CH4_EQ_0	CH4_SCP
SMBus Register			0x2C[6]	0x2C[5]	0x2C[4]	0x2C[3]	0x2C[2]	0x2C[1]	0x2C[0]	0x2D[7]
Default Value	0x5F		0	1	0	1	1	1	1	1
Description		0x18	Reserved	Reserved	Reserved	Reserved	CH4_VOD_2	CH4_VOD_1	CH4_VOD_0	CH4_VOD_DB_2
SMBus Register			0x2D[6]	0x2D[5]	0x2D[4]	0x2D[3]	0x2D[2]	0x2D[1]	0x2D[0]	0x2E[2]
Default Value	0x5A		0	1	0	1	1	0	1	0

Table 6. EEPROM Register Map - Single Device With Default Value (continued)

EEPROM Address Byte			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description		0x19	CH4_VOD_DB_1	CH4_VOD_DB_0	Reserved	CH4_THa_1	CH4_THa_0	CH4_THd_1	CH4_THd_0	Reserved
SMBus Register			0x2E[1]	0x2E[0]	0x2F[7]	0x2F[3]	0x2F[2]	0x2F[1]	0x2F[0]	0x32[5]
Default Value	0x80		1	0	0	0	0	0	0	0
Description		0x1A	Reserved	CH5_RXDET_1	CH5_RXDET_0	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x32[4]	0x32[3]	0x32[2]	0x33[7]	0x33[6]	0x33[5]	0x33[4]	0x33[3]
Default Value	0x05		0	0	0	0	0	1	0	1
Description		0x1B	Reserved	CH5_EQ_1	CH5_EQ_0	CH5_SCP	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x33[2]	0x33[1]	0x33[0]	0x34[7]	0x34[6]	0x34[5]	0x34[4]	0x34[3]
Default Value	0xF5		1	1	1	1	0	1	0	1
Description		0x1C	CH5_VOD_2	CH5_VOD_1	CH5_VOD_0	CH5_VOD_DB_2	CH5_VOD_DB_1	CH5_VOD_DB_0	Reserved	CH5_THa_1
SMBus Register			0x34[2]	0x34[1]	0x34[0]	0x35[2]	0x35[1]	0x35[0]	0x36[7]	0x36[3]
Default Value	0xA8		1	0	1	0	1	0	0	0
Description		0x1D	CH5_THa_0	CH5_THd_1	CH5_THd_0	Reserved	Reserved	CH6_RXDET_1	CH6_RXDET_0	Reserved
SMBus Register			0x36[2]	0x36[1]	0x36[0]	0x39[5]	0x39[4]	0x39[3]	0x39[2]	0x3A[7]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x1E	Reserved	Reserved	Reserved	Reserved	Reserved	CH6_EQ_1	CH6_EQ_0	CH6_SCP
SMBus Register			0x3A[6]	0x3A[5]	0x3A[4]	0x3A[3]	0x3A[2]	0x3A[1]	0x3A[0]	0x3B[7]
Default Value	0x5F		0	1	0	1	1	1	1	1
Description		0x1F	Reserved	Reserved	Reserved	Reserved	CH6_VOD_2	CH6_VOD_1	CH6_VOD_0	CH6_VOD_DB_2
SMBus Register			0x3B[6]	0x3B[5]	0x3B[4]	0x3B[3]	0x3B[2]	0x3B[1]	0x3B[0]	0x3C[2]
Default Value	0x5A		0	1	0	1	1	0	1	0
Description		0x20	CH6_VOD_DB_1	CH6_VOD_DB_0	Reserved	CH6_THa_1	CH6_THa_0	CH6_THd_1	CH6_THd_0	Reserved
SMBus Register			0x3C[1]	0x3C[0]	0x3D[7]	0x3D[3]	0x3D[2]	0x3D[1]	0x3D[0]	0x40[5]
Default Value	0x80		1	0	0	0	0	0	0	0

Table 6. EEPROM Register Map - Single Device With Default Value (continued)

EEPROM Address Byte			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description		0x21	Reserved	CH7_RXDET_1	CH7_RXDET_0	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x40[4]	0x40[3]	0x40[2]	0x41[7]	0x41[6]	0x41[5]	0x41[4]	0x41[3]
Default Value	0x05		0	0	0	0	0	1	0	1
Description		0x22	Reserved	CH7_EQ_1	CH7_EQ_0	CH7_SCP	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x41[2]	0x41[1]	0x41[0]	0x42[7]	0x42[6]	0x42[5]	0x42[4]	0x42[3]
Default Value	0xF5		1	1	1	1	0	1	0	1
Description		0x23	CH7_VOD_2	CH7_VOD_1	CH7_VOD_0	CH7_VOD_DB_2	CH7_VOD_DB_1	CH7_VOD_DB_0	Reserved	CH7_THa_1
SMBus Register			0x42[2]	0x42[1]	0x42[0]	0x43[2]	0x43[1]	0x43[0]	0x44[7]	0x44[3]
Default Value	0xA8		1	0	1	0	1	0	0	0
Description		0x24	CH7_THa_0	CH7_THd_1	CH7_THd_0	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x44[2]	0x44[1]	0x44[0]	0x47[3]	0x47[2]	0x47[1]	0x47[0]	0x48[7]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x25	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x48[6]	0x4C[7]	0x4C[6]	0x4C[5]	0x4C[4]	0x4C[3]	0x4C[0]	0x59[0]
Default Value	0x00		0	0	0	0	0	0	0	0
Description		0x26	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x5A[7]	0x5A[6]	0x5A[5]	0x5A[4]	0x5A[3]	0x5A[2]	0x5A[1]	0x5A[0]
Default Value	0x54		0	1	0	1	0	1	0	0
Description		0x27	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SMBus Register			0x5B[7]	0x5B[6]	0x5B[5]	0x5B[4]	0x5B[3]	0x5B[2]	0x5B[1]	0x5B[0]
Default Value	0x54		0	1	0	1	0	1	0	0

Table 7. Example Of EEPROM for Four Devices Using Two Address Maps

EEPROM ADDRESS	ADDRESS (Hex)	EEPROM DATA	COMMENTS
0	00	0x43	CRC_EN = 0, Address Map = 1, >256 bytes = 0, Device Count[3:0] = 3
1	01	0x00	
2	02	0x10	EEPROM Burst Size
3	03	0x00	CRC not used
4	04	0x0B	Device 0 Address Location
5	05	0x00	CRC not used
6	06	0x0B	Device 1 Address Location
7	07	0x00	CRC not used
8	08	0x30	Device 2 Address Location
9	09	0x00	CRC not used
10	0A	0x30	Device 3 Address Location
11	0B	0x00	Begin Device 0, 1 - Address Offset 3
12	0C	0x00	
13	0D	0x04	
14	0E	0x07	
15	0F	0x00	
16	10	0x01	EQ CHB0 = 0x01
17	11	0xAD	VOD CHB0 = 101'b
18	12	0x00	VOD_DB CHB0 = 000'b
19	13	0x00	
20	14	0x1A	EQ CHB1 = 0x01
21	15	0xD0	VOD CHB1 = 101'b, VOD_DB CHB1 = 000'b
22	16	0x00	
23	17	0x01	EQ CHB2 = 0x01
24	18	0xAD	VOD CHB2 = 101'b
25	19	0x00	VOD_DB CHB2 = 000'b
26	1A	0x00	
27	1B	0x1A	EQ CHB3 = 0x01
28	1C	0xD0	VOD CHB3 = 101'b, VOD_DB CHB3 = 000'b
29	1D	0x09	Signal Detect Status Threshold Control
30	1E	0x80	Signal Detect Status Threshold Control
31	1F	0x07	EQ CHA0 = 0x03
32	20	0x5C	VOD CHA0 = 110'b
33	21	0x00	VOD_DB CHA0 = 000'b
34	22	0x00	
35	23	0x15	EQ CHA1 = 0x00
36	24	0xC0	VOD CHA1 = 110'b, VOD_DB CHA1 = 000'b
37	25	0x00	
38	26	0x07	EQ CHA2 = 0x03
39	27	0x5C	VOD CHA2 = 110'b
40	28	0x00	VOD_DB CHA2 = 000'b
41	29	0x00	
42	2A	0x75	EQ CHA3 = 0x00
43	2B	0xC0	VOD CHA3 = 110'b, VOD_DB CHA3 = 000'b
44	2C	0x00	
45	2D	0x00	
46	2E	0x54	

Table 7. Example Of EEPROM for Four Devices Using Two Address Maps (continued)

EEPROM ADDRESS	ADDRESS (Hex)	EEPROM DATA	COMMENTS
47	2F	0x54	End Device 0, 1 - Address Offset 39
48	30	0x00	Begin Device 2, 3 - Address Offset 3
49	31	0x00	
50	32	0x04	
51	33	0x07	
52	34	0x00	
53	35	0x01	EQ CHB0 = 0x01
54	36	0xAB	VOD CHB0 = 011'b
55	37	0x00	VOD_DB CHB0 = 000'b
56	38	0x00	
57	39	0x1A	EQ CHB1 = 0x01
58	3A	0xB0	VOD CHB1 = 011'b, VOD_DB CHB1 = 000'b
59	3B	0x00	
60	3C	0x01	EQ CHB2 = 0x01
61	3D	0xAB	VOD CHB2 = 011'b
62	3E	0x00	VOD_DB CHB2 = 000'b
63	3F	0x00	
64	40	0x1A	EQ CHB3 = 0x01
65	41	0xB0	VOD CHB3 = 011'b, VOD_DB CHB3 = 000'b
66	42	0x09	Signal Detect Status Threshold Control
67	43	0x80	Signal Detect Status Threshold Control
68	44	0x07	EQ CHA0 = 0x03
69	45	0x5C	VOD CHA0 = 110'b
70	46	0x00	VOD_DB CHA0 = 000'b
71	47	0x00	
72	48	0x15	EQ CHA1 = 0x00
73	49	0xA0	VOD CHA1 = 101'b, VOD_DB CHA1 = 000'b
74	4A	0x00	
75	4B	0x07	EQ CHA2 = 0x03
76	4C	0x5C	VOD CHA2 = 110'b
77	4D	0x00	VOD_DB CHA2 = 000'b
78	4E	0x00	
79	4F	0x15	EQ CHA3 = 0x00
80	50	0xA0	VOD CHA3 = 101'b, VOD_DB CHA3 = 000'b
81	51	0x00	
82	52	0x00	
83	53	0x54	
84	54	0x54	End Device 2, 3 - Address Offset 39

Note: CRC_EN = 0, Address Map = 1, >256 byte = 0, Device Count[3:0] = 3. Multiple devices can point to the same address map. Maximum EEPROM size is 8 kbits (1024 x 8-bits).

7.7 Register Maps

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. Tie ENSMB = 1 kΩ to VDD (2.5 V mode) or VIN (3.3 V mode) to enable SMBus Slave Mode and allow access to the configuration registers.

The DS125BR820 uses AD[3:0] inputs in both SMBus Modes. These AD[3:0] pins are the user set SMBus slave address inputs and have internal pull-downs. Based on the SMBus 2.0 specification, the DS125BR820 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). When AD[3:0] pins are left floating or pulled low, AD[3:0] = 0000'b, and the device default address byte is 0xB0. The device supports up to 16 address bytes, as shown in Table 8:

Table 8. Device Slave Address Bytes

AD[3:0] SETTINGS	FULL SLAVE ADDRESS BYTE (7-Bit ADDRESS + WRITE BIT)	7-Bit SLAVE ADDRESS (HEX)
0000	B0	58
0001	B2	59
0010	B4	5A
0011	B6	5B
0100	B8	5C
0101	BA	5D
0110	BC	5E
0111	BE	5F
1000	C0	60
1001	C2	61
1010	C4	62
1011	C6	63
1100	C8	64
1101	CA	65
1110	CC	66
1111	CE	67

The SDA/SCL pins are 3.3 V tolerant, but are not 5V tolerant. An external pull-up resistor is required on the SDA line. The resistor value can be from 2 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

7.7.1 Transfer Of Data Via The SMBus

During normal operation, the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH}, then the bus transfers to the IDLE state.

7.7.2 SMBus Transactions

The device supports WRITE and READ transactions. See Table 9 for register address, type (Read/Write, Read Only), default value, and function information.

7.7.3 Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE, and communication with other SMBus devices may now occur.

7.7.4 Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1”indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE, and communication with other SMBus devices may now occur.

7.7.5 Detailed Register Map

Table 9. SMBus Slave Mode Register Map

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x00	Observation	7	Reserved	R/W	0x00		Set bit to 0
		6:3	Address Bit AD[3:0]	R			Observation of AD[3:0] bits [6]: AD3 [5]: AD2 [4]: AD1 [3]: AD0
		2	EEPROM Read Done	R			1 = Device completed the read from external EEPROM
		1	Reserved	R/W			Set bit to 0
		0	Reserved	R/W			Set bit to 0
0x01	PWDN Channels	7:0	PWDN CHx	R/W	0x00	Yes	Power Down per Channel [7]: CH7 – CHA_3 [6]: CH6 – CHA_2 [5]: CH5 – CHA_1 [4]: CH4 – CHA_0 [3]: CH3 – CHB_3 [2]: CH2 – CHB_2 [1]: CH1 – CHB_1 [0]: CH0 – CHB_0 0x00 = all channels enabled 0xFF = all channels disabled Note: Override PWDN pin and enable register control via Reg 0x02[0]
0x02	Override PWDN, PRSNT	7	Override $\overline{\text{PRSNT}}$	R/W	0x00		1 = Override Automatic Rx Detect State Machine Reset
		6	$\overline{\text{PRSNT}}$ Value				1 = Set Rx Detect State Machine Reset 0 = Clear Rx Detect State Machine Reset
		5:2	Reserved			Yes	Set bits to 0
		1	Reserved				Set bit to 0
		0	Override PWDN			Yes	1 = Block PWDN pin control (Register control enabled) 0 = Allow PWDN pin control (Register control disabled)
0x03	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x04	Reserved	7:0	Reserved	R/W	0x00	Yes	Set bits to 0
0x05	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x06	Slave Register Control	7:5	Reserved	R/W	0x10		Set bits to 0
		4	Reserved			Yes	Set bit to 1
		3	Register Enable				1 = Enable SMBus Slave Mode Register Control **Note: In order to change VOD, VOD_DB, and EQ of the channels in slave mode, this bit must be set to 1.**
		2:0	Reserved				Set bits to 0
0x07	Digital Reset and Control	7	Reserved	R/W	0x01		Set bit to 0
		6	Reset Registers				1 = Self clearing reset for SMBus registers (register settings return to default values)
		5	Reset SMBus Master				1 = Self clearing reset to SMBus master state machine
		4:0	Reserved				Set bits to 0 0001'b
0x08	Override Pin Control	7	Reserved	R/W	0x00		Set bit to 0
		6	Override SD_TH			Yes	1 = Block SD_TH pin control (Register control enabled) 0 = Allow SD_TH pin control (Register control disabled)
		5:4	Reserved			Yes	Set bits to 0
		3	Override RXDET			Yes	1 = Block RXDET pin control (Register control enabled) 0 = Allow RXDET pin control (Register control disabled)
		2:0	Reserved			Yes	Set bits to 0

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x09	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x0A	Signal Detect Monitor	7:0	SD_TH Status	R	0x00		CH7 - CH0 Internal Signal Detect Indicator [7]: CH7 – CHA_3 [6]: CH6 – CHA_2 [5]: CH5 – CHA_1 [4]: CH4 – CHA_0 [3]: CH3 – CHB_3 [2]: CH2 – CHB_2 [1]: CH1 – CHB_1 [0]: CH0 – CHB_0 0 = Signal detected at input 1 = Signal not detected at input Note: These bits only function when RESERVED2 pin = FLOAT
0x0B	Reserved	7	Reserved	R/W	0x00		Set bit to 0
		6:0	Reserved	R/W	0x70	Yes	Set bits to 111 0000'b
0x0C-0x0D	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x0E	CH0 - CHB_0 RXDET	7:6	Reserved	R/W	0x00		Set bits to 0
		5:4	Reserved			Yes	Set bits to 0
		3:2	RXDET			Yes	00'b = Input is Hi-Z impedance 01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω 10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: Override RXDET pin and enable register control via Reg 0x08[3]
		1:0	Reserved				Set bits to 0
0x0F	CH0 - CHB_0 EQ	7:0	EQ Control	R/W	0x2F	Yes	INB_0 EQ Control - total of four levels. See Table 4.
0x10	CH0 - CHB_0 VOD	7	Short Circuit Protection	R/W	0xAD	Yes	1 = Enable the short circuit protection 0 = Disable the short circuit protection
		6:3	Reserved			Yes	Set bits to 0101'b
		2:0	VOD Control			Yes	OUTB_0 VOD Control: VOD / VID Ratio 000'b = 0.57 001'b = 0.65 010'b = 0.71 011'b = 0.77 100'b = 0.83 101'b = 0.90 (default) 110'b = 1.00 (recommended) 111'b = 1.04

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x11	CH0 - CHB_0 VOD_DB	7	RXDET Status	R	0x02		Observation bit for RXDET CH0 - CHB_0 1 = Input 50 Ω terminated to VDD 0 = Input is Hi-Z
		6:5	Reserved				Set bits to 0
		4:3	Reserved	R/W			Set bits to 0
		2:0	VOD_DB Control			Yes	OUTB_0 VOD_DB Control 000'b = 0 dB (recommended) 001'b = –1.5 dB 010'b = –3.5 dB (default) 011'b = –5 dB 100'b = –6 dB 101'b = –8 dB 110'b = –9 dB 111'b = –12 dB Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.
0x12	CH0 - CHB_0 SD_TH	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	Signal Detect Status Assert Threshold			Yes	Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default) 01'b = 40 mVp-p 10'b = 75 mVp-p 11'b = 58 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
		1:0	Signal Detect Status De-assert Threshold			Yes	Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default) 01'b = 22 mVp-p 10'b = 55 mVp-p 11'b = 45 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
0x13-0x14	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x15	CH1 - CHB_1 RXDET	7:6	Reserved	R/W	0x00		Set bits to 0
		5:4	Reserved			Yes	Set bits to 0
		3:2	RXDET			Yes	00'b = Input is Hi-Z impedance 01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω 10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: Override RXDET pin and enable register control via Reg 0x08[3]
		1:0	Reserved				Set bits to 0
0x16	CH1 - CHB_1 EQ	7:0	EQ Control	R/W	0x2F	Yes	INB_1 EQ Control - total of four levels. See Table 4.

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x17	CH1 - CHB_1 VOD	7	Short Circuit Protection	R/W	0xAD	Yes	1 = Enable the short circuit protection 0 = Disable the short circuit protection
		6:3	Reserved			Yes	Set bits to 0101'b
		2:0	VOD Control			Yes	OUTB_1 VOD Control: VOD / VID Ratio 000'b = 0.57 001'b = 0.65 010'b = 0.71 011'b = 0.77 100'b = 0.83 101'b = 0.90 (default) 110'b = 1.00 (recommended) 111'b = 1.04
0x18	CH1 - CHB_1 VOD_DB	7	RXDET Status	R	0x02		Observation bit for RXDET CH1 - CHB_1 1 = Input 50 Ω terminated to VDD 0 = Input is Hi-Z
		6:5	Reserved				Set bits to 0
		4:3	Reserved	R/W			Set bits to 0
		2:0	VOD_DB Control			Yes	OUTB_1 VOD_DB Control 000'b = 0 dB (recommended) 001'b = –1.5 dB 010'b = –3.5 dB (default) 011'b = –5 dB 100'b = –6 dB 101'b = –8 dB 110'b = –9 dB 111'b = –12 dB Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.
0x19	CH1 - CHB_1 SD_TH	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	Signal Detect Status Assert Threshold			Yes	Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default) 01'b = 40 mVp-p 10'b = 75 mVp-p 11'b = 58 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
		1:0	Signal Detect Status De-assert Threshold			Yes	Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default) 01'b = 22 mVp-p 10'b = 55 mVp-p 11'b = 45 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
0x1A-0x1B	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x1C	CH2 - CHB_2 RXDET	7:6	Reserved	R/W	0x00		Set bits to 0
		5:4	Reserved			Yes	Set bits to 0
		3:2	RXDET			Yes	00'b = Input is Hi-Z impedance 01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω 10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: Override RXDET pin and enable register control via Reg 0x08[3]
		1:0	Reserved				Set bits to 0
0x1D	CH2 - CHB_2 EQ	7:0	EQ Control	R/W	0x2F	Yes	INB_2 EQ Control - total of four levels. See Table 4.
0x1E	CH2 - CHB_2 VOD	7	Short Circuit Protection	R/W	0xAD	Yes	1 = Enable the short circuit protection 0 = Disable the short circuit protection
		6:3	Reserved			Yes	Set bits to 0101'b
		2:0	VOD Control			Yes	OUTB_2 VOD Control: VOD / VID Ratio 000'b = 0.57 001'b = 0.65 010'b = 0.71 011'b = 0.77 100'b = 0.83 101'b = 0.90 (default) 110'b = 1.00 (recommended) 111'b = 1.04
0x1F	CH2 - CHB_2 VOD_DB	7	RXDET Status	R	0x02		Observation bit for RXDET CH2 - CHB_2 1 = Input 50 Ω terminated to VDD 0 = Input is Hi-Z
		6:5	Reserved				Set bits to 0
		4:3	Reserved	R/W			Set bits to 0
		2:0	VOD_DB Control			Yes	OUTB_2 VOD_DB Control 000'b = 0 dB (recommended) 001'b = –1.5 dB 010'b = –3.5 dB (default) 011'b = –5 dB 100'b = –6 dB 101'b = –8 dB 110'b = –9 dB 111'b = –12 dB Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x20	CH2 - CHB_2 SD_TH	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	Signal Detect Status Assert Threshold			Yes	Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default) 01'b = 40 mVp-p 10'b = 75 mVp-p 11'b = 58 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
		1:0	Signal Detect Status De-assert Threshold			Yes	Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default) 01'b = 22 mVp-p 10'b = 55 mVp-p 11'b = 45 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
0x21-0x22	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x23	CH3 - CHB_3 RXDET	7:6	Reserved	R/W	0x00		Set bits to 0
		5:4	Reserved			Yes	Set bits to 0
		3:2	RXDET			Yes	00'b = Input is Hi-Z impedance 01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω 10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: Override RXDET pin and enable register control via Reg 0x08[3]
		1:0	Reserved				Set bits to 0
0x24	CH3 - CHB_3 EQ	7:0	EQ Control	R/W	0x2F	Yes	INB_3 EQ Control - total of four levels. See Table 4.
0x25	CH3 - CHB_3 VOD	7	Short Circuit Protection	R/W	0xAD	Yes	1 = Enable the short circuit protection 0 = Disable the short circuit protection
		6:3	Reserved			Yes	Set bits to 0101'b
		2:0	VOD Control			Yes	OUTB_3 VOD Control: VOD / VID Ratio 000'b = 0.57 001'b = 0.65 010'b = 0.71 011'b = 0.77 100'b = 0.83 101'b = 0.90 (default) 110'b = 1.00 (recommended) 111'b = 1.04

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x26	CH3 - CHB_3 VOD_DB	7	RXDET Status	R	0x02		Observation bit for RXDET CH3 - CHB_3 1 = Input 50 Ω terminated to VDD 0 = Input is Hi-Z
		6:5	Reserved				Set bits to 0
		4:3	Reserved	R/W			Set bits to 0
		2:0	VOD_DB Control			Yes	OUTB_3 VOD_DB Control 000'b = 0 dB (recommended) 001'b = –1.5 dB 010'b = –3.5 dB (default) 011'b = –5 dB 100'b = –6 dB 101'b = –8 dB 110'b = –9 dB 111'b = –12 dB Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.
0x27	CH3 - CHB_3 SD_TH	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	Signal Detect Status Assert Threshold			Yes	Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default) 01'b = 40 mVp-p 10'b = 75 mVp-p 11'b = 58 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
		1:0	Signal Detect Status De-assert Threshold			Yes	Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default) 01'b = 22 mVp-p 10'b = 55 mVp-p 11'b = 45 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
0x28	Signal Detect Status Control	7	Reserved	R/W	0x4C		Set bit to 0
		6	Reserved			Yes	Set bit to 1
		5:4	High SD_TH Status			Yes	Enable Higher Range of Signal Detect Status Thresholds [5]: CH0 - CH3 [4]: CH4 - CH7
		3:2	Fast Signal Detect Status			Yes	Enable Fast Signal Detect Status [3]: CH0 - CH3 [2]: CH4 - CH7 Note: In Fast Signal Detect, assert/de-assert response occurs after approximately 3-4 ns
		1:0	Reduced SD Status Gain			Yes	Enable Reduced Signal Detect Status Gain [1]: CH0 - CH3 [0]: CH4 - CH7
0x29-0x2A	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x2B	CH4 - CHA_0 RXDET	7:6	Reserved	R/W	0x00		Set bits to 0
		5:4	Reserved			Yes	Set bits to 0
		3:2	RXDET			Yes	00'b = Input is Hi-Z impedance 01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω 10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: Override RXDET pin and enable register control via Reg 0x08[3]
		1:0	Reserved				Set bits to 0
0x2C	CH4 - CHA_0 EQ	7:0	EQ Control	R/W	0x2F	Yes	INA_0 EQ Control - total of four levels. See Table 4.
0x2D	CH4 - CHA_0 VOD	7	Short Circuit Protection	R/W	0xAD	Yes	1 = Enable the short circuit protection 0 = Disable the short circuit protection
		6:3	Reserved			Yes	Set bits to 0101'b
		2:0	VOD Control			Yes	OUTA_0 VOD Control: VOD / VID Ratio 000'b = 0.57 001'b = 0.65 010'b = 0.71 011'b = 0.77 100'b = 0.83 101'b = 0.90 (default) 110'b = 1.00 (recommended) 111'b = 1.04
0x2E	CH4 - CHA_0 VOD_DB	7	RXDET Status	R	0x02		Observation bit for RXDET CH4 - CHA_0 1 = Input 50 Ω terminated to VDD 0 = Input is Hi-Z
		6:5	Reserved				Set bits to 0
		4:3	Reserved	R/W			Set bits to 0
		2:0	VOD_DB Control			Yes	OUTA_0 VOD_DB Control 000'b = 0 dB (recommended) 001'b = –1.5 dB 010'b = –3.5 dB (default) 011'b = –5 dB 100'b = –6 dB 101'b = –8 dB 110'b = –9 dB 111'b = –12 dB Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x2F	CH4 - CHA_0 SD_TH	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	Signal Detect Status Assert Threshold			Yes	Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default) 01'b = 40 mVp-p 10'b = 75 mVp-p 11'b = 58 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
		1:0	Signal Detect Status De-assert Threshold			Yes	Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default) 01'b = 22 mVp-p 10'b = 55 mVp-p 11'b = 45 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
0x30-0x31	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x32	CH5 - CHA_1 RXDET	7:6	Reserved	R/W	0x00		Set bits to 0
		5:4	Reserved			Yes	Set bits to 0
		3:2	RXDET			Yes	00'b = Input is Hi-Z impedance 01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω 10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: Override RXDET pin and enable register control via Reg 0x08[3]
		1:0	Reserved				Set bits to 0
0x33	CH5 - CHA_1 EQ	7:0	EQ Control	R/W	0x2F	Yes	INA_1 EQ Control - total of four levels. See Table 4.
0x34	CH5 - CHA_1 VOD	7	Short Circuit Protection	R/W	0xAD	Yes	1 = Enable the short circuit protection 0 = Disable the short circuit protection
		6:3	Reserved			Yes	Set bits to 0101'b
		2:0	VOD Control			Yes	OUTA_1 VOD Control: VOD / VID Ratio 000'b = 0.57 001'b = 0.65 010'b = 0.71 011'b = 0.77 100'b = 0.83 101'b = 0.90 (default) 110'b = 1.00 (recommended) 111'b = 1.04

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x35	CH5 - CHA_1 VOD_DB	7	RXDET Status	R	0x02		Observation bit for RXDET CH5 - CHA1 1 = Input 50 Ω terminated to VDD 0 = Input is Hi-Z
		6:5	Reserved				Set bits to 0
		4:3	Reserved	R/W			Set bits to 0
		2:0	VOD_DB Control			Yes	OUTA_1 VOD_DB Control 000'b = 0 dB (recommended) 001'b = –1.5 dB 010'b = –3.5 dB (default) 011'b = –5 dB 100'b = –6 dB 101'b = –8 dB 110'b = –9 dB 111'b = –12 dB Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.
0x36	CH5 - CHA_1 SD_TH	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	Signal Detect Status Assert Threshold			Yes	Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default) 01'b = 40 mVp-p 10'b = 75 mVp-p 11'b = 58 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
		1:0	Signal Detect Status De-assert Threshold			Yes	Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default) 01'b = 22 mVp-p 10'b = 55 mVp-p 11'b = 45 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
0x37-0x38	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x39	CH6 - CHA_2 RXDET	7:6	Reserved	R/W	0x00		Set bits to 0
		5:4	Reserved			Yes	Set bits to 0
		3:2	RXDET			Yes	00'b = Input is Hi-Z impedance 01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω 10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: Override RXDET pin and enable register control via Reg 0x08[3]
		1:0	Reserved				Set bits to 0
0x3A	CH6 - CHA_2 EQ	7:0	EQ Control	R/W	0x2F	Yes	INA_2 EQ Control - total of four levels. See Table 4.

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x3B	CH6 - CHA_2 VOD	7	Short Circuit Protection	R/W	0xAD	Yes	1 = Enable the short circuit protection 0 = Disable the short circuit protection
		6:3	Reserved			Yes	Set bits to 0101'b
		2:0	VOD Control			Yes	OUTA_2 VOD Control: VOD / VID Ratio 000'b = 0.57 001'b = 0.65 010'b = 0.71 011'b = 0.77 100'b = 0.83 101'b = 0.90 (default) 110'b = 1.00 (recommended) 111'b = 1.04
0x3C	CH6 - CHA_2 VOD_DB	7	RXDET Status	R	0x02		Observation bit for RXDET CH6 - CHA_2 1 = Input 50 Ω terminated to VDD 0 = Input is Hi-Z
		6:5	Reserved				Set bits to 0
		4:3	Reserved	R/W			Set bits to 0
		2:0	VOD_DB Control			Yes	OUTA_2 VOD_DB Control 000'b = 0 dB (recommended) 001'b = –1.5 dB 010'b = –3.5 dB (default) 011'b = –5 dB 100'b = –6 dB 101'b = –8 dB 110'b = –9 dB 111'b = –12 dB Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.
0x3D	CH6 - CHA_2 SD_TH	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	Signal Detect Status Assert Threshold			Yes	Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default) 01'b = 40 mVp-p 10'b = 75 mVp-p 11'b = 58 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
		1:0	Signal Detect Status De-assert Threshold			Yes	Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default) 01'b = 22 mVp-p 10'b = 55 mVp-p 11'b = 45 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
0x3E-0x3F	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x40	CH7 - CHA_3 RXDET	7:6	Reserved	R/W	0x00		Set bits to 0
		5:4	Reserved			Yes	Set bits to 0
		3:2	RXDET			Yes	00'b = Input is Hi-Z impedance 01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω 10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: Override RXDET pin and enable register control via Reg 0x08[3]
		1:0	Reserved				Set bits to 0
0x41	CH7 - CHA_3 EQ	7:0	EQ Control	R/W	0x2F	Yes	INA_3 EQ Control - total of four levels. See Table 4.
0x42	CH7 - CHA_3 VOD	7	Short Circuit Protection	R/W	0xAD	Yes	1 = Enable the short circuit protection 0 = Disable the short circuit protection
		6:3	Reserved			Yes	Set bits to 0101'b
		2:0	VOD Control			Yes	OUTA_3 VOD Control: VOD / VID Ratio 000'b = 0.57 001'b = 0.65 010'b = 0.71 011'b = 0.77 100'b = 0.83 101'b = 0.90 (default) 110'b = 1.00 (recommended) 111'b = 1.04
0x43	CH7 - CHA_3 VOD_DB	7	RXDET Status	R	0x02		Observation bit for RXDET CH7 - CHA_3 1 = Input 50 Ω terminated to VDD 0 = Input is Hi-Z
		6:5	Reserved				Set bits to 0
		4:3	Reserved	R/W			Set bits to 0
		2:0	VOD_DB Control			Yes	OUTA_3 VOD_DB Control 000'b = 0 dB (recommended) 001'b = –1.5 dB 010'b = –3.5 dB (default) 011'b = –5 dB 100'b = –6 dB 101'b = –8 dB 110'b = –9 dB 111'b = –12 dB Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.

Table 9. SMBus Slave Mode Register Map (continued)

Address	Register Name	Bit	Field	Type	Default	EEPROM Reg Bit	Description
0x44	CH7 - CHA_3 SD_TH	7	Reserved	R/W	0x00	Yes	Set bit to 0
		6:4	Reserved				Set bits to 0
		3:2	Signal Detect Status Assert Threshold			Yes	Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default) 01'b = 40 mVp-p 10'b = 75 mVp-p 11'b = 58 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
		1:0	Signal Detect Status De-assert Threshold			Yes	Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default) 01'b = 22 mVp-p 10'b = 55 mVp-p 11'b = 45 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]
0x45	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x46	Reserved	7:0	Reserved	R/W	0x38		Set bits to 0x38
0x47	Reserved	7:4	Reserved	R/W	0x00		Set bits to 0
		3:0	Reserved			Yes	Set bits to 0
0x48	Reserved	7:6	Reserved	R/W	0x05	Yes	Set bits to 0
		5:0	Reserved	R/W			Set bits to 00 0101'b
0x49-0x4B	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x4C	Reserved	7:3	Reserved	R/W	0x00	Yes	Set bits to 0
		2:1	Reserved	R/W			Set bits to 0
		0	Reserved	R/W		Yes	Set bits to 0
0x4D-0x50	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x51	Device ID	7:5	VERSION	R	0x85		100'b
		4:0	ID				0 0101'b
0x52-0x55	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0
0x56	Reserved	7:0	Reserved	R/W	0x10		Set bits to 0x10
0x57	Reserved	7:0	Reserved	R/W	0x64		Set bits to 0x64
0x58	Reserved	7:0	Reserved	R/W	0x21		Set bits to 0x21
0x59	Reserved	7:1	Reserved	R/W	0x00		Set bits to 0
		0	Reserved			Yes	Set bit to 0
0x5A	Reserved	7:0	Reserved	R/W	0x54	Yes	Set bits to 0x54
0x5B	Reserved	7:0	Reserved	R/W	0x54	Yes	Set bits to 0x54
0x5C-0x61	Reserved	7:0	Reserved	R/W	0x00		Set bits to 0

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Signal Integrity in 40G-CR4/KR4/SAS/SATA/PCIe Applications

In 40G-CR4/KR4/SAS/SATA/PCIe applications, specifications require Rx-Tx link training to establish and optimize signal conditioning settings for data rates up to 12.5 Gbps. In link training, the Rx partner requests a series of FIR coefficients from the Tx partner at speed. This polling sequence is designed to pre-condition the signal path with an optimized link between the endpoints. Link training occurs at the following data-rates:

Table 10. Link Training Data-Rates

PROTOCOL (1)	OPERATING DATA RATE (Gbps)
40G-CR4	10.3125
40G-KR4	10.3125
SAS-3	12.0
PCIe Gen-3	8.0

(1) There is no link training with Tx FIR coefficients for the respective lower generation data rates.

The DS125BR820 works to extend the reach possible by using active linear equalization to the channel, boosting attenuated signals so that they can be more easily recovered at the Rx. The repeater outputs are specially designed to be transparent to Tx FIR signaling in order to pass information critical for optimal link training to the Rx. Suggested settings for the A-channels and B-channels are given in Table 11 and Table 12. Further adjustments to EQx and VODx settings may optimize signal margin on the link for different system applications:

Table 11. Suggested Device Settings in Pin Mode

CHANNEL SETTINGS	PIN MODE
EQx	Level 1
VODx[1:0]	Level 6 (1, 0)

Table 12. Suggested Device Settings in SMBus Modes

CHANNEL SETTINGS	SMBus MODES
EQx	0x00
VODx	110'b
VOD_DB	000'b

The SMBus Slave Mode code example in Table 13 may be used to program the DS125BR820 with the recommended device settings.

Table 13. SMBus Example Sequence

REGISTER	WRITE VALUE	COMMENTS
0x06	0x18	Set SMBus Slave Mode Register Enable.
0x0F	0x00	Set CHB_0 EQ to 0x00.
0x10	0xAE	Set CHB_0 VOD to 110'b.
0x11	0x00	Set CHB_0 VOD_DB to 000'b.
0x16	0x00	Set CHB_1 EQ to 0x00.
0x17	0xAE	Set CHB_1 VOD to 110'b.

Table 13. SMBus Example Sequence (continued)

REGISTER	WRITE VALUE	COMMENTS
0x18	0x00	Set CHB_1 VOD_DB to 000'b.
0x1D	0x00	Set CHB_2 EQ to 0x00.
0x1E	0xAE	Set CHB_2 VOD to 110'b.
0x1F	0x00	Set CHB_2 VOD_DB to 000'b.
0x24	0x00	Set CHB_3 EQ to 0x00.
0x25	0xAE	Set CHB_3 VOD to 110'b.
0x26	0x00	Set CHB_3 VOD_DB to 000'b.
0x2C	0x00	Set CHA_0 EQ to 0x00.
0x2D	0xAE	Set CHA_0 VOD to 110'b.
0x2E	0x00	Set CHA_0 VOD_DB to 000'b.
0x33	0x00	Set CHA_1 EQ to 0x00.
0x34	0xAE	Set CHA_1 VOD to 110'b.
0x35	0x00	Set CHA_1 VOD_DB to 000'b.
0x3A	0x00	Set CHA_2 EQ to 0x00.
0x3B	0xAE	Set CHA_2 VOD to 110'b.
0x3C	0x00	Set CHA_2 VOD_DB to 000'b.
0x41	0x00	Set CHA_3 EQ to 0x00.
0x42	0xAE	Set CHA_3 VOD to 110'b.
0x43	0x00	Set CHA_3 VOD_DB to 000'b.

8.1.2 Signal Integrity in 40G-SR4/LR4 Applications

In 40G-SR4/LR4 applications, the ideal device settings must be tuned. In particular, EQ and VOD settings must be optimized in order to aid the link partners in meeting the nPPI eye mask test. While tuning the DS125BR820 contributes to signal quality improvement, it is equally important to ensure that the link partner ASIC Tx FIR signal characteristics are optimized as well to facilitate error-free data transmission. Suggested settings for the A-channels and B-channels in a 40G-SR4/LR4 environment can be referenced in Table 11 and Table 12.

8.1.3 Rx Detect Functionality in 40G-CR4/KR4/SAS/SATA Applications

Unlike PCIe systems, 40G-CR4/KR4/SAS/SATA systems use a low speed communications sequence to detect and communicate device capabilities between host ASIC and link partners. This communication eliminates the need to detect for endpoints like in a PCIe application. For 40G-CR4/KR4/SAS/SATA systems, it is recommended to tie the RXDET pin high. This ensures any link-training sequences sent by the host ASIC can reach the link partner receiver without any additional latency due to termination detection sequences.

8.2 Typical Applications

8.2.1 Generic High Speed Repeater

The DS125BR820 extends PCB and cable reach in multiple applications by using active linear equalization. The high linearity of this device aids specifically in protocols requiring link training and can be used in line cards, backplanes, motherboards, and active cable assemblies, thereby improving margin and overall eye performance. The capability of the repeater can be explored across a range of data rates and ASIC-to-link-partner signaling, as shown in the following two test setup connections.

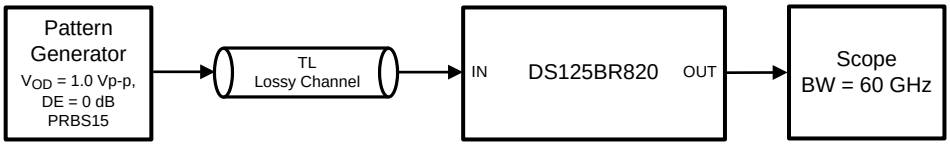


Figure 9. Test Setup Connections Diagram

Typical Applications (continued)

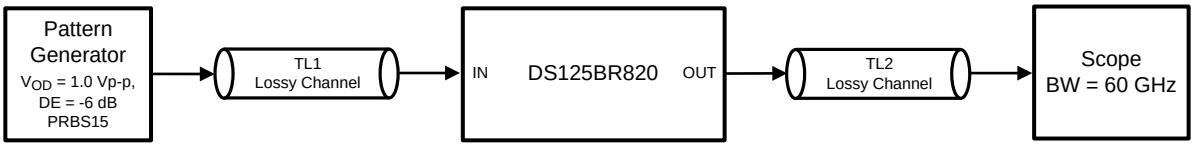


Figure 10. Test Setup Connections Diagram

8.2.1.1 Design Requirements

As with any high speed design, there are many factors which influence the overall performance. Below are a list of critical areas for consideration and study during design.

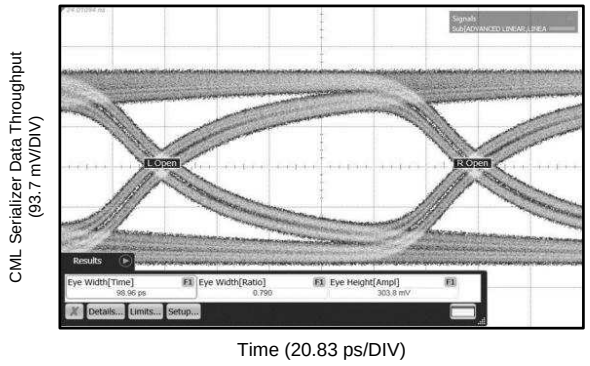
- Use 100 Ω impedance traces. Generally these are very loosely coupled to ease routing length differences.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- The maximum body size for AC-coupling capacitors is 0402.
- Back-drill connector vias and signal vias to minimize stub length.
- Use Reference plane vias to ensure a low inductance path for the return current.

8.2.1.2 Detailed Design Procedure

The DS125BR820 is designed to be placed at an offset location with respect to the overall channel attenuation. In order to optimize performance, the repeater requires tuning to extend the reach of the cable or trace length while also recovering a solid eye opening. To tune the repeater, the settings mentioned in Table 11 (for Pin Mode) and Table 12 (for SMBus Modes) are recommended as a default starting point for most applications. Once these settings are configured, additional tuning of the EQ and, to a lesser extent, VOD may be required to optimize the repeater performance for each specific application environment.

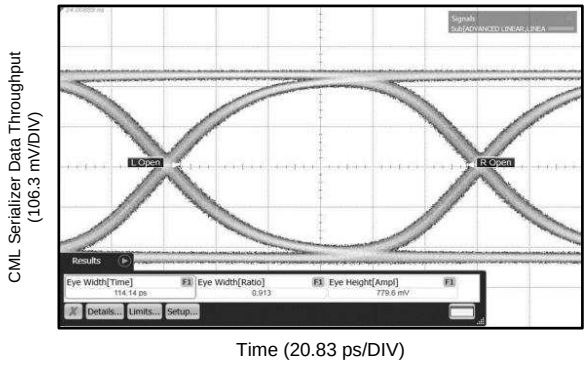
Examples of the repeater performance as a generic high speed datapath repeater are illustrated in the performance curves in the next section.

8.2.1.3 Application Performance Plots



No Repeater Used
TJ (1.0E-12) = 21.6 ps

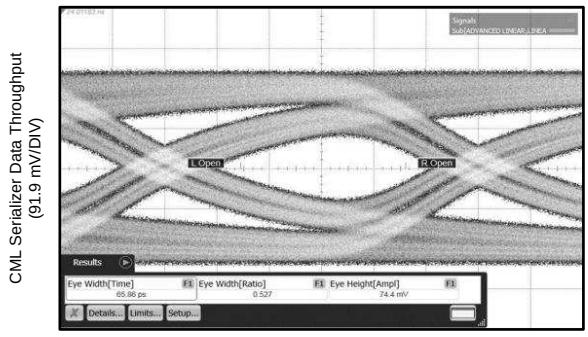
Figure 11. TL = 5 Inch 5–Mil FR4 Trace, No Repeater, 8 Gbps



DS125BR820 Settings: EQA = Level 2, VODA = Level 6
TJ (1.0E-12) = 13.6 ps

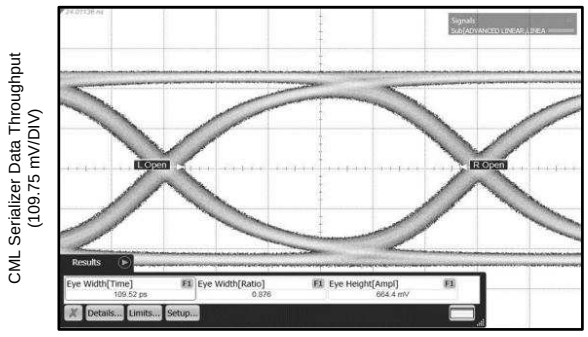
Figure 12. TL = 5 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 8 Gbps

Typical Applications (continued)



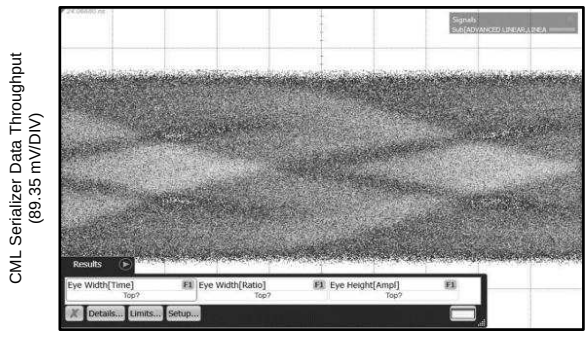
No Repeater Used
TJ (1.0E-12) = 43.7 ps

Figure 13. TL = 10 Inch 5–Mil FR4 Trace, No Repeater, 8 Gbps



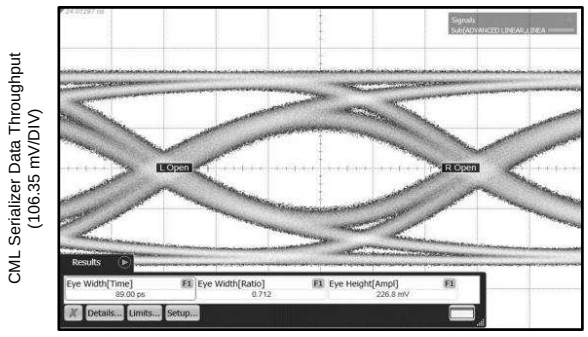
DS125BR820 Settings: EQA = Level 3, VODA = Level 6
TJ (1.0E-12) = 18.1 ps

Figure 14. TL= 10 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 8 Gbps



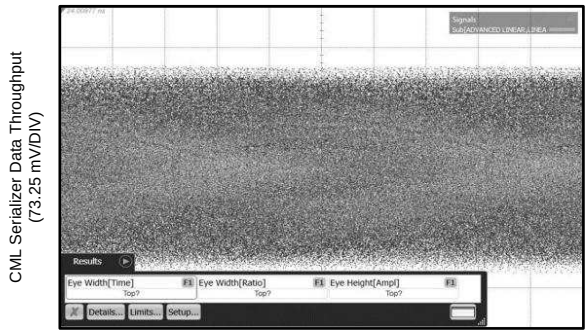
No Repeater Used
TJ (1.0E-12) = Not Available Due to Closed Eye

Figure 15. TL = 20 Inch 5–Mil FR4 Trace, No Repeater, 8 Gbps



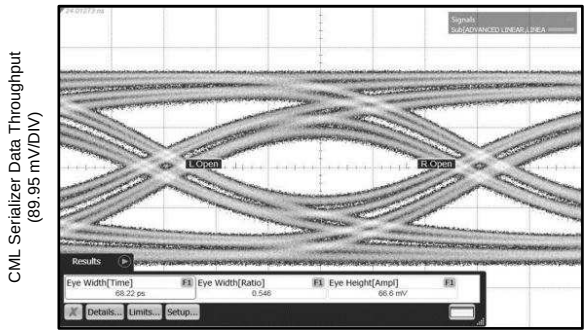
DS125BR820 Settings: EQA = Level 4, VODA = Level 6
TJ (1.0E-12) = 35.5 ps

Figure 16. TL = 20 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 8 Gbps



No Repeater
TJ (1.0E-12) = Not Available Due to Closed Eye

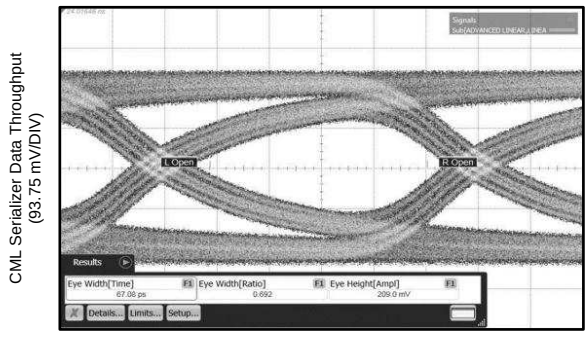
Figure 17. TL = 5-Meter 30-AWG 100 Ω Twin-Axial Cable, No Repeater, 8 Gbps



DS125BR820 Settings: EQA = Level 4, VODA = Level 6
TJ (1.0E-12) = 41.4 ps

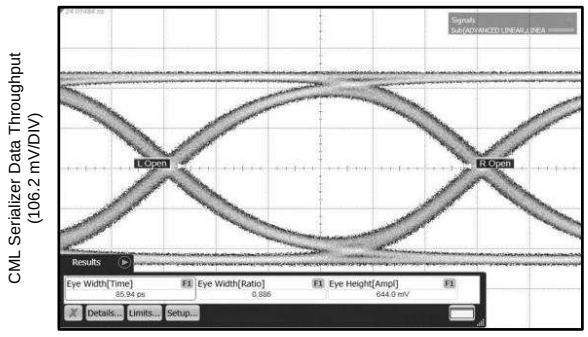
Figure 18. TL = 5-Meter 30-AWG 100 Ω Twin-Axial Cable, DS125BR820 CHA_0, 8 Gbps

Typical Applications (continued)



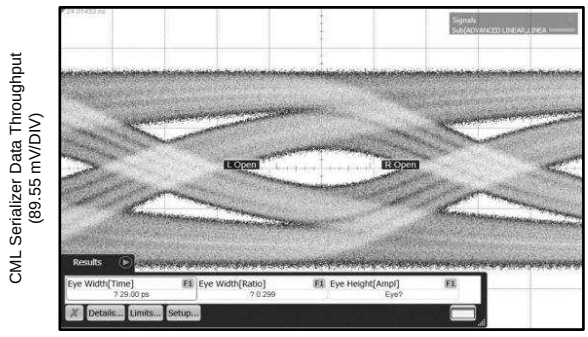
No Repeater Used
TJ (1.0E-12) = 24.3 ps

Figure 19. TL = 5 Inch 5–Mil FR4 Trace, No Repeater, 10.3125 Gbps



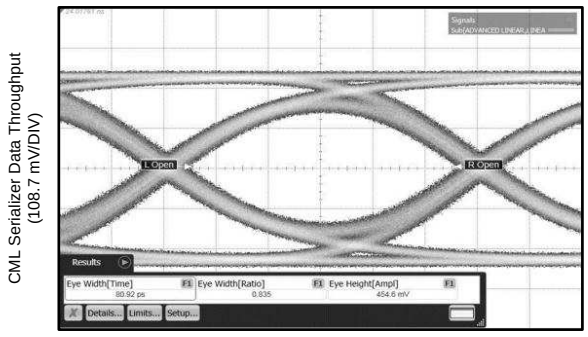
DS125BR820 Settings: EQA = Level 2, VODA = Level 6
TJ (1.0E-12) = 14.0 ps

Figure 20. TL = 5 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 10.3125 Gbps



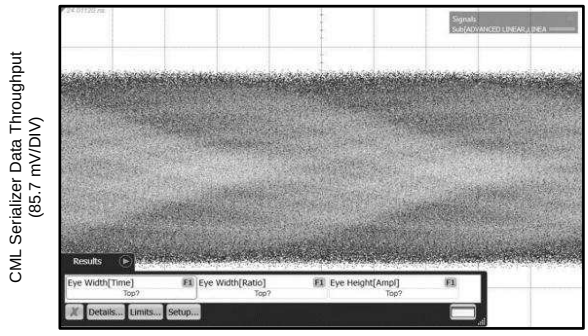
No Repeater Used
TJ (1.0E-12) = 50.6 ps

Figure 21. TL = 10 Inch 5–Mil FR4 Trace, No Repeater, 10.3125 Gbps



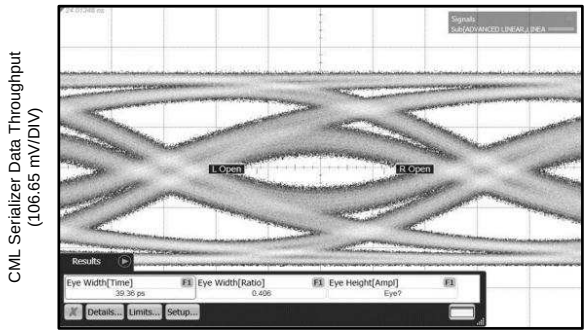
DS125BR820 Settings: EQA = Level 3, VODA = Level 6
TJ (1.0E-12) = 18.7 ps

Figure 22. TL= 10 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 10.3125 Gbps



No Repeater Used
TJ (1.0E-12) = Not Available Due to Closed Eye

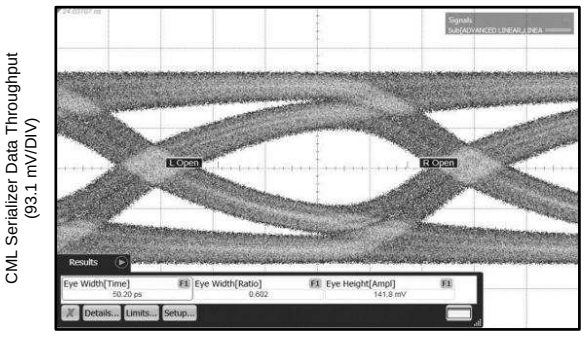
Figure 23. TL = 20 Inch 5–Mil FR4 Trace, No Repeater, 10.3125 Gbps



DS125BR820 Settings: EQA = Level 4, VODA = Level 6
TJ (1.0E-12) = 49.1 ps

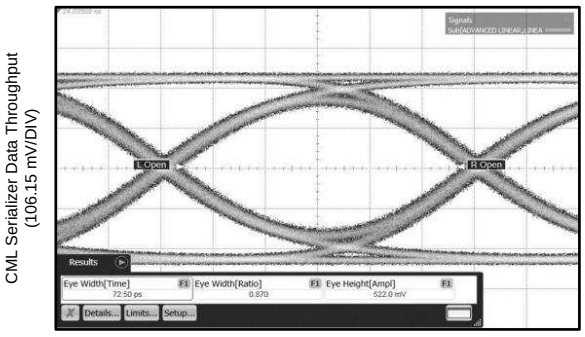
Figure 24. TL = 20 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 10.3125 Gbps

Typical Applications (continued)



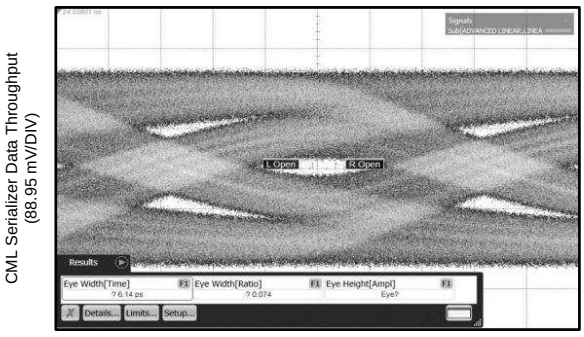
No Repeater
TJ (1.0E-12) = 26.1 ps

Figure 25. TL = 5 Inch 5–Mil FR4 Trace, No Repeater, 12 Gbps



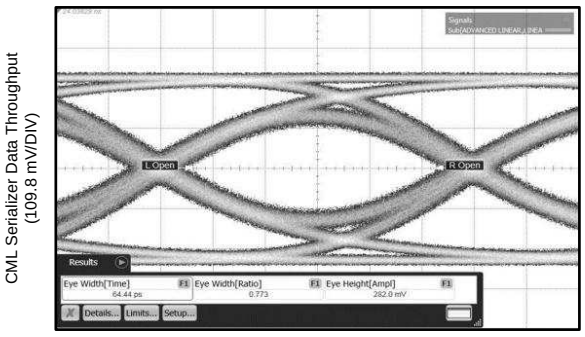
DS125BR820 Settings: EQA = Level 2, VODA = Level 6
TJ (1.0E-12) = 13.1 ps

Figure 26. TL = 5 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 12 Gbps



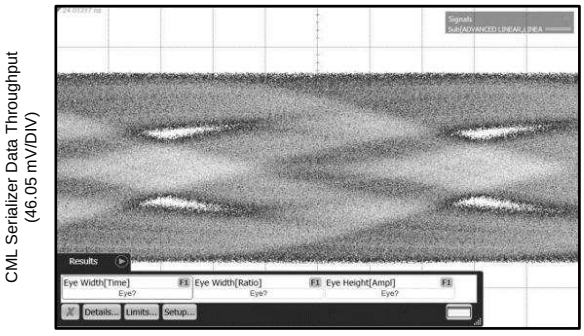
No Repeater
TJ (1.0E-12) = 56.6 ps

Figure 27. TL = 10 Inch 5–Mil FR4 Trace, No Repeater, 12 Gbps



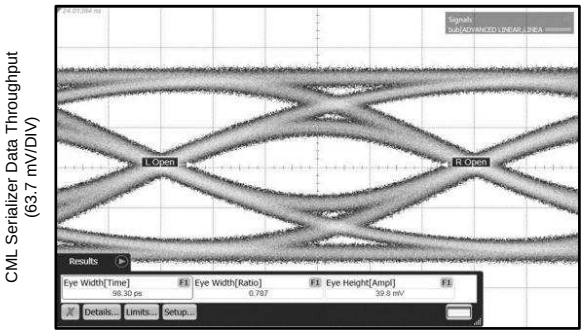
DS125BR820 Settings: EQA = Level 3, VODA = Level 6
TJ (1.0E-12) = 20.1 ps

Figure 28. TL = 10 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 12 Gbps



No Repeater Used
TJ (1.0E-12) = Not Available Due to Closed Eye

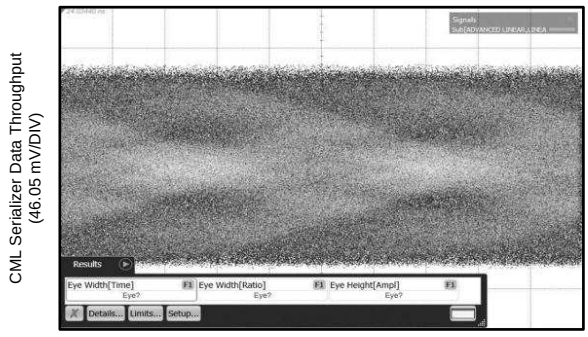
Figure 29. TL1 = 15 Inch 5–Mil FR4 Trace, TL2 = 10 Inch 5–Mil FR4 Trace, No Repeater, 8 Gbps



DS125BR820 Settings: EQA = Level 4, VODA = Level 6
TJ (1.0E-12) = 33.0 ps

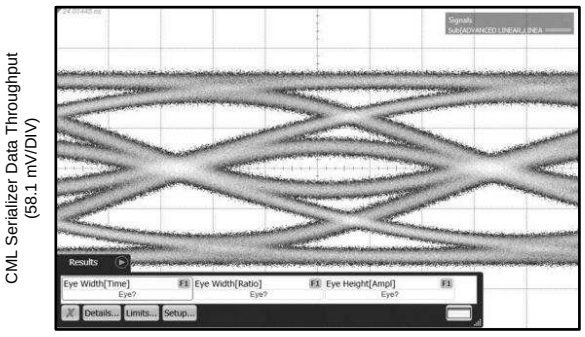
Figure 30. TL1 = 15 Inch 5–Mil FR4 Trace, TL2 = 10 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 8 Gbps

Typical Applications (continued)



No Repeater Used
TJ (1.0E-12) = Not Available Due to Closed Eye

Figure 31. TL1 = 15 Inch 5–Mil FR4 Trace, TL2 = 10 Inch 5–Mil FR4 Trace, No Repeater, 10.3125 Gbps



DS125BR820 Settings: EQA = Level 4, VODA = Level 6
TJ (1.0E-12) = 47.9 ps

Figure 32. TL1 = 15 Inch 5–Mil FR4 Trace, TL2 = 10 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 10.3125 Gbps

8.2.2 Front Port Applications (40G-CR4/SR4/LR4)

The DS125BR820 can be used in front port applications to extend the reach between the host ASIC and the front-port cage. Front port applications typically include 40G-CR4/SR4/LR4. For 40GbE front port optical protocols like 40G-SR4/LR4, the DS125BR820 is designed to support the front-port eye mask and jitter requirements of applicable standards like nPPI. For 40GbE front port copper protocols like 40G-CR4, the DS125BR820 is designed to provide channel equalization in a transparent fashion so as not to inhibit IEEE802.3ba Clause 72 link training. In all of these front port cases, the DS125BR820 can also be used to support eye mask and jitter requirements for SFF-8431 if the 40GbE QSFP+ port is intended to support 4x10G SFP+ applications as well. Below is a typical example of the DS125BR820 used in a front port line-card application.

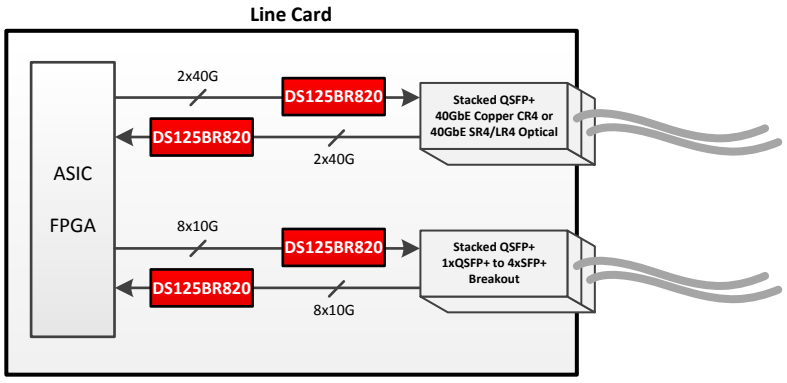


Figure 33. Typical Front-Port System Configuration

8.2.2.1 Design Requirements

As with any high speed design, there are many factors that influence the overall performance. Please reference Design Requirements in the Generic High Speed Repeater application section for a list of critical areas for consideration and study during design.

Typical Applications (continued)

8.2.2.2 Detailed Design Procedure

In front port applications, it is important to ensure that the placement of the DS125BR820 corresponds with the direction of the data flow, since the device is unidirectional. For egress applications, the DS125BR820 should be placed close to the connector cage, and for ingress applications, the DS125BR820 should be placed closer to the switch ASIC. Once the DS125BR820 placement is decided on the signal path, the repeater must be tuned. To tune the repeater, the settings mentioned in Table 11 (for Pin Mode) and Table 12 (for SMBus Modes) are recommended as a default starting point for most applications. Once these settings are configured, additional tuning of the EQ and, to a lesser extent, VOD may be required to optimize the repeater performance in order to meet the link training requirements for 40G-CR4 and eye mask requirements for 40G-SR4/LR4.

An example of a test configuration used to evaluate the DS125BR820 in this application can be seen in Figure 34. For more information about DS125BR820 front port applications, please refer to application note SNLA226:

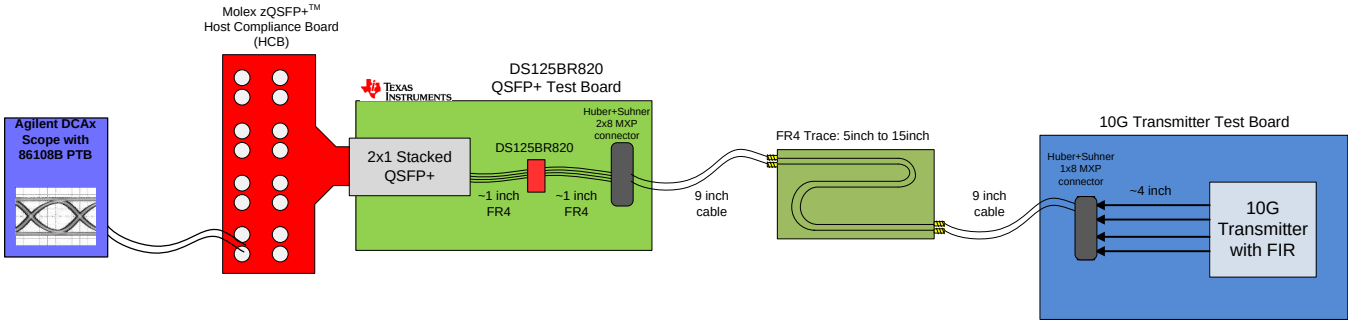
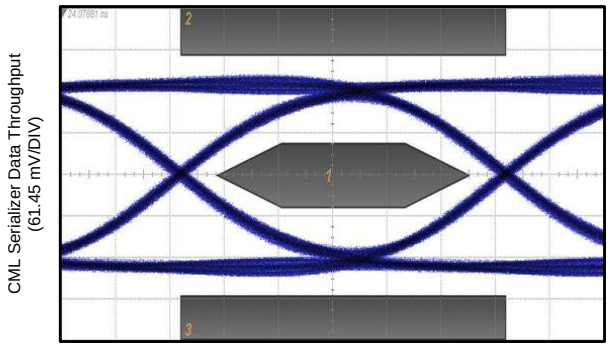


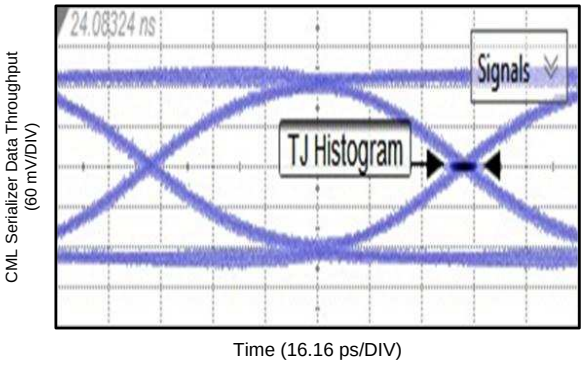
Figure 34. 10 GbE Transmitter with DS125BR820 QSFP+ Test Board

8.2.2.3 Application Performance Plots



DS125BR820 Settings: EQA = Level 2, VODA = Level 6

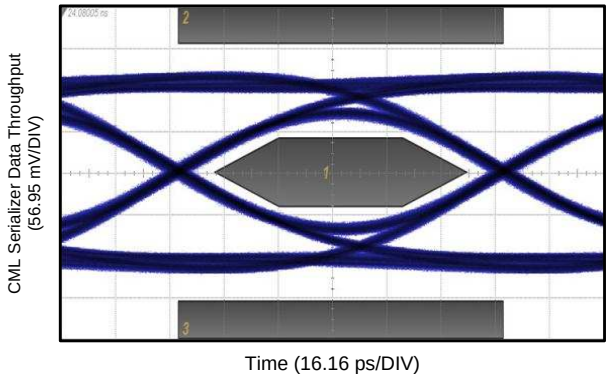
Figure 35. nPPI Eye Mask Performance with 5 Inch 4-Mil FR4 Input Trace, Test Pattern = PRBS-9, 10.3125 Gbps



DS125BR820 Settings: EQA = Level 2, VODA = Level 6

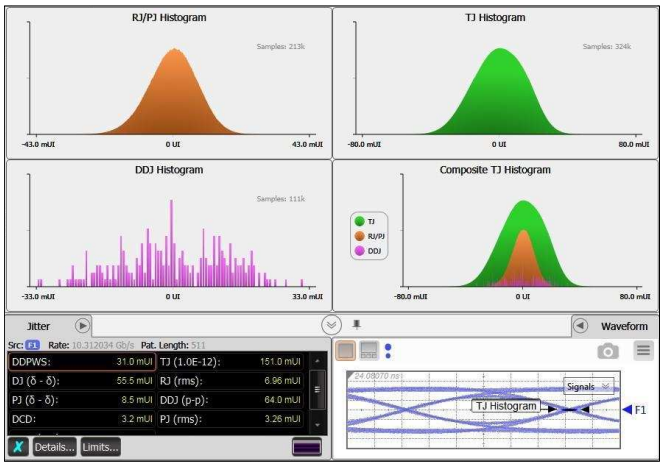
Figure 36. nPPI Jitter Performance with 5 Inch 4-Mil FR4 Input Trace, Test Pattern = PRBS-9, 10.3125 Gbps

Typical Applications (continued)



DS125BR820 Settings: EQA = Level 3, VODA = Level 6

Figure 37. nPPI Eye Mask Performance with 15 Inch 5-Mil FR4 Input Trace, Test Pattern = PRBS-9, 10.3125 Gbps



DS125BR820 Settings: EQA = Level 3, VODA = Level 6

Figure 38. nPPI Jitter Performance with 15 Inch 5-Mil FR4 Input Trace, Test Pattern = PRBS-9, 10.3125 Gbps

8.2.3 PCIe Board Applications (PCIe Gen-3)

The DS125BR820 can be used to extend trace length on motherboards and line cards in PCIe Gen-3 applications. The high linearity of the DS125BR820 aids in the link training protocol required by PCIe Gen-3 at 8 Gbps in accordance with PCI-SIG standards. For PCIe Gen-3, preservation of the pre-cursor and post-cursor Tx FIR presets (P1-P10) is crucial to successful signal transmission from motherboard system root complex to line card ASIC or Embedded Processor. Below is a typical example of the DS125BR820 used in a PCIe application:

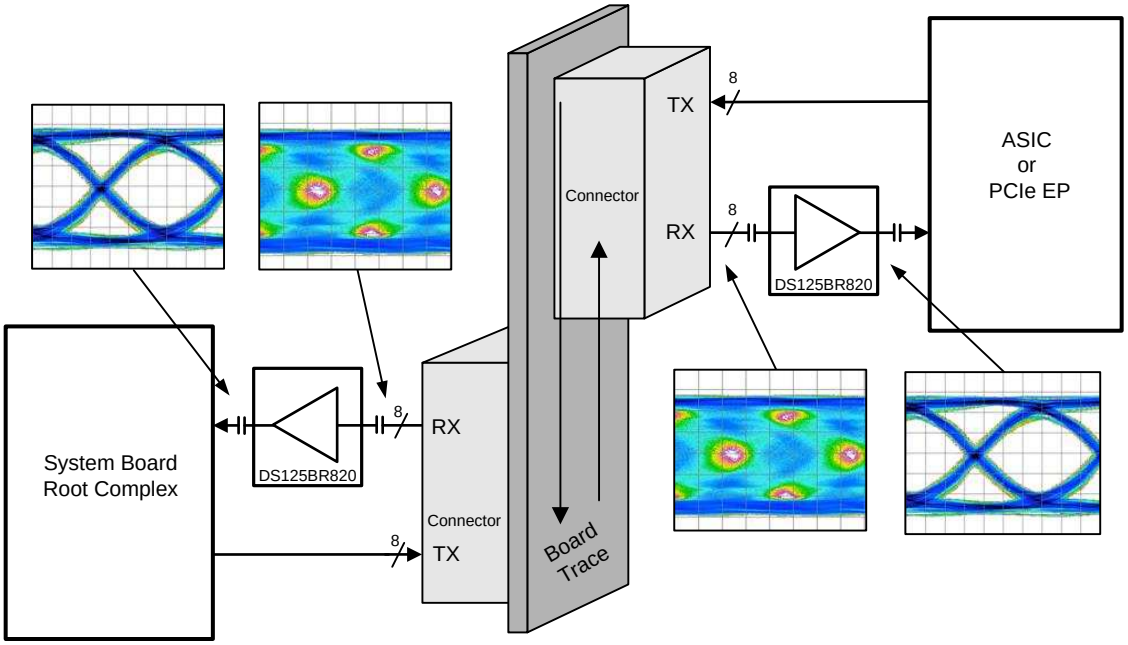


Figure 39. Typical PCIe Gen-3 Configuration Diagram

8.2.3.1 Design Requirements

As with any high speed design, there are many factors that influence the overall performance. Please reference Design Requirements in the Generic High Speed Repeater application section for a list of critical areas for consideration and study during design.

Typical Applications (continued)

8.2.3.2 Design Procedure

In PCIe Gen-3 applications, there is a large range of flexibility regarding the placement of the DS125BR820 in the signal path due to the high linearity of the device. If the PCIe slot must also support lower speeds like PCIe Gen-1 (2.5 Gbps) and Gen-2 (5.0 Gbps), it is recommended to place the DS125BR820 closer to the endpoint Rx. Once the DS125BR820 is placed on the signal path, the repeater must be tuned. To tune the repeater, the settings mentioned in Table 11 (for Pin Mode) and Table 12 (for SMBus Modes) are recommended as a default starting point for most applications. Once these settings are configured, additional tuning of the EQ and, to a lesser extent, VOD may be required to optimize the repeater performance to pass link training preset requirements for PCIe Gen-3.

An example of a test configuration used to evaluate the DS125BR820 in this application can be seen in Figure 40. For more information about DS125BR820 PCIe applications, please refer to application note SNLA227:

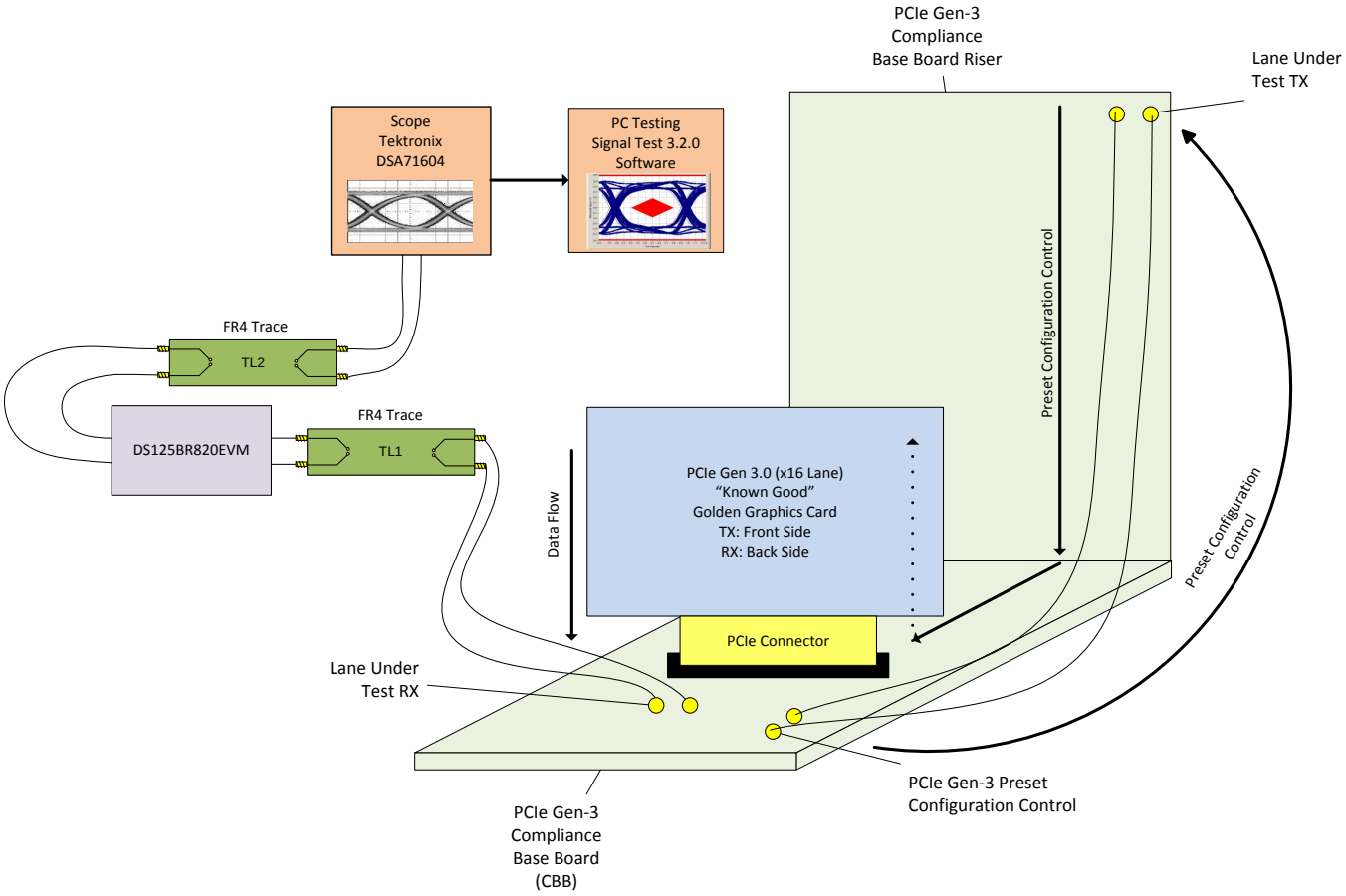
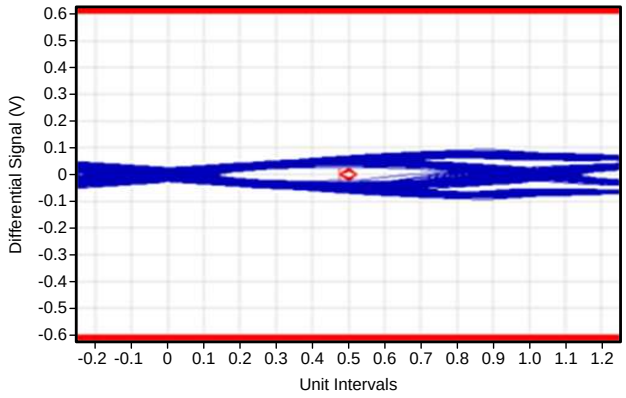


Figure 40. Typical PCIe Gen-3 Add-In Card Test Diagram

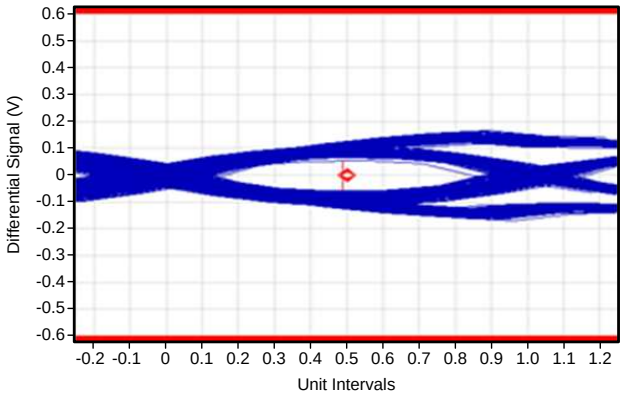
Typical Applications (continued)

8.2.3.3 Application Performance Plots



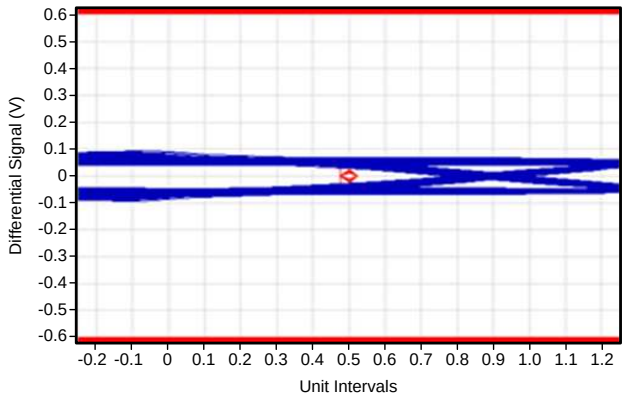
No Repeater Used
Composite Eye Height: 50.39 mV
Minimum Eye Width: 49.87 ps
Overall SigTest Result: Fail

Figure 41. PCIe Gen-3, Preset 7, Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace, No TL2
No Repeater, 8 Gbps



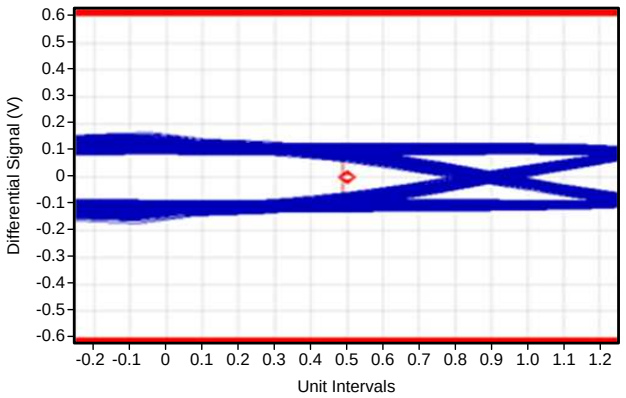
DS125BR820 Settings: EQA = Level 4, VODA = Level 6
Composite Eye Height: 112.2 mV
Minimum Eye Width: 83.82 ps
Overall SigTest Result: Pass

Figure 42. PCIe Gen-3, Preset 7, Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace, No TL2
DS125BR820, 8 Gbps



No Repeater Used
Composite Eye Height: 50.39 mV
Minimum Eye Width: 49.87 ps
Overall SigTest Result: Fail

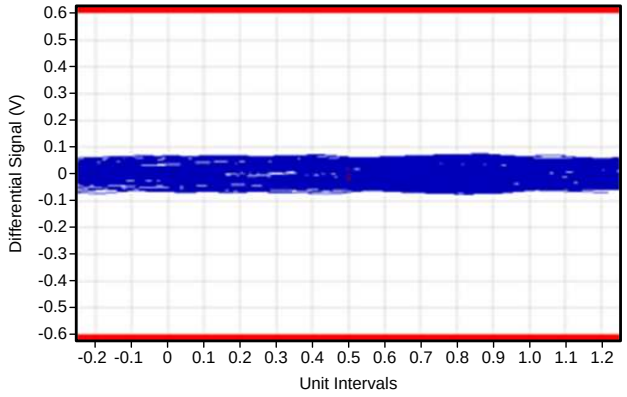
Figure 43. PCIe Gen-3, Preset 7, Non-Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace, No TL2
No Repeater, 8 Gbps



DS125BR820 Settings: EQA = Level 4, VODA = Level 6
Composite Eye Height: 112.2 mV
Minimum Eye Width: 83.82 ps
Overall SigTest Result: Pass

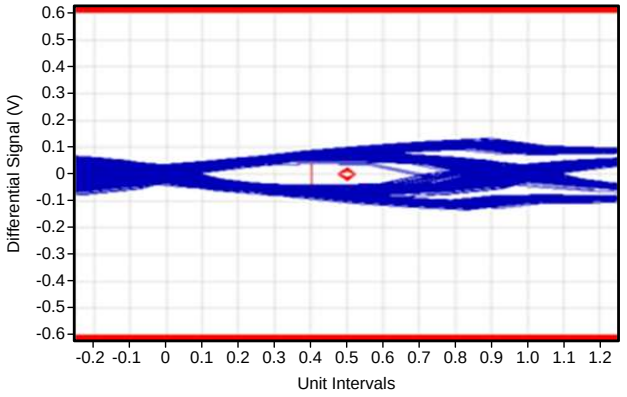
Figure 44. PCIe Gen-3, Preset 7, Non-Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace, No TL2
DS125BR820, 8 Gbps

Typical Applications (continued)



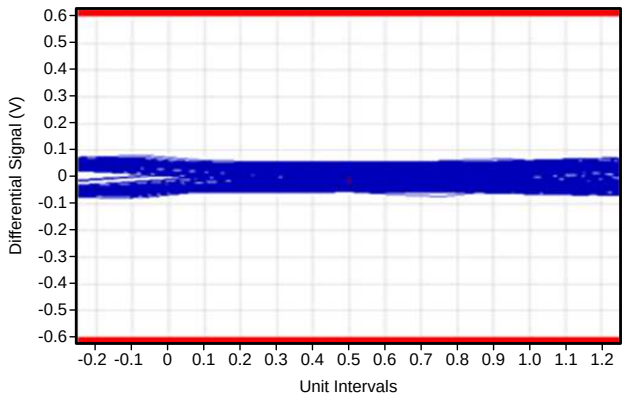
No Repeater Used
Composite Eye Height: 0.057 mV
Minimum Eye Width: 37.66 ps
Overall SigTest Result: Fail

Figure 45. PCIe Gen-3, Preset 7, Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace,
TL2 = 5 Inch 4-Mil FR4 Trace
No Repeater, 8 Gbps



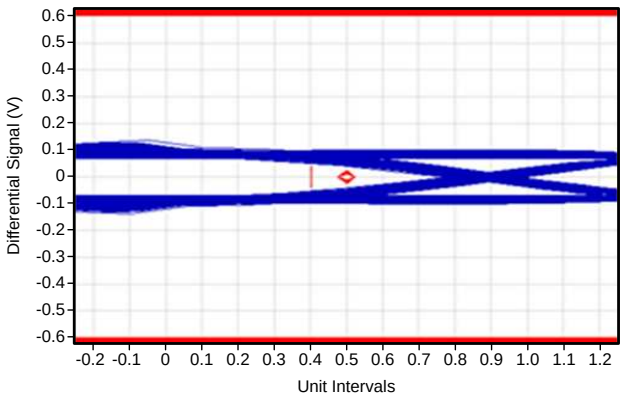
DS125BR820 Settings: EQA = Level 4, VODA = Level 6
Composite Eye Height: 77.26 mV
Minimum Eye Width: 78.24 ps
Overall SigTest Result: Pass

Figure 46. PCIe Gen-3, Preset 7, Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace,
TL2 = 5 Inch 4-Mil FR4 Trace
DS125BR820, 8 Gbps



No Repeater Used
Composite Eye Height: 0.057 mV
Minimum Eye Width: 37.66 ps
Overall SigTest Result: Fail

Figure 47. PCIe Gen-3, Preset 7, Non-Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace,
TL2 = 5 Inch 4-Mil FR4 Trace
No Repeater, 8 Gbps



DS125BR820 Settings: EQA = Level 4, VODA = Level 6
Composite Eye Height: 77.26 mV
Minimum Eye Width: 78.24 ps
Overall SigTest Result: Pass

Figure 48. PCIe Gen-3, Preset 7, Non-Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace,
TL2 = 5 Inch 4-Mil FR4 Trace
DS125BR820, 8 Gbps

9 Power Supply Recommendations

Two approaches are recommended to ensure that the DS125BR820 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to the DS125BR820. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of 1 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

The DS125BR820 has an optional internal voltage regulator to provide the 2.5 V supply to the device. In 3.3 V mode operation, the VIN pin = 3.3 V is used to supply power to the device. The internal regulator then provides the 2.5 V to the VDD pins of the device and a 0.1 µF cap is needed at each of the five VDD pins for power supply de-coupling (total capacitance should equal 0.5 µF). The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5 V mode operation, the VIN pin should be left open and 2.5 V supply must be applied to the five VDD pins to power the device. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

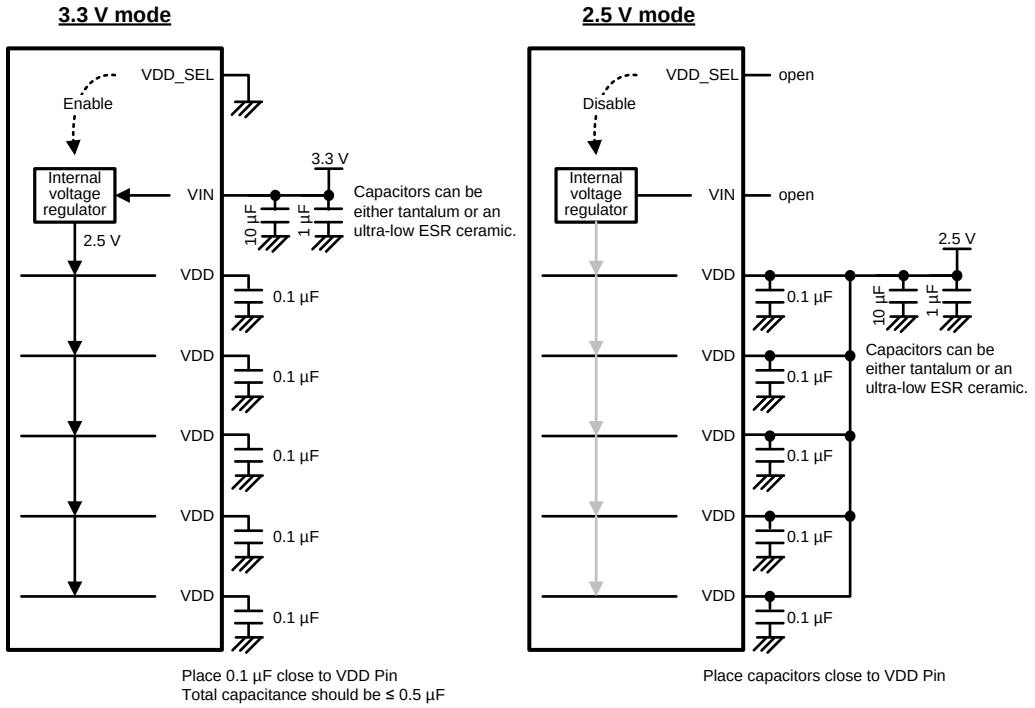


Figure 49. 3.3 V or 2.5 V Supply Connection Diagram

10 Layout

10.1 Layout Guidelines

The CML inputs and outputs have been optimized to work with interconnects using a controlled differential impedance of 100 Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. To minimize the effects of crosstalk, a 5:1 ratio or greater should be maintained between inter-pair and intra-pair spacing. See AN-1187 *"Leadless Leadframe Package (LLP) Application Report"* (literature number SNOA401) for additional information on QFN (WQFN) packages.

10.2 Layout Example

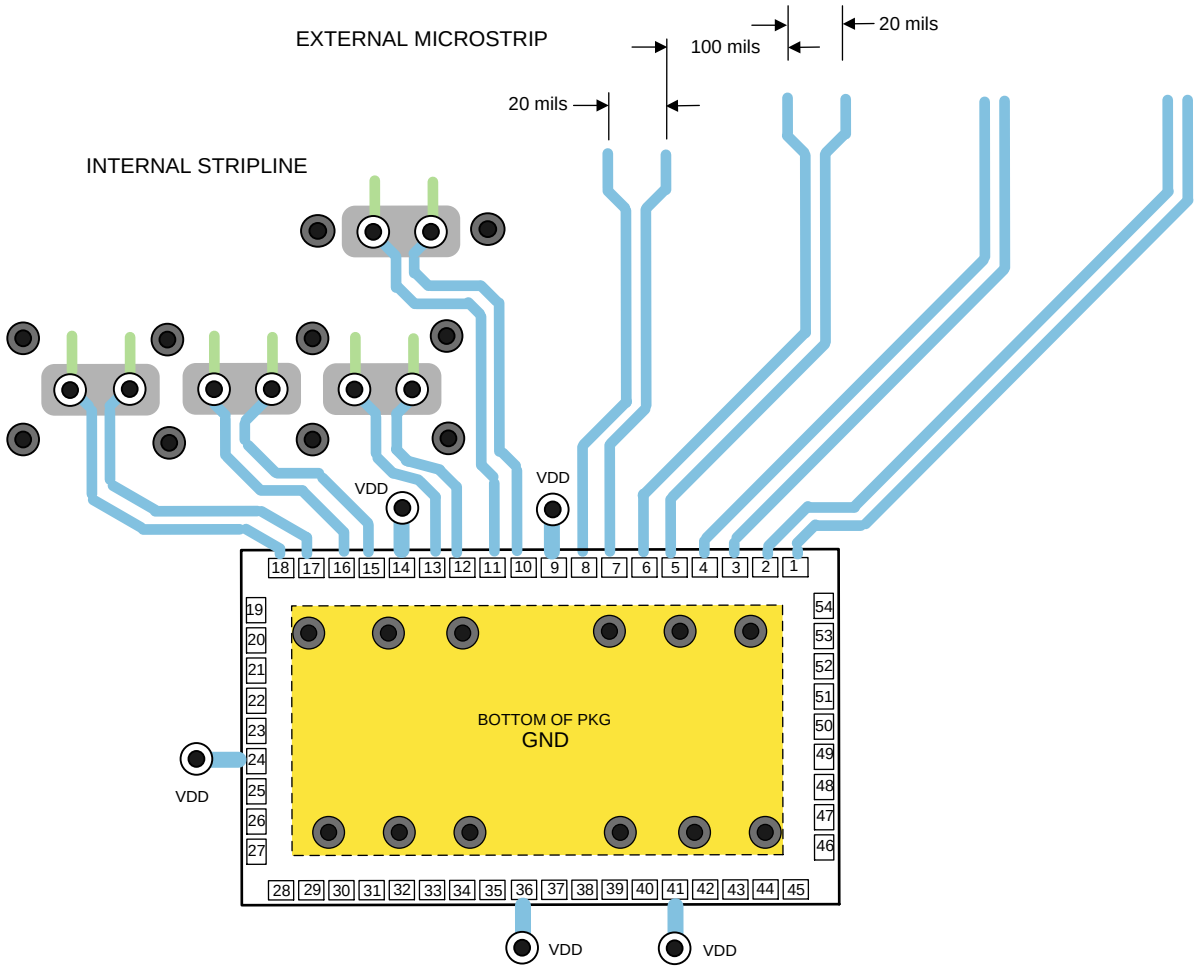


Figure 50. Typical Routing Options

The graphic shown above depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and by providing for a low inductance return current path. When the via structure is associated with a thick backplane PCB, further optimization such as back drilling is often used to reduce the detrimental high frequency effects of stubs on the signal path.

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS125BR820NJYR	ACTIVE	WQFN	NJY	54	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	125B820A0	Samples
DS125BR820NJYT	ACTIVE	WQFN	NJY	54	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	125B820A0	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

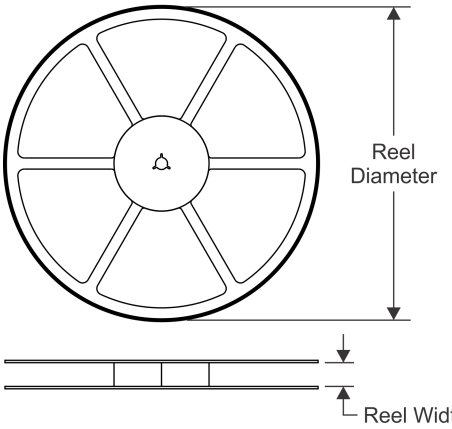
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

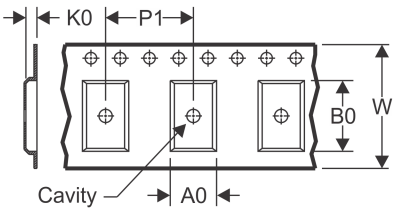
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

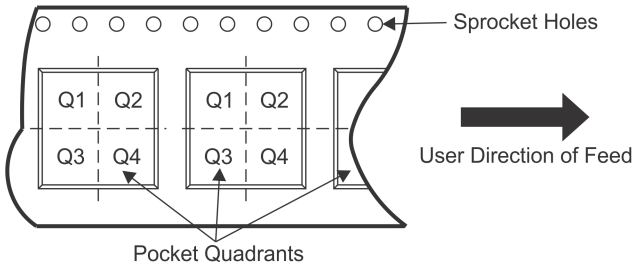


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

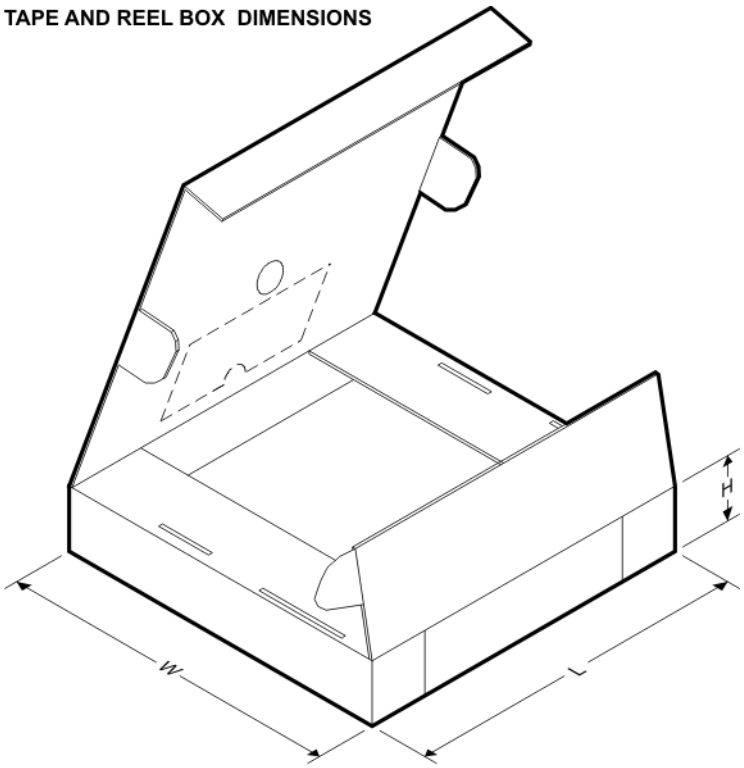
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

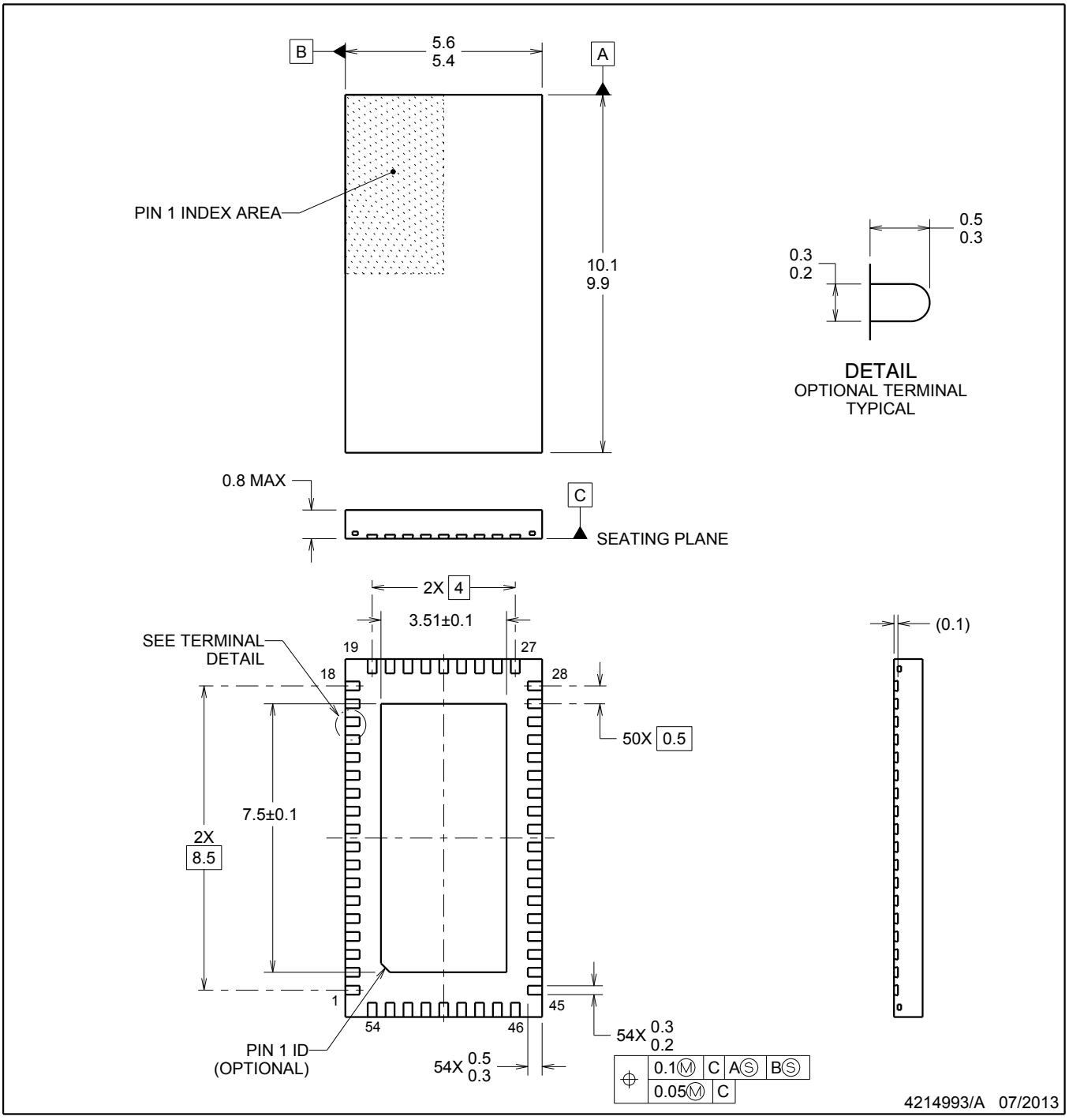
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS125BR820NJYR	WQFN	NJY	54	2000	330.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1
DS125BR820NJYT	WQFN	NJY	54	250	178.0	16.4	5.8	10.3	1.0	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



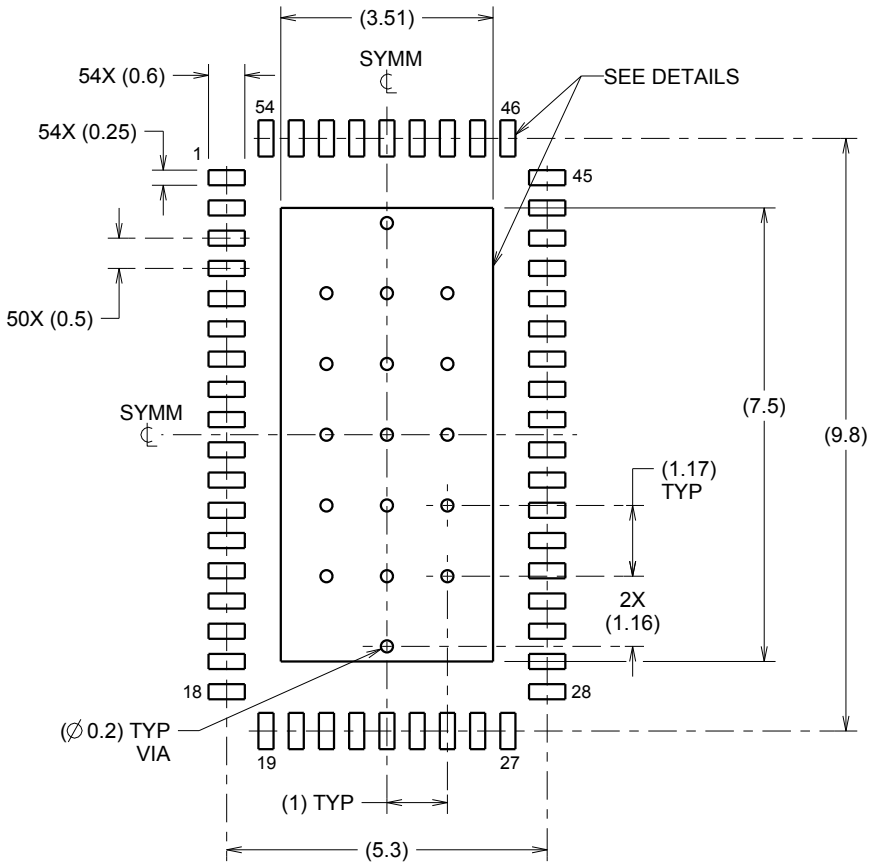
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS125BR820NJYR	WQFN	NJY	54	2000	367.0	367.0	38.0
DS125BR820NJYT	WQFN	NJY	54	250	210.0	185.0	35.0

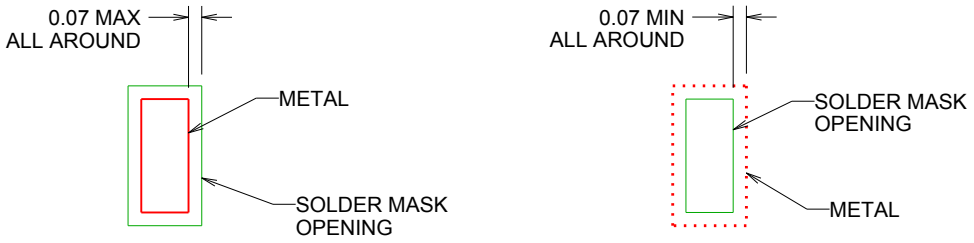


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED
(PREFERRED)

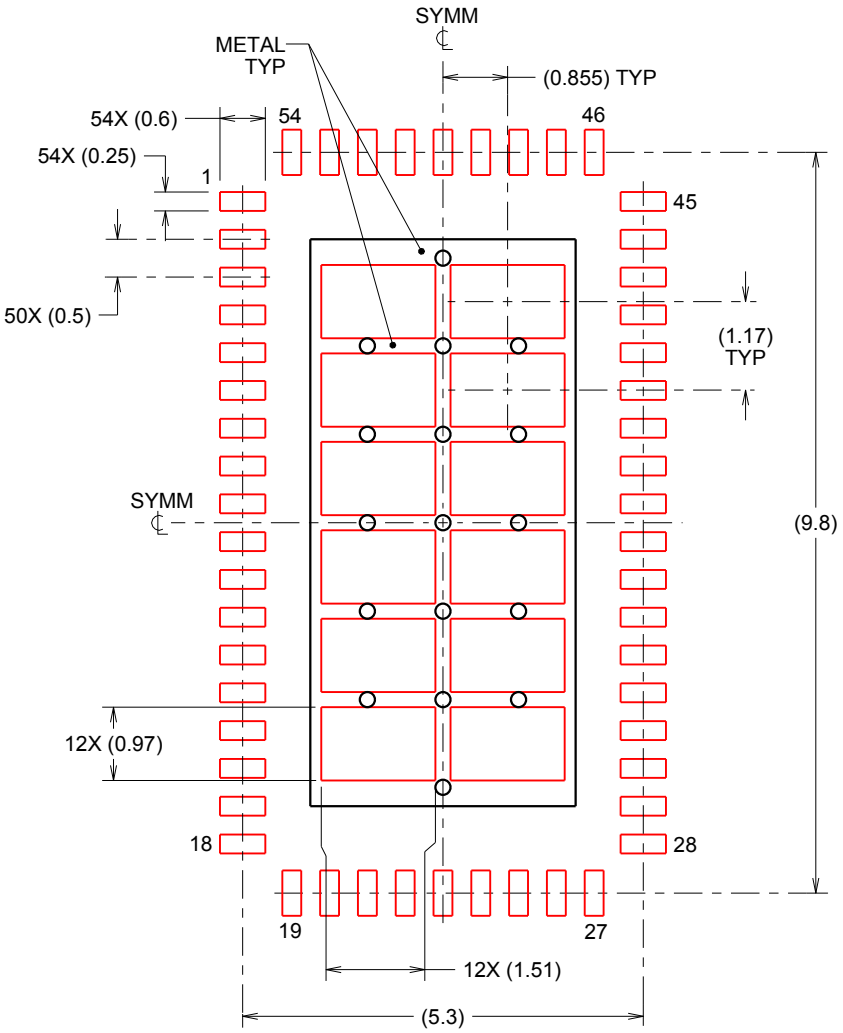
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214993/A 07/2013

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
67% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4214993/A 07/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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