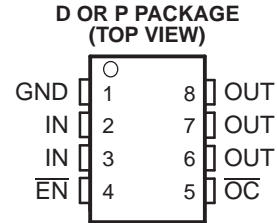


POWER-DISTRIBUTION SWITCHES

FEATURES

- 33-mΩ (5-V Input) High-Side MOSFET Switch
- Short-Circuit and Thermal Protection
- Overcurrent Logic Output
- Operating Range . . . 2.7 V to 5.5 V
- Logic-Level Enable Input
- Typical Rise Time . . . 6.1 ms
- Undervoltage Lockout
- Maximum Standby Supply Current . . . 10 μA
- No Drain-Source Back-Gate Diode
- Available in 8-Pin SOIC and PDIP Packages
- Ambient Temperature Range, -40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection

- UL Listed - File No. E169910



DESCRIPTION

The TPS202x family of power distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices are 50-mΩ N-channel MOSFET high-side power switches. The switch is controlled by a logic enable compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS202x limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (\overline{OC}) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

The TPS202x devices differ only in short-circuit current threshold. The TPS2020 limits at 0.3-A load, the TPS2021 at 0.9-A load, the TPS2022 at 1.5-A load, the TPS2023 at 2.2-A load, and the TPS2024 at 3-A load (see [Available Options](#)). The TPS202x is available in an 8-pin small-outline integrated-circuit (SOIC) package and in an 8-pin dual in-line package (DIP) and operates over a junction temperature range of -40°C to 125°C.

| GENERAL SWITCH CATALOG | | | | | | |
|---|---|---|--|--|---|--|
| 33 mΩ, Single | 80 mΩ, Single | 80 mΩ, Dual | 80 mΩ, Dual | 80 mΩ, Triple | 80 mΩ, Quad | 80 mΩ, Quad |
| | | | | | | |
| TPS201xA 0.2 A to 2 A TPS202x 0.2 A to 2 A TPS203x 0.2 A to 2 A | TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A | TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A | TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA | TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A | TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA | TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA |



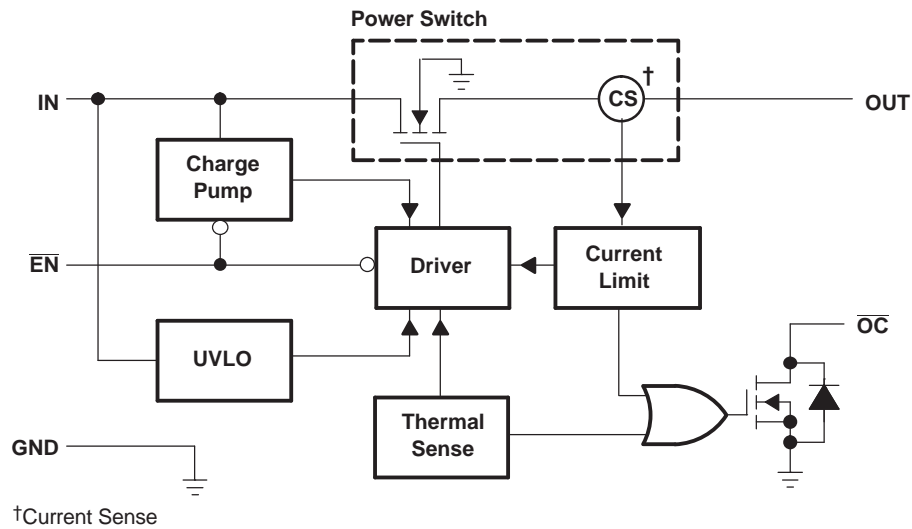
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 1. AVAILABLE OPTIONS

| T _A | ENABLE | RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A) | TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A) | PACKAGED DEVICES | |
|----------------|------------|---|---|----------------------------------|-----------------|
| | | | | SMALL OUTLINE (D) ⁽¹⁾ | PLASTIC DIP (P) |
| –40°C to 85°C | Active low | 0.2 | 0.3 | TPS2020D | TPS2020P |
| | | 0.6 | 0.9 | TPS2021D | TPS2021P |
| | | 1 | 1.5 | TPS2022D | TPS2022P |
| | | 1.5 | 2.2 | TPS2023D | TPS2023P |
| | | 2 | 3 | TPS2024D | TPS2024P |

(1) The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2020DR)

TPS2020 FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|------------------------|------------|-----|--|
| NAME | NO. D OR P | | |
| $\overline{\text{EN}}$ | 4 | I | Enable input. Logic-low turns on power switch. |
| GND | 1 | I | Ground |
| IN | 2, 3 | I | Input voltage |
| $\overline{\text{OC}}$ | 5 | O | Overcurrent. Logic output, active-low |
| OUT | 6, 7, 8 | O | Power-switch output |

DETAILED DESCRIPTION

POWER SWITCH

The power switch is an N-channel MOSFET with a maximum on-state resistance of 50 m Ω ($V_{I(IN)} = 5$ V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled.

CHARGE PUMP

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

DRIVER

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 9-ms range.

ENABLE (\overline{EN})

The logic enable disables the power switch, the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μ A when a logic-high is present on \overline{EN} . A logic-zero input on \overline{EN} restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

OVERCURRENT (\overline{OC})

The \overline{OC} open drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed.

CURRENT SENSE

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver, in turn, reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

THERMAL SENSE

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

UNDERVOLTAGE LOCKOUT

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | |
|-----------------------------|--|-------------------------------|
| $V_{I(IN)}$ ⁽²⁾ | Input voltage range | –0.3 V to 6 V |
| $V_{O(OUT)}$ ⁽²⁾ | Output voltage range | –0.3 V to $V_{I(IN)} + 0.3$ V |
| $V_{I(EN)}$ | Input voltage range | –0.3 V to 6 V |
| $I_{O(OUT)}$ | Continuous output current | Internally limited |
| | Continuous total power dissipation | See Dissipation Rating Table |
| T_J | Operating virtual junction temperature range | –40°C to 125°C |
| T_{stg} | Storage temperature range | –65°C to 150°C |
| | Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| | Electrostatic discharge (ESD) protection: | |
| | Human body model | 2 kV |
| | Machine model | 200 V |
| | Charged device model (CDM) | 750 V |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---|---|--|--|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW |
| P | 1175 mW | 9.4 mW/°C | 752 mW | 611 mW |

RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT | |
|-------------|--|---------|-----|------|---|
| $V_{I(IN)}$ | Input voltage | 2.7 | 5.5 | V | |
| $V_{I(EN)}$ | | 0 | 5.5 | V | |
| I_O | Continuous output current | TPS2020 | 0 | 0.2 | A |
| | | TPS2021 | 0 | 0.6 | |
| | | TPS2022 | 0 | 1 | |
| | | TPS2023 | 0 | 1.5 | |
| | | TPS2024 | 0 | 2 | |
| T_J | Operating virtual junction temperature | –40 | 125 | °C | |

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)} = 5.5\text{ V}$, $I_O = \text{rated current}$, $\overline{EN} = 0\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP | MAX | UNIT |
|--|---|---|---|------|-----|-----|------|
| POWER SWITCH | | | | | | | |
| $r_{DS(on)}$ | Static drain-source on-state resistance | $V_{I(IN)} = 5\text{ V}$, $T_J = 25^\circ\text{C}$, $I_O = 1.8\text{ A}$ | | 33 | 36 | | mΩ |
| | | $V_{I(IN)} = 5\text{ V}$, $T_J = 85^\circ\text{C}$, $I_O = 1.8\text{ A}$ | | 38 | 46 | | |
| | | $V_{I(IN)} = 5\text{ V}$, $T_J = 125^\circ\text{C}$, $I_O = 1.8\text{ A}$ | | 44 | 50 | | |
| | | $V_{I(IN)} = 3.3\text{ V}$, $T_J = 25^\circ\text{C}$, $I_O = 1.8\text{ A}$ | | 37 | 41 | | |
| | | $V_{I(IN)} = 3.3\text{ V}$, $T_J = 85^\circ\text{C}$, $I_O = 1.8\text{ A}$ | | 43 | 52 | | |
| | | $V_{I(IN)} = 3.3\text{ V}$, $T_J = 125^\circ\text{C}$, $I_O = 1.8\text{ A}$ | | 51 | 61 | | |
| | | $V_{I(IN)} = 5\text{ V}$, $T_J = 25^\circ\text{C}$, $I_O = 0.18\text{ A}$ | | 30 | 34 | | |
| | | $V_{I(IN)} = 5\text{ V}$, $T_J = 85^\circ\text{C}$, $I_O = 0.18\text{ A}$ | | 35 | 41 | | |
| | | $V_{I(IN)} = 5\text{ V}$, $T_J = 125^\circ\text{C}$, $I_O = 0.18\text{ A}$ | | 39 | 47 | | |
| | | $V_{I(IN)} = 3.3\text{ V}$, $T_J = 25^\circ\text{C}$, $I_O = 0.18\text{ A}$ | | 33 | 37 | | |
| | | $V_{I(IN)} = 3.3\text{ V}$, $T_J = 85^\circ\text{C}$, $I_O = 0.18\text{ A}$ | | 39 | 46 | | |
| | | $V_{I(IN)} = 3.3\text{ V}$, $T_J = 125^\circ\text{C}$, $I_O = 0.18\text{ A}$ | | 44 | 56 | | |
| t_r | Rise time, output | $V_{I(IN)} = 5.5\text{ V}$, $C_L = 1\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$, $R_L = 10\text{ }\Omega$ | | 6.1 | | | ms |
| | | $V_{I(IN)} = 2.7\text{ V}$, $C_L = 1\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$, $R_L = 10\text{ }\Omega$ | | 8.6 | | | |
| t_f | Fall time, output | $V_{I(IN)} = 5.5\text{ V}$, $C_L = 1\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$, $R_L = 10\text{ }\Omega$ | | 3.4 | | | ms |
| | | $V_{I(IN)} = 2.7\text{ V}$, $C_L = 1\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$, $R_L = 10\text{ }\Omega$ | | 3 | | | |
| ENABLE INPUT (\overline{EN}) | | | | | | | |
| V_{IH} | High-level input voltage | $2.7\text{ V} \leq V_{I(IN)} \leq 5.5\text{ V}$ | | 2 | | | V |
| V_{IL} | Low-level input voltage | $4.5\text{ V} \leq V_{I(IN)} \leq 5.5\text{ V}$ | | | | 0.8 | V |
| | | $2.7\text{ V} \leq V_{I(IN)} \leq 4.5\text{ V}$ | | | | 0.5 | |
| I_I | Input current | $\overline{EN} = 0\text{ V}$ or $\overline{EN} = V_{I(IN)}$ | | -0.5 | | 0.5 | μA |
| t_{on} | Turnon time | $C_L = 100\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | | | | 20 | ms |
| t_{off} | Turnoff time | $C_L = 100\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$ | | | | 40 | |
| CURRENT LIMIT | | | | | | | |
| I_{OS} | Short-circuit output current | $T_J = 25^\circ\text{C}$, $V_I = 5.5\text{ V}$, OUT connected to GND, Device enabled into short circuit | TPS2020 | 0.22 | 0.3 | 0.4 | A |
| | | | TPS2021 | 0.66 | 0.9 | 1.1 | |
| | | | TPS2022 | 1.1 | 1.5 | 1.8 | |
| | | | TPS2023 | 1.65 | 2.2 | 2.7 | |
| | | | TPS2024 | 2.2 | 3 | 3.8 | |
| SUPPLY CURRENT | | | | | | | |
| Supply current, low-level output | No load on OUT | $\overline{EN} = V_{I(IN)}$ | $T_J = 25^\circ\text{C}$ | 0.3 | 1 | μA | |
| | | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | | 10 | | |
| Supply current, high-level output | No load on OUT | $\overline{EN} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | 58 | 75 | μA | |
| | | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 75 | 100 | | |
| Leakage current | OUT connected to ground | $\overline{EN} = V_{I(IN)}$ | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 10 | | μA | |
| UNDERVOLTAGE LOCKOUT | | | | | | | |
| Low-level input voltage | | | | 2 | | 2.5 | V |
| Hysteresis | | $T_J = 25^\circ\text{C}$ | | | 100 | | mV |
| OVERCURRENT (\overline{OC}) | | | | | | | |
| Output low voltage | | $I_O = 10\text{ mA}$, $V_{OL(OC)}$ | | | | 0.4 | V |
| Off-state current ⁽²⁾ | | $V_O = 5\text{ V}$, $V_O = 3.3\text{ V}$ | | | | 1 | μA |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

(2) Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

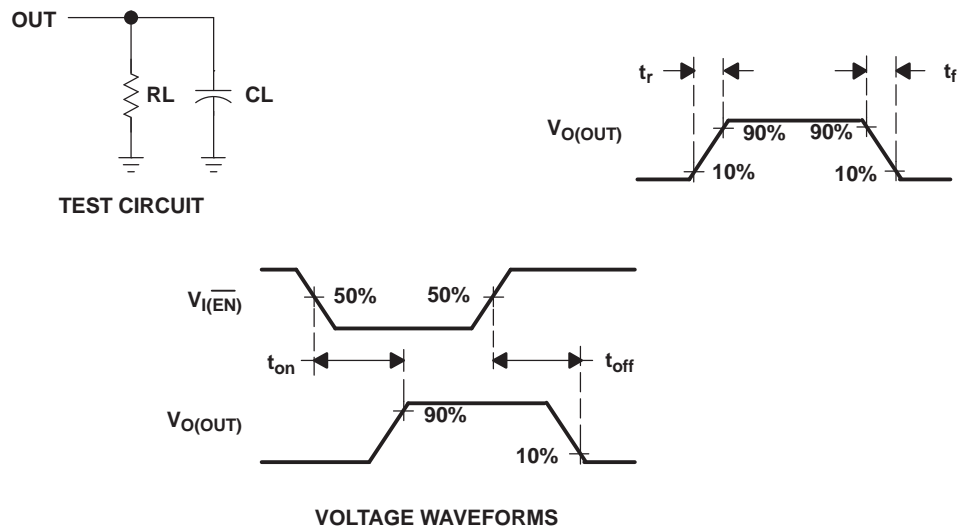


Figure 1. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

TABLE OF TIMING DIAGRAMS

| | FIGURE |
|--|-----------------|
| Turnon Delay and Rise Time | 2 |
| Turnoff Delay and Fall Time | 3 |
| Turnon Delay and Rise Time with 1- μ F Load | 4 |
| Turnoff Delay and Rise Time with 1- μ F Load | 5 |
| Device Enabled into Short | 6 |
| TPS2020, TPS2021, TPS2022, TPS2023, and TPS2024, Ramped Load on Enabled Device | 7, 8, 9, 10, 11 |
| TPS2024, Inrush Current | 12 |
| 7.9- Ω Load Connected to an Enabled TPS2020 Device | 13 |
| 3.7- Ω Load Connected to an Enabled TPS2020 Device | 14 |
| 3.7- Ω Load Connected to an Enabled TPS2021 Device | 15 |
| 2.6- Ω Load Connected to an Enabled TPS2021 Device | 16 |
| 2.6- Ω Load Connected to an Enabled TPS2022 Device | 17 |
| 1.2- Ω Load Connected to an Enabled TPS2022 Device | 18 |
| 1.2- Ω Load Connected to an Enabled TPS2023 Device | 19 |
| 0.9- Ω Load Connected to an Enabled TPS2023 Device | 20 |
| 0.9- Ω Load Connected to an Enabled TPS2024 Device | 21 |
| 0.5- Ω Load Connected to an Enabled TPS2024 Device | 22 |

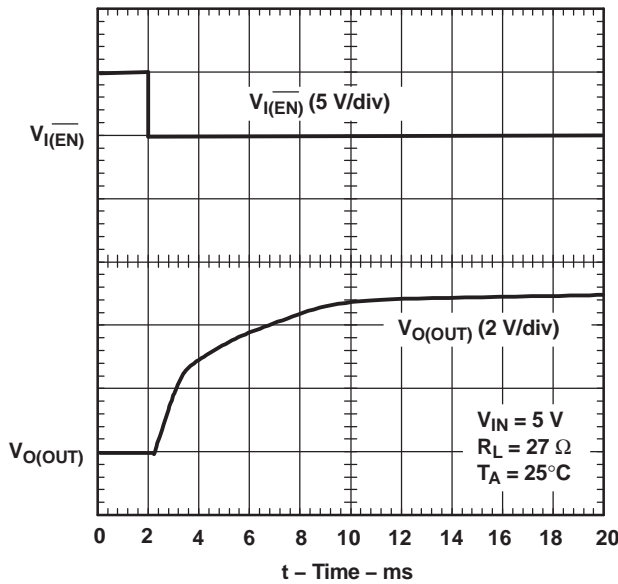


Figure 2. Turnon Delay and Rise Time

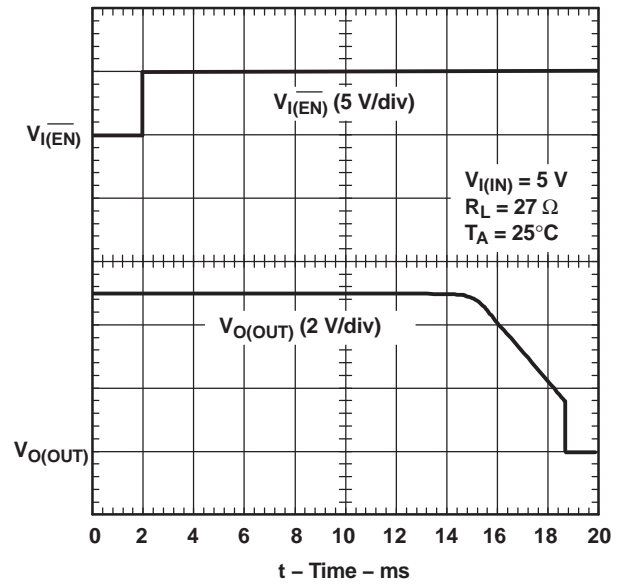


Figure 3. Turnoff Delay and Fall Time

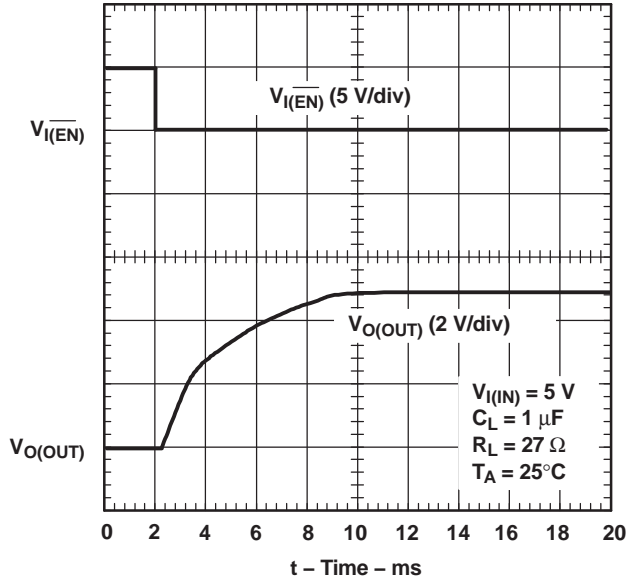


Figure 4. Turnon Delay and Rise Time with 1-µF Load

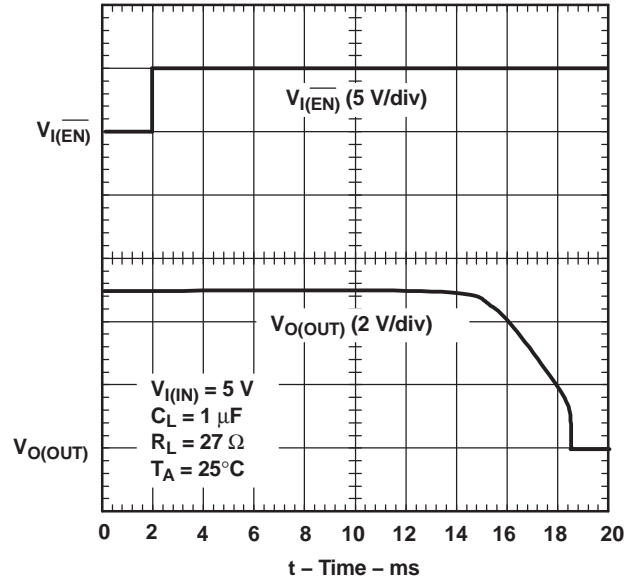


Figure 5. Turnoff Delay and Fall Time with 1-µF Load

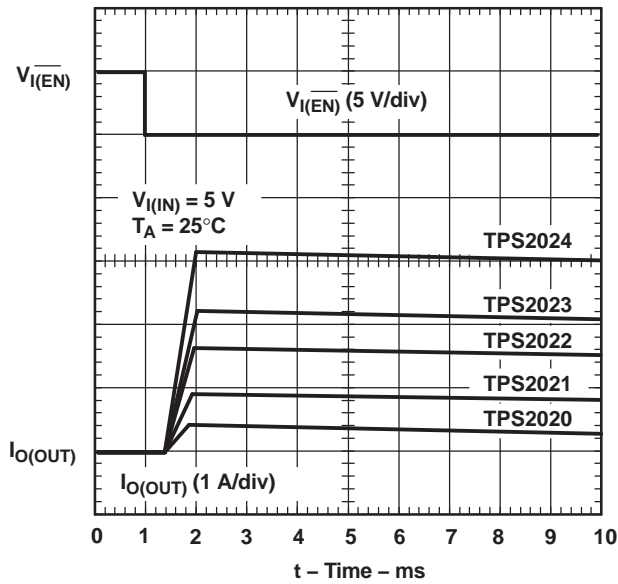


Figure 6. Device Enabled Into Short

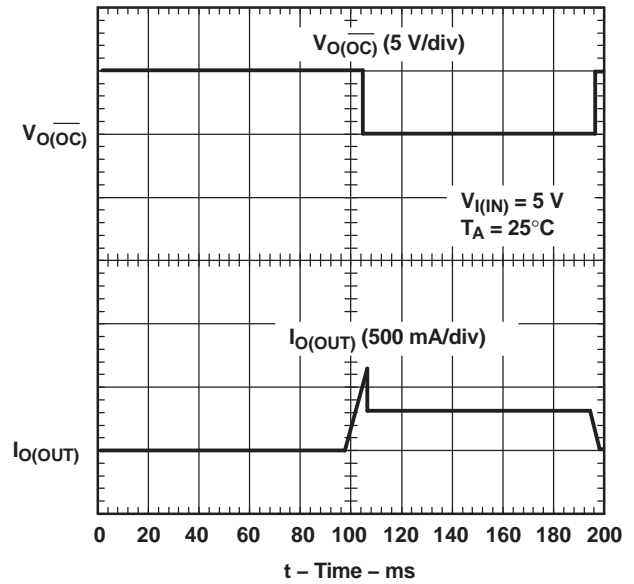


Figure 7. TPS2020, Ramped Load on Enabled Device

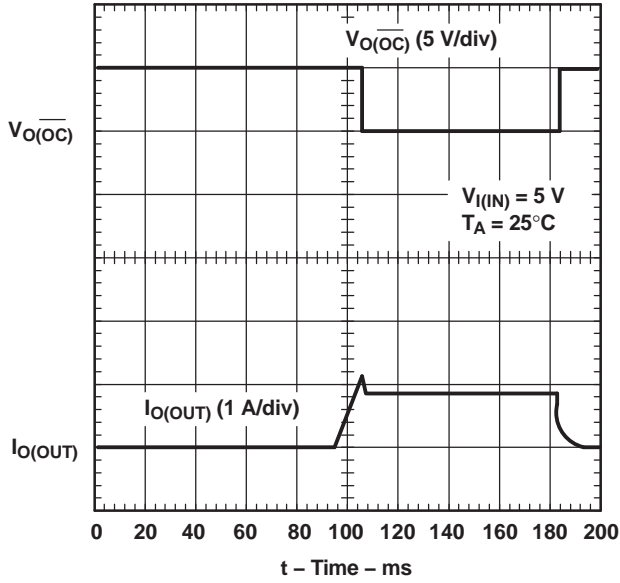


Figure 8. TPS2021, Ramped Load on Enabled Device

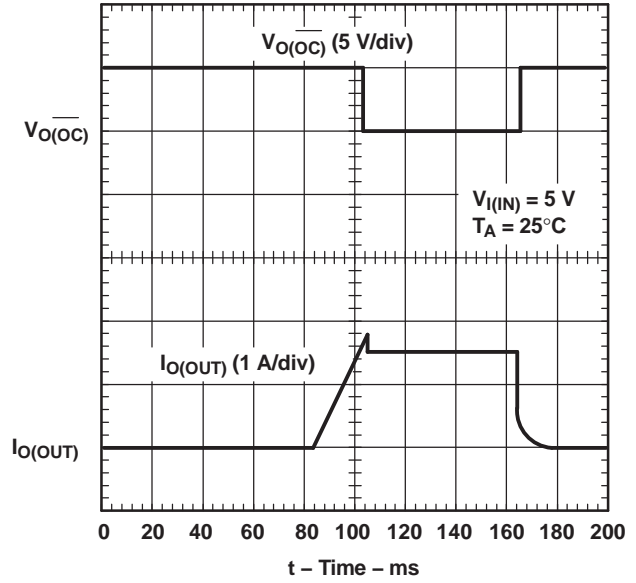


Figure 9. TPS2022, Ramped Load on Enabled Device

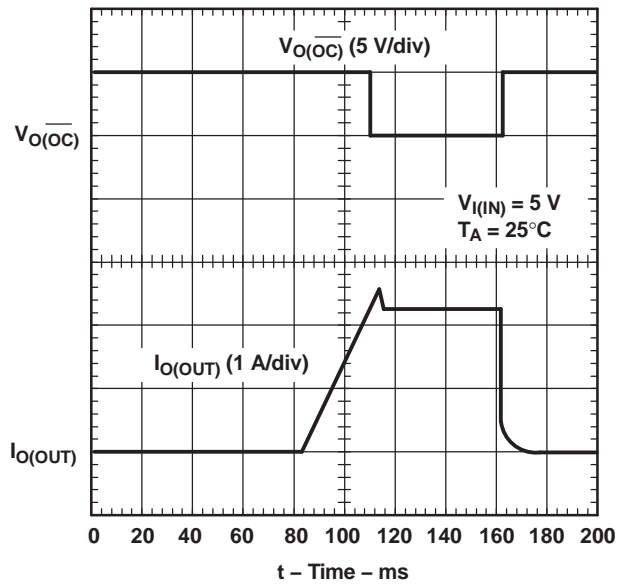


Figure 10. TPS2023, Ramped Load on Enabled Device

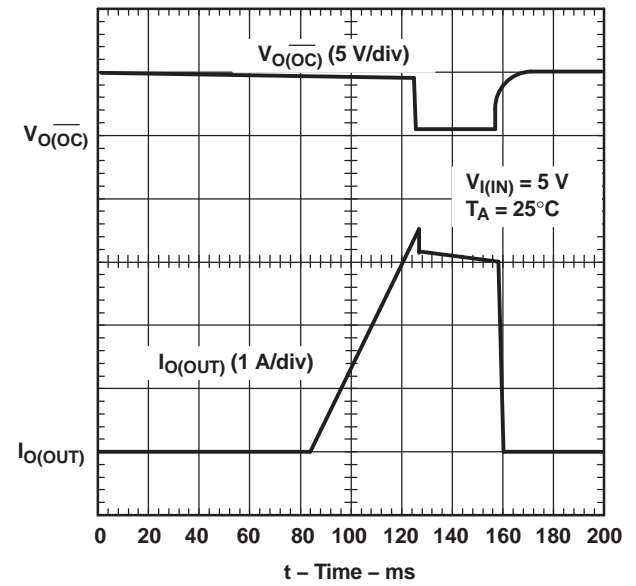


Figure 11. TPS2024, Ramped Load on Enabled Device

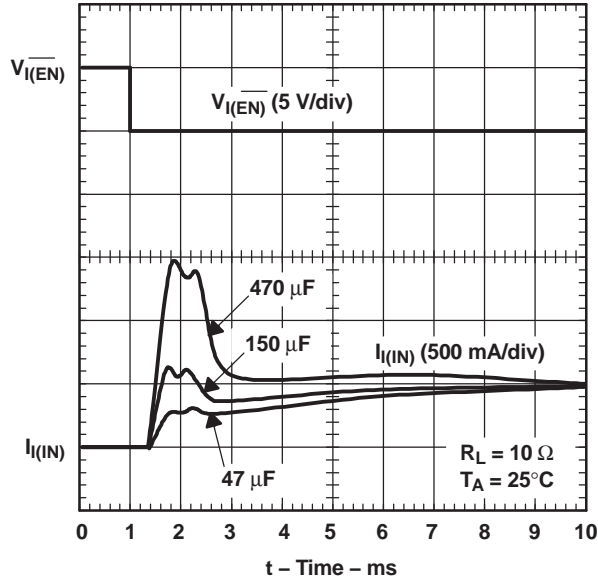


Figure 12. TPS2024, Inrush Current

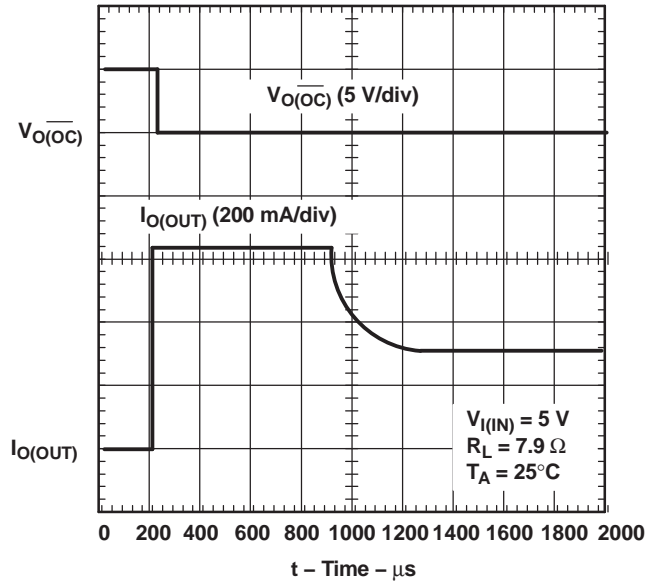


Figure 13. 7.9-Ω Load Connected to an Enabled TPS2020 Device

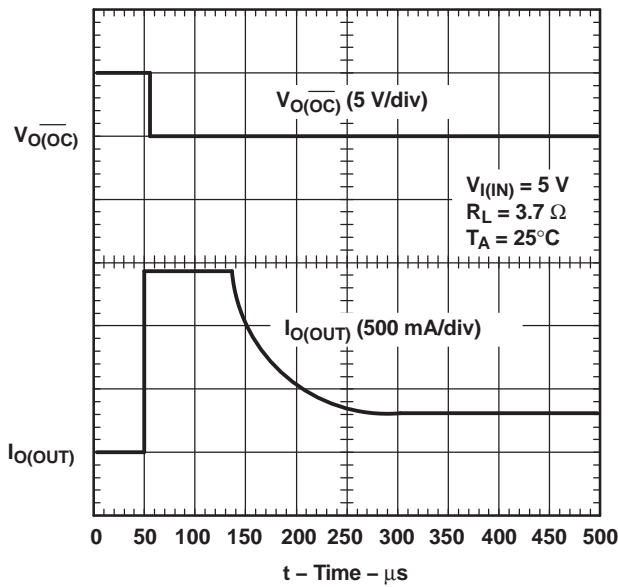


Figure 14. 3.7-Ω Load Connected to an Enabled TPS2020 Device

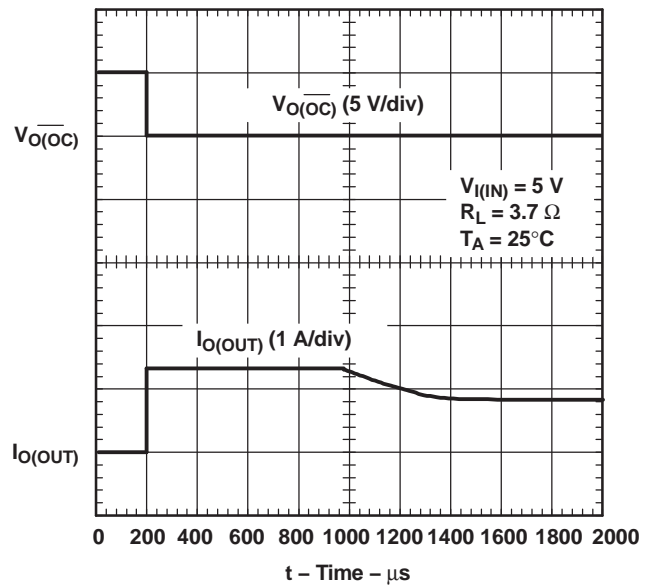


Figure 15. 3.7-Ω Load Connected to an Enabled TPS2021 Device

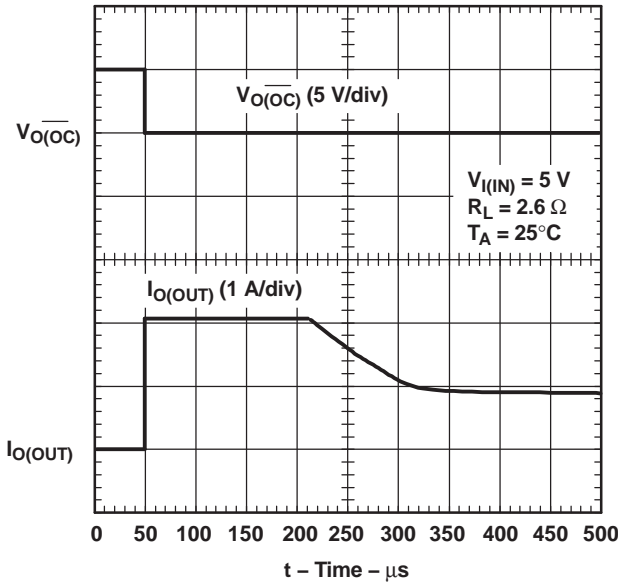


Figure 16. 2.6- Ω Load Connected to an Enabled TPS2021 Device

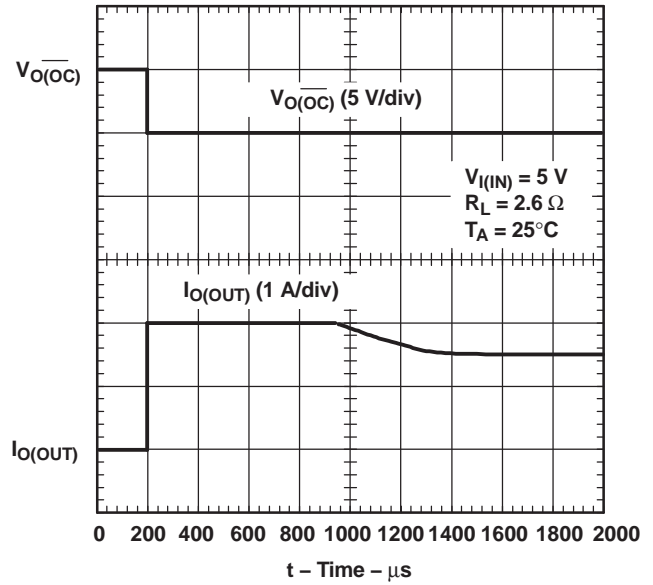


Figure 17. 2.6- Ω Load Connected to an Enabled TPS2022 Device

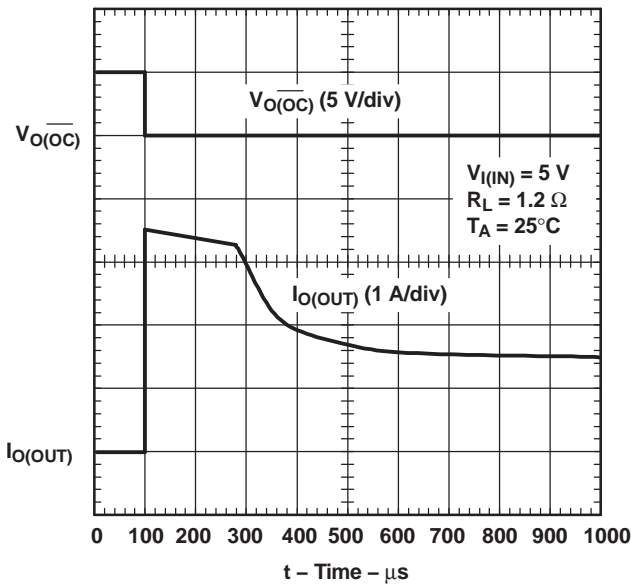


Figure 18. 1.2- Ω Load Connected to an Enabled TPS2022 Device

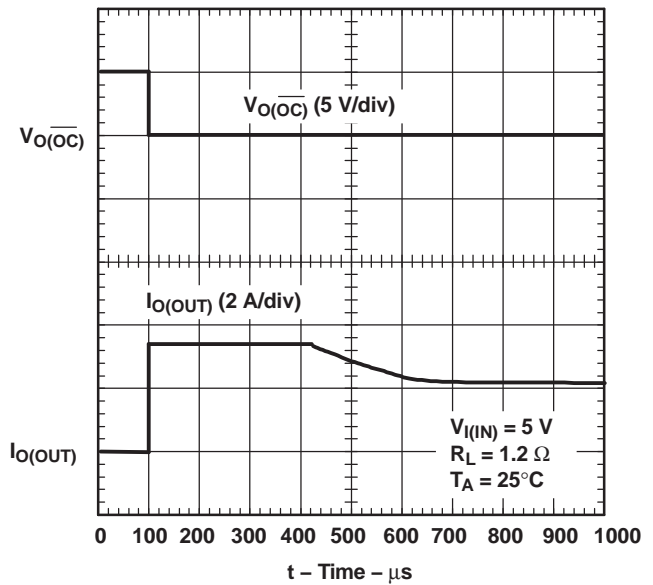


Figure 19. 1.2- Ω Load Connected to an Enabled TPS2023 Device

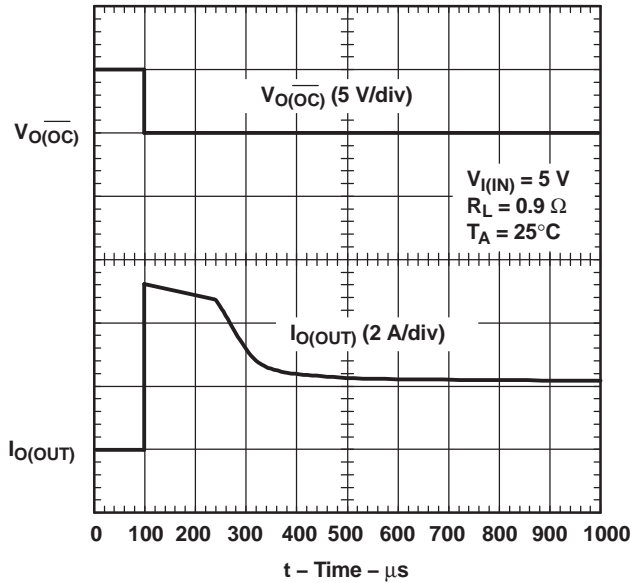


Figure 20. 0.9- Ω Load Connected to an Enabled TPS2023 Device

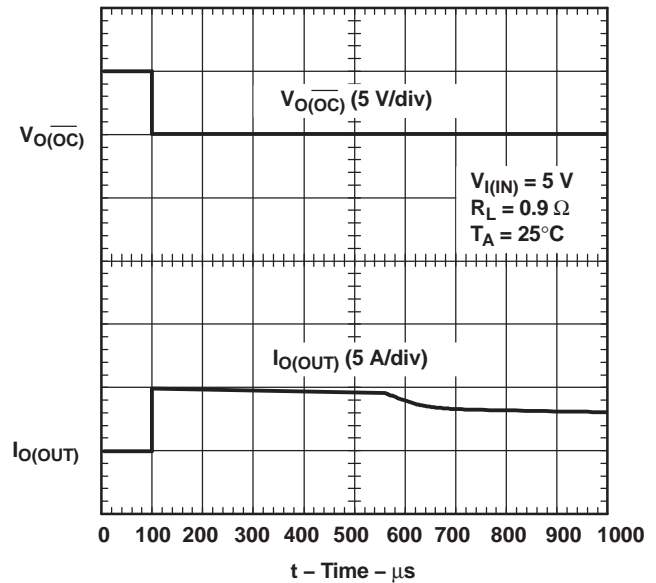


Figure 21. 0.9- Ω Load Connected to an Enabled TPS2024 Device

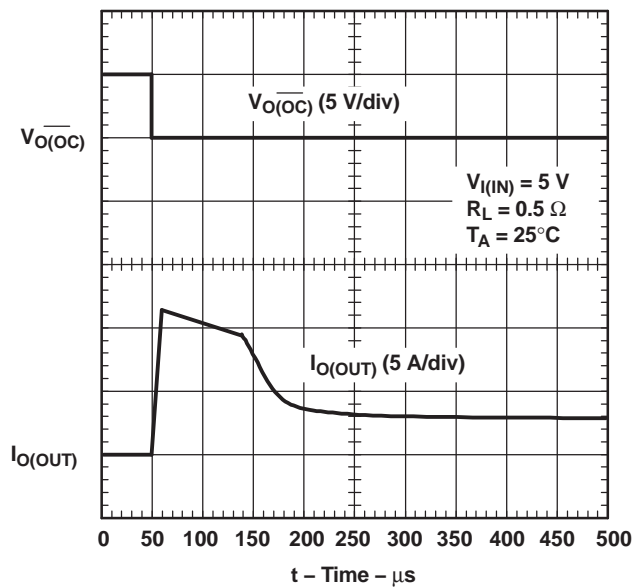


Figure 22. 0.5- Ω Load Connected to an Enabled TPS2024 Device

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

| | | | FIGURE |
|--------------|---|-------------------------|--------|
| $t_{d(on)}$ | Turnon delay time | vs Output voltage | 23 |
| $t_{d(off)}$ | Turnoff delay time | vs Input voltage | 24 |
| t_r | Rise time | vs Load current | 25 |
| t_f | Fall time | vs Load current | 26 |
| | Supply current (enabled) | vs Junction temperature | 27 |
| | Supply current (disabled) | vs Junction temperature | 28 |
| | Supply current (enabled) | vs Input voltage | 29 |
| | Supply current (disabled) | vs Input voltage | 30 |
| I_{OS} | Short-circuit current limit | vs Input voltage | 31 |
| | | vs Junction temperature | 32 |
| $r_{DS(on)}$ | Static drain-source on-state resistance | vs Input voltage | 33 |
| | | vs Junction temperature | 34 |
| | | vs Input voltage | 35 |
| | | vs Junction temperature | 36 |
| V_I | Input voltage | Undervoltage lockout | 37 |

**TURNON DELAY TIME
vs
OUTPUT VOLTAGE**

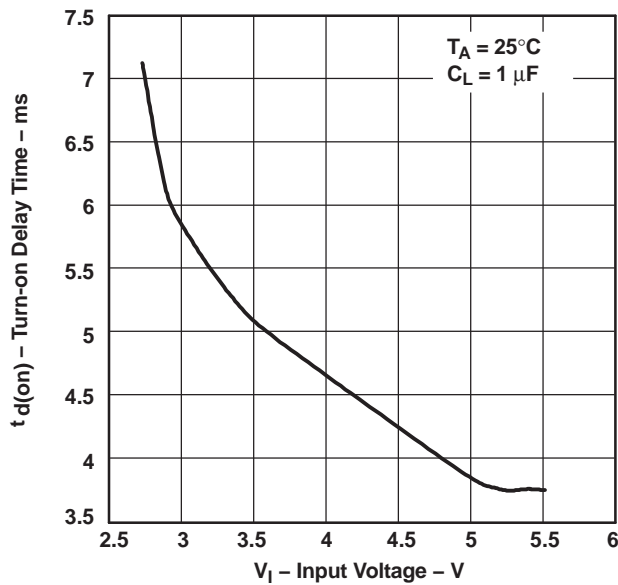


Figure 23.

**TURNOFF DELAY TIME
vs
INPUT VOLTAGE**

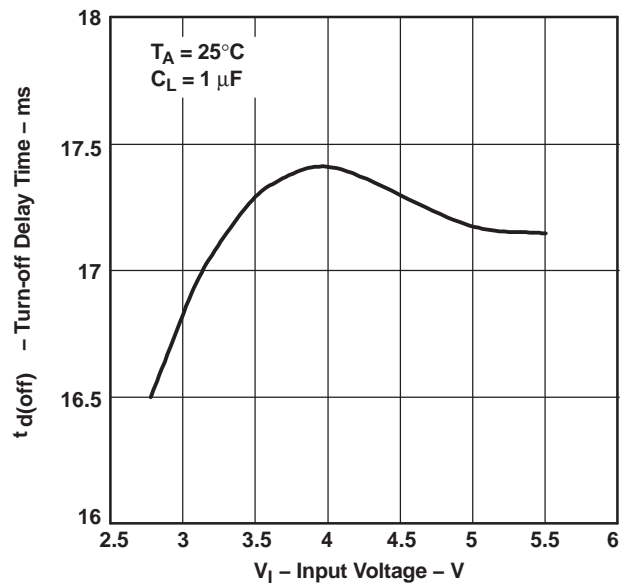
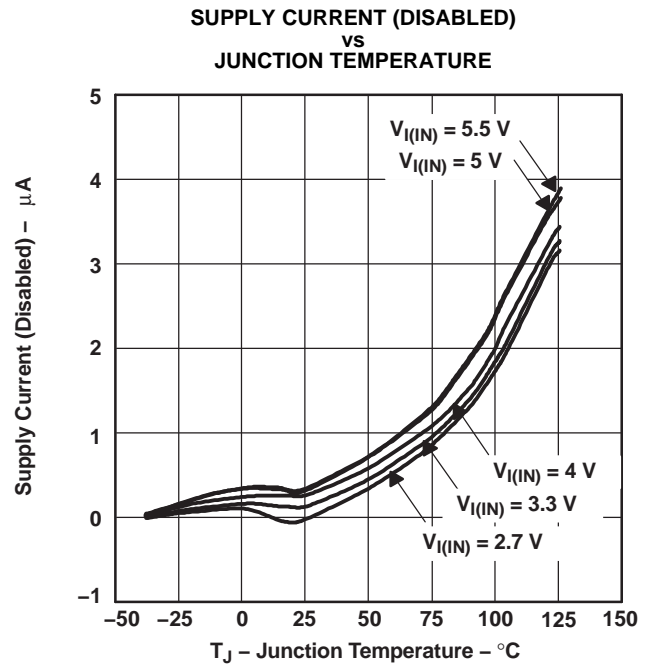
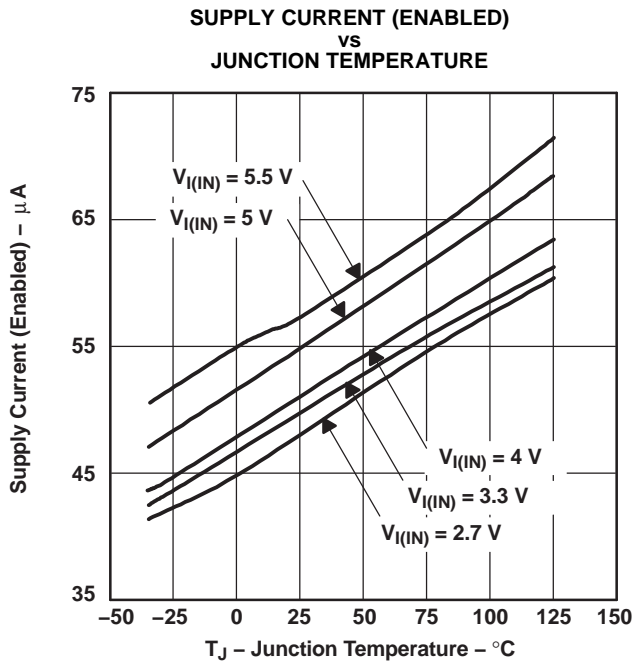
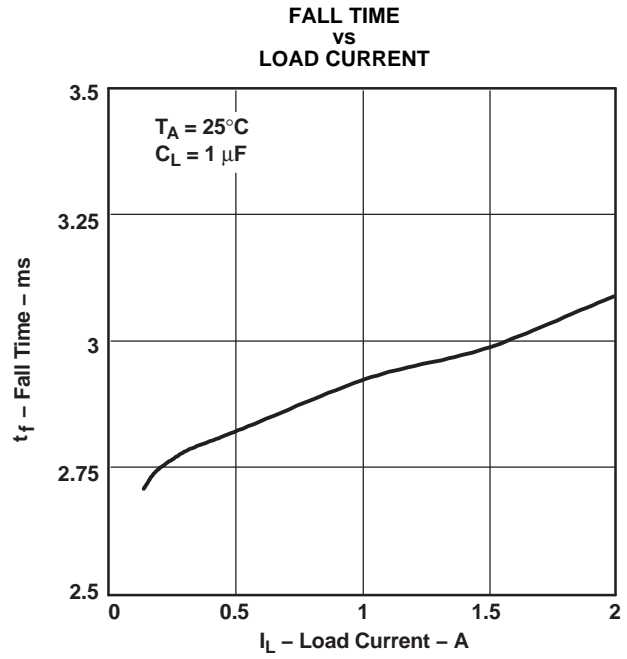
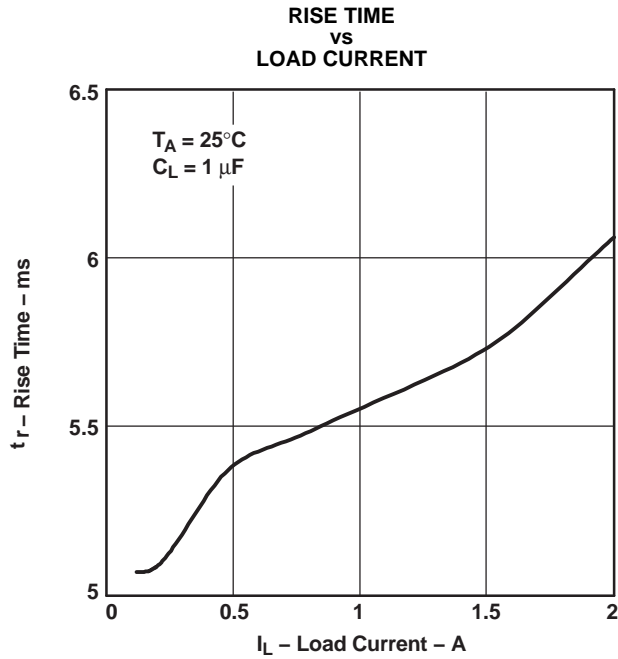


Figure 24.



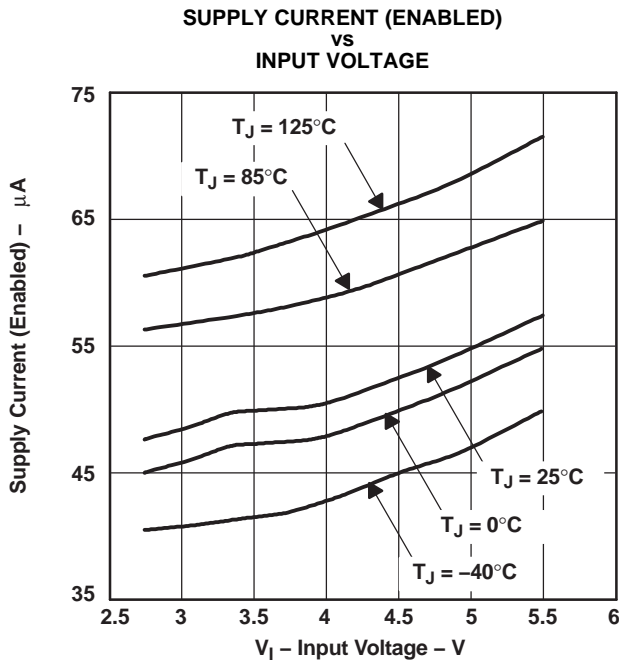


Figure 29.

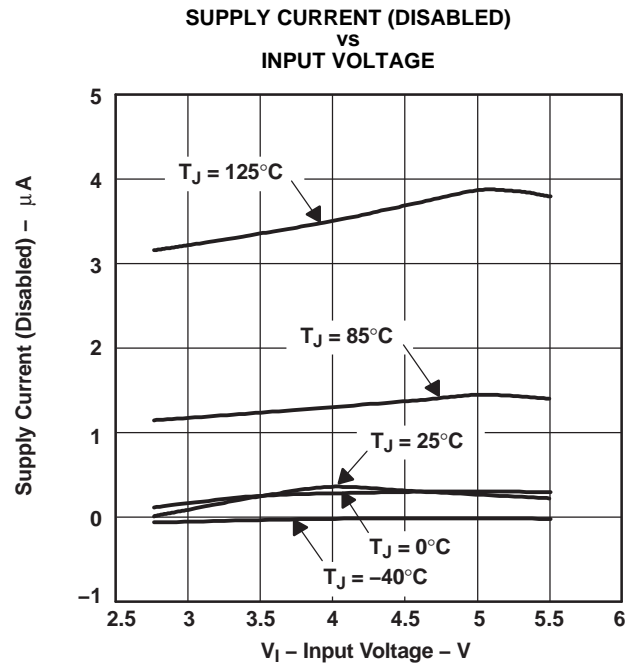


Figure 30.

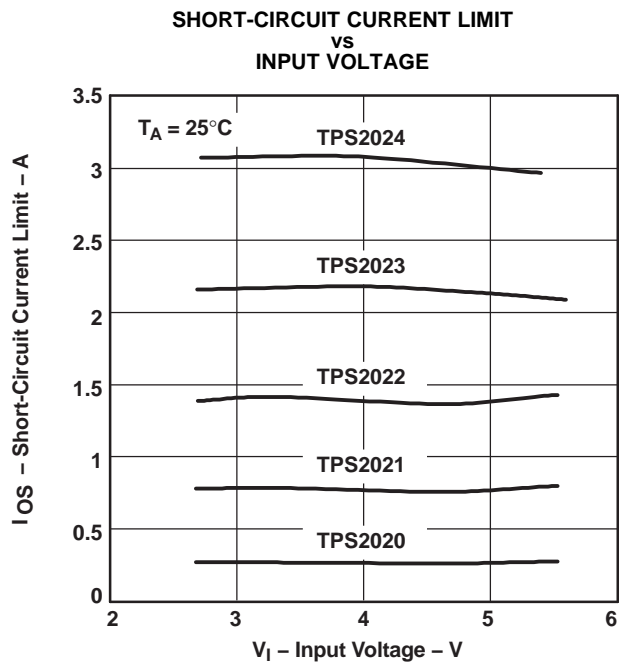


Figure 31.

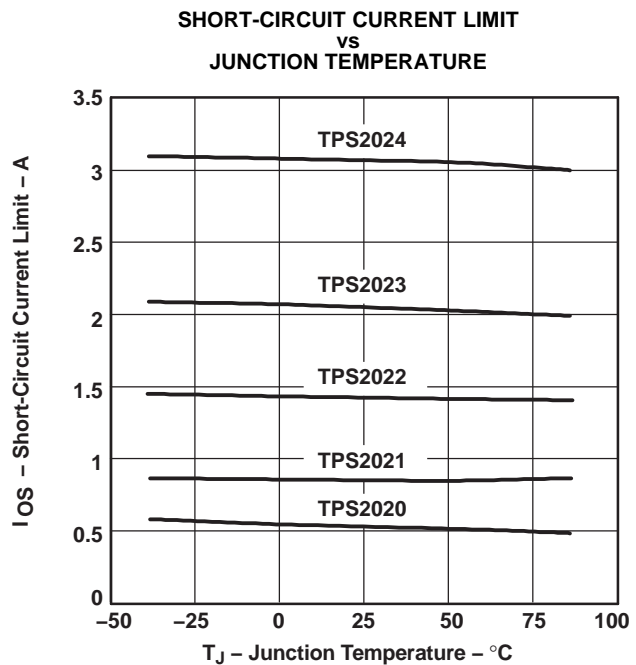


Figure 32.

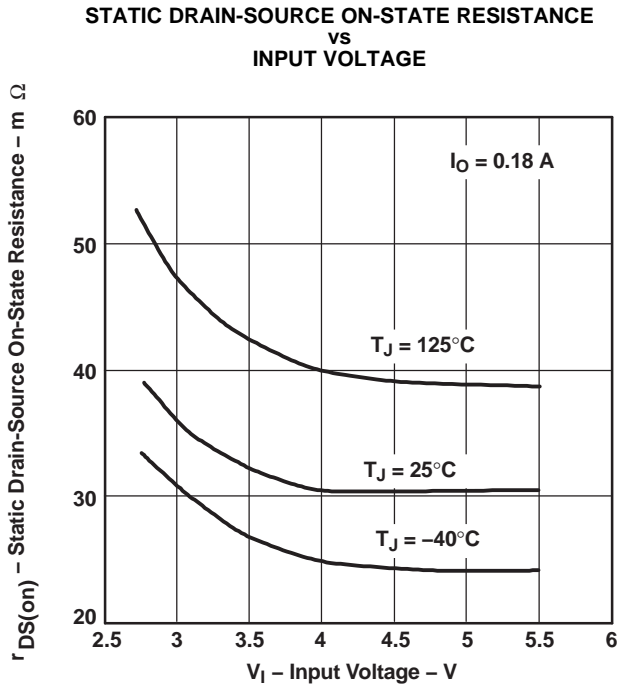


Figure 33.

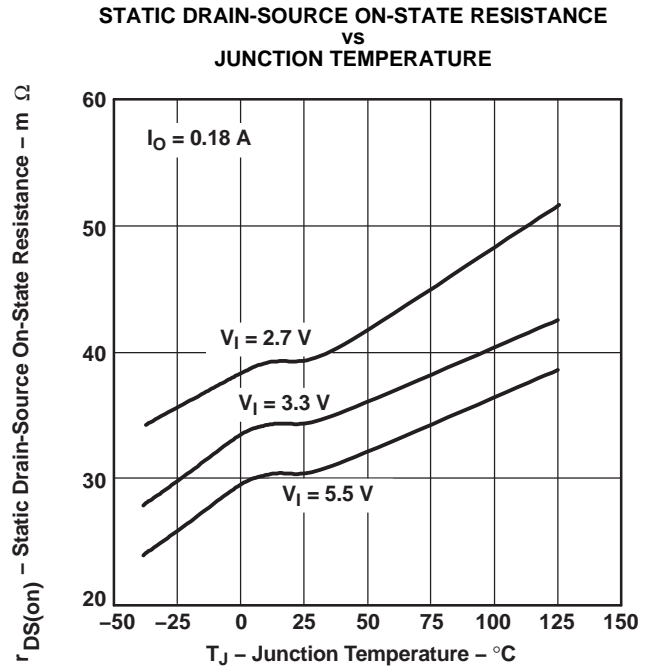


Figure 34.

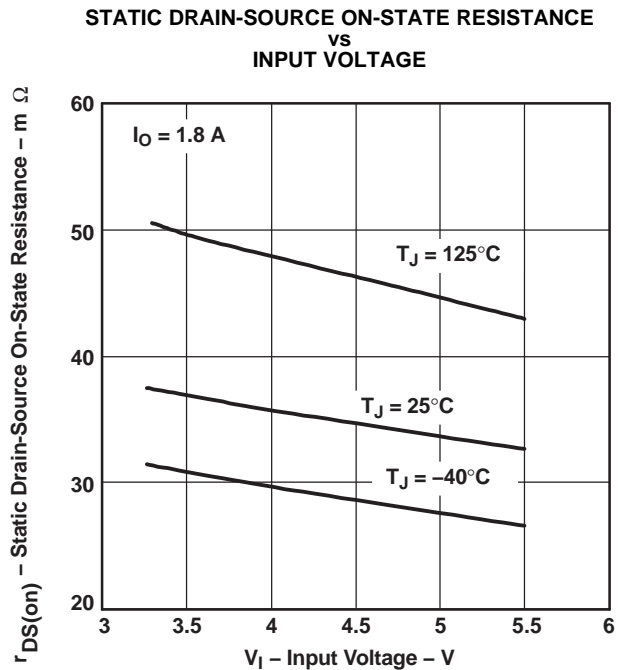


Figure 35.

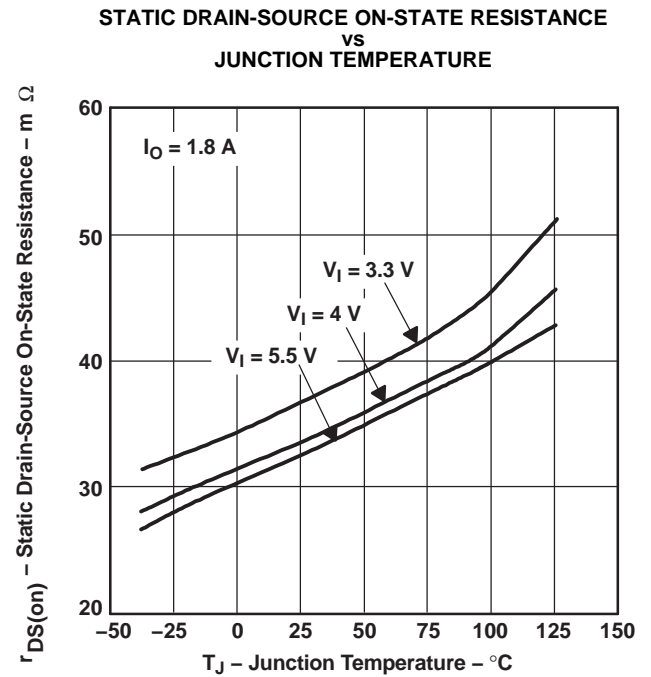


Figure 36.

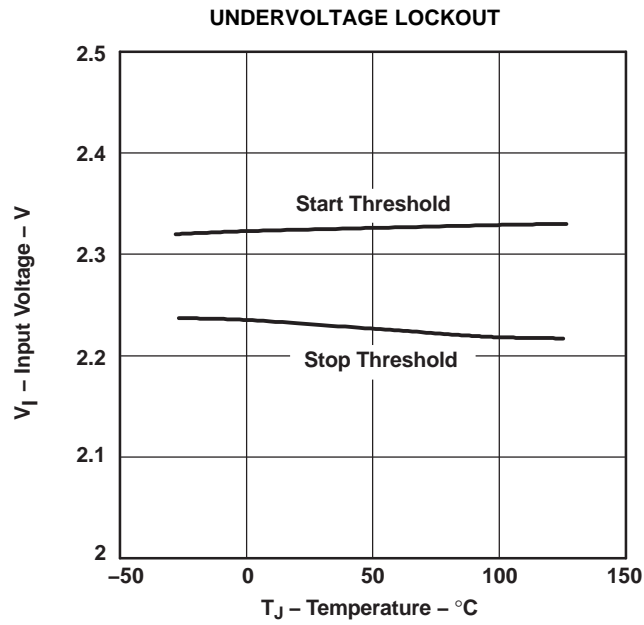


Figure 37.

APPLICATION INFORMATION

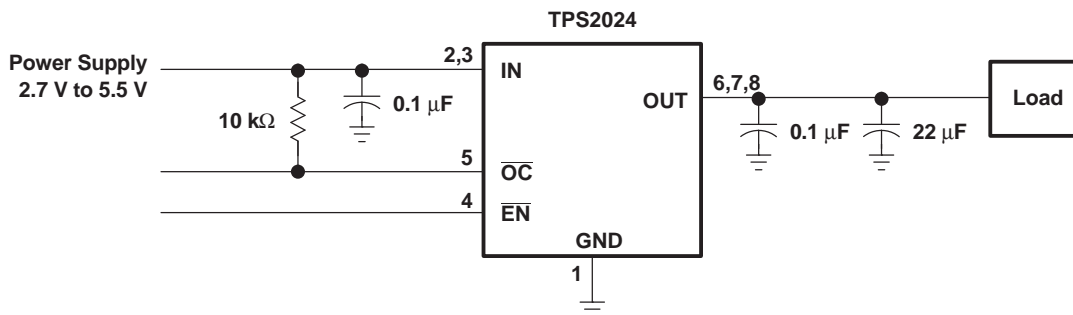


Figure 38. Typical Application

POWER SUPPLY CONSIDERATIONS

A 0.01- μF to 0.1- μF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output and input pins is recommended when the output load is heavy. This precaution reduces power supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01- μF to 0.1- μF ceramic capacitor improves the immunity of the device to short-circuit transients.

OVERCURRENT

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied, see Figure 6. The TPS202x senses the short and immediately switches into a constant-current output.

In the second condition, the excessive load occurs while the device is enabled. At the instant the excessive load occurs, very high currents may flow for a short time before the current-limit circuit can react (see Figures 13–22). After the current-limit circuit has tripped (reached the overcurrent trip threshold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figures 7–11). The TPS202x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ RESPONSE

The $\overline{\text{OC}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter can be connected to the $\overline{\text{OC}}$ pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

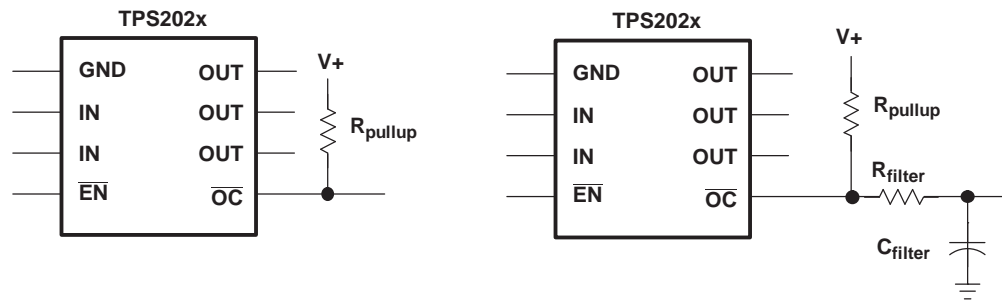


Figure 39. Typical Circuit for $\overline{\text{OC}}$ Pin and RC Filter for Damping Inrush $\overline{\text{OC}}$ Responses

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{\text{DS(on)}}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{\text{DS(on)}}$ from Figures 33–36. Next, calculate the power dissipation using:

$$P_D = r_{\text{DS(on)}} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta\text{JA}} + T_A$$

where:

T_A = Ambient temperature °C

$R_{\theta\text{JA}}$ = Thermal resistance—SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get an acceptable answer.

THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS202x into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at powerup. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

GENERIC HOT-PLUG APPLICATIONS (See [Figure 40](#))

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Because of the controlled rise times and fall times of the TPS202x series, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS202x also ensures the switch is off after the card has been removed, and the switch remains off during the next insertion. The UVLO feature ensures a soft start with a controlled rise time for every insertion of the card or module.

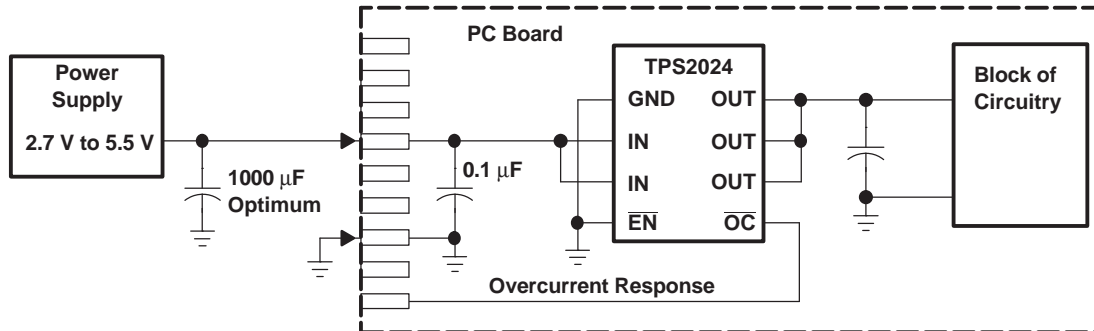


Figure 40. Typical Hot-Plug Implementation

By placing the TPS202x between the V_{CC} input and the rest of the circuitry, the input power reaches this device first after insertion. The typical rise time of the switch is approximately 9 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS2020D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2020 | Samples |
| TPS2020DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2020 | Samples |
| TPS2021D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2021 | Samples |
| TPS2021DG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2021 | Samples |
| TPS2021DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2021 | Samples |
| TPS2021DRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2021 | Samples |
| TPS2021P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TPS2021P | Samples |
| TPS2022D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2022 | Samples |
| TPS2022DG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2022 | Samples |
| TPS2022DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2022 | Samples |
| TPS2023D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2023 | Samples |
| TPS2023DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2023 | Samples |
| TPS2023P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TPS2023P | Samples |
| TPS2024D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2024 | Samples |
| TPS2024DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2024 | Samples |
| TPS2024DRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2024 | Samples |
| TPS2024P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TPS2024P | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS2020, TPS2021, TPS2022, TPS2024 :

- Automotive : [TPS2020-Q1](#), [TPS2021-Q1](#), [TPS2022-Q1](#), [TPS2024-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS2020DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2021DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2022DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2023DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2024DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS2020DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TPS2021DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TPS2022DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TPS2023DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| TPS2024DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated